QPA0524

24.25 – 26.5 GHz 5 Watt GaN Power Amplifier

Product Overview

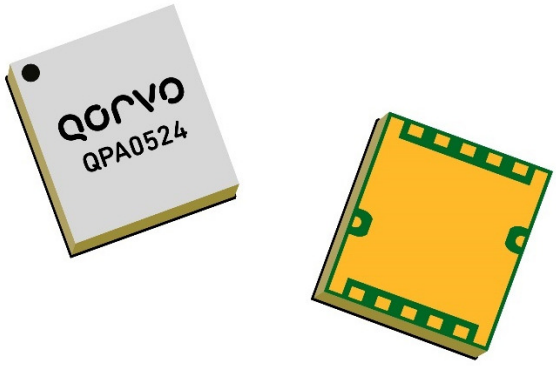
Qorvo's QPA0524 is a high power, packaged Ku-Band MMIC amplifier fabricated using Qorvo's production 0.15 um GaN-on-SiC process (QGaN15). The QPA0524 targets the 24.25-26.5 GHz for 5G and Satcom band. It provides 400 mW linear power with ACPR of -30 dBc at 802.11ac 160MHz MSC9. Furthermore, The QPA0524 can deliver output powers up to 5 W with 35 dB of small-signal gain and 23% power-added efficiency.

To simplify system integration, the QPA0524 is fully matched to 50 ohms with DC grounded I/O ports for optimum ESD performance.

The QPA0524 is ideal for supporting 5G linear power, communications, and radar applications in both commercial and military markets.

The QPA0524 is 100% DC and RF tested to ensure compliance to electrical specifications.

Lead-free and RoHS compliant

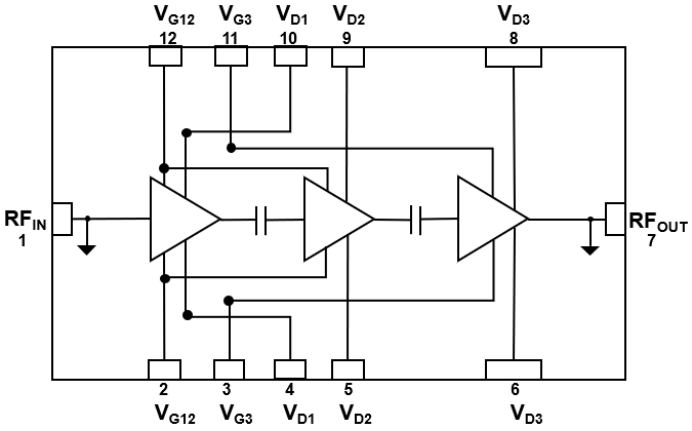


Key Features

- Frequency Range: 24.25 – 26.5 GHz
- Linear P_{OUT}: 26 dBm
- ACPR (P_{OUT} = 26 dBm, 802.11ac): -30 dBc
- P_{OUT} (P_{IN} = 20 dBm): 37 dBm
- PAE (P_{IN} = 20 dBm): 23 %
- Small Signal Gain: 23 dB
- Bias: V_D = 20 V, I_{DQ} = 126 mA, V_G = -2.2 V typ. range
- Package Dimensions: 5.00 x 5.50 x 1.63 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- 5G
- Satellite Communications
- Radar

Ordering Information

Part No.	Description
QPA0524	5 Watt GaN PA Package
QPA0524TR7	250 pieces on a 7” reel (standard)
QPA0524EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-5 V to 0 V
Drain Current Total (I_D)	1800 mA
Gate Current (I_G)	See p. 22
Power Dissipation (P_{DISS}), CW, T_{BASE} = 85 °C	31 W
Input Power (P_{IN}), 50 Ω, CW, V_D = 20 V, I_{DQ} = 126 mA, T_{BASE} = 85 °C	30 dBm
Input Power (P_{IN}), 3:1 VSWR, CW, V_D = 20 V, I_{DQ} = 126 mA, T_{BASE} = 85 °C	23 dBm
Mounting Temperature (30 seconds)	260 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Drain Voltage (V_D) – CW		20	24 (1)	V
Drain Current Total, Quiescent (I_{DQ} = I_{D12} + I_{D3})		126		mA
Drain Current Total, RF (I_{D_Drive})	See plots page 4, 5, 9, 12, 15			mA
Gate Voltage Typ. Range (V_G)	–1.5 to -2.9			V
Gate Current, RF (I_{G_Drive})	See plots page 4, 5			mA
Input Power, P_{IN} (2)		20		dBm
Operating Temp. (T_{BASE}) (3)	–40		+85	ºC

1. 24 V requires ≥ 3 dBm back off from P_{SAT} due to thermal
2. Compression is varied due to thermal, see p. 6
3. T_{BASE} is back side of QPA0524 (see p. 25, offset temperature based on Qorvo's EVB Cu filled vias for reference).

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

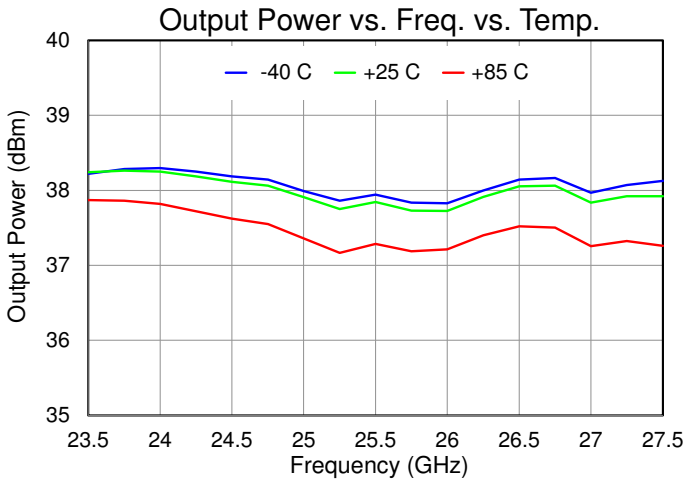
Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		24.25		26.5	GHz
Linear Output Power			26		dBm
Output Power, P_{OUT}	P_{IN} = 20 dBm		37		dBm
Power Added Efficiency, PAE	P_{IN} = 20 dBm		23		%
ACPR	P_{OUT} = 26 dBm 802.11ac, 160 MHz, MSC9 (256QAM), PAR = 12 dB		-30		dBc
Small Signal Gain, S21	P_{IN} = -30 dBm		23		dB
Input Return Loss, IRL			15		
Output Return Loss, ORL			15		
P_{SAT} Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC; P_{IN} = 20 dBm		-0.01		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC		-0.15		dB/ºC

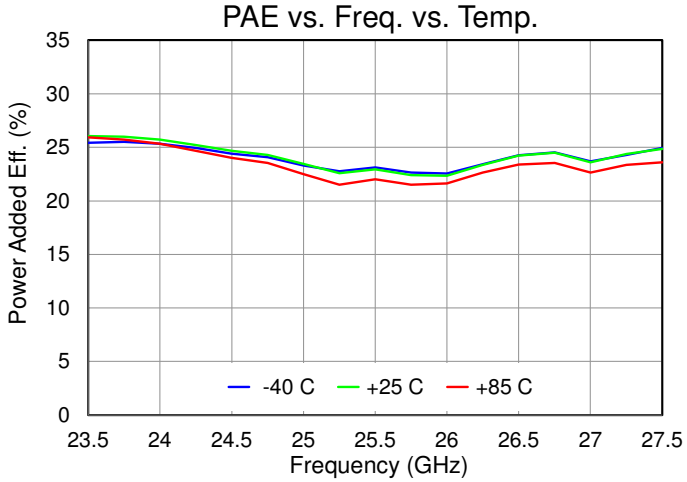
Notes:

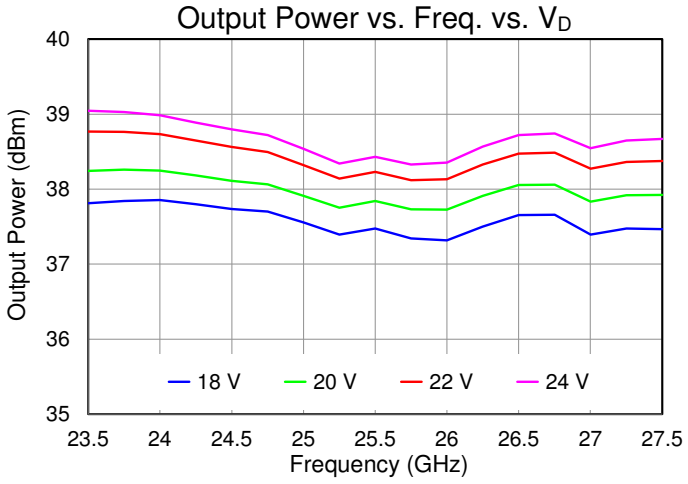
1. Test conditions unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, V_G = -2.2 V +/- 0.7 V typical, T_{BASE} = +25ºC, Z_0 = 50 Ω (reference planes are at QPA0524).
2. T_{BASE} is back side of QPA0524 (see page 28, offset temperature based on Qorvo's EVB design for reference).

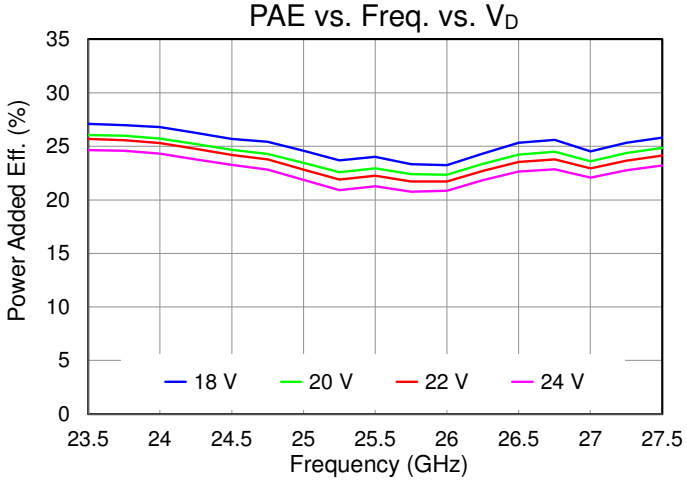
Performance Plots – Large Signal (CW)

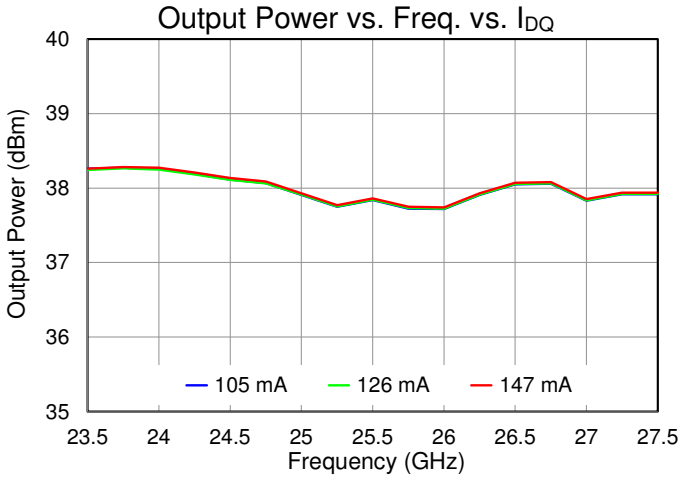
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = 20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

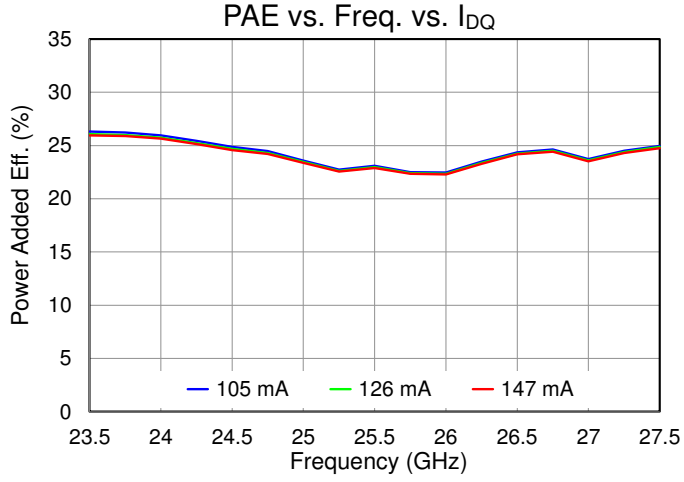






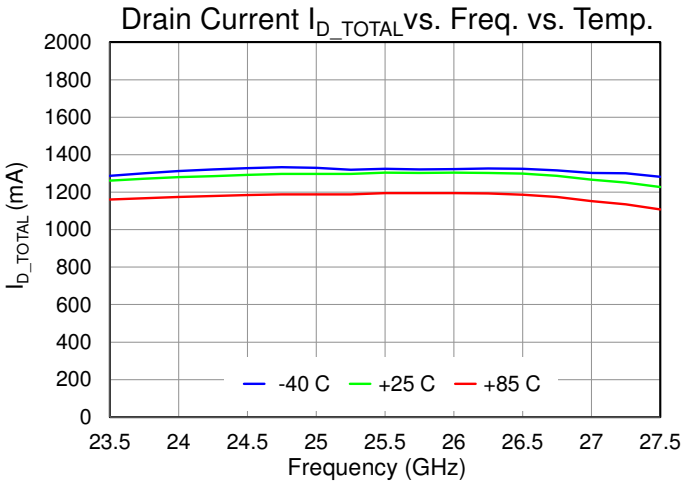


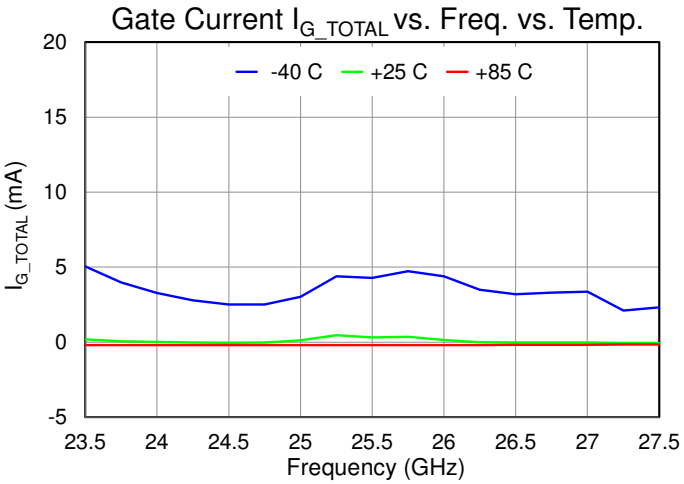


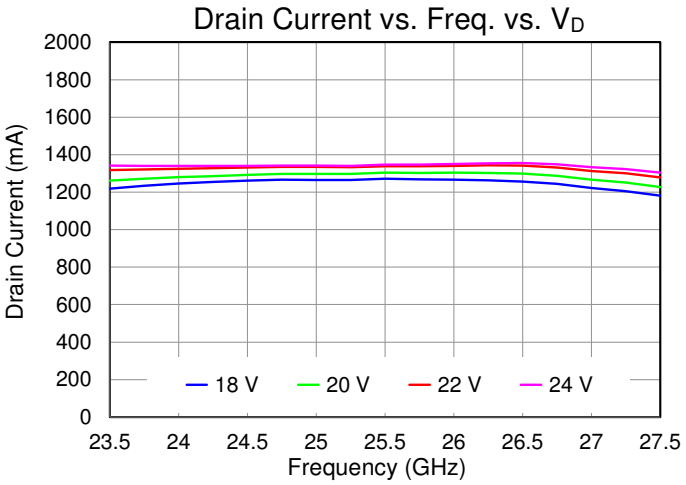


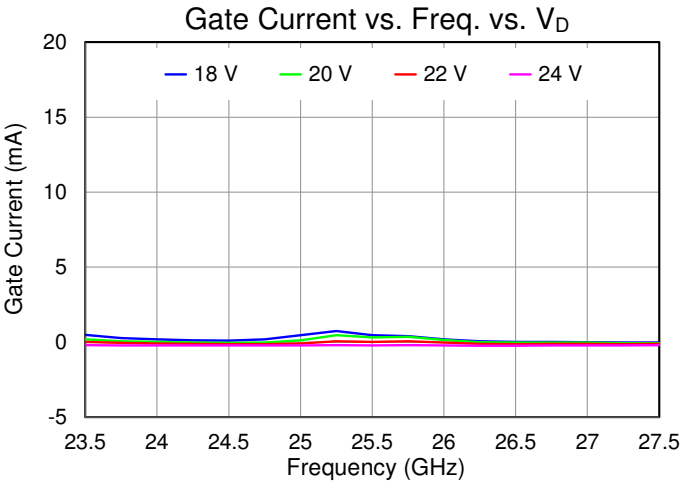
Performance Plots – Large Signal (CW)

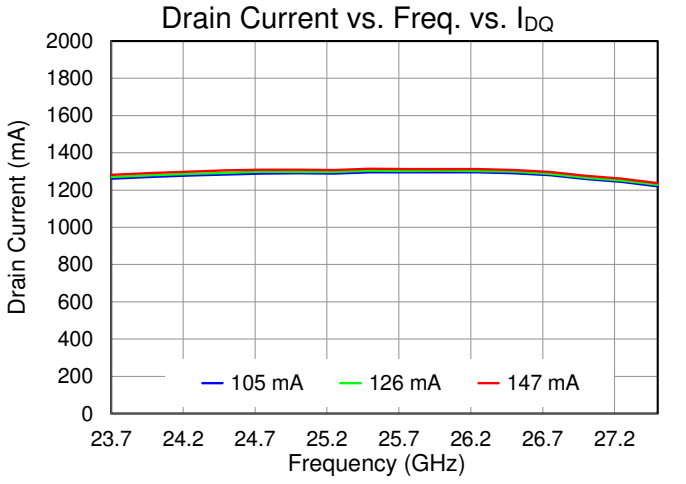
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = 20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

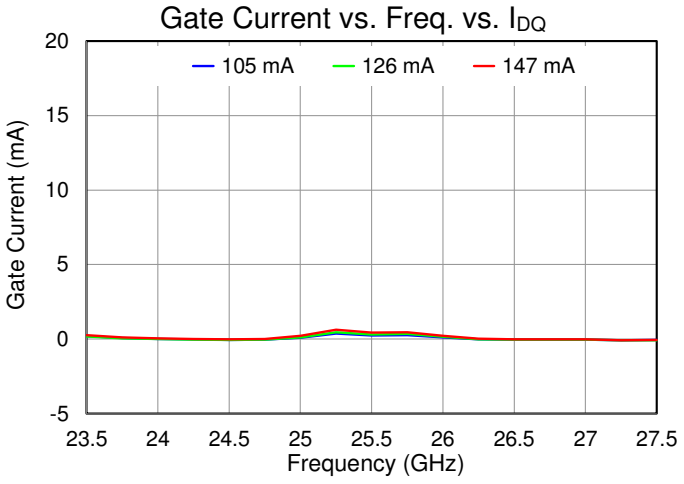












Performance Plots – Large Signal (CW)

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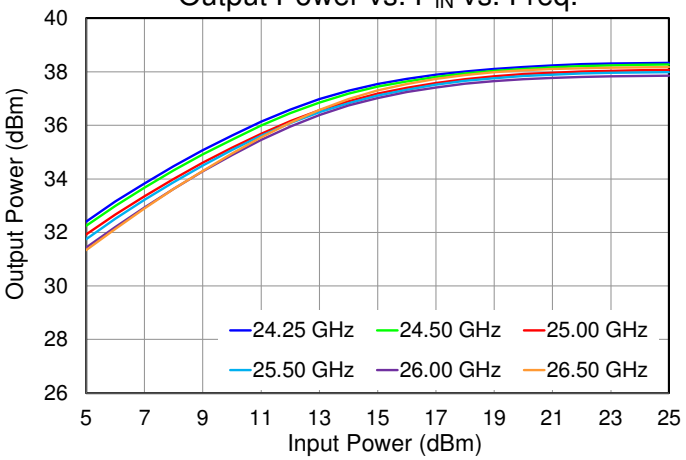
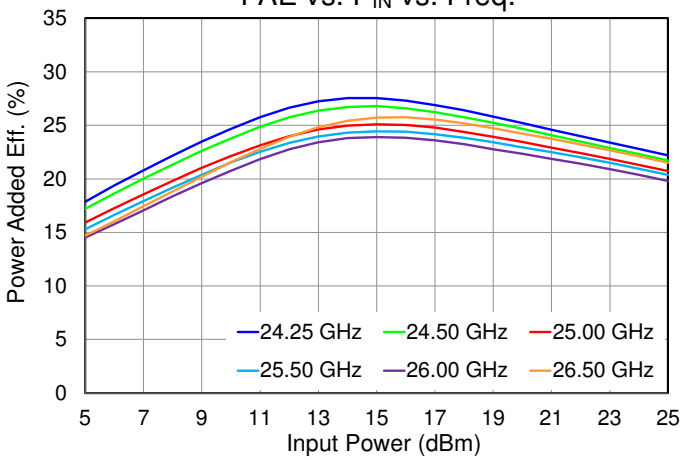
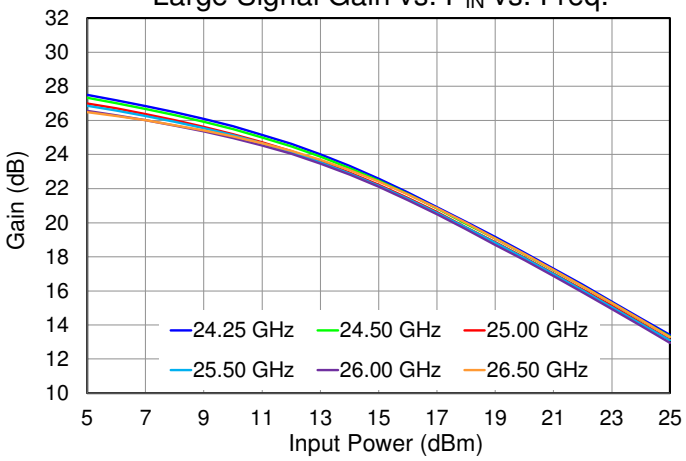
Output Power vs. P_{IN} vs. Freq.



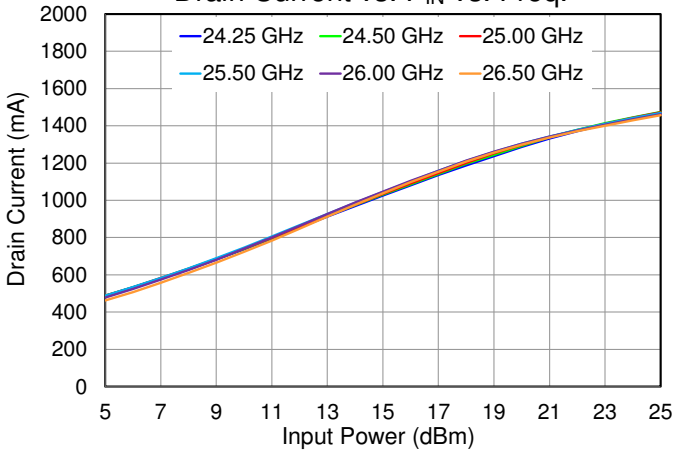
PAE vs. P_{IN} vs. Freq.



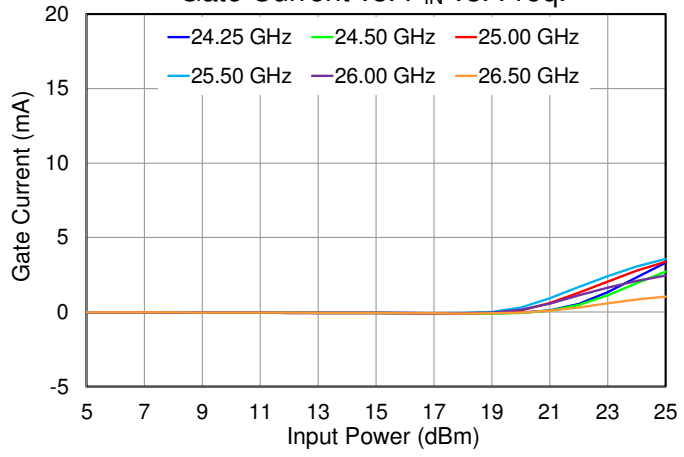
Large Signal Gain vs. P_{IN} vs. Freq.



Drain Current vs. P_{IN} vs. Freq.



Gate Current vs. P_{IN} vs. Freq.



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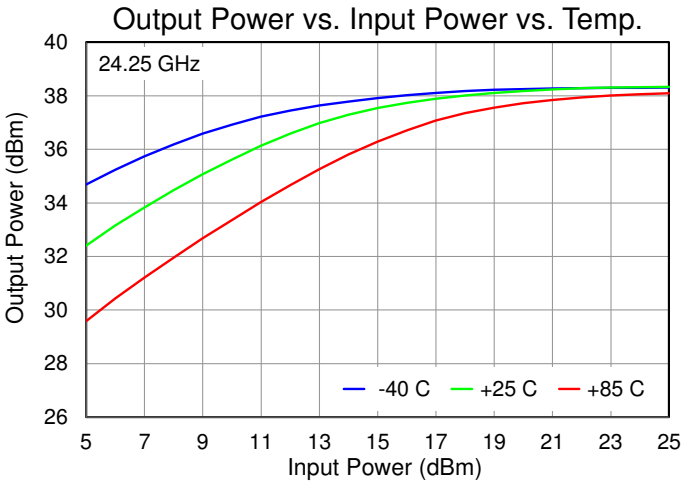

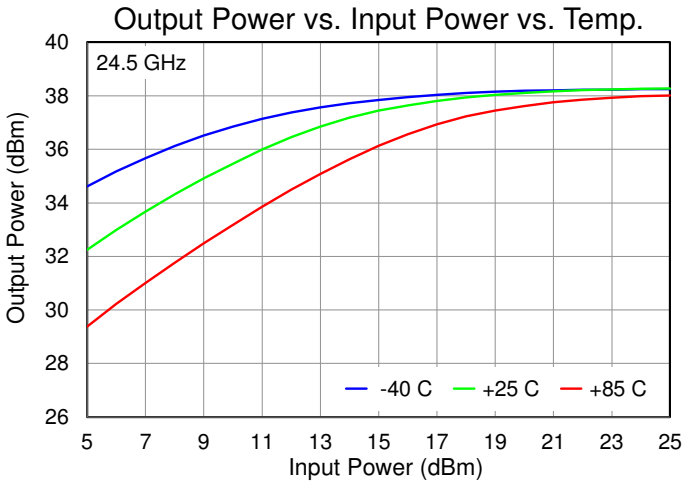

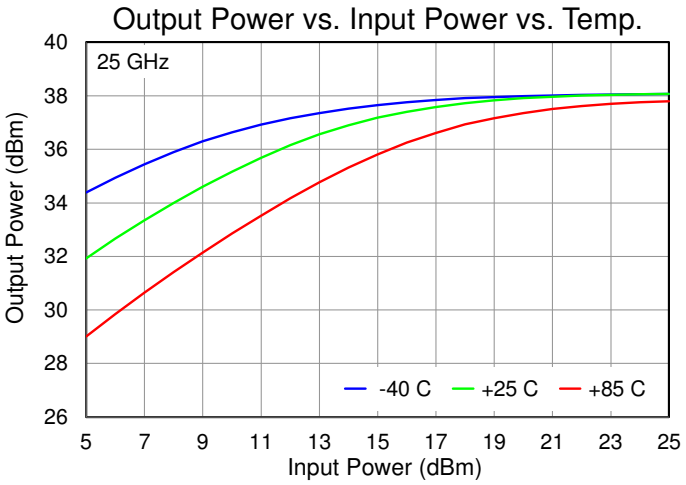

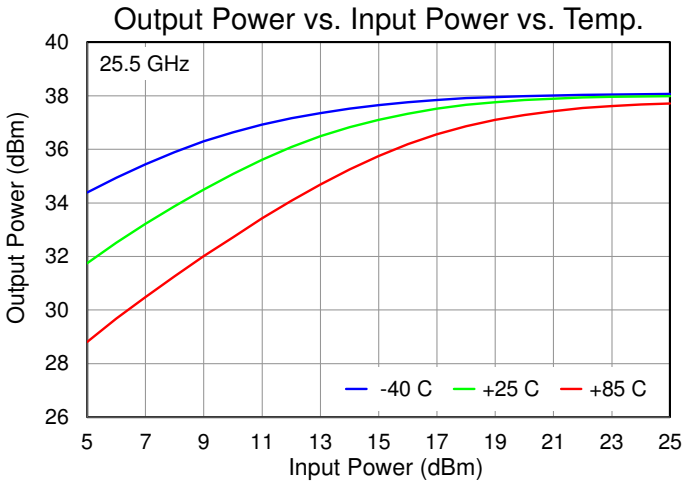

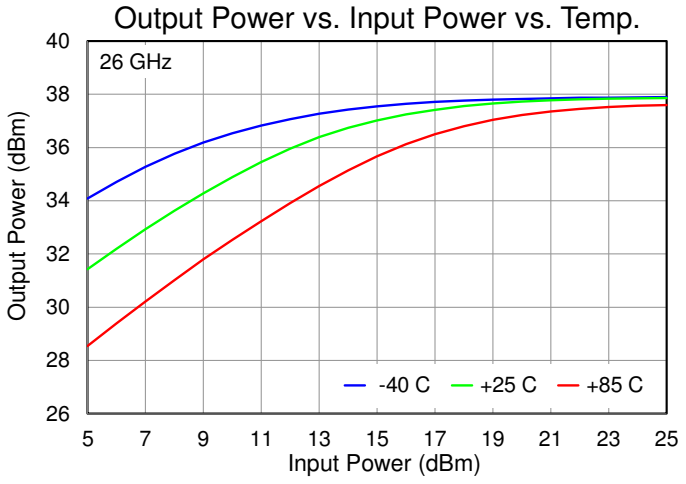

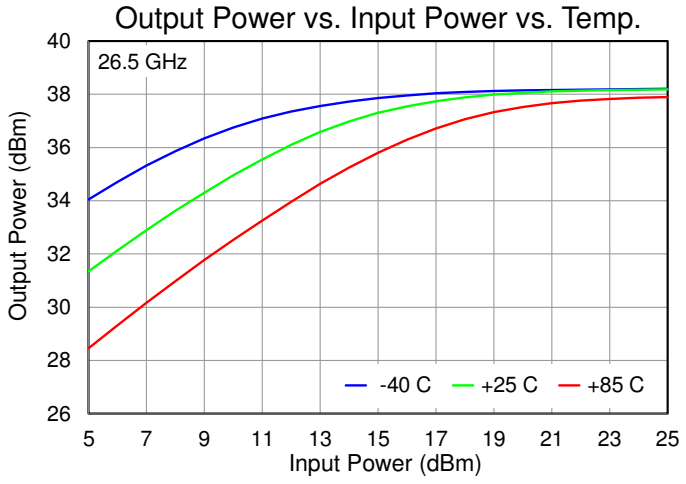

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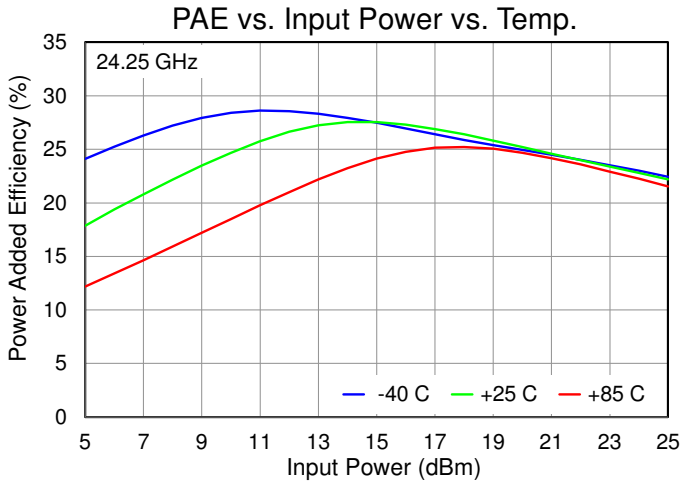

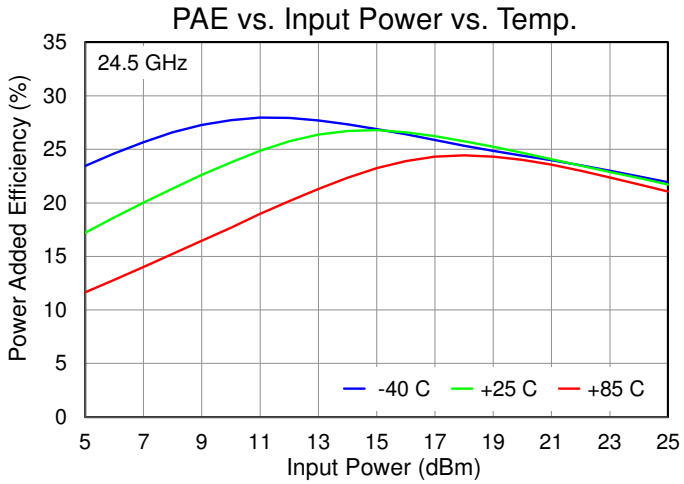

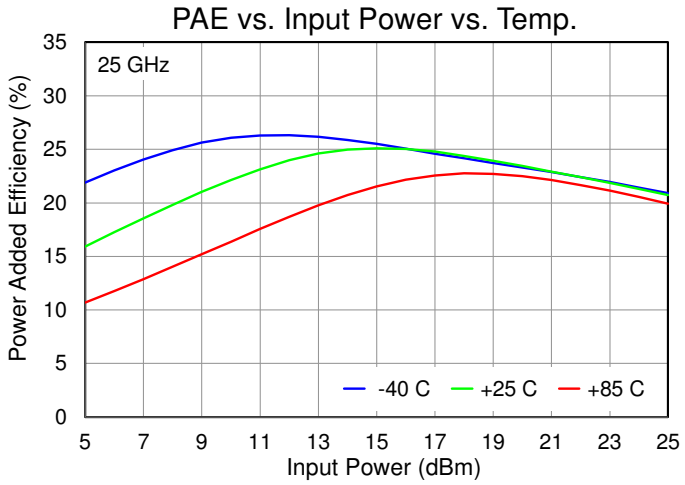

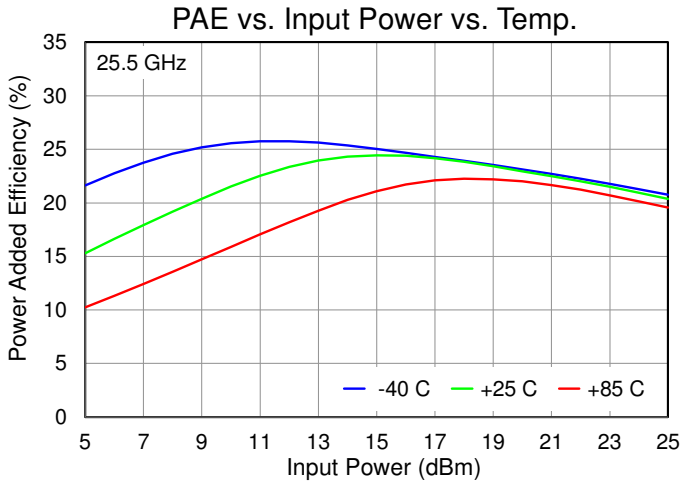

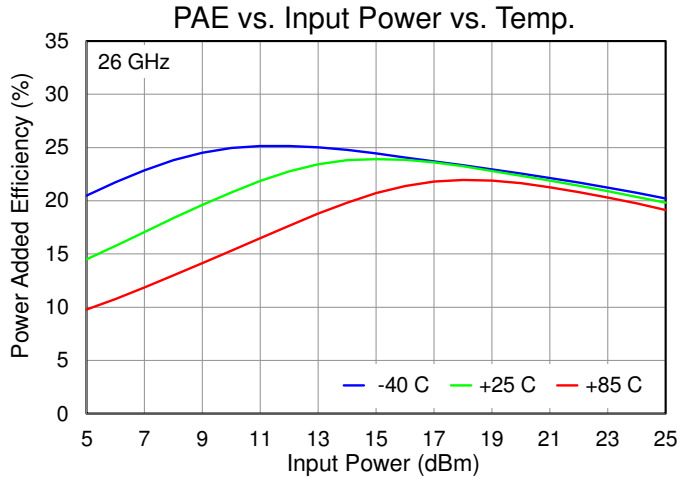

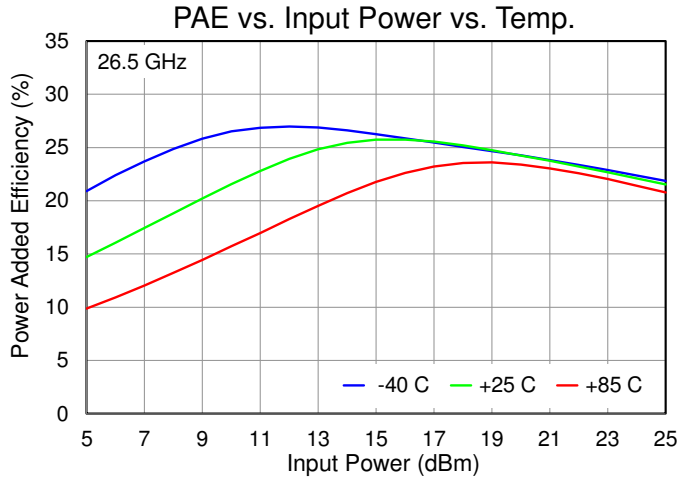

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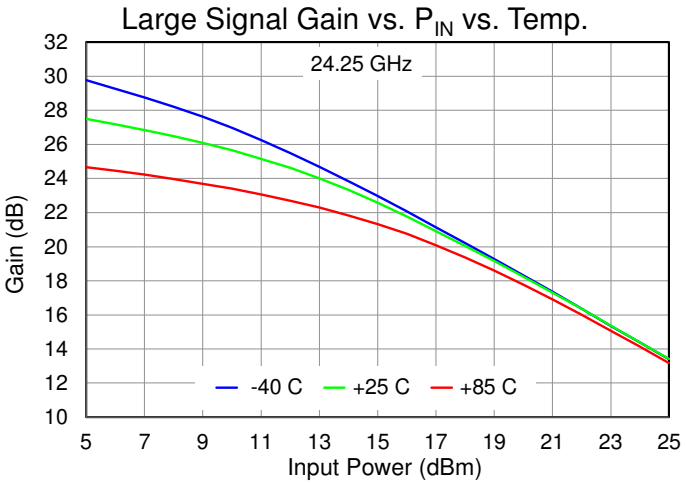

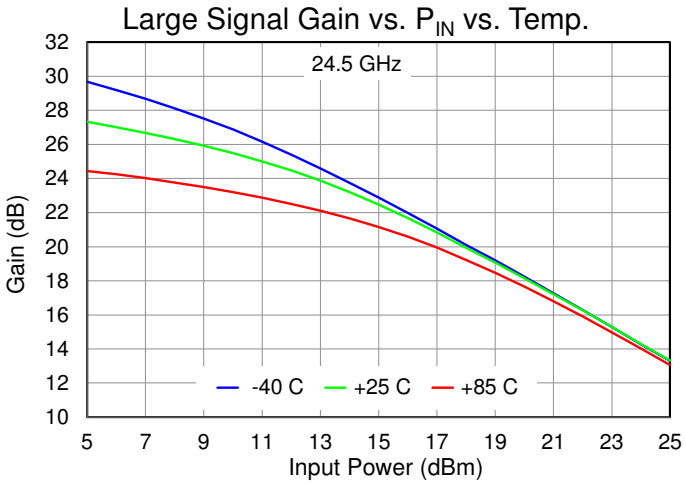

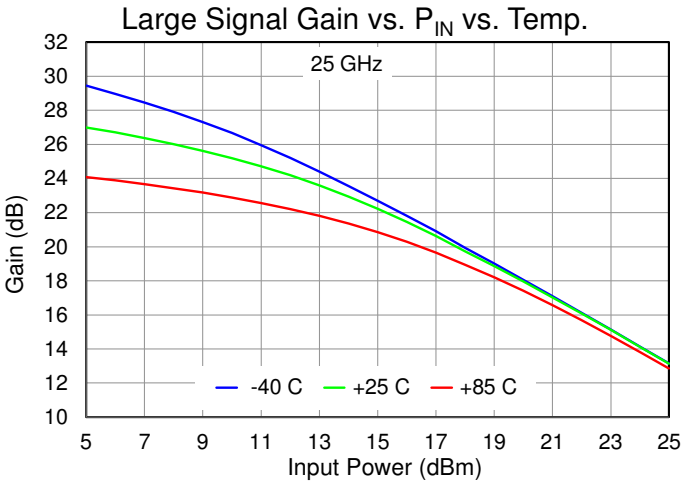

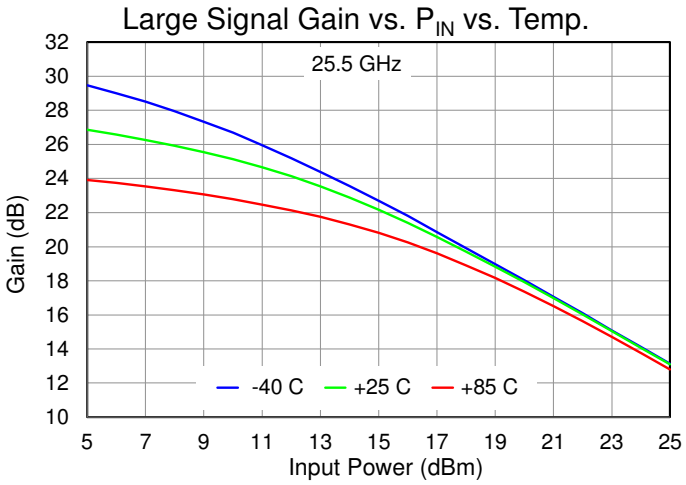

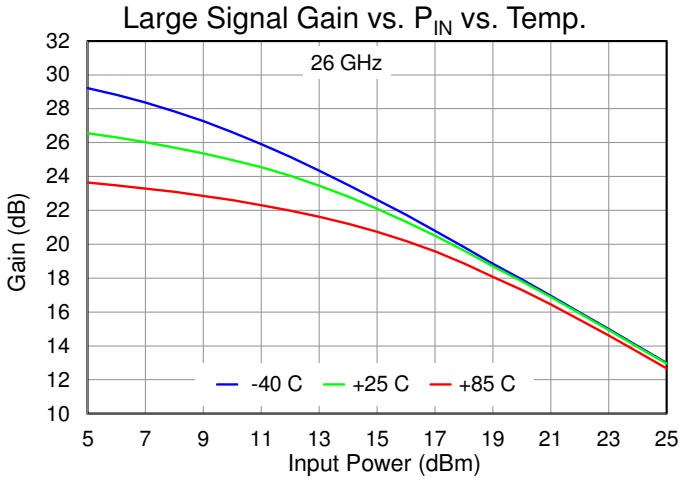

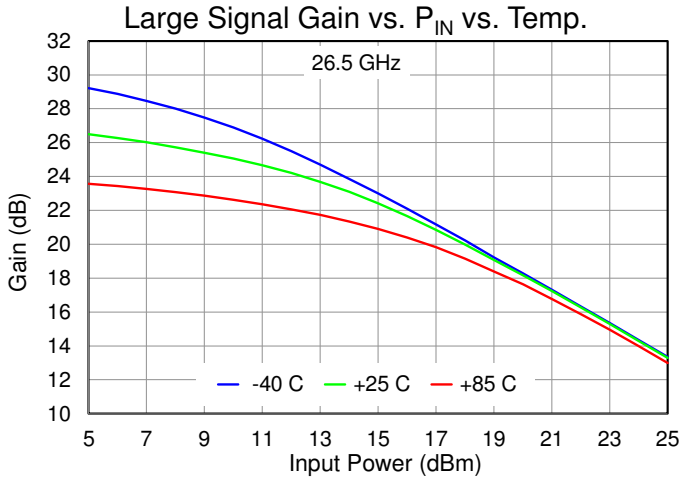

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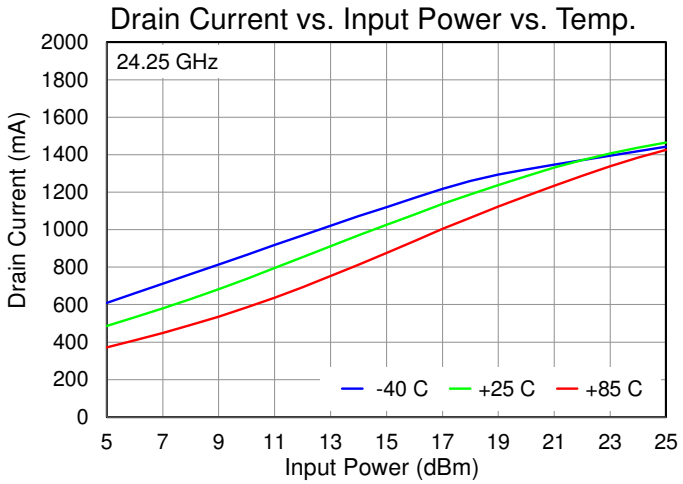

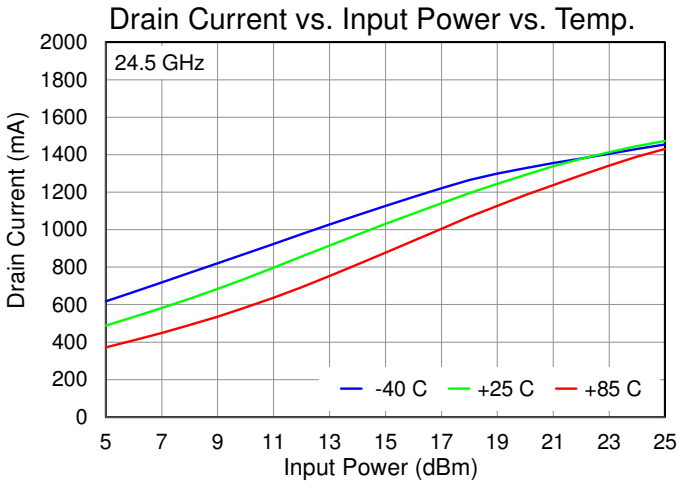

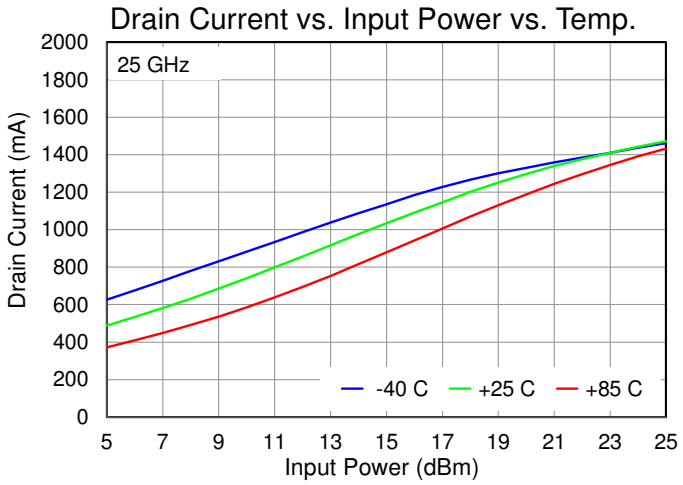

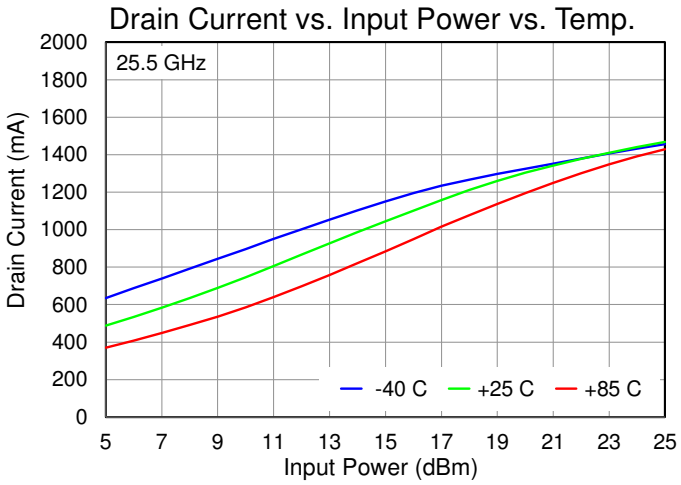

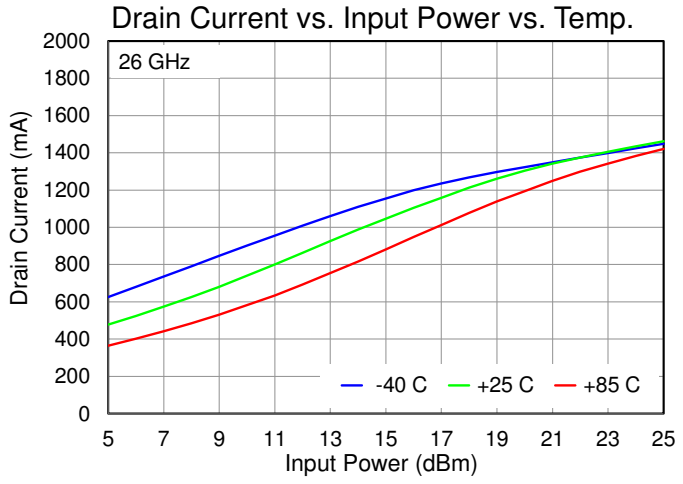

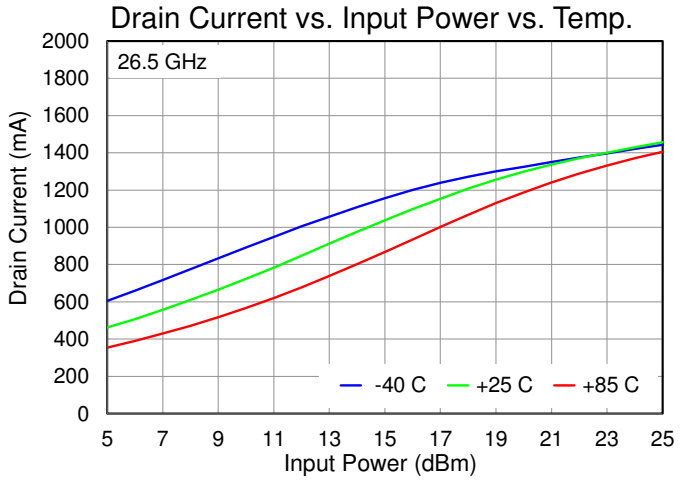

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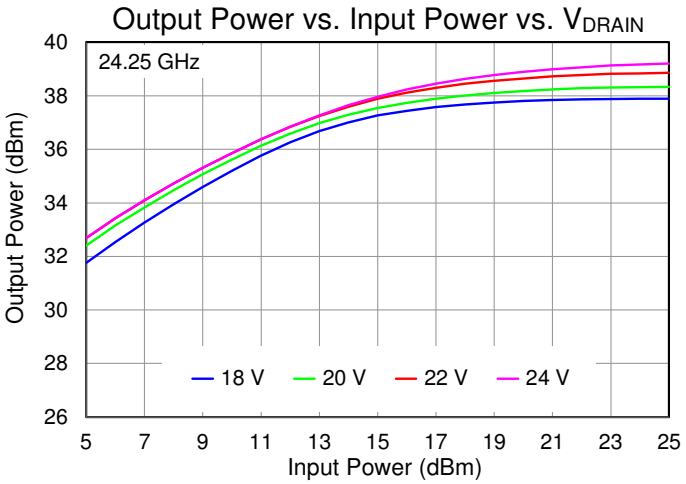
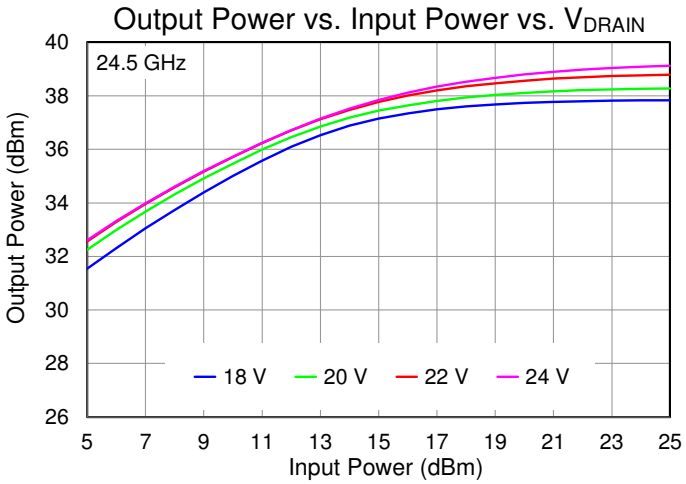
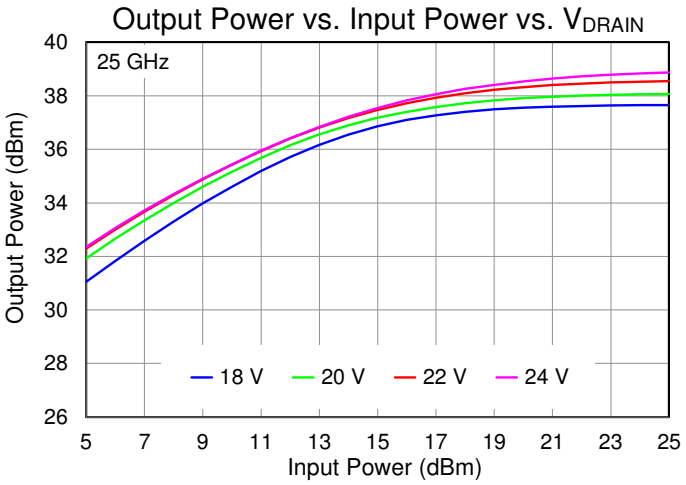
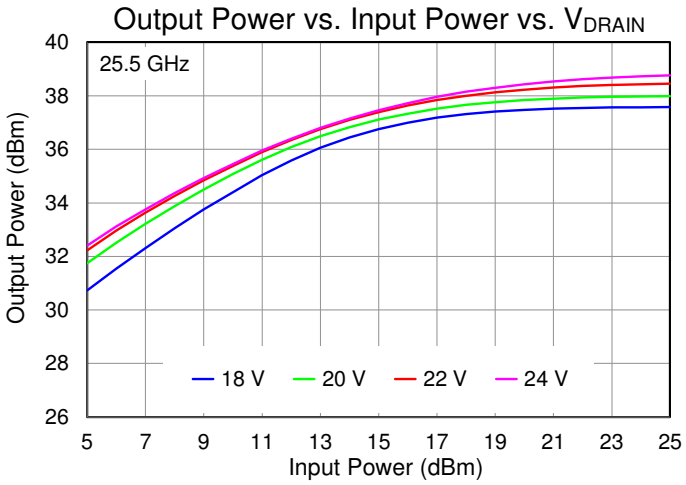
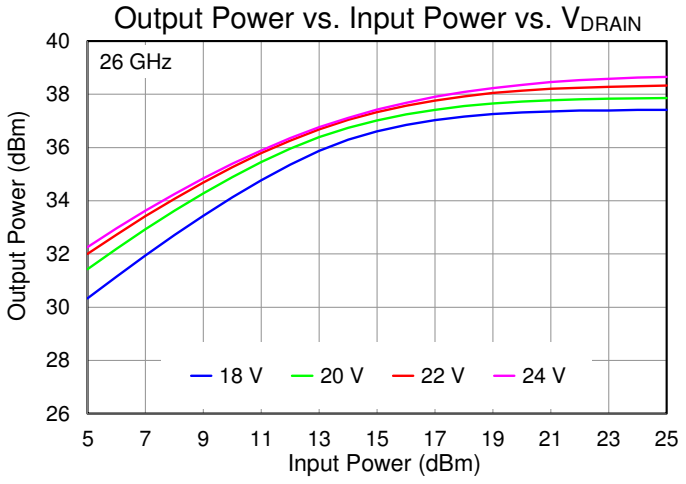
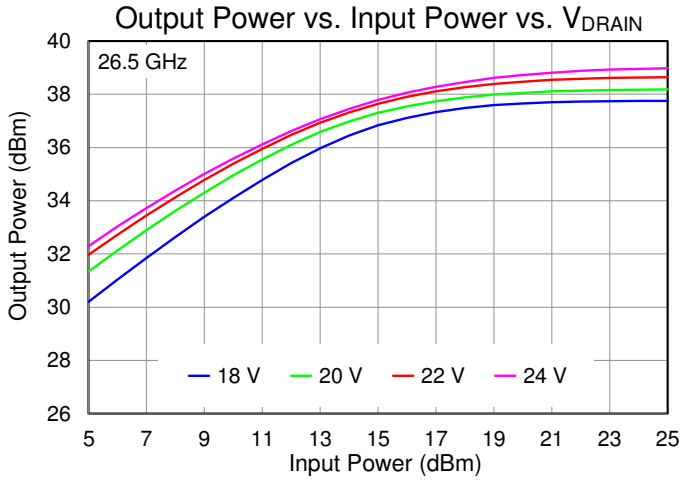






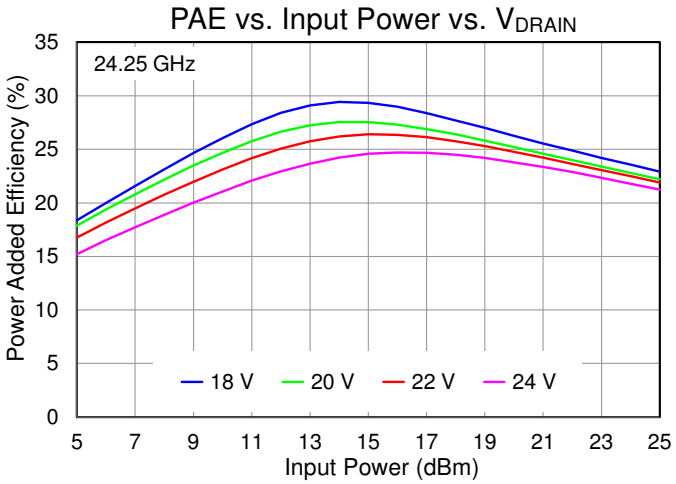


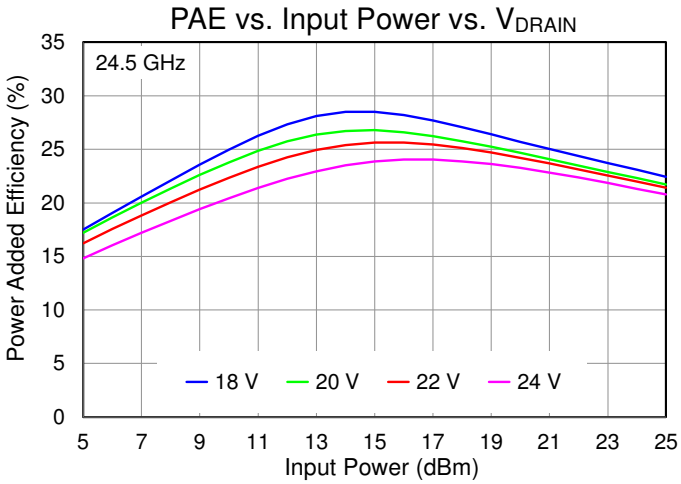


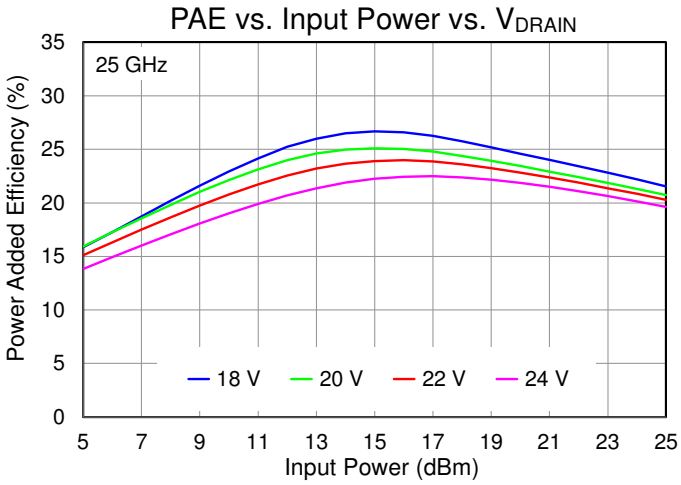


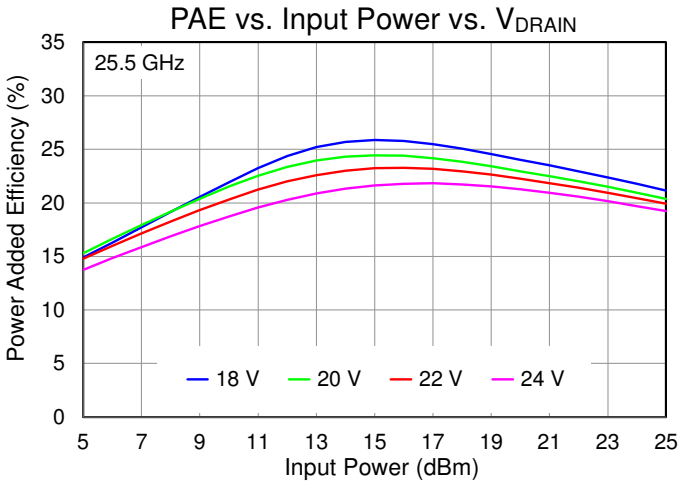
Performance Plots – Large Signal (CW)

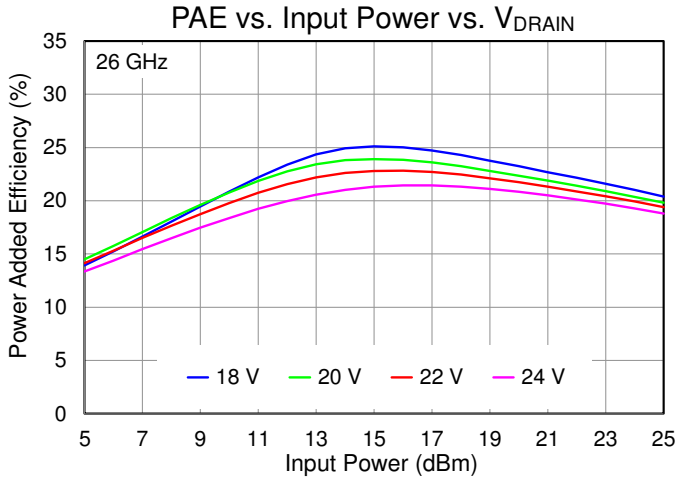
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = 20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

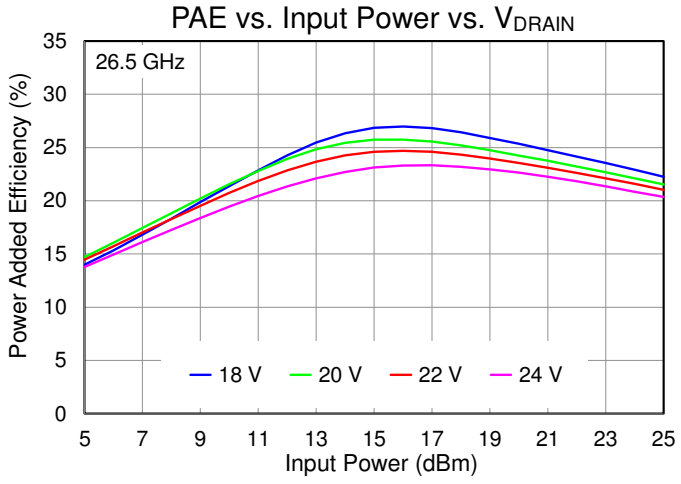






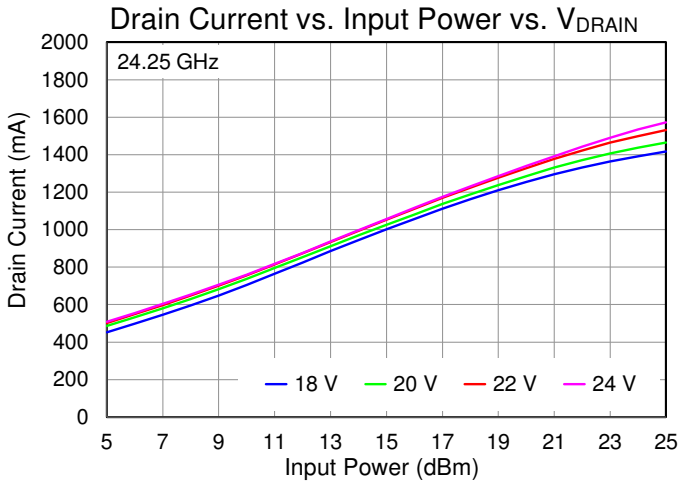


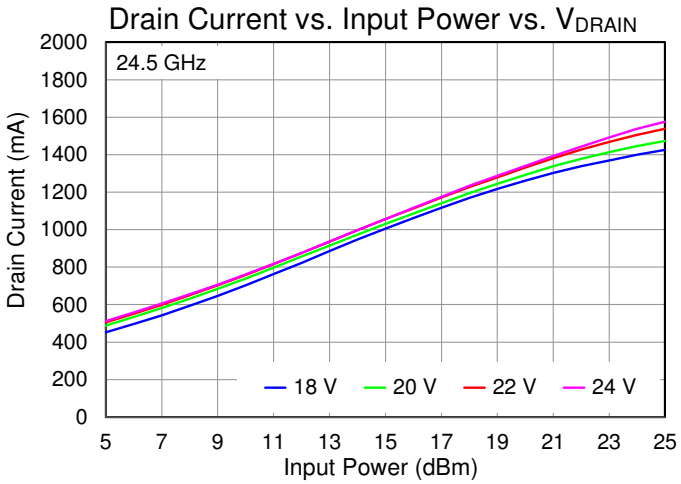


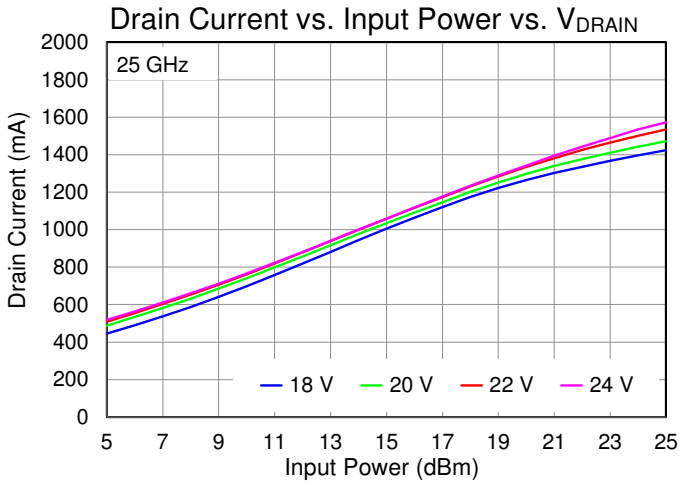


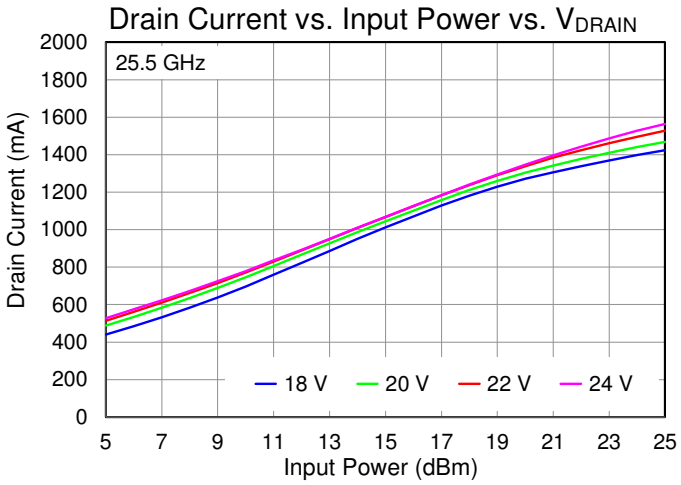
Performance Plots – Large Signal (CW)

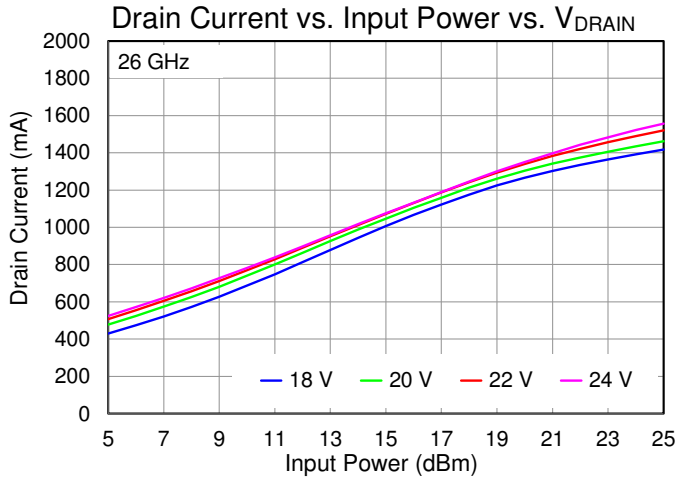
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = 20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

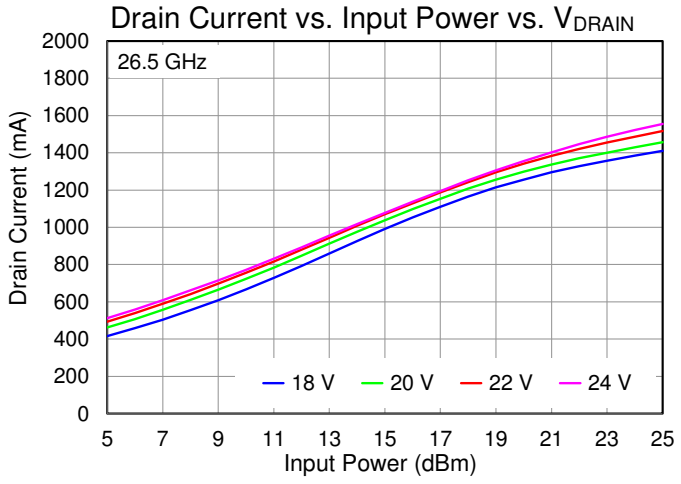






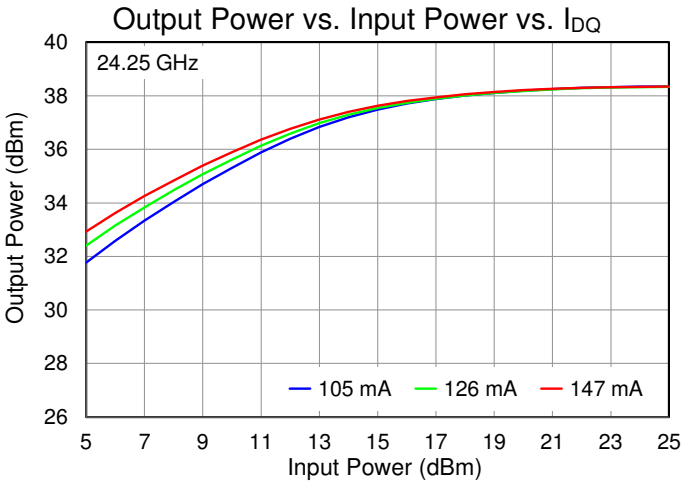


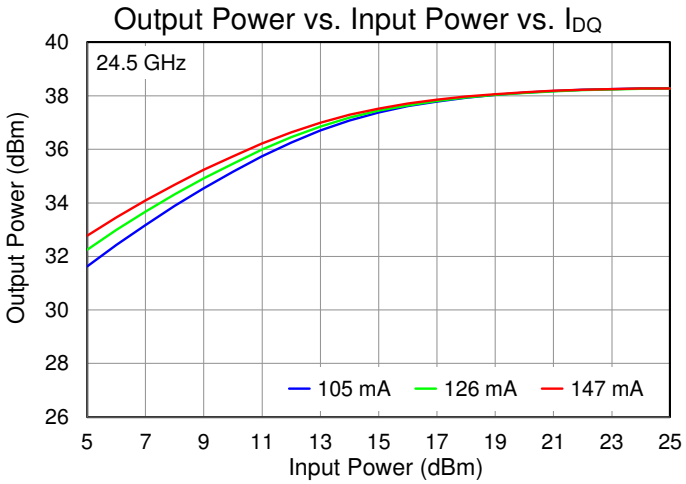


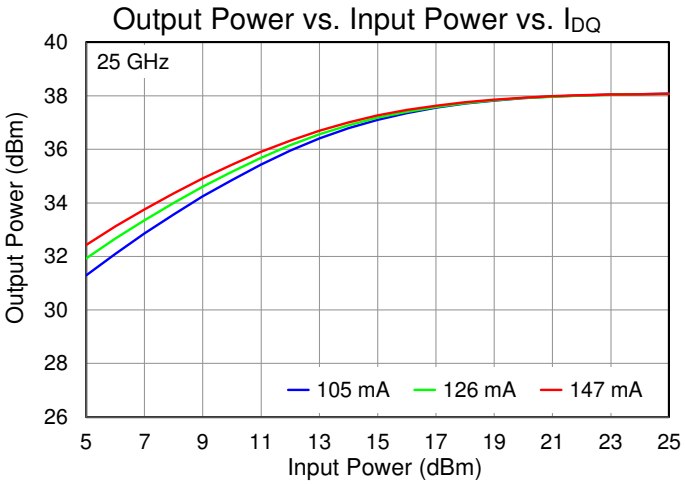


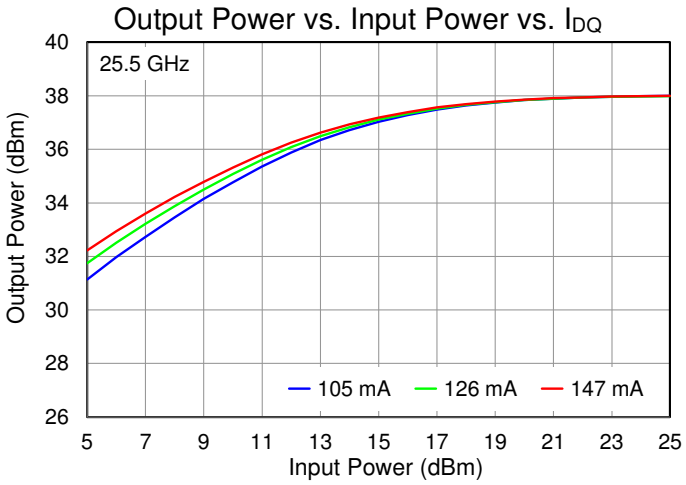
Performance Plots – Large Signal (CW)

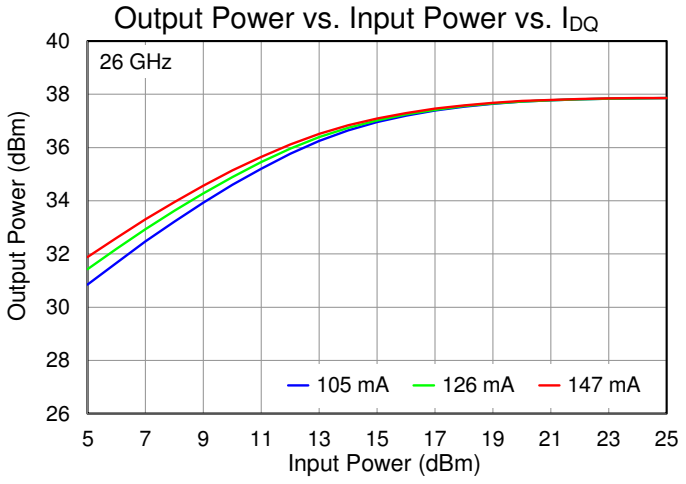
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = 20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

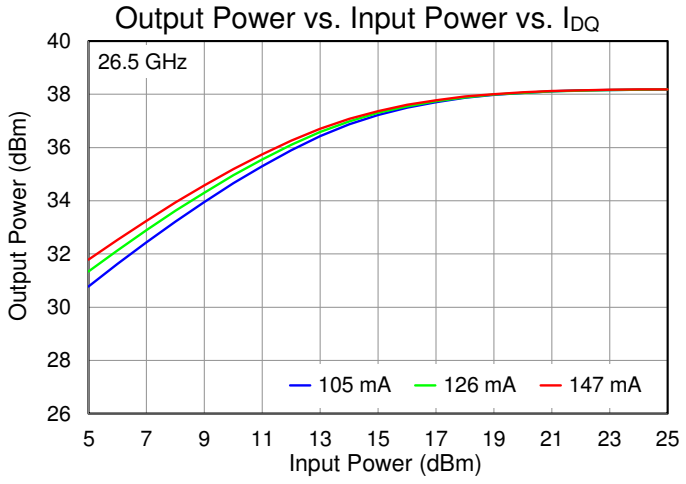






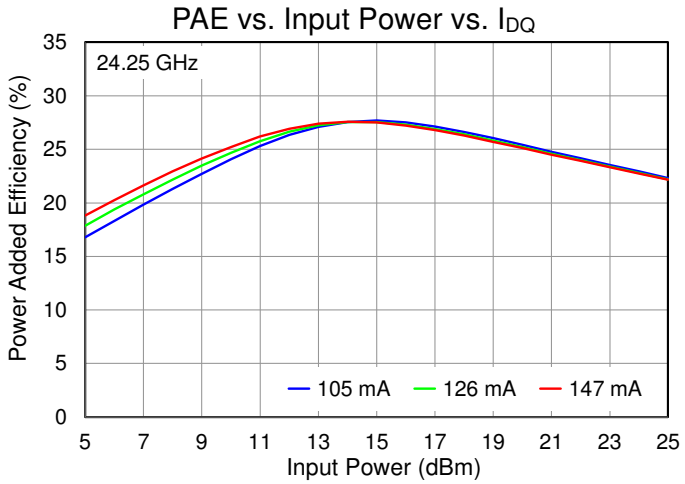


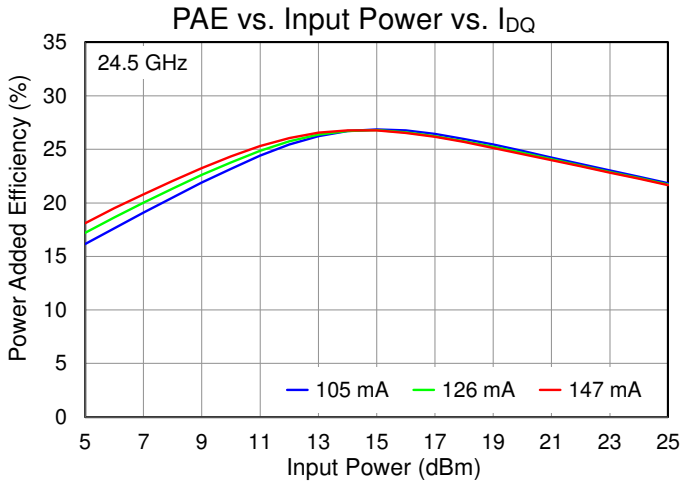


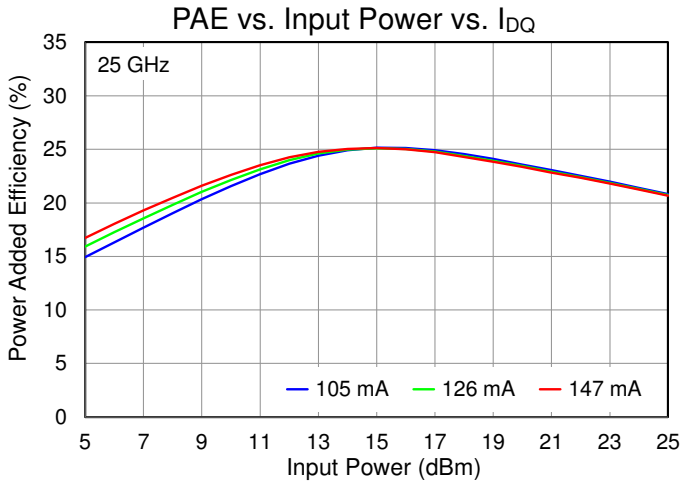


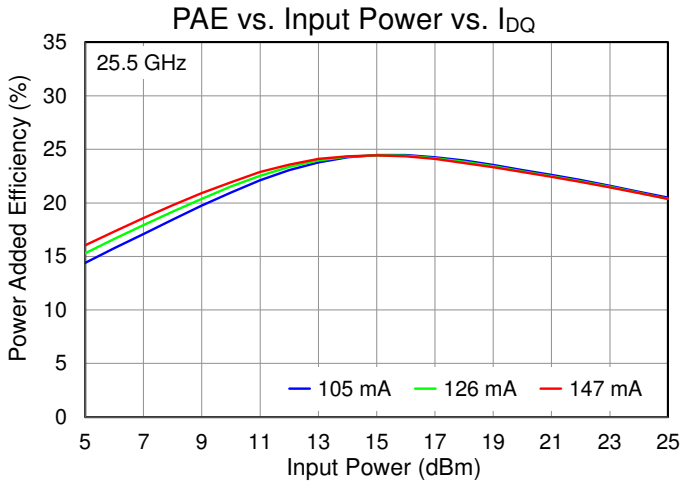
Performance Plots – Large Signal (CW)

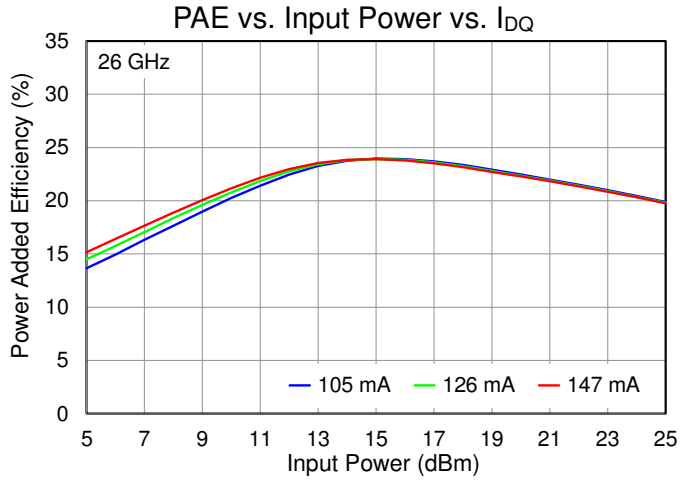
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = 20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

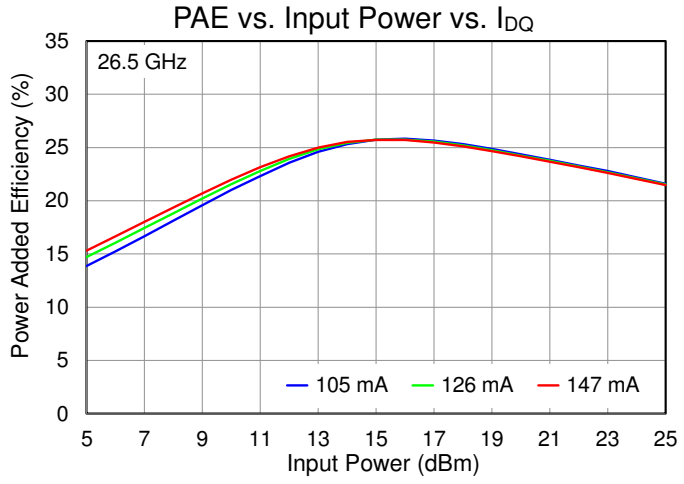






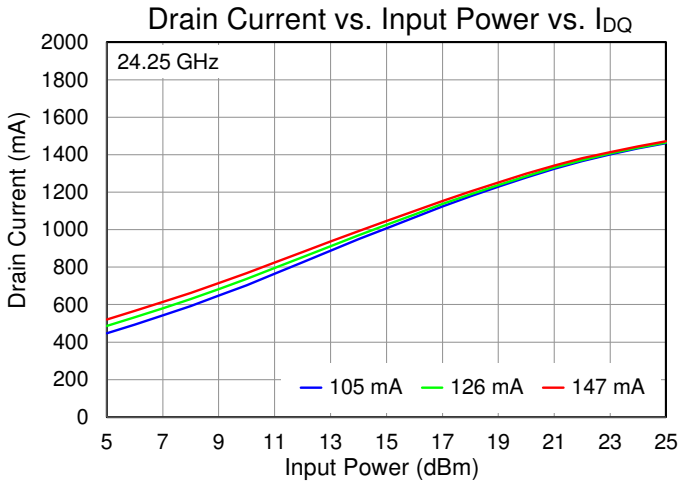


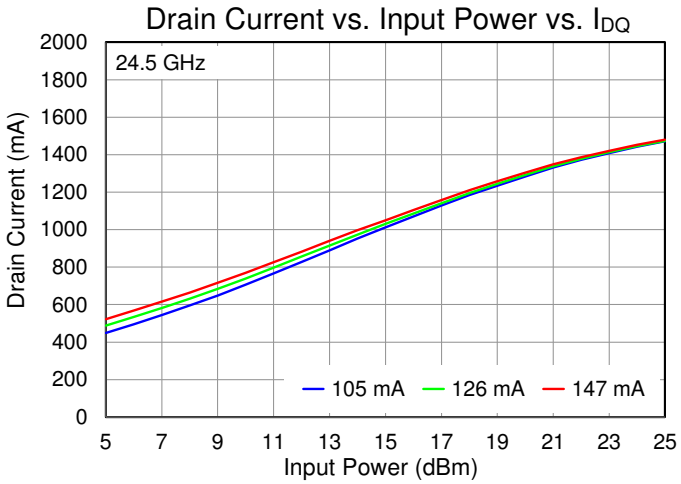


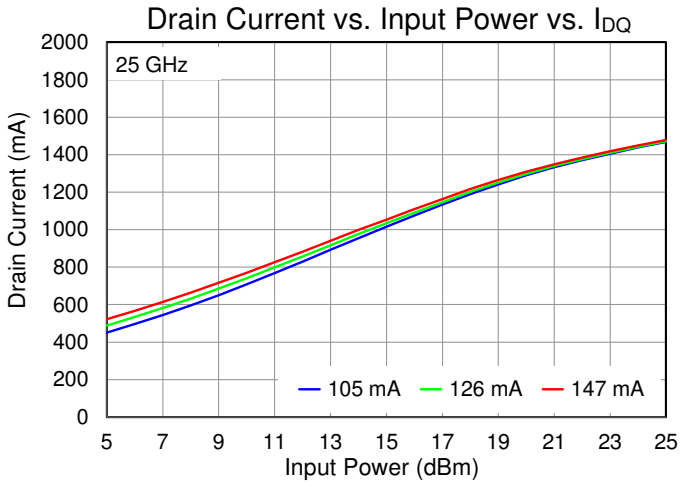


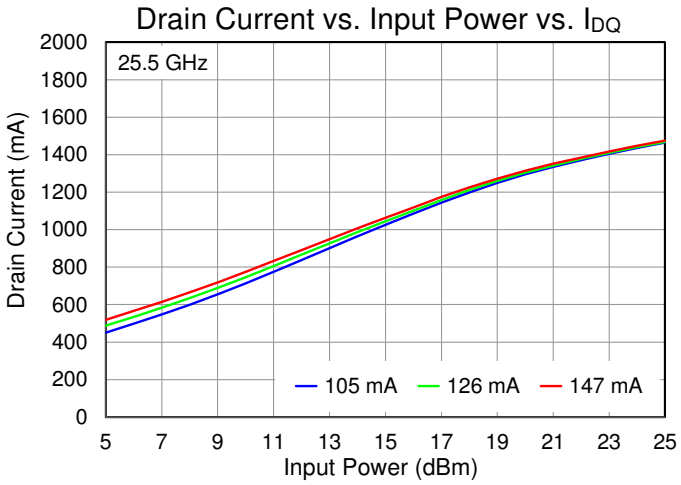
Performance Plots – Large Signal (CW)

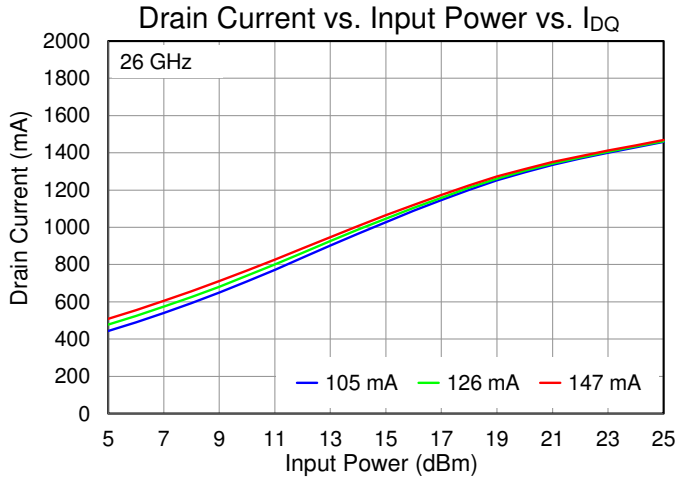
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = 20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

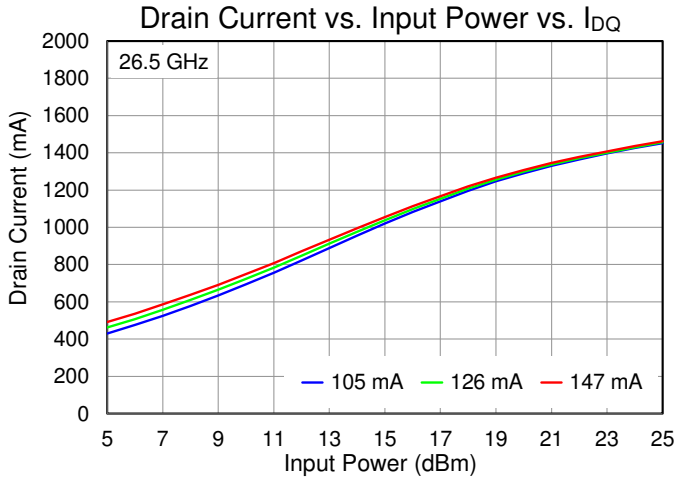






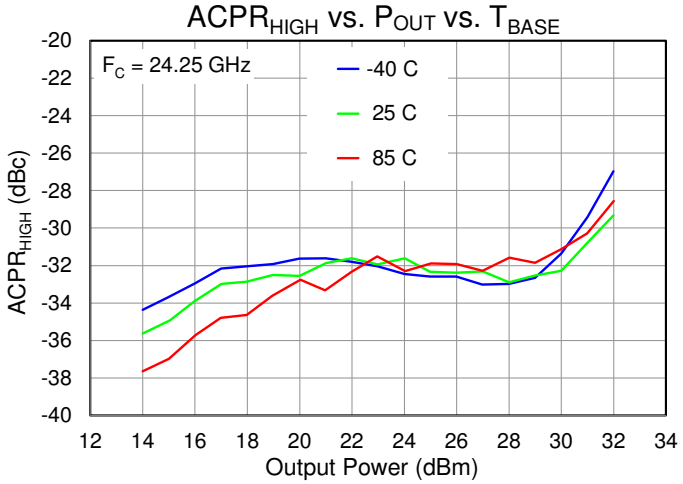


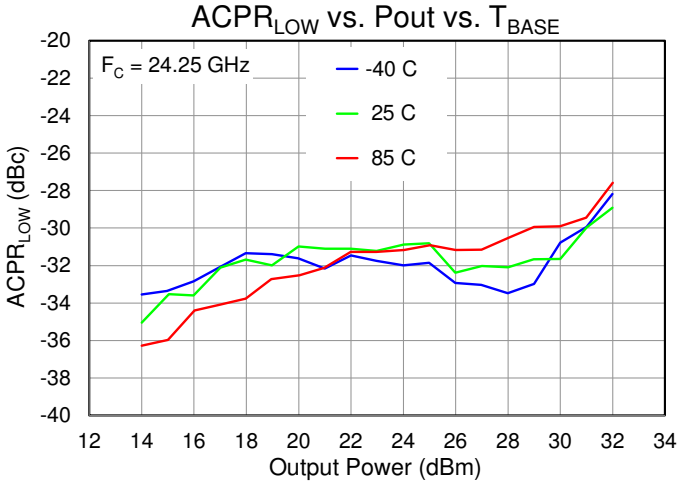


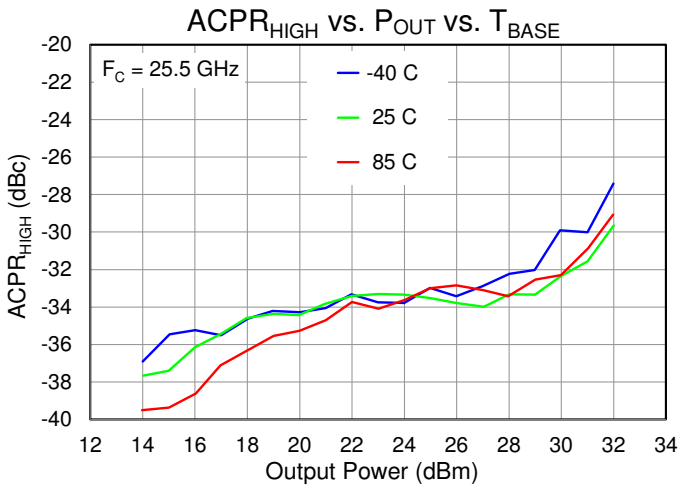


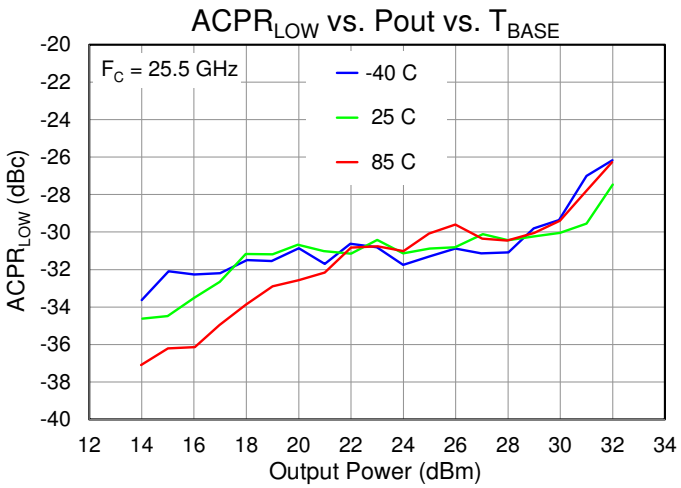
Performance Plots – Linearity (CW)

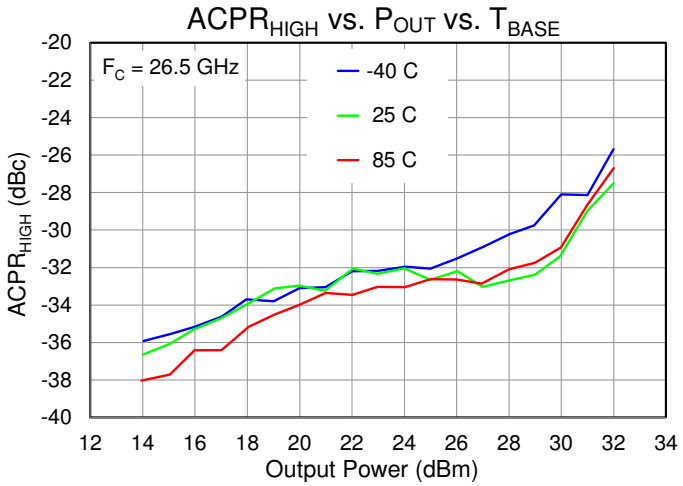
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, 802.11ac, 160 MHz, MSC9, PAR = 12 dB, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

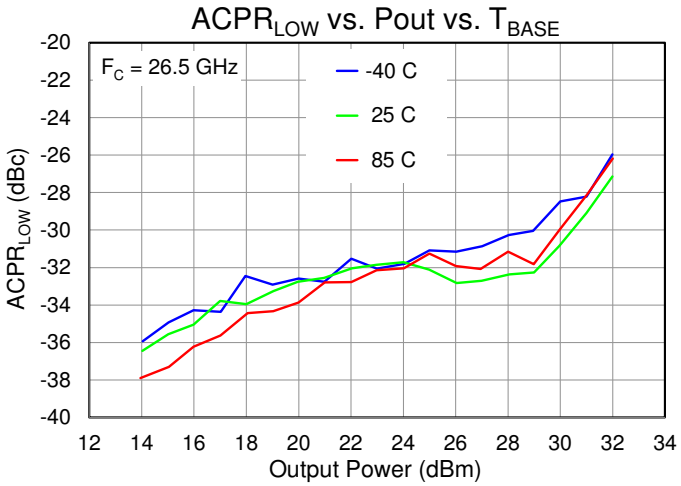






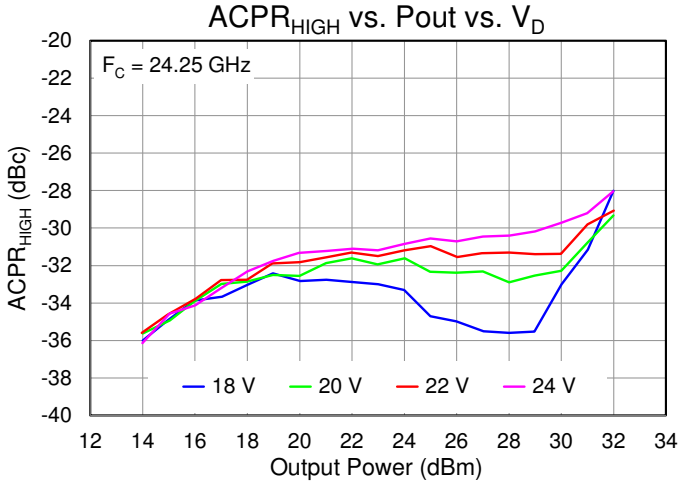


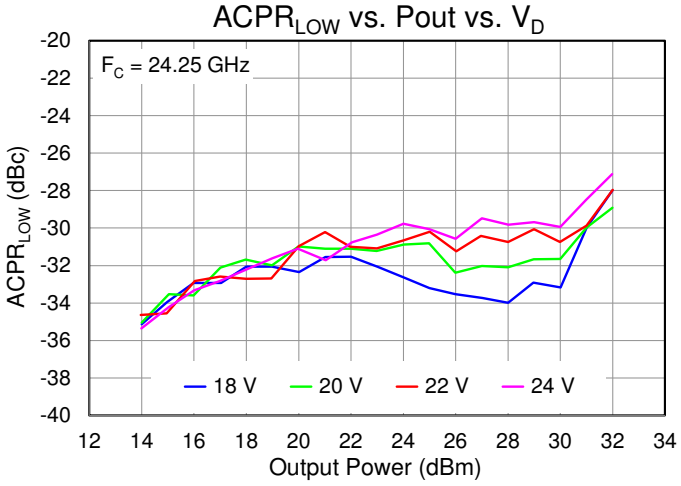


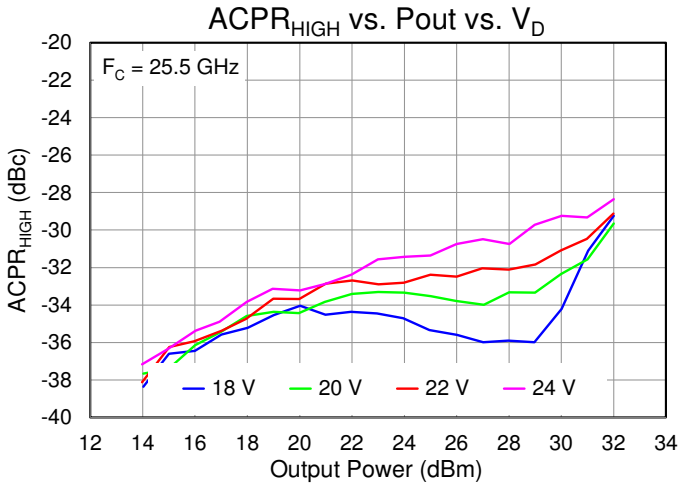


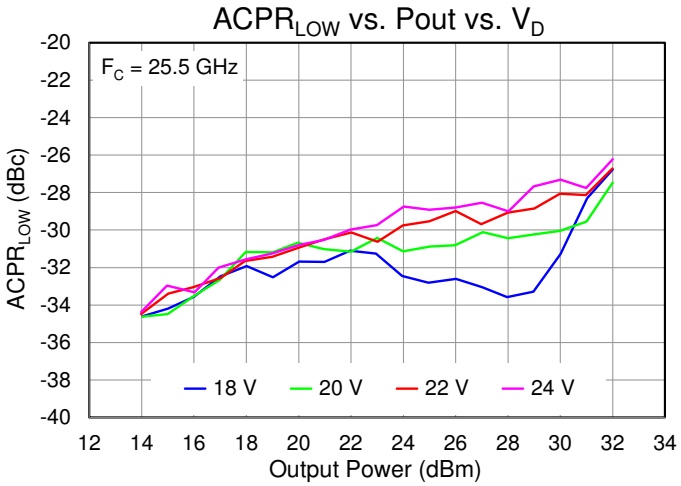
Performance Plots – Linearity (CW)

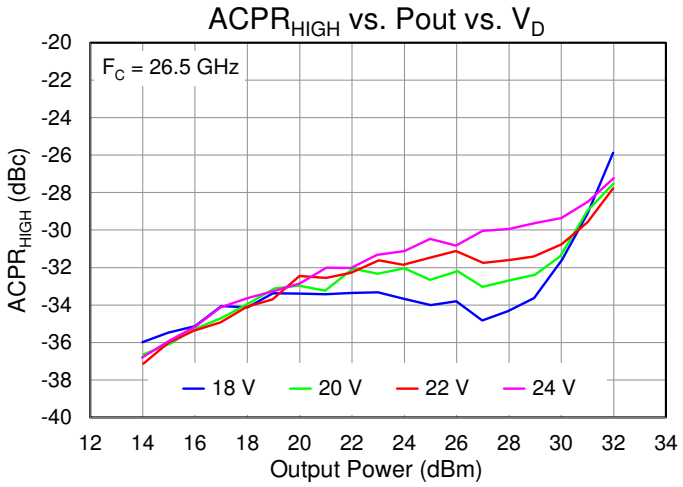
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, 802.11ac, 160 MHz, MSC9, PAR = 12 dB, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

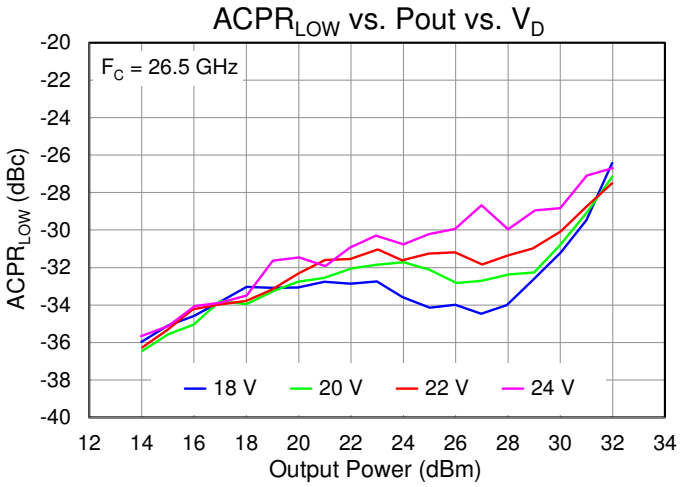






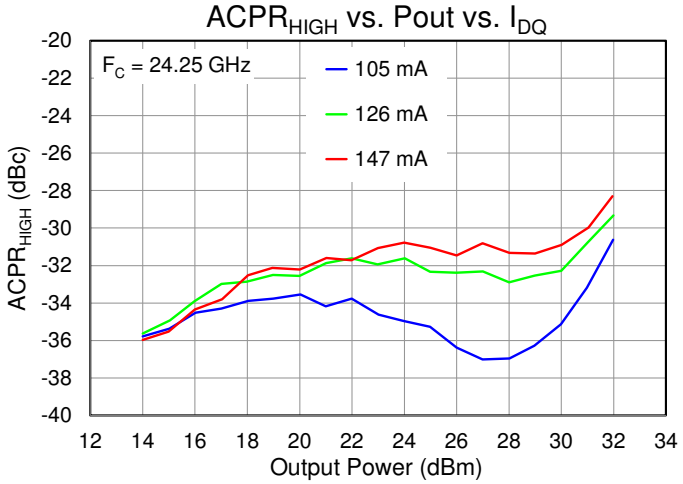


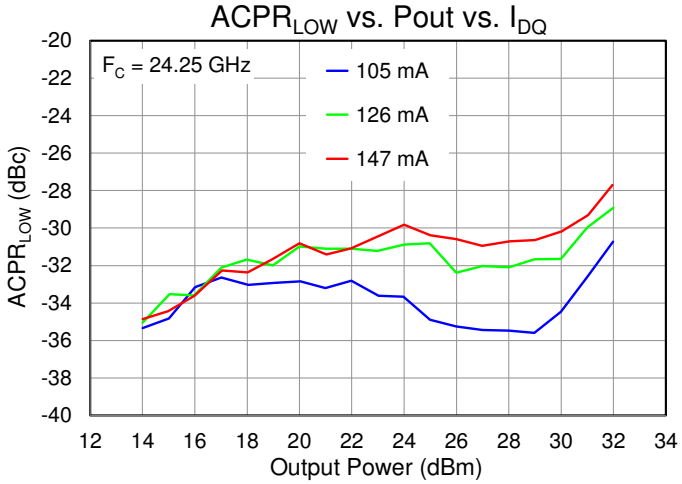


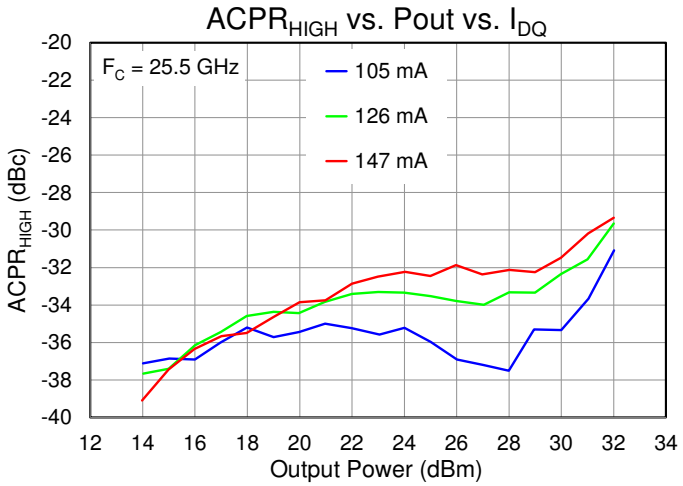


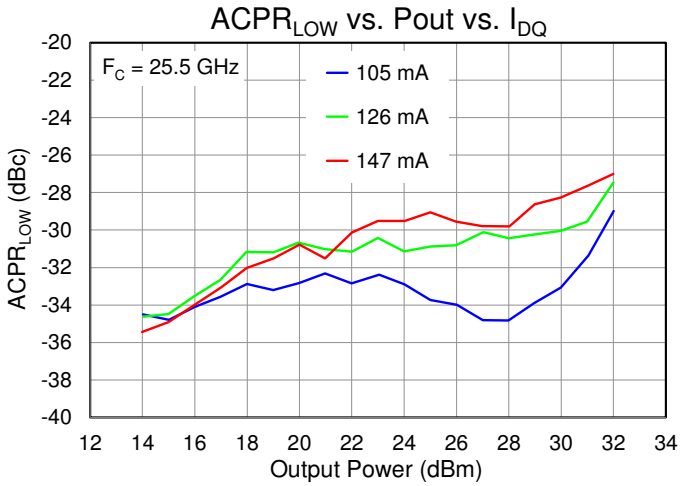
Performance Plots – Linearity (CW)

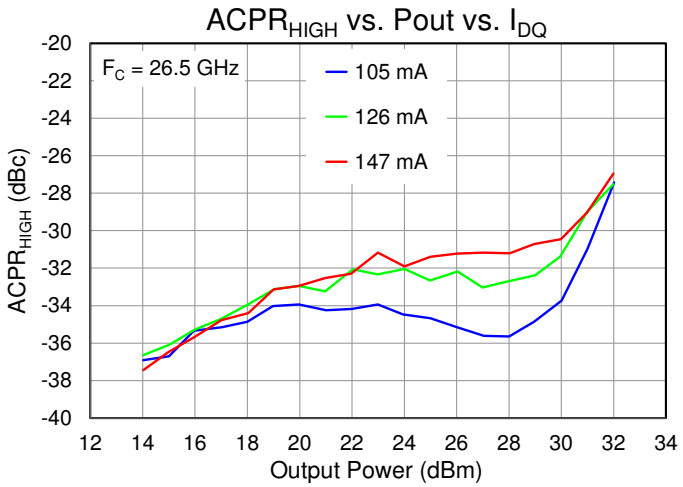
Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, 802.11ac, 160 MHz, MSC9, PAR = 12 dB, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

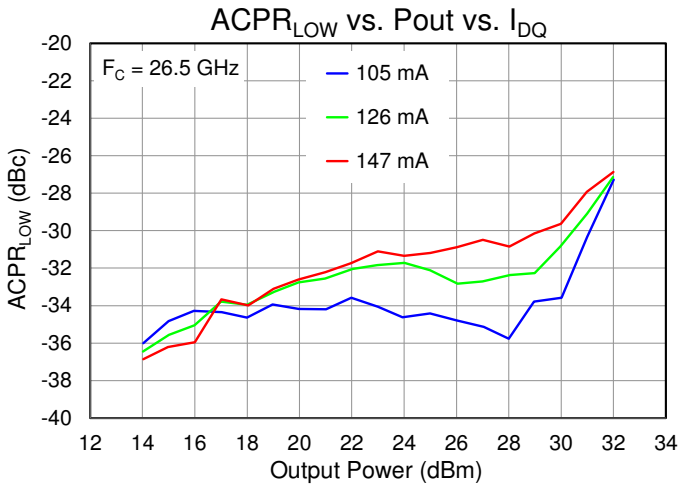








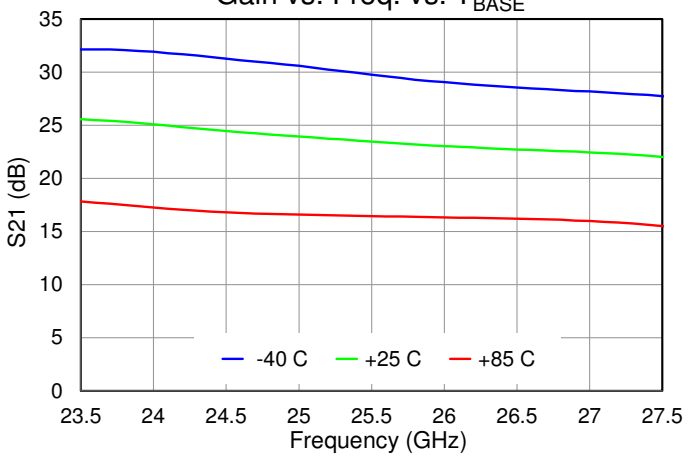




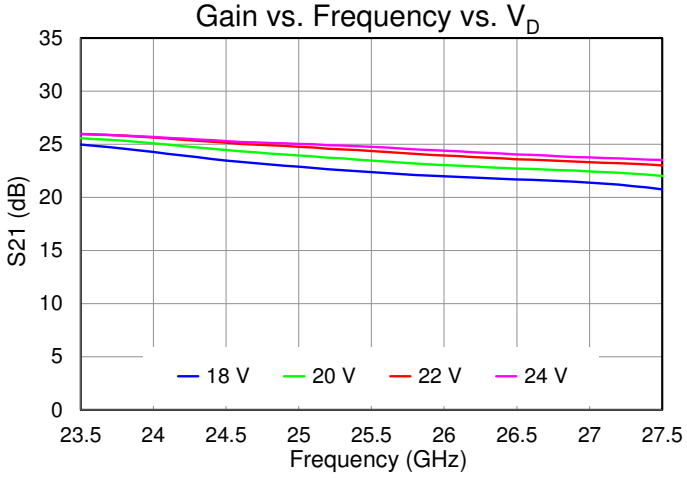
Performance Plots – Small Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).

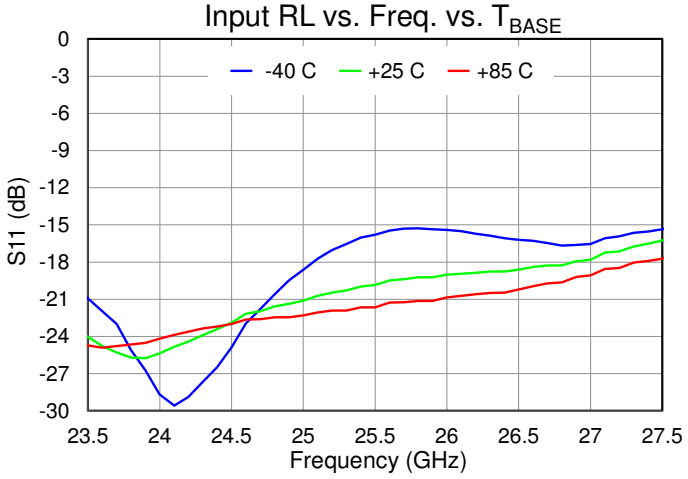
Gain vs. Freq. vs. T_{BASE}



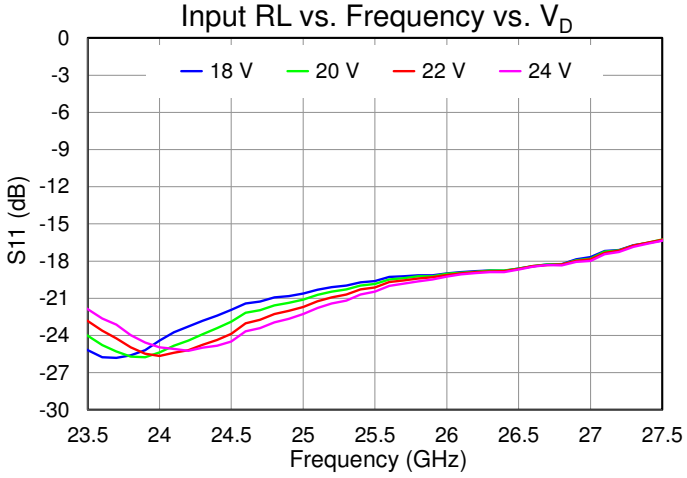
Gain vs. Frequency vs. V_D



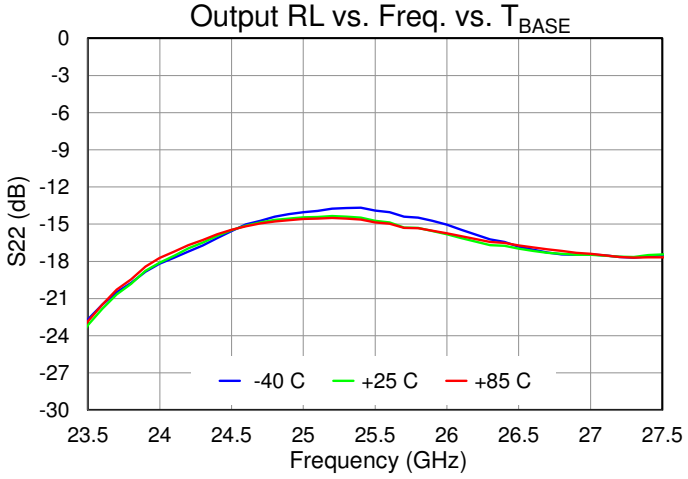
Input RL vs. Freq. vs. T_{BASE}



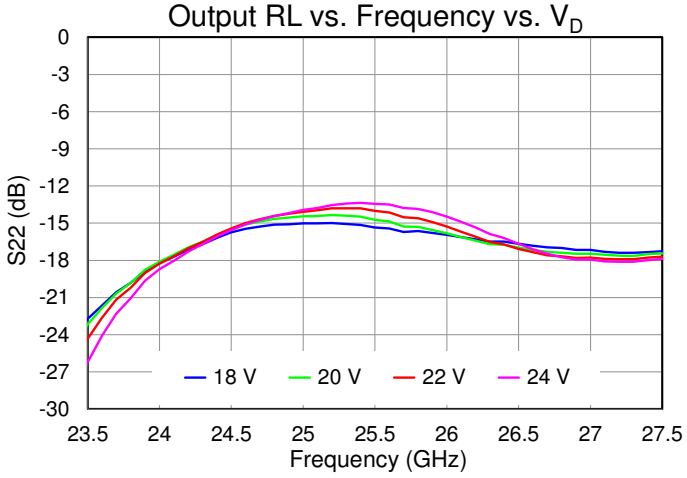
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. T_{BASE}

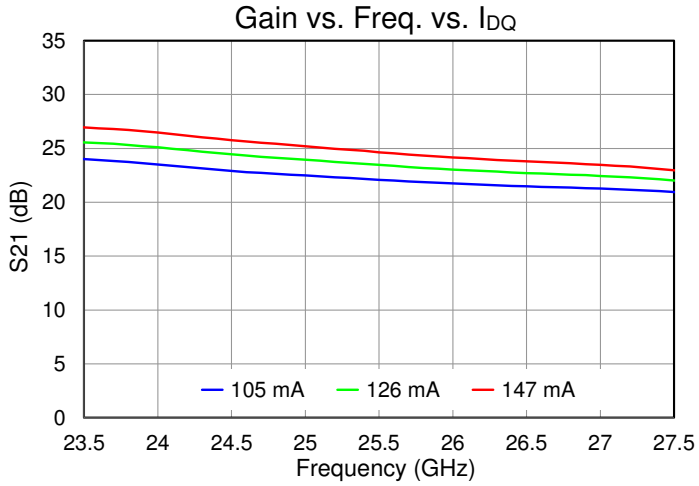


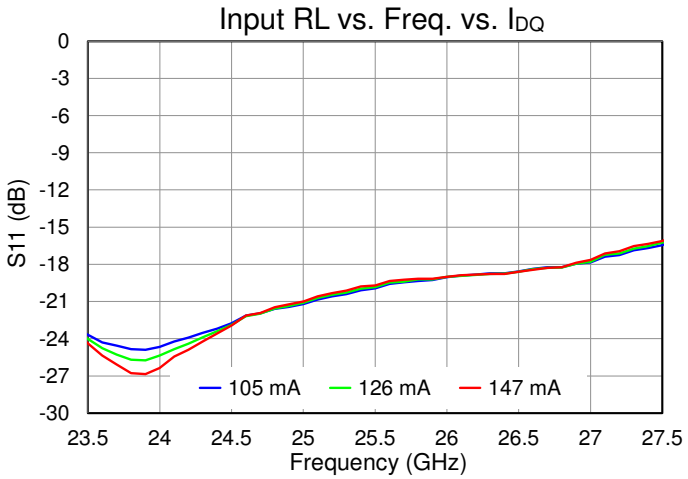
Output RL vs. Frequency vs. V_D

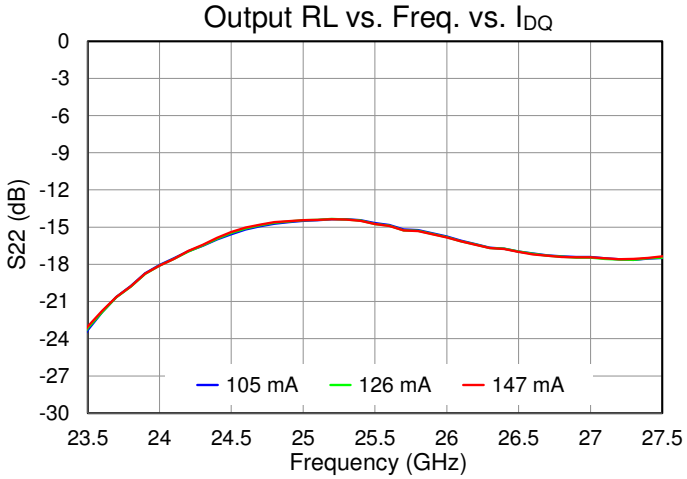


Performance Plots – Small Signal (CW)

Test conditions, unless otherwise noted: CW, V_D = 20 V, I_{DQ} = 126 mA, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA0524).







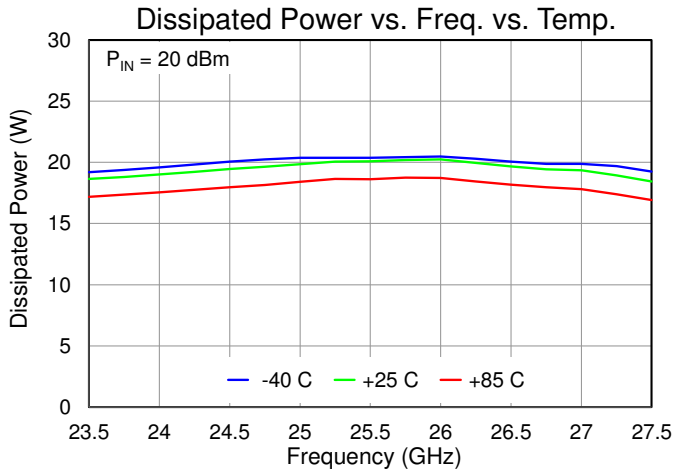
Thermal and Reliability Information

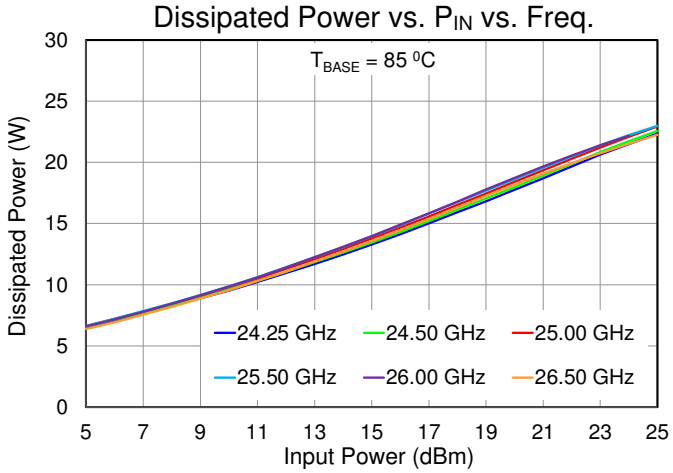
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent, no RF T_{BASE} = 85 °C, V_D = 20 V, I_{DQ} = 126 mA, P_{DISS} = 2.52 W	3.5	ºC/W
Channel Temperature, T_{CH} (2)		94	°C
Thermal Resistance, θ_{JC} (1)	CW, P_{IN} = 20 dBm, T_{BASE} = 85 °C, V_D = 20 V, I_{DQ} = 126 mA, I_{D_DRIVE} = 1195 mA, Freq = 25.75 GHz, P_{OUT} = 37.2 dBm, P_{DISS} = 18.75 W.	3.5	ºC/W
Channel Temperature, T_{CH} (2)		150	°C

Notes:

1. Thermal resistance determined to T_{BASE} (T_{BASE} is backside of package QPA0524; see p. 29 offset temperature based on Qorvo's EVB design for reference).
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note "GaN Device TCHMAX Theta-JC and Reliability Estimates," located here https://www.qorvo.com/products/d/da006480

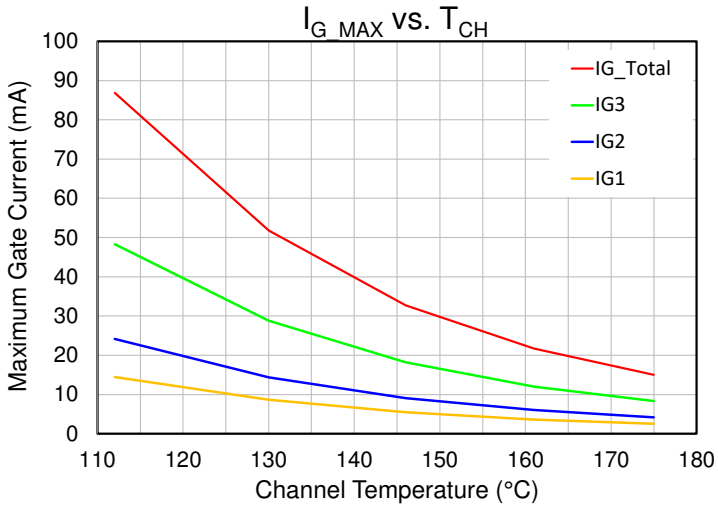
Dissipated Power





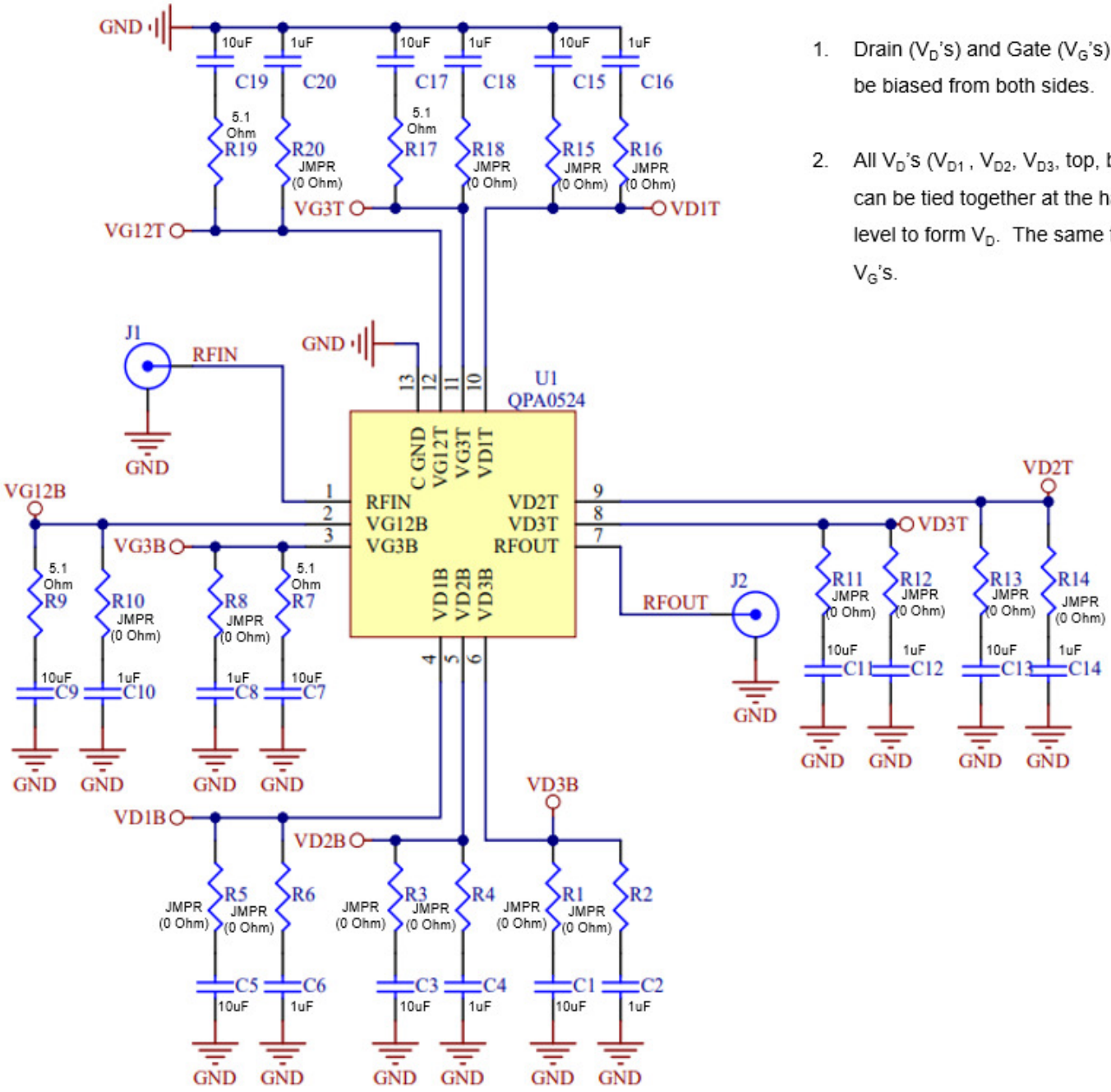
Test conditions, unless otherwise noted.
CW, V_D = 20 V, I_{DQ} = 126 mA, T_{BASE} = 85 ºC (T_{BASE} is back side of QPA0524)

Maximum Gate Current



Channel Temperature is an IR scan equivalent

Applications Information



1. Drain (V_D's) and Gate (V_G's) must be biased from both sides.
2. All V_D's (V_{D1}, V_{D2}, V_{D3}, top, bottom) can be tied together at the harness level to form V_D. The same for all V_G's.

Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C3, C5, C7, C9, C11, C13, C15, C17, C19	10	10 uF	CAP, 10 uF, ±20%, 50V, X5R, 1206	
C2, C4, C6, C8, C10, C12, C14, C16, C18, C20	10	1 uF	CAP, 1 uF, ±10%, 50V, STD, 0603	
R1 – R6, R8, R10 – R16, R18, R20	16	0 Ω	RES, 0 Ohm, JMPR, 0402	
R7, R9, R17, R19	4	5.1 Ω	RES, 5.1 Ohm, ±1%, 1/16W, 0402	
R7, R24	2	0 Ω	RES, 0 Ohm, 1/10W, 0603	
PCB	1		PCB for QPA0524 (Cu-filled vias, see page 26)	Qorvo, Custom
H1, H2	2		DC Header, ST, 2x7, 0.100”, SMD	
J1, J2	2		RF Connector, 2.4mm, F, Pin 0.005, Diel 0.0295	Southwest Microwave
H-Block	1		H-Block, Copper C110, 1.248 x 2.246 x 0.275 in	Qorvo, Custom
S1 – S4	4		Screw, Cap, Socket Head, 2-56X1/8”	
Epoxy Preform			Epoxy 5025E, Preform, 0.003 in thickness	
Solder			Paste, solder, Syntech, Sn63/Pb37	

Bias-Up Procedure

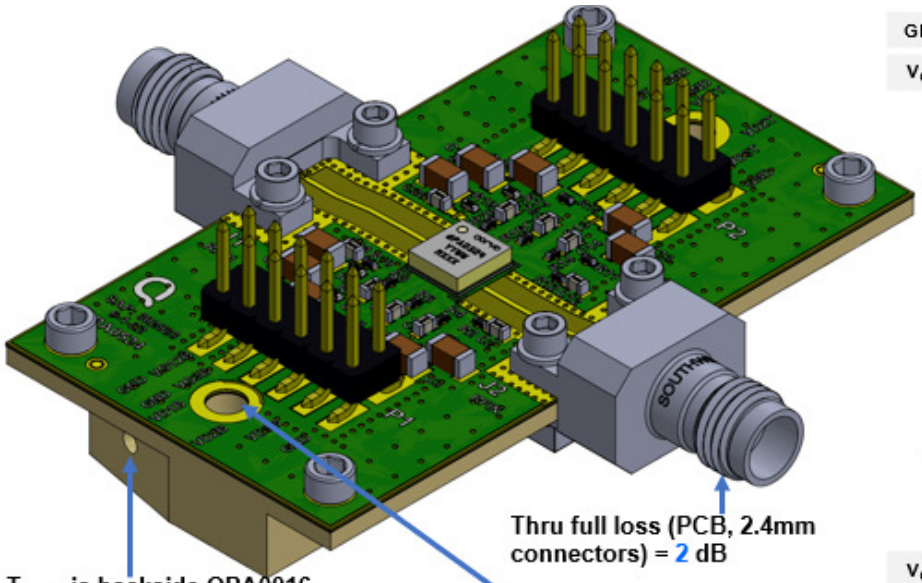
1. Set limit: I_D to 1800 mA, I_G to 20 mA
2. Set V_G = –4 V
3. Set V_D = +22 V. Ensure I_D ~ 0 mA
4. Adjust V_G more positive until I_{DQ} = 126 mA; V_G ≈ -2.2 V +/- 0.7 V typical
5. Wait 15 seconds; then repeat step 4
6. Apply RF signal

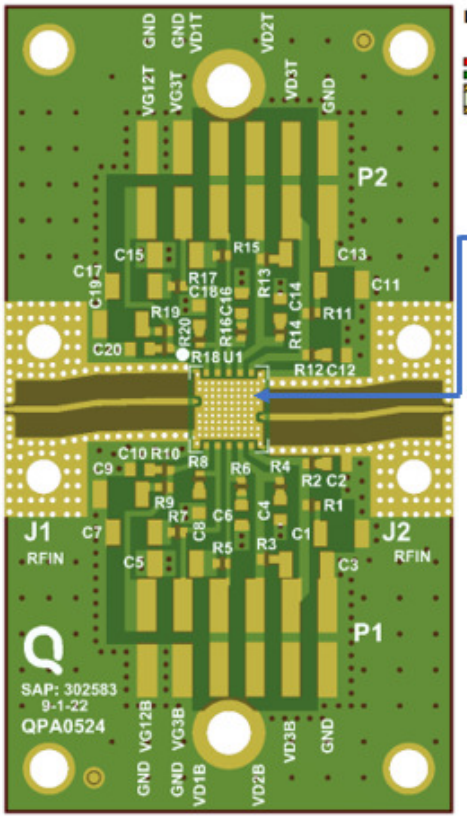
Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to –4 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Wait 5 seconds
6. Turn off V_G supply

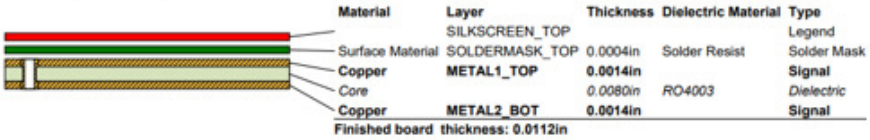
All V_D’s (V_{D1}, V_{D2}, V_{D3}, top, bottom) can be tied together at the harness level to form V_D. The same for all V_G’s

Evaluation Board (EVB) Layout



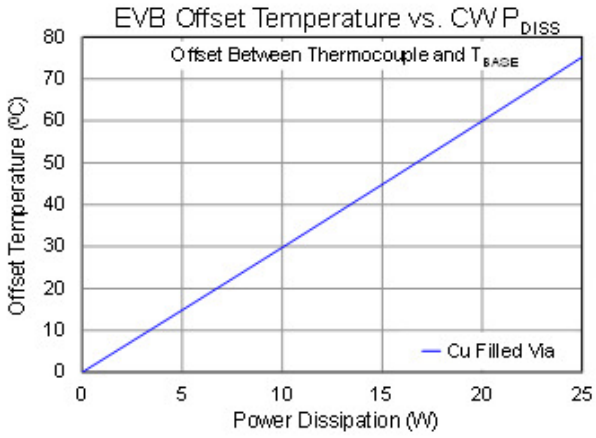


LAYER STACK LEGEND

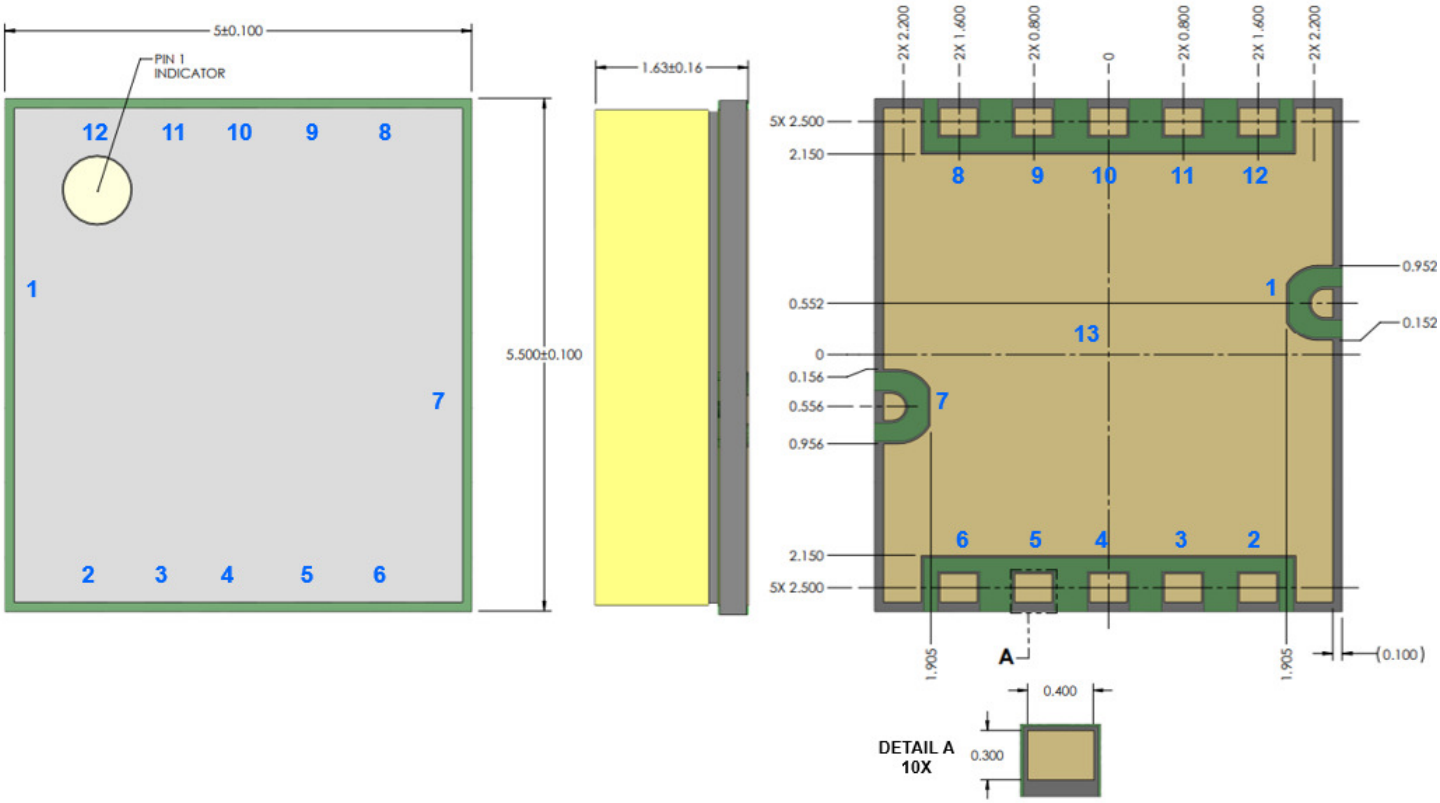


Material	Layer	Thickness	Dielectric Material	Type
	SILKSCREEN_TOP			Legend
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask
Copper	METAL1_TOP	0.0014in		Signal
Core		0.0080in	RO4003	Dielectric
Copper	METAL2_BOT	0.0014in		Signal
Finished board thickness: 0.0112in				

Cu Filled Vias (as shown 90 vias) or
Cu Coined Via (best recommended)
Offset Temp. (Thermocouple – T_{BASE}) @ 18.75 W P_{DISS}:
Cu filled: ~ 58 °C
Cu coined: ~ 40 °C



Mechanical Information



Dimensions (unless otherwise specified): mm.
Tolerances (unless noted): .xx = ± .25; .xxx = ± .100; .xxxx = ± .0254; angles = 0.5^0
Package is air-cavity, non-hermetic, epoxy sealed; lid is IT 180A; base is laminate; leads are Au plated.

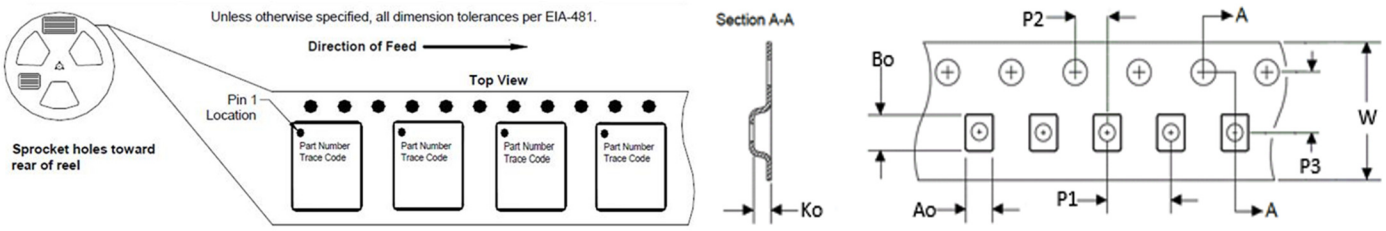
Pin Description

Pin Number	Symbol	Description
1	RF_{IN}	RF Input. Matched to 50 Ω, DC shorted to ground
2, 12	V_{G12}	Gate voltage for stage 1 and 2 (1)
3, 11	V_{G3}	Gate voltage for stage 3 (1)
4, 10	V_{D1}	Drain voltage for stage 1 (1)
5, 9	V_{D2}	Drain voltage for stage 2 (1)
6, 8	V_{D3}	Drain voltage for stage 3 (1)
7	RF_{OUT}	RF Output. Matched to 50 Ω, DC shorted to ground
13	GND	Ground (backside paddle); grounded on PCB; Cu-coined via (most recommended) or Cu-filled vias to minimize inductance and thermal resistance.

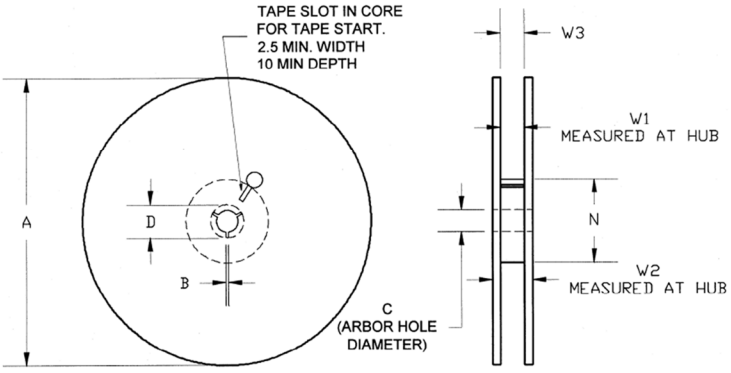
1. External bypassing required; refer to page 23 for recommendation.

Tape & Reel Information

Standard T/R size = 250 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.207	5.25
	Width	B0	0.228	5.8
	Depth	K0	0.079	2
	Pitch	P1	0.315	8
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	P3	0.217	5.5
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.724	18.4
	Space Between Flange	W1	0.488	12.4
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

Solderability

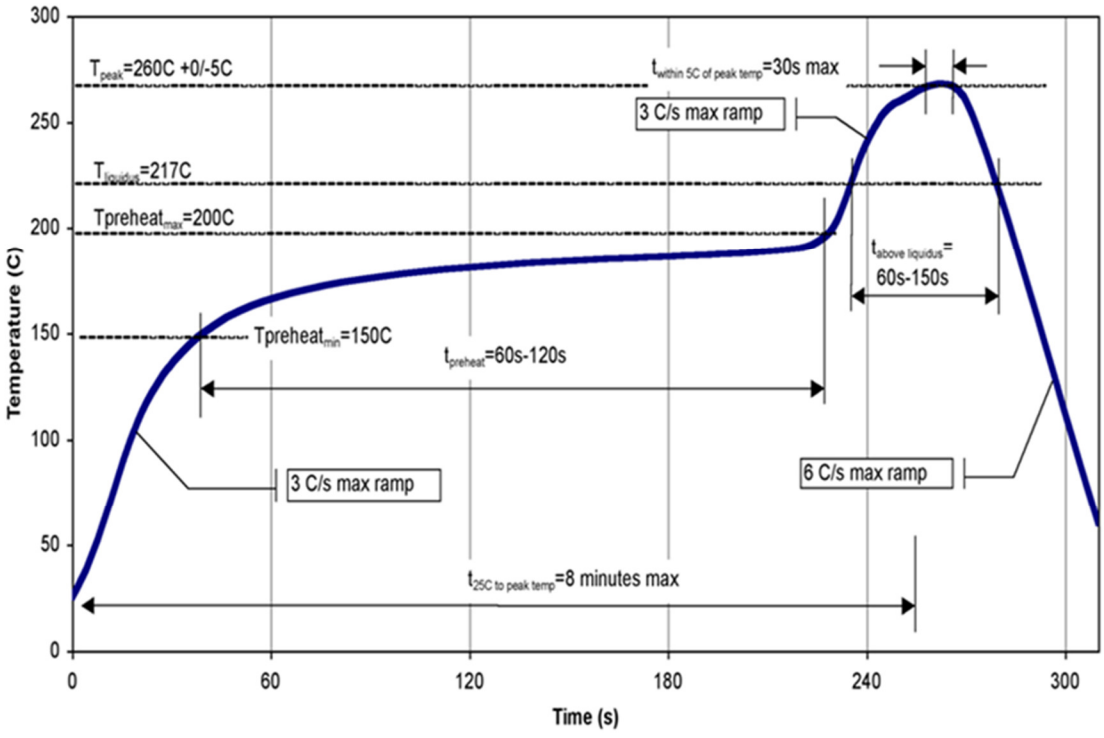
Compatible with the latest version of J-STD-020, lead-free solder, 260 °C peak reflow temperature

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended. Contact Qorvo for latest aqueous wash capabilities.

Contact plating: Ni-Au

Solder rework not recommended.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C1	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	5A	IPC/JEDEC J-STD-020

Caution!

ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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