



QPA4605

5 W, 48 V, 4.5 – 4.6 GHz, GaN PAM

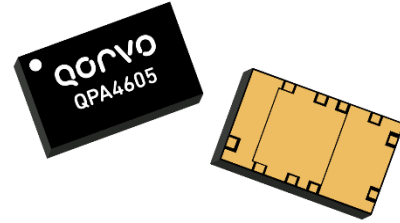
Product Overview

The QPA4605 is an integrated 2-stage Power Amplifier Module designed for massive MIMO applications with 5 W RMS at the device output covering frequency range from 4.5 to 4.6 GHz.

The module is 50 Ω input and output and requires minimal external components. The module is also compact and offers a much smaller footprint than traditional discrete component solutions.

The QPA4605 incorporates a driver and Doherty final stage delivering high power added efficiency for the entire module at 5 W average power.

RoHS compliant

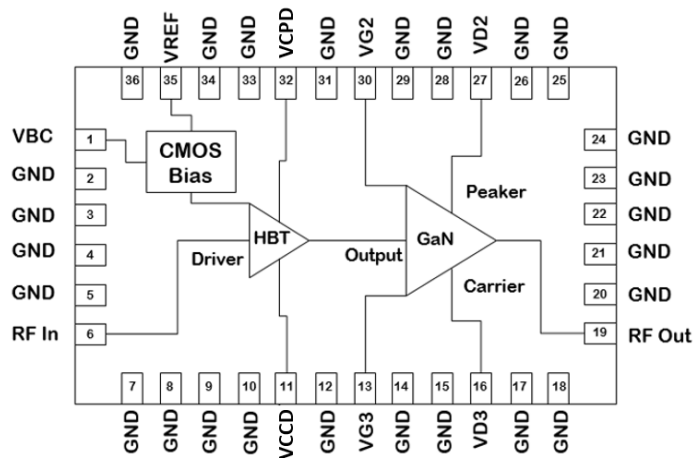


6 x 10 mm Over Mold Laminate

Key Features

- Operating Frequency Range: 4.5 – 4.6 GHz
- Operating Drain Voltage: +48 V
- 50 Ω input / output
- Integrated Doherty Final Stage
- Gain at 5W avg.: 25.4dB
- Power Added Efficiency at 5W avg.: 39.7%
- 6x10 mm Plastic Surface Mount Package

Functional Block Diagram



Applications

- WCDMA / LTE
- Macrocell Base Station
- Microcell Base Station
- Small Cell
- Active Antenna
- 5G Massive MIMO
- General Purpose Applications

Ordering Information

Part Number	Description
QPA4605SR	7" Reel – 100 Pieces
QPA4605TR13	13" Reel – 2500 Pieces
QPA4605EVB-01	4.5 – 4.6GHz EVB

Absolute Maximum Ratings

Parameter	Rating
Breakdown Voltage (V_{DG})	+165 V
Gate Voltage Range (V_G)	-7 to +2 V
Drain Voltage (V_D)	+55 V
RF Input Power, pulsed, 10%, 100us	+25 dBm
VSWR Mismatch, P3dB Pulse (10% Duty Cycle, 100 μ s Width), $T = +25^\circ\text{C}$	10:1
Storage Temperature	-65 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Peaker Gate Voltage (V_{G2})		-4.2		V
Carrier Gate Voltage (V_{G3})		-2.8		V
Supply Voltages HBT (V_{CC})		+5.0		V
CMOS Bias Controller (V_{BC})	+1.8			V
CMOS Bias Controller (V_{REF})	+3.3	+5.0	+5.5	V
Supply Voltages GaN ($V_{D2,3}$)		+48		V
Quiescent Current (I_{DQ3})		40		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range		4500		4600	MHz
Driver Quiescent Current (I_{CCD})			55		mA
Carrier Quiescent Current (I_{DQ3})			40		mA
Gain ^{1,2}	$P_{OUT} = 37$ dBm	23.0	25.4		dB
Power Added Efficiency (PAE) ^{1,2}	$P_{OUT} = 37$ dBm	35.5	39.7		%
Raw ACLR ^{1,2}	$P_{OUT} = 37$ dBm		-26.5	-20.0	dBc
P_{sat} ³	$P_{IN} = 24$ dBm, $f = 4600$ MHz	44.6	45.7		dBm
V_{EN} Low ⁴		0		0.63	V
V_{EN} High ⁴		1.17		V_{CC}	V

Test conditions unless otherwise noted:

- $V_{REF} = 5V$, $V_{CC} = 5V$, $V_{BC} = 1.8V$, $V_{G2} = V_{G2_Set} - 1.5V$, $I_{DQ3} = 40mA$, $V_{D2} = V_{D3} = +48V$, $T = +25^\circ\text{C}$, using a single-carrier, 20 MHz LTE signal with 7.8 dB PAR at 0.01% CCDF on the reference design fixture.
- Typical parameter value averaged over 4500, 4550, and 4600MHz frequency values.
- $V_{REF} = 5V$, $V_{CC} = 5V$, $V_{BC} = 1.8V$, $V_{G2} = V_{G2_Set} - 1.5V$, $I_{DQ3} = 40mA$, $V_{D2} = V_{D3} = +48V$, $T = +25^\circ\text{C}$, using Pulsed CW, 10% Duty Cycle, PW 100us, on the reference design fixture.
- V_{EN} guaranteed by design.

Thermal Information

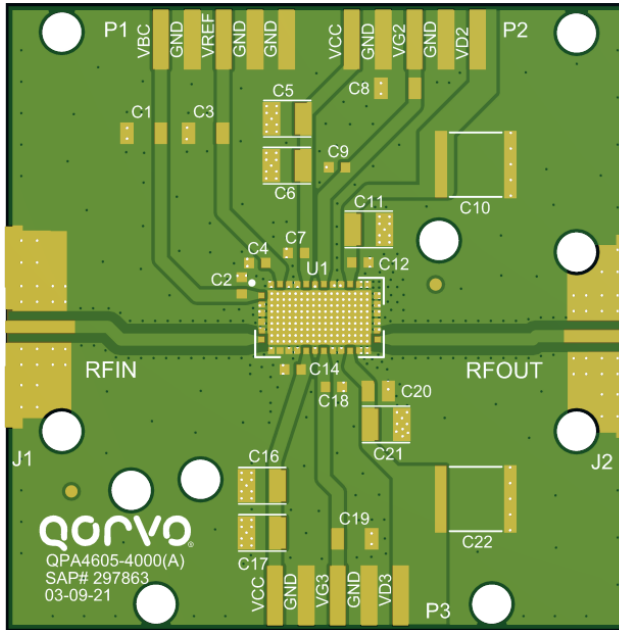
Parameter	Conditions	Values	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	$T_{CASE} = +85^\circ\text{C}$, $T_{CH} = 116^\circ\text{C}$ CW: $P_{DISS} = 7.59$ W, $P_{OUT} = 5$ W	4.08	$^\circ\text{C/W}$

Notes:

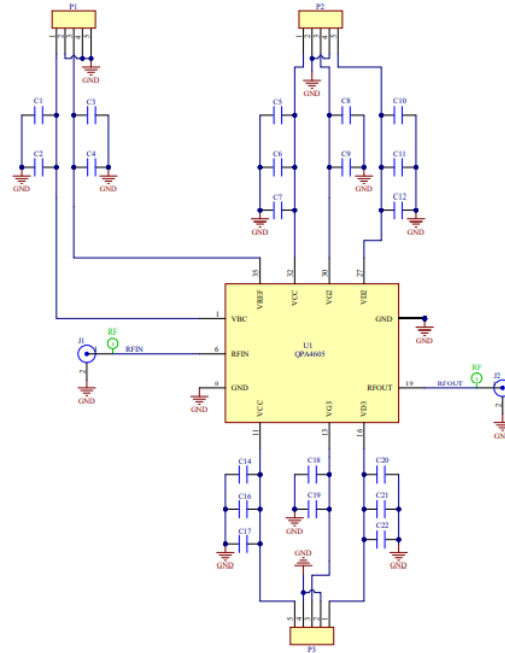
- Thermal resistance is measured to package backside.
- Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

QPA4605 4.5 – 4.6 GHz Reference Design

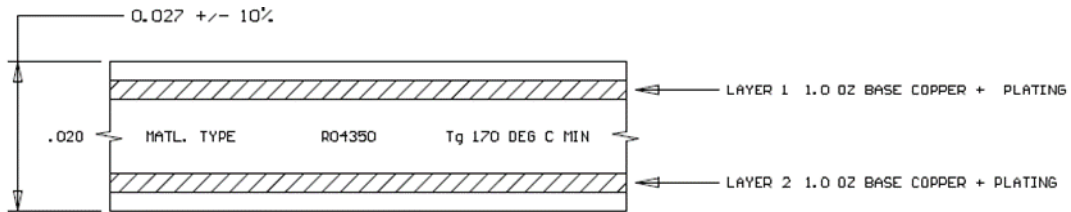
EVB Layout



EVB Schematic



PCB Stackup and Material



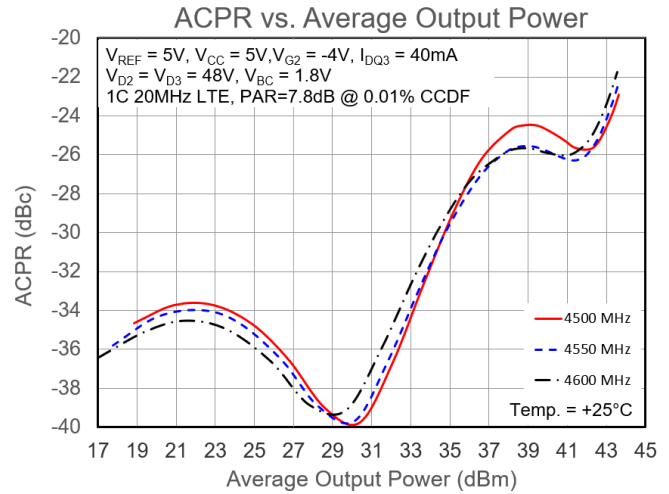
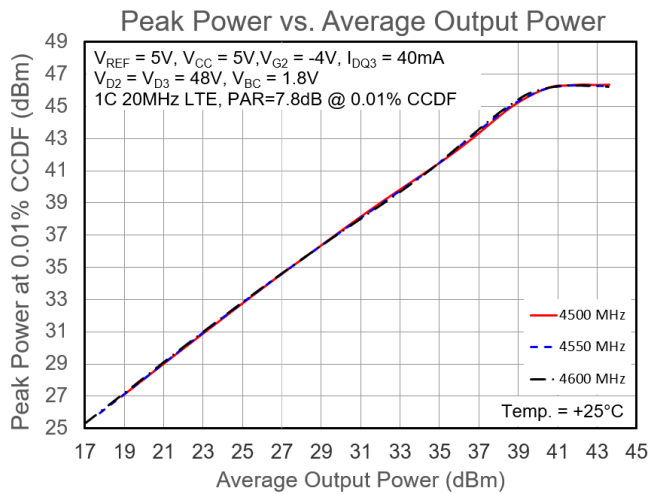
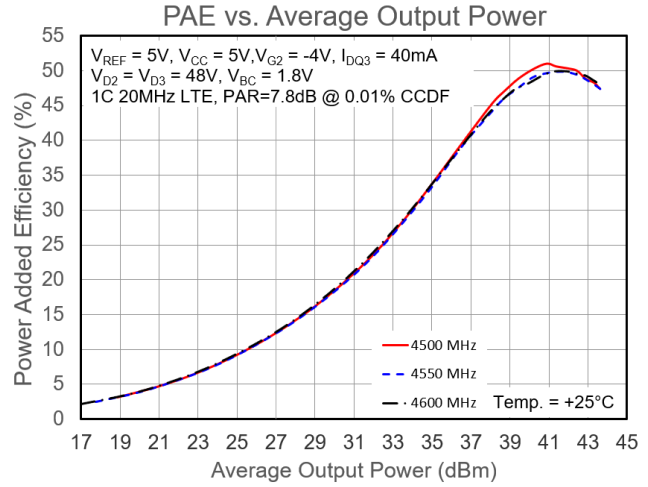
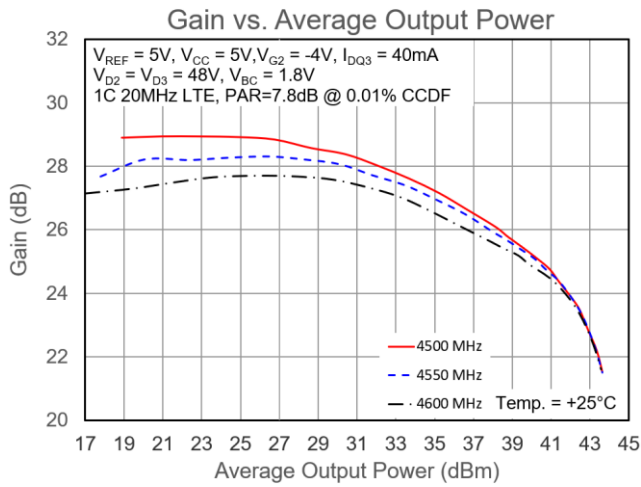
Notes:

1. All dimensions are in inches.
2. PCB is soldered on a 2 in. x 2 in. copper base plate with 0.25 in. thickness.

Bill of Materials – QPA4605 4.5 – 4.6 GHz Evaluation Board

Reference Des.	Value	Description	Manufacturer	Part Number
C2, C4, C7, C9, C12, C14, C18, C20	0.022 μ F	CAP, 0.022 μ F, 10%, 100V, X7R, 0603	TDK	CGA3E2X7R2A223K080AA
C3, C8, C19	4.7 μ F	CAP, 4.7 μ F, 10%, 50V, X7R, 1206	Murata	GRM31CR71H475KA12L
C5, C6, C16, C17	10 μ F	CAP, 10 μ F, 10%, 50V, X7R, 1210	Murata	GRM32ER71H106KA12L
C10, C22	10 μ F	CAP, 10 μ F, 20%, 100V, X7S, 2220	TDK	C5750X7S2A106M230KB
C11, C21	4.7 μ F	CAP, 4.7 μ F, 10%, 100V, X7S, 1206	Murata	GRM31CC72A475KE11L
J1, J2		Connector, SMA, 4-Hole Panel Mount Jack	Gigalane	PAF-S00-000
P1, P2, P3		Connector, HDR, ST, PLRZD, 5-Pin, 0.100"	AMP	640454-5
U1		5 W 4.5 – 4.6 GHz PA Module	Qorvo	QPA4605

Performance Plots

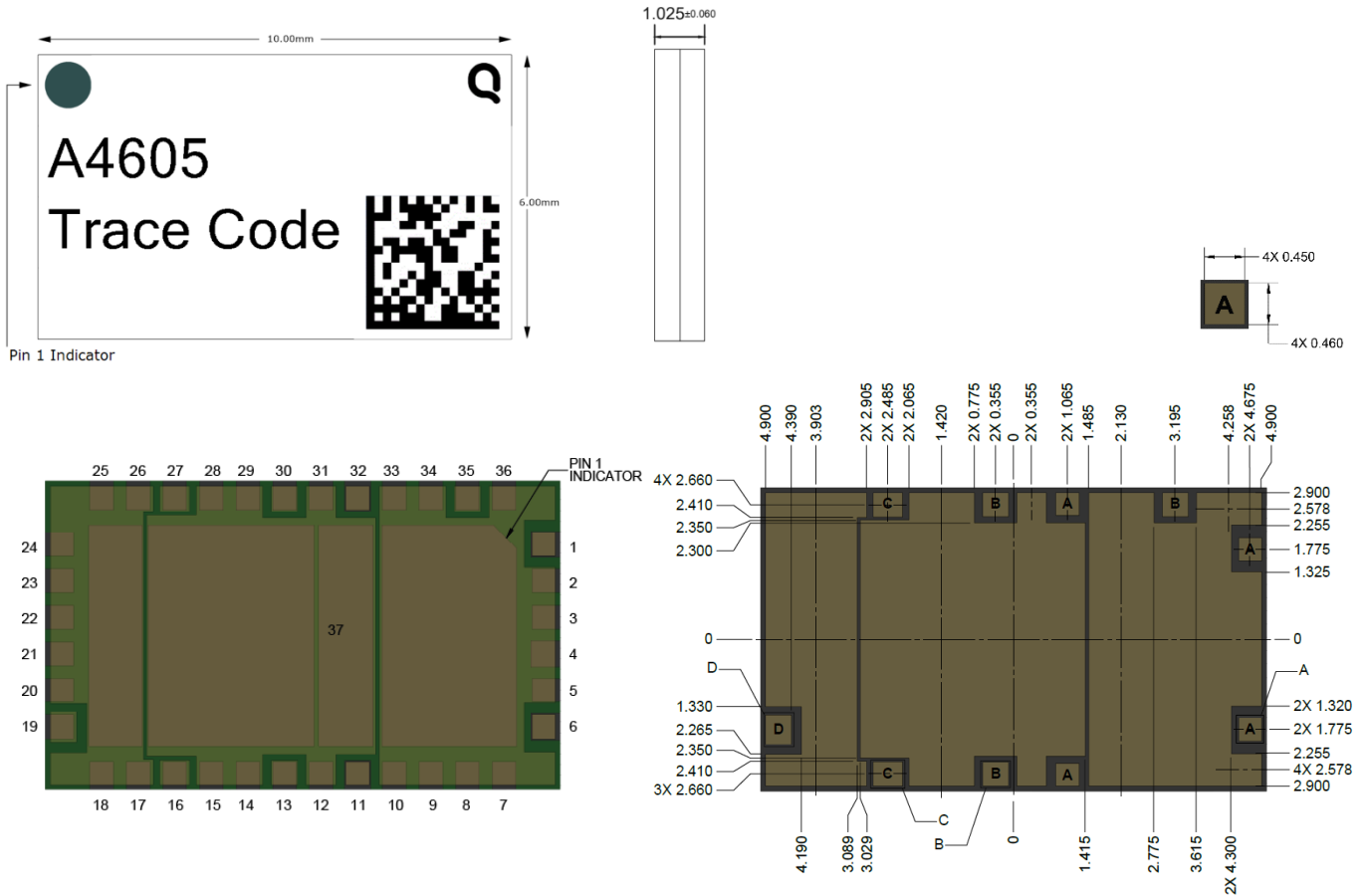


Note:

Test conditions unless otherwise noted: $V_{REF} = 5V, V_{CC} = 5V, V_{BC} = 1.8V, V_{G2} = -4V, I_{DQ3} = 40mA, V_{D2} = V_{D3} = 48V, T = +25°C$, tested using a single-carrier, 20 MHz LTE signal with 7.8 dB PAR at 0.01% CCDF on a reference design fixture.

Package Marking and Dimensions

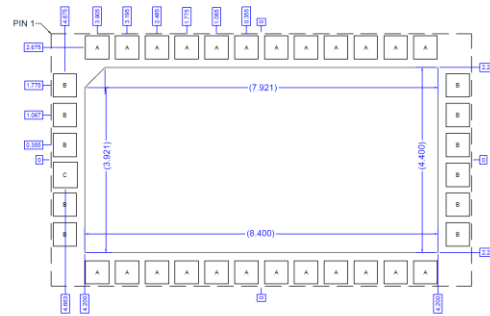
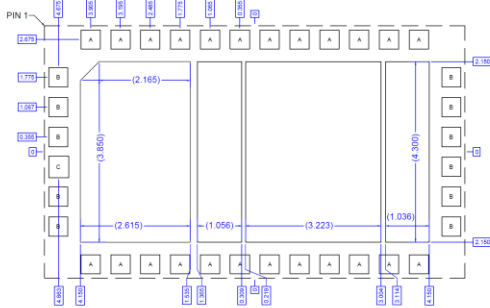
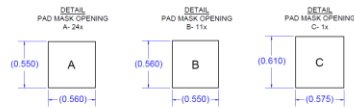
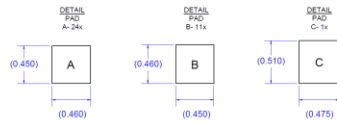
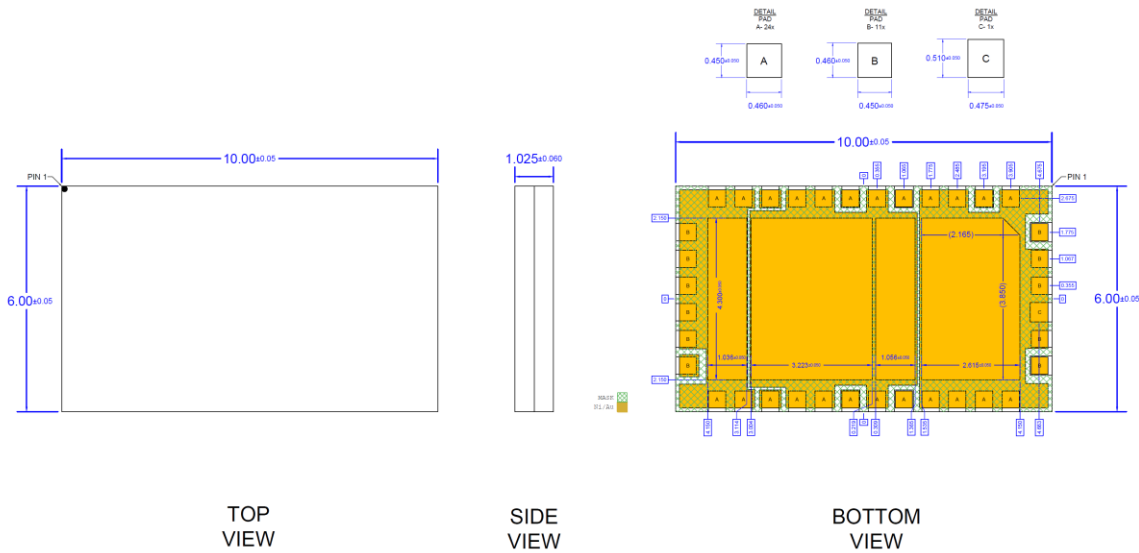
Marking: Qorvo Logo
 Part Number – QPA4605



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. General tolerance is ±0.05 unless otherwise shown.
3. Part is overmold encapsulated.
4. Contact plating is ENEPIG. Au nominal thickness is 0.095 ± 0.025 μm.

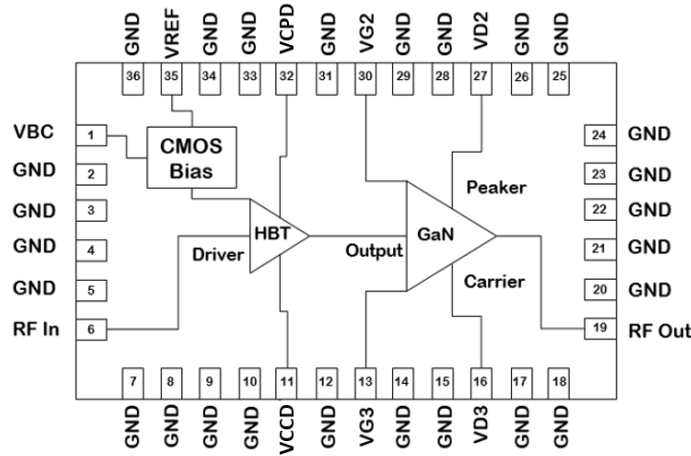
PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. General tolerance is ± 0.05 unless otherwise shown.
3. Part is overmold encapsulated.
4. Contact plating is ENEPIG. Au nominal thickness is $0.095 \pm 0.025 \mu\text{m}$.

Pad Configuration and Description



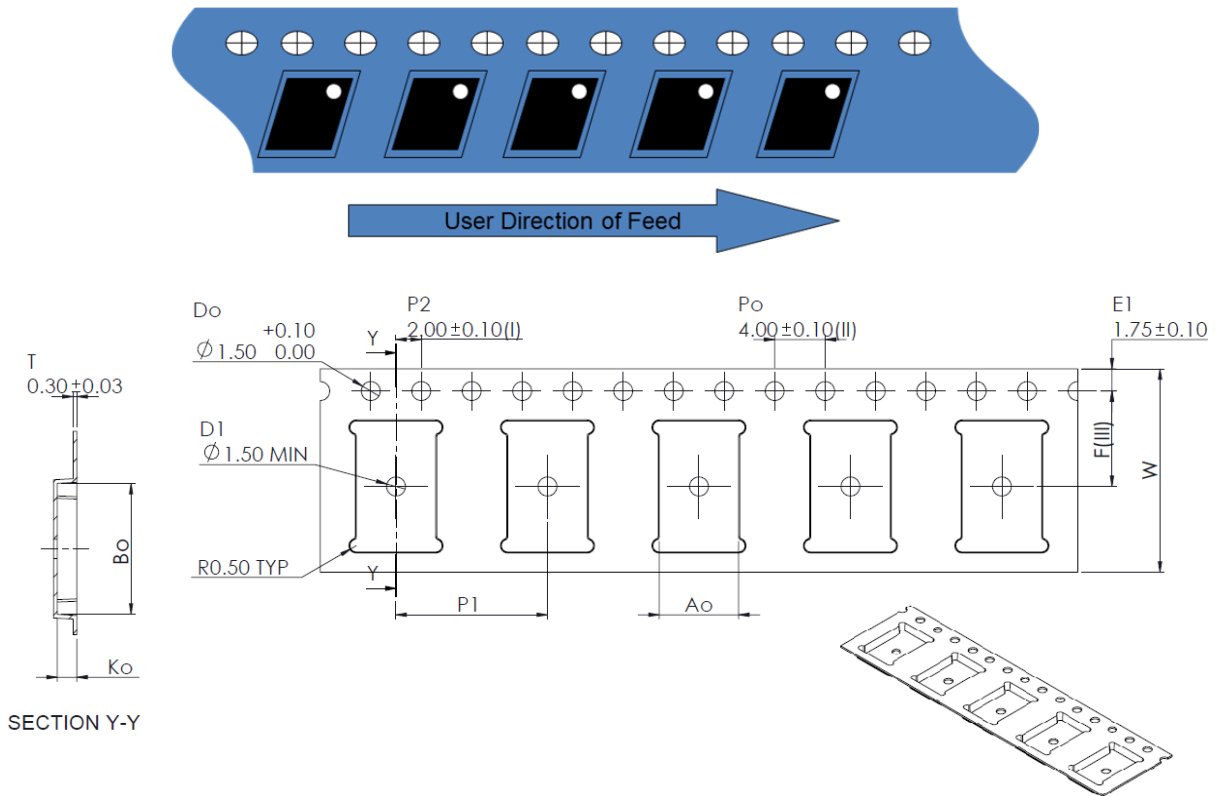
Pad No.	Label	Description
1	VBC	CMOS Controller Enable
6	RFIN	RF Input
11	VCCD	Carrier Amplifier Driver Vcc = +5V
13	VG3	Carrier Amplifier, Gate Bias
16	VD3	Carrier Amplifier, Drain Bias
19	RFOUT	RF Output, DC Blocked
27	VD2	Peaking Amplifier, Drain Bias
30	VG2	Peaking Amplifier, Gate Bias
32	VCPD	Peaking Amplifier Driver Vcc = +5V
35	VREF	CMOS Controller +5V
2,3,4,5,7,8,9,10,12,14,15,17,18,20,21,22,23,24,25,26,28,29,31,33,34,36	GND	Internal Grounding, recommend connecting to EPAD ground
EPAD	GND	DC/RF Ground. Must be soldered to EVB Ground Plane over an array of vias for thermal and RF performance. Solder voids under the EPAD will result in excessive junction temperatures causing permanent damage.

Biasing Procedure

Bias On	Bias Off
<ol style="list-style-type: none"> Set V_{G2}, $V_{G3} = -5V$ Set $V_{REF} = 5V$ Set $V_{CC} = 5V$ Set $V_{D2} = V_{D3} = 48V$ Set I_{DQ2} (Peaker) = 80mA Adjust V_{G2} offset voltage $-1.5V$ Typical V_{G2} after offset is $-4.2V$ Adjust V_{G3} to get $I_{DQ3} = 40mA$ Typical $V_{G3} = -2.8V$ Set $V_{BC} = 1.8V$ 	<ol style="list-style-type: none"> Set $V_{BC} = 0V$ Set $V_{G2} = V_{G3} = -5V$ Set $V_{D2} = V_{D3} = 0V$ Set $V_{CC} = V_{REF} = 0V$

Tape and Reel Information – Carrier and Cover Tape Dimensions

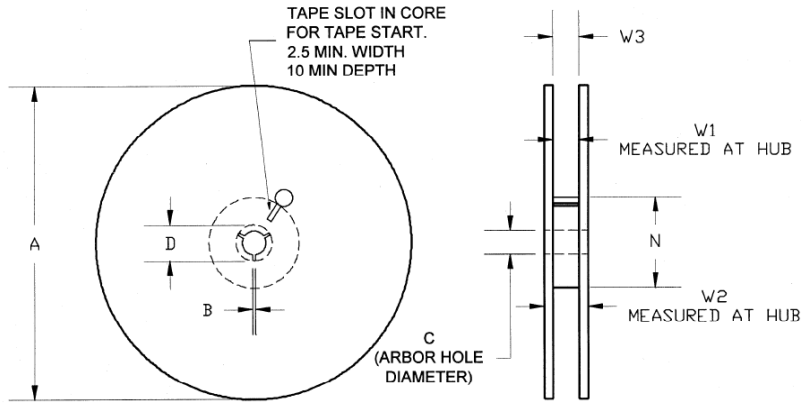
Tape and reel specifications for this part are also available on the Qorvo website.
 Standard T/R size = 2500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.248	6.30
	Width	B0	0.406	10.30
	Depth	K0	0.061	1.55
	Pitch	P1	0.472	12.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width	C	0.524	13.30
Carrier Tape	Width	W	0.630	16.00

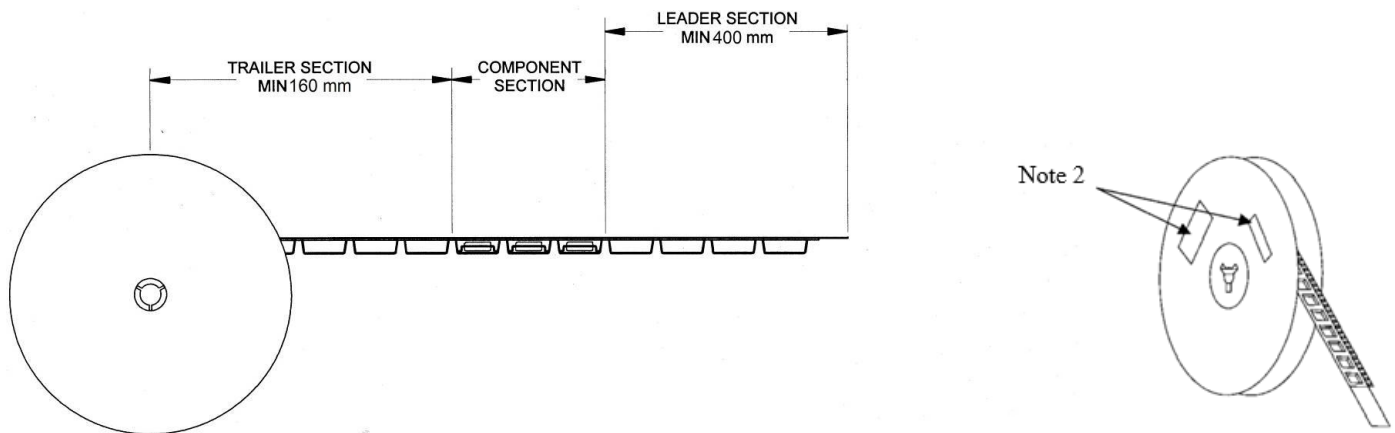
Tape and Reel Information – Reel Dimensions

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.



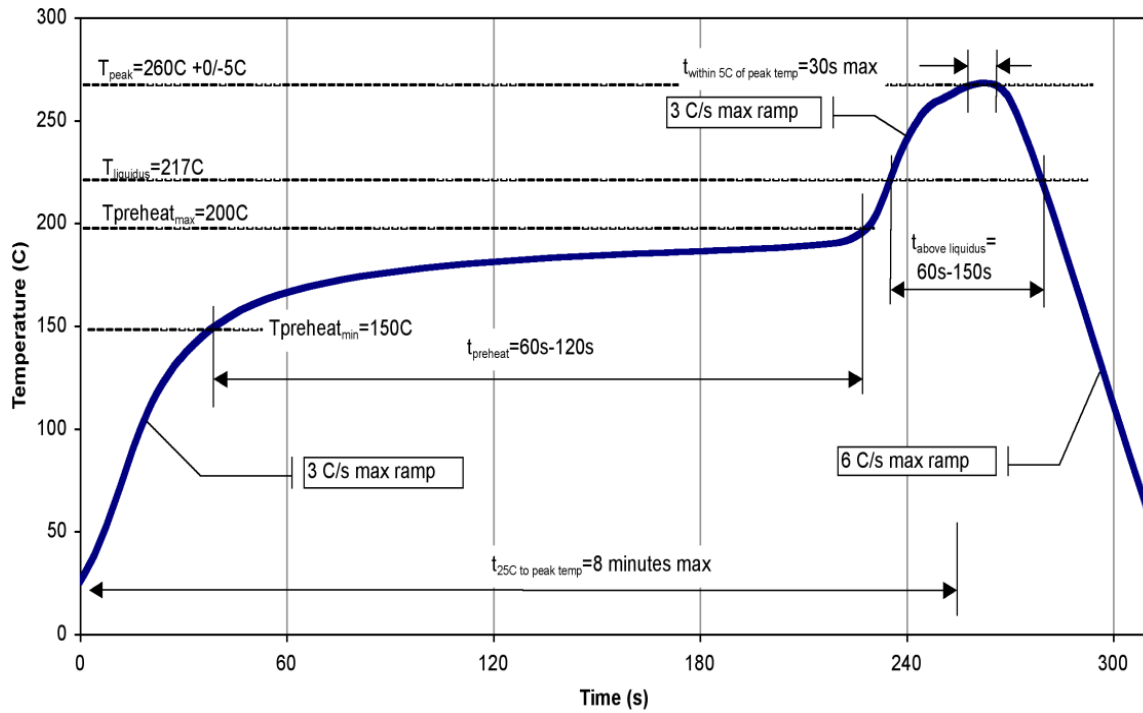
Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.00
	Thickness	W2	0.874	22.20
	Space Between Flange	W1	0.661	16.80
Hub	Outer Diameter	N	4.016	102.00
	Arbor Hole Diameter	C	0.512	13.00
	Key Slit Width	B	0.079	2.00
	Key Slit Diameter	D	0.787	20.00

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Recommended Solder Temperature Profile



Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering processes.
Package lead plating is ENEPIG. Au nominal thickness is $0.095 \pm 0.025\ \mu m$.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B (500V)	ANSI/ESDA/JEDEC Standard JS-001
ESD – Charged Device Model (CDM)	Class C3 (1000V)	ANSI/ESDA/JEDEC Standard JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC Standard J-STD-020



RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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