TriQuint | Qorvo

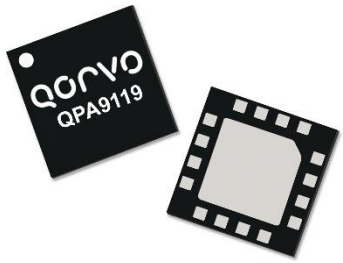
RFMD + TriQuint = Qorvo

QPA9119

½ W High Linearity Amplifier

Applications

- Repeaters / DAS
- Mobile Infrastructure
- Defense Communications
- General Purpose Wireless

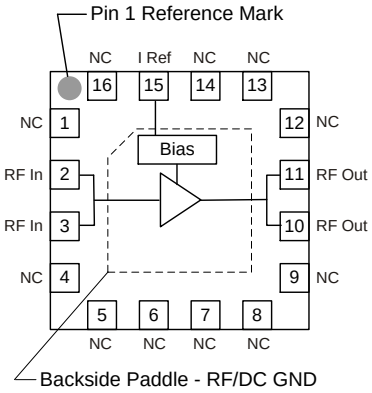


16-Pin 3 x 3 mm Leadless QFN Package

Product Features

- 400-4200 MHz
- +27.2 dBm P1dB
- +44 dBm Output IP3
- 17 dB Gain at 2140 MHz
- +5 V Single Supply, 130 mA I_{CQ}
- Internal RF overdrive protection
- Internal DC overvoltage protection
- On chip ESD protection
- 3x3 mm QFN Package

Functional Block Diagram



Top View

General Description

The QPA9119 is a high linearity driver amplifier in a low-cost, RoHS compliant, surface mount package. This InGaP/GaAs HBT delivers high performance across a broad range of frequencies with +44 dBm OIP3 and +27.2 dBm P1dB while only consuming 130 mA quiescent current. All devices are 100% RF and DC tested.

The QPA9119 incorporates on-chip features that differentiate it from other products in the market. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system. On-chip ESD protection allows the amplifier to have a very robust Class 1C HBM ESD rating.

The QPA9119 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G / 4G base stations.

Pin Configuration

Pin No.	Label
1, 4, 5, 6, 7, 8, 9, 12, 13, 14, 16	No Connection
2, 3	RF In
10, 11	RF Out
15	I Ref
Backside Paddle	GND

Ordering Information

Part No.	Description
QPA9119	0.5 W High Linearity Amplifier
QPA9119−PCB900	869−960 MHz Evaluation Board
QPA9119−PCB2140	2.11–2.17 GHz Evaluation Board

Standard T/R size = 2,500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to +150 °C
RF Input Power, CW, 50 Ω, T=25 °C	+27 dBm
Device Voltage (V_{CC})	+8 V
Dissipated Power (P_{DISS})	1.7 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{CC})	+4.75	+5	+5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+175	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: $V_{CC} = V_{PD}$ = +5.0 V, Temp = +25 °C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		400		4200	MHz
Test Frequency			2140		MHz
Gain		15.5	17.1	18.5	dB
Input Return Loss			14		dB
Output Return Loss			11		dB
Output P1dB		+26.4	+27.2		dBm
Output IP3	Pout = +9 dBm/tone, Δf = 1 MHz	+41.0	+43.8		dBm
LTE Channel Power(1)	−50 dBc ACLR See Note 1		+18.1		dBm
Noise Figure			4.8		dB
Reference Bias current	Pin 15		7		mA
Quiescent Current, I_{CQ}	Pins 10, 11	115	130	155	mA
Total Current			137		mA
Thermal Resistance, θ_{jc}	Junction to case			50.3	°C/W

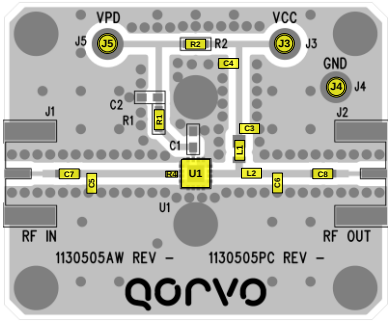
Notes:
1. ACLR test set-up: LTE, 20 MHz E-UTRA, +20 MHz offset, PAR = 9.5 dB at 0.01% Probability

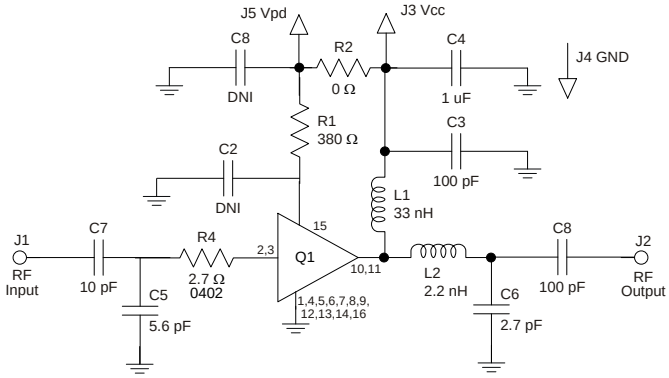
S-Parameters

Test Conditions: V_{CC}=+5 V, I_{CQ}=135 mA (typ.), Temp.=+25 °C, unmatched 50 Ohm system, reference plane at device leads

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.05	-6.62	-174.41	27.28	124.83	-24.82	87.65	-4.37	-172.48
0.10	-6.11	-174.19	23.31	125.16	-36.26	0.46	-2.80	-159.87
0.20	-7.34	-152.53	17.32	131.27	-40.20	9.27	-2.05	-177.15
0.40	-0.95	-162.11	20.48	144.17	-33.75	33.77	-4.17	166.09
0.60	-0.67	-177.80	19.46	120.55	-32.49	22.94	-4.88	167.74
0.80	-0.81	174.16	17.80	105.64	-32.11	18.72	-4.89	167.06
1.00	-0.92	168.52	16.25	94.63	-31.86	16.69	-4.81	164.86
1.20	-1.00	163.75	14.88	85.61	-31.62	15.38	-4.73	162.09
1.40	-1.06	159.42	13.67	77.74	-31.39	14.42	-4.66	158.97
1.60	-1.10	155.28	12.59	70.57	-31.16	13.48	-4.57	155.65
1.80	-1.12	151.20	11.59	63.86	-30.95	12.50	-4.48	152.21
2.00	-1.13	147.13	10.68	57.49	-30.74	11.44	-4.38	148.80
2.20	-1.13	142.97	9.83	51.35	-30.56	10.16	-4.26	145.35
2.40	-1.13	138.79	9.03	45.42	-30.40	8.87	-4.15	142.00
2.60	-1.12	134.61	8.25	39.65	-30.26	7.52	-4.03	138.91
2.80	-1.09	130.44	7.50	34.07	-30.15	5.99	-3.89	136.04
3.00	-1.05	126.28	6.77	28.70	-30.06	4.49	-3.75	133.19
3.20	-1.03	122.34	6.07	23.53	-30.00	3.00	-3.63	130.49
3.40	-1.00	118.66	5.38	18.51	-29.95	1.37	-3.52	128.09
3.60	-0.95	115.17	4.72	13.69	-29.93	-0.17	-3.38	125.84
3.80	-0.91	111.69	4.09	9.01	-29.91	-1.72	-3.25	123.58
4.00	-0.89	109.84	3.55	4.09	-29.84	-3.69	-3.09	118.66
4.20	-0.86	107.48	2.95	-0.05	-29.86	-5.00	-2.99	116.78
4.40	-0.82	105.44	2.38	-3.91	-29.88	-6.15	-2.88	115.15
4.60	-0.79	103.60	1.84	-7.62	-29.91	-7.26	-2.76	113.43
4.80	-0.77	102.20	1.34	-11.12	-29.93	-8.27	-2.68	111.71
5.00	-0.76	100.98	0.87	-14.54	-29.95	-9.25	-2.61	110.10
5.20	-0.75	100.03	0.44	-17.85	-29.97	-10.10	-2.54	108.53
5.40	-0.74	99.00	0.04	-21.17	-29.98	-11.00	-2.47	106.94
5.60	-0.74	98.11	-0.33	-24.43	-29.98	-11.73	-2.41	105.20
5.80	-0.75	97.20	-0.67	-27.76	-29.96	-12.52	-2.36	103.39
6.00	-0.76	96.42	-0.99	-31.12	-29.92	-13.30	-2.32	101.42

869 – 960 MHz Evaluation Board (QPA9119−PCB900)





Notes:
1. See Evaluation Board PCB Information for material and stack up.
2. The recommended component values are dependent upon the frequency of operation.
3. All components are of 0603 size unless stated on the schematic.
4. Critical component placement locations:
   - Distance from U1 (left edge) to R4 (right edge): 25 mils (1.2 deg. at 920 MHz)
   - Distance from U1 (left edge) to C5 (right edge): 360 mils (17 deg. at 920 MHz)
   - Distance from U1 (right edge) to L2 (left edge): 120 mils (5.7 deg. at 920 MHz)
   - Distance from U1 (right edge) to C6 (left edge): 347 mils (16.5 deg. at 920 MHz)

Bill of Material QPA9119−PCB900

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	QPA9119 Amplifier, QFN pkg.	Qorvo	QPA9119
R2	0 Ω	Resistor, Chip, 0603	various	
R4	2.7 Ω	Resistor, Chip, 0402, 1%, 1/16W	various	
R1	380 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
L2	2.2 nH	Inductor, 0603, +/-0.3 nH	Toko	LL1608-FSL2N2S
L1	33 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-330XJLB
C7	10 pF	Cap., Chip, 0603, 5%, 50V. NPO/COG	various	
C6	2.7 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	
C2, C8	100 pF	Cap., Chip, 0603, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 0603, 10%, 10V, X5R	various	
C5	5.6 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	

Typical Performance QPA9119−PCB900

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, I_{CQ} = 130 mA , I_{REF} = 7 mA , Temp.=+25 °C

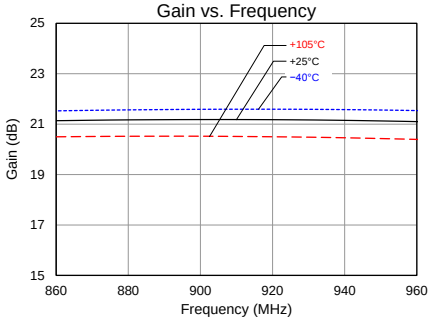
Parameter	Conditions	Typical Value			Units
Frequency		869	920	960	MHz
Gain		21.1	21.2	21.1	dB
Input Return Loss		10	13	17	dB
Output Return Loss		13	12	11	dB
Output P1dB		+28.0	+28.2	+28.3	dBm
OIP3	Pout= +21 dBm/tone, Δf=1 MHz	+43.5	+43.8	+43.5	dBm
LTE Channel Power(1)	−50 dBc ACLR	+18.3	+18.7	+18.7	dBm
Noise Figure		6.8	6.7	6.7	dB

Notes:
1. ACLR Test set-up: LTE, 20 MHz E-UTRA, +20 MHz offset, PAR = 9.5 dB at 0.01% Probability

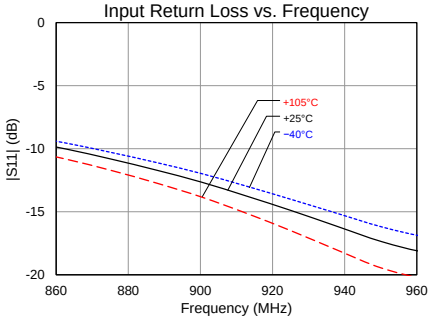
Performance Plots QPA9119−PCB900

Test conditions unless otherwise noted: $V_{CC} = V_{PD} = +5V$, $I_{CQ} = 130$ mA , $I_{REF} = 7$ mA , Temp.=+25 °C

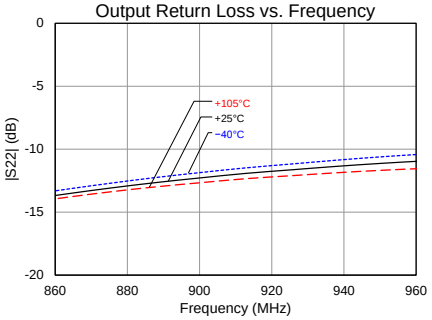
Gain vs. Frequency



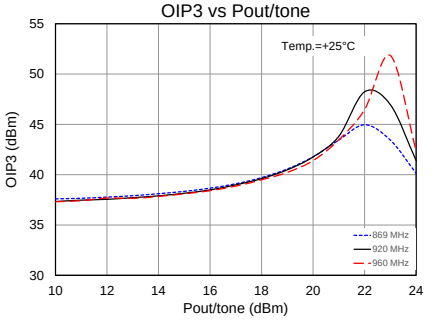
Input Return Loss vs. Frequency



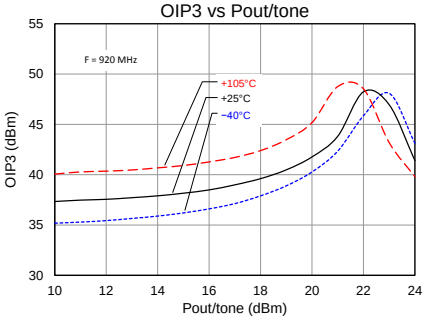
Output Return Loss vs. Frequency



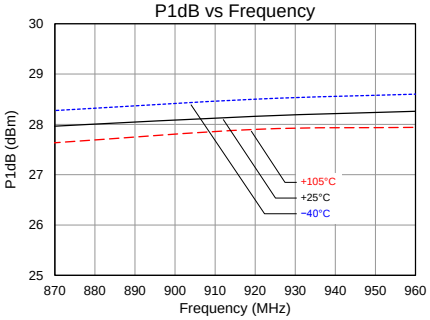
OIP3 vs Pout/tone



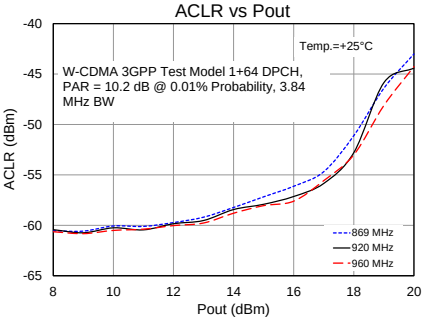
OIP3 vs Pout/tone



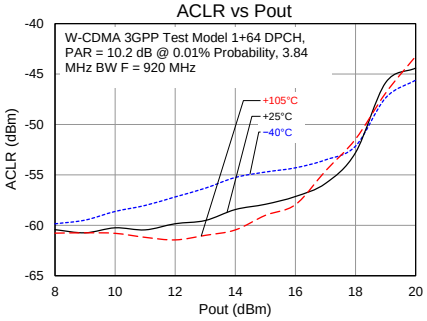
P1dB vs Frequency



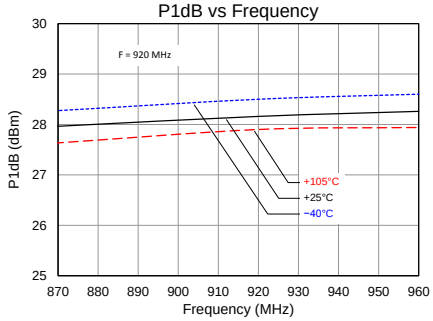
ACLR vs Pout



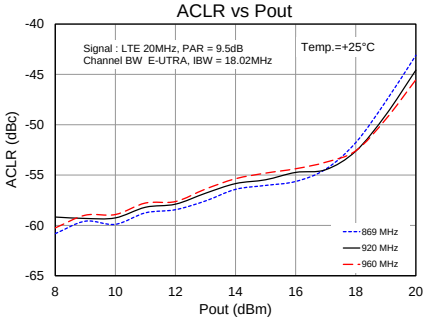
ACLR vs Pout



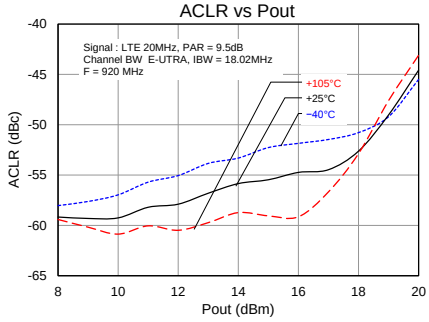
P1dB vs Frequency



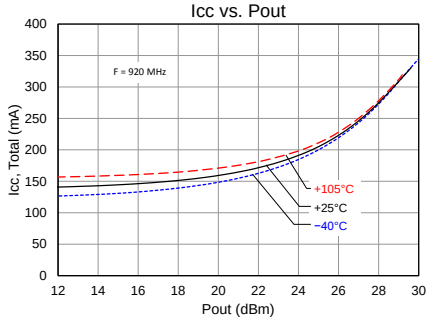
ACLR vs Pout



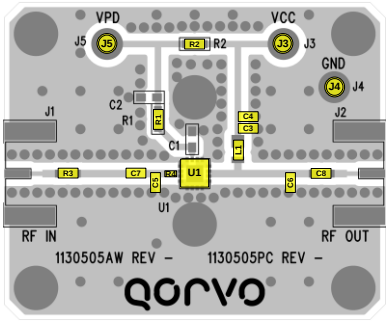
ACLR vs Pout

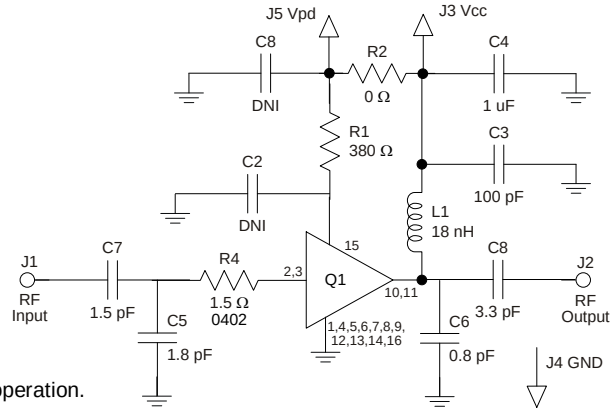


Icc vs. Pout



2110 – 2140 MHz Evaluation Board (QPA9119−PCB2140)





Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. The recommended component values are dependent upon the frequency of operation.
3. All components are of 0603 size unless stated on the schematic.
4. Critical component placement locations:
   - Distance from U1 (left edge) to R4 (right edge): 32 mils (3.6 deg. at 2140 MHz)
   - Distance from U1 (left edge) to C5 (right edge): 70 mils (7.8 deg. at 2140 MHz)
   - Distance from U1 (left edge) to C7 (right edge): 152 mils (16.8 deg. at 2140 MHz)
   - Distance from U1 (right edge) to C8 (left edge): 380 mils (42.0 deg. at 2140 MHz)
   - Distance from U1 (right edge) to C6 (left edge): 305 mils (33.7 deg. at 2140 MHz)

Bill of Material QPA9119−PCB2140

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	QPA9119 Amplifier, QFN pkg.	Qorvo	QPA9119
R2	0 Ω	Resistor, Chip, 0603	various	
R4	1.5 Ω	Resistor, Chip, 0402, 1%, 1/16W	various	
R1	380 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
C3	100 pF	Cap., Chip, 0603, 5%, 50V, NPO/COG	various	
L1	18 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-180XJLB
C7	1.5 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	
C6	0.8 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	
C8	3.3 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	
C4	1.0 uF	Cap., Chip, 0603, 10%, 10V, X5R	various	
C5	1.8 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	

Typical Performance QPA9119−PCB2140

Test conditions unless otherwise noted: V_{CC} = V_{PD} = +5V, I_{CQ} = 130 mA , I_{REF} = 7 mA , Temp.=+25 °C

Parameter	Conditions	Typical Value			Units
Frequency		2110	2140	2170	MHz
Gain		17.1	17.1	17.0	dB
Input Return Loss		13	14	14	dB
Output Return Loss		12	11	11	dB
Output P1dB		+27.4	+27.2	+27.1	dBm
OIP3	Pout= +13 dBm/tone, Δf=1 MHz	+43.5	+43.8	+43.6	dBm
LTE Channel Power(1)	−50 dBc ACLR	+18.2	+18.1	+18.4	dBm
Noise Figure		4.8	4.8	4.8	dB

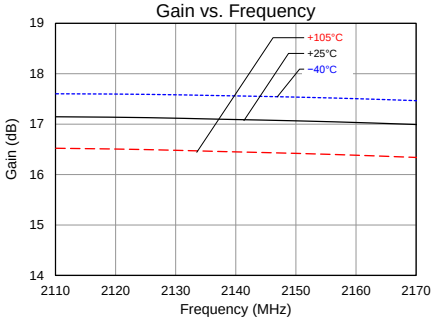
Notes:

1. ACLR Test set-up: LTE, 1-CH E-UTRA, +20 MHz offset, PAR = 9.5 dB at 0.01% Probability

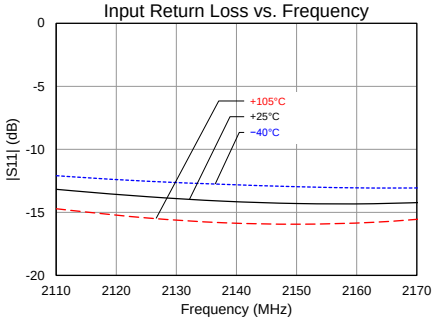
Performance Plots QPA9119−PCB2140

Test conditions unless otherwise noted: $V_{CC} = V_{PD} = +5V$, $I_{CQ} = 130$ mA , $I_{REF} = 7$ mA , Temp.=+25 °C

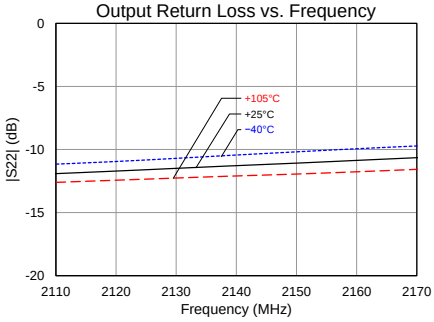
Gain vs. Frequency



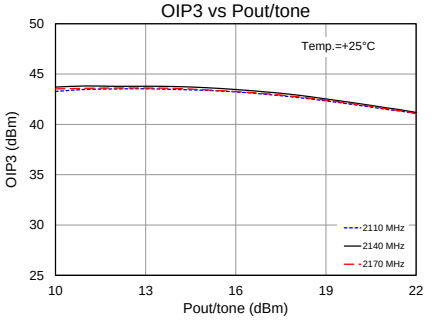
Input Return Loss vs. Frequency



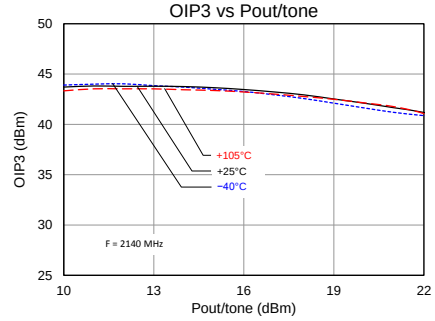
Output Return Loss vs. Frequency



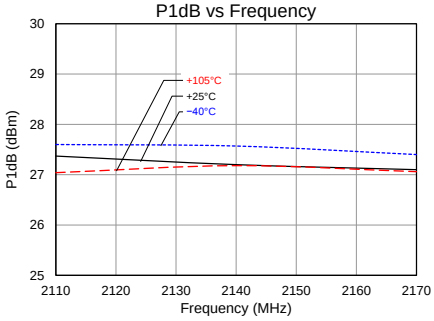
OIP3 vs Pout/tone



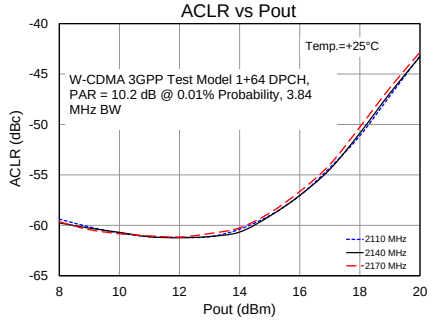
OIP3 vs Pout/tone



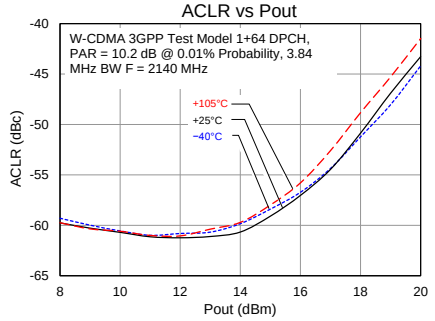
P1dB vs Frequency



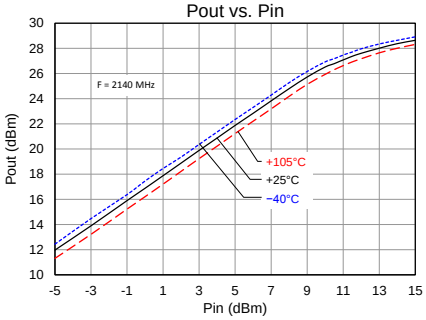
ACLR vs Pout



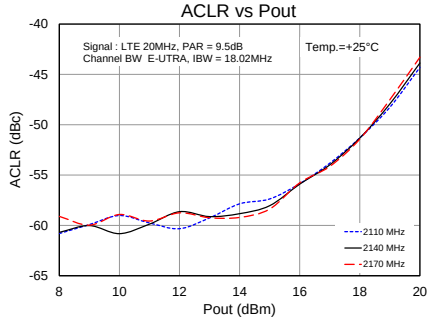
ACLR vs Pout



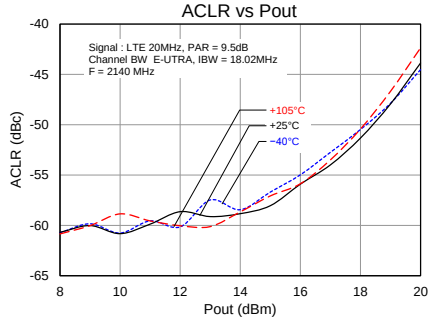
Pout vs. Pin



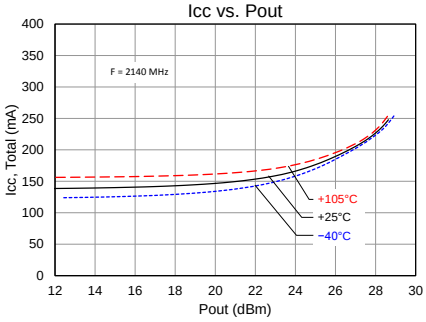
ACLR vs Pout



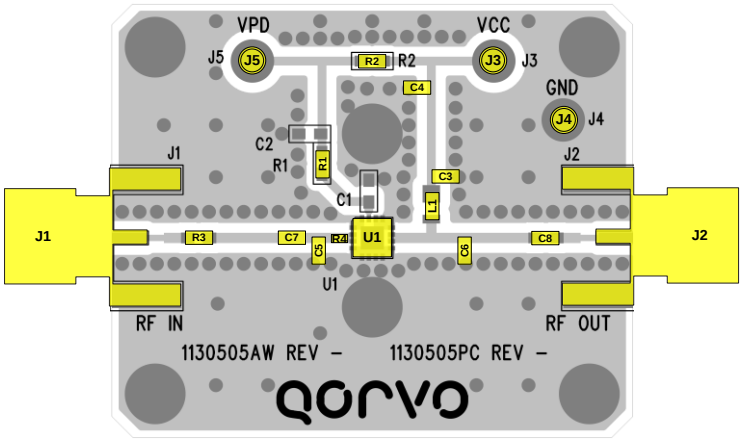
ACLR vs Pout

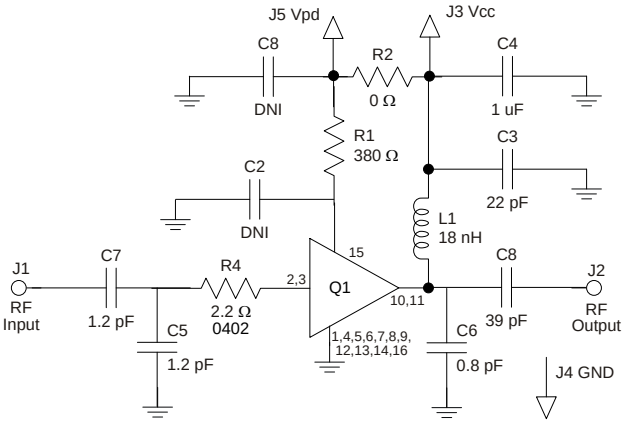


Icc vs. Pout



2300 – 2700 MHz Reference Design





Notes:

1. All components are of 0603 size unless stated on the schematic.
2. The recommended component values are dependent upon the frequency of operation.
3. Critical component placement locations:
   - Distance between U1 (left edge) to R4 (right edge): 15 mil
   - Distance between U1 (left edge) to C5 (right edge): 80 mil
   - Distance between U1 (left edge) to C7 (right edge): 130 mil
   - Distance between U1 (right edge) to C6 (left edge): 130 mil

Bill of Material 2300 – 2700 MHz Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	0.5 W High Linearity Amplifier	Qorvo	QPA9119
R1	380 Ω	Res., Chip, 0603, +/-1%, 1/10W	various	
R2, R3	0 Ω	Res., Chip, 0603	various	
C5, C7	1.2 pF	CAP, 0603, +/-0.1pF. 200V. NPO/COG	various	
C6	0.8 pF	CAP, 0603, +/-0.1pF. 200V. NPO/COG	various	
C8	39 pF	Cap., Chip, 0603, +/-5%. 50V NPO/COG	various	
C3	22 pF	Cap., Chip, 0603, +/-5%. 50V NPO/COG	various	
R4	2.2 Ω	Res., Chip, 0603, +/-1%, 1/10W	various	
C4	1.0 uF	CAP, 0603, 10%, X5R , 10V	various	
L1	18 nH	Inductor, 0805, 5%, Coilcraft CS series	Coilcraft	0805CS-180XJLB

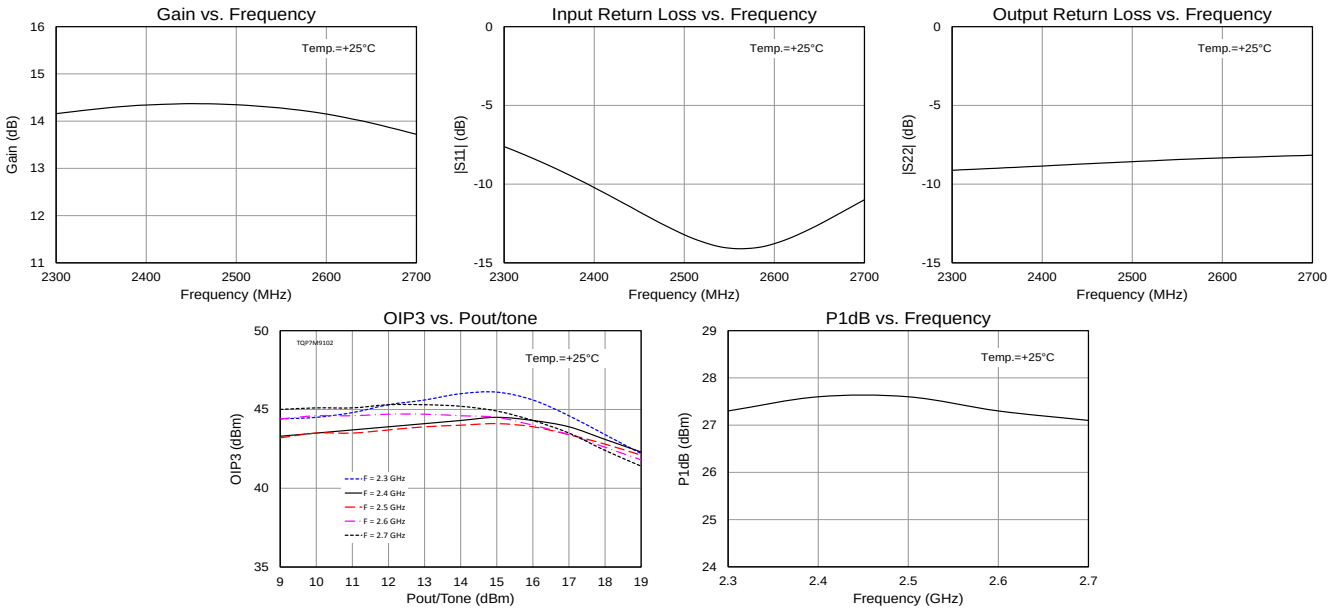
Typical Performance 2300 – 2700 MHz Reference Design

Test Conditions: V_{CC} = V_{PD} = +5V, I_{CQ} = 130 mA , I_{REF} = 7 mA , Temp.=+25 °C

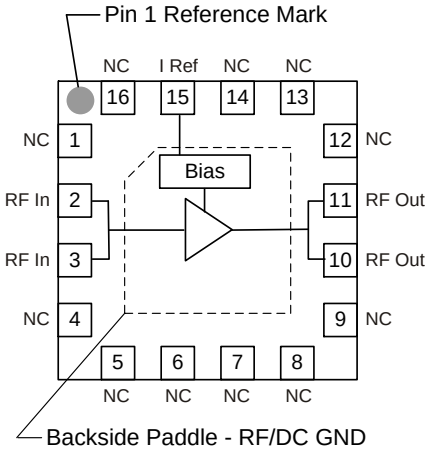
Parameter	Conditions	Typical Value					Units
Frequency		2300	2400	2500	2600	2700	MHz
Gain		14.1	14.3	14.3	14.1	13.7	dB
Input Return Loss		7.6	10	13	13	11	dB
Output Return Loss		9.1	8.8	8.6	8.3	8.2	dB
Output P1dB		+27.3	+27.6	+27.6	+27.3	+27.1	dBm
Output IP3	Pout= +15 dBm/tone, Δf= 1 MHz	+46.1	+44.5	+44.1	+44.5	+44.9	dBm
Quiescent Collector Current, I_{CQ}		130					mA

Performance Plots 2300 – 2700 MHz Reference Design

Test Conditions: V_{CC} = V_{PD} = +5V, I_{CQ} = 130 mA , I_{REF} = 7 mA , Temp.=+25 °C



Pin Configuration and Description



Top View

Pin No.	Label	Description
1, 4, 5, 6, 7, 8, 9, 12, 13, 14, 16	NC	No electrical connection. Land pads should be provided for PCB mounting integrity.
2, 3	RF IN	RF input. External DC Block required. Requires conjugate match for optimal performance.
10, 11	RF OUT / V_{CC}	RF output. External DC Block and bias voltage required. Requires matching.
15	I REF	Sets the bias current for the amp. Also can be used to power down device.
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

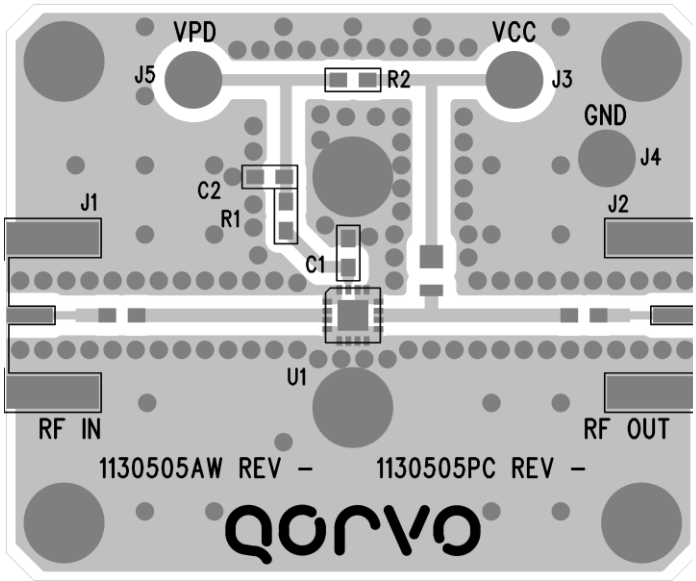
Evaluation Board PCB Information

PC Board Layout

PCB Material (stackup):
1 oz. Cu top layer
0.014 inch Nelco N-4000-13, ε_r=3.7
1 oz. Cu MIDDLE layer 1
Core Nelco N-4000-13
1 oz. Cu middle layer 2
0.014 inch Nelco N-4000-13
1 oz. Cu bottom layer
Finished board thickness is 0.062±.006

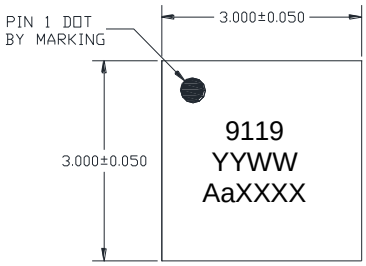
50 ohm line dimensions: width = .029”, spacing = .029”.

The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

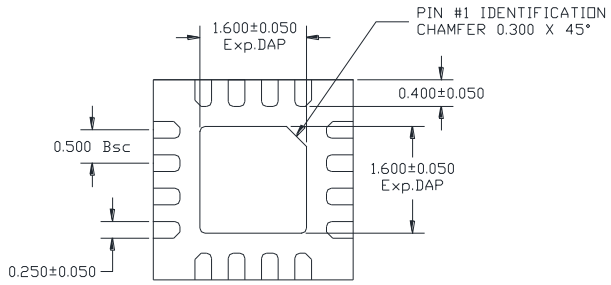


Package Marking and Dimensions

Marking: Part number – 9119
Date - YYWW
Lot code – AaXXXX

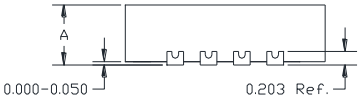


TOP VIEW



BOTTOM VIEW

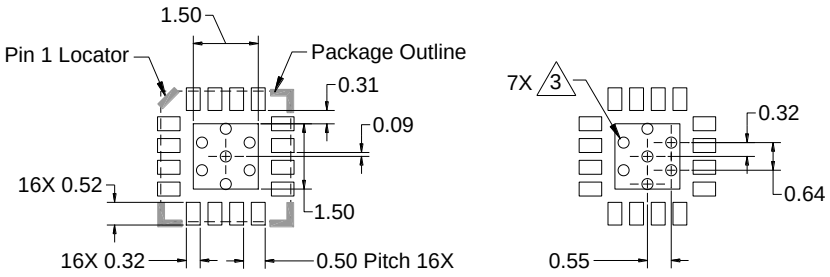
		TSLP
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800



TOP VIEW

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: NiPdAu

PCB Mounting Pattern



COMPONENT SIDE

NOTES:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Class: Class 1C
Volt. Range: >1000V to <2000V
Test: Human Body Model (HBM)
Standard: ESAD/JEDEC Standard JS-001-2012

ESD Class: Class C3
Volt. Range: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.triquint.com **Tel: 1-844-890-8163**
Email: customer.support@qorvo.com

For information about the merger of RFMD and Qorvo as Qorvo:

Web: www.qorvo.com

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