QPA9501

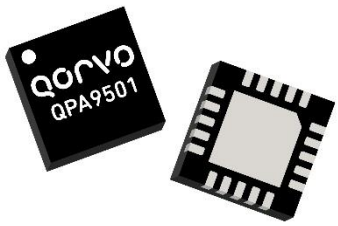
3-Stage LTE-U/LAA Power Amplifier

General Description

The QPA9501 is high power amplifier module containing an internally matched 3-stage PA, compensated DC biasing circuit and output power detector. This PA module is optimized for the WiFi bands from 5.1-5.9GHz and hence well suited for LTE-U/LAA applications. It provides high gain (32 dB) and -47dBc ACLR at Pout of 22dBm with a 20MHz LTE signal without any DPD.

The QPA9501 features chipset logic compatible control voltages and buffered PA enable pin (PAEN) all of which draw very low current to facilitate ease of use and compatibility with current and future transceiver generations. With its optimized power dissipation, this amplifier module is well suited for implementation into next generation MIMO configurations and well designed to work with or without digital pre-distortion (DPD).

The QPA9501 is assembled in a small footprint 4.0 x 4.0 x 0.85 mm 20-pin QFN package.

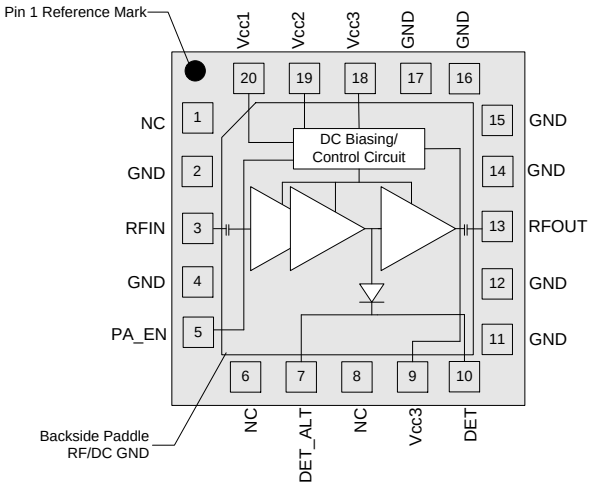


4 x 4 mm 20-pin Leadless QFN Package

Product Features

- 4.9 GHz to 5.9 GHz Operational Bandwidth
- Fully Integrated Power Amplifier Module With Power Detector
- Internally Matched Input / Output
- -47dBc ACLR with Pout = 22dBm avg
- Temperature Compensated Bias Network
- High Gain = 32 dB
- Integrated CMOS Compatible Logic and Shutdown
- Supply Voltage: +3.3 V to +5.0 V
- Leadless 4.0 x 4.0 x 0.85 mm Pb-Free QFN Package

Functional Block Diagram



Top View

Applications

- 5G, Pre-5G Small Cell BTS
- LTE-U/LAA
- WiFi Access Points and Small Cells
- Telematics
- Point-to-point and Backhaul
- ISM Band

Ordering Information

Part No.	Description
QPA9501TR13	2,500 pieces on a 13” reel (standard)
QPA9501PCB401	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to 150 °C
RF Input Power, CW, 50 Ω, T = 25 °C	+5 dBm
Device Voltage	+6.0 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC1}, V_{CC2}, V_{CC3}	+3.15	+5	+5.5	V
T_{AMB}	−40	25	+105	°C
Tj (for>10^6 hours MTTF)			170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

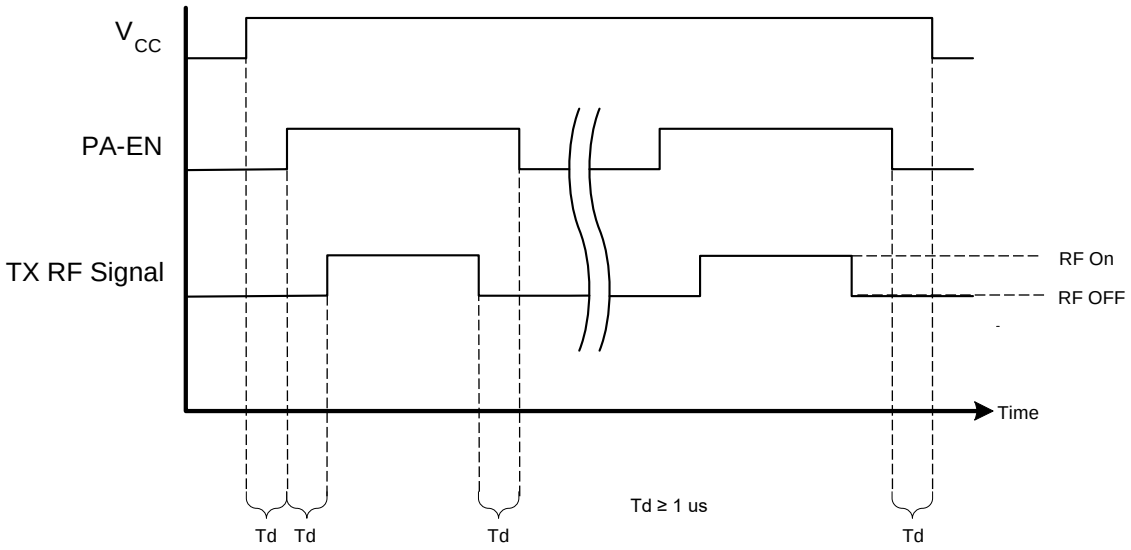
Parameter	Conditions(1)	Min	Typ	Max	Units
Operational Freq. Range		4900		5900	MHz
Small Signal Gain	4900 MHz		33.6		dB
	5200 MHz	30	34	36	dB
	5800 MHz	29.5	32	36	dB
Input Return Loss	5800 MHz		10		dB
Output Return Loss			8		dB
Power Added Efficiency (2)	4900 MHz		6.0		%
	5200 MHz	5.5	6.2		%
	5800 MHz	5.5	6.5		%
ACLR (2)	4900 MHz		-46		dBc
	5200 MHz		-47	-45	dBc
	5800 MHz		-48	-45	dBc
P1dB	4900 MHz		+31.1		dBm
	5200 MHz	+29.5	+31.8		dBm
	5800 MHz	+29.5	+33		dBm
Noise Figure			7		dB
Rise/Fall Time (3)			0.4	0.8	us
PA Enable Voltage	Input Voltage for High State	+1.8	+3.0	V_{CC1}	V
	Input Voltage for Low State	0		+0.45	
PA Enable Current				100	µA
Icq	Total current with no RF	250	350	450	mA
Icc	Operating current with Pout = 22dBm	450	520	650	mA
TX Shut Down Current	PA_EN= Low, No RF		8		µA
Detector Voltage	No RF	+0.25	+0.35	+0.40	V
	Pout = +22 dBm		+0.68		
Stability	Pout = +28 dBm, VSWR = 6:1, all phases	All non-harmonically related outputs < –50 dBc/100 kHz			-
Thermal Resistance, θ_{jc}	Junction to backside paddle		17		°C/W

Notes:
1. Test conditions unless otherwise noted: $V_{CC1} = V_{CC2} = V_{CC3}$ = +5.0 V, PA Enable High = 3.0 V. Temp. = +25 °C
2. Pout = 22dBm average, 20MHz LTE, PAR 9.5dB
3. Maximum specification listed is guaranteed be design. Not tested in production.

Timing Diagram

Transmit Timing Diagram

RF/DC Power On/Off Sequence



Notes: DC and RF signal levels per data sheet specification.
Observe the timing sequence shown in the diagram above and described below.

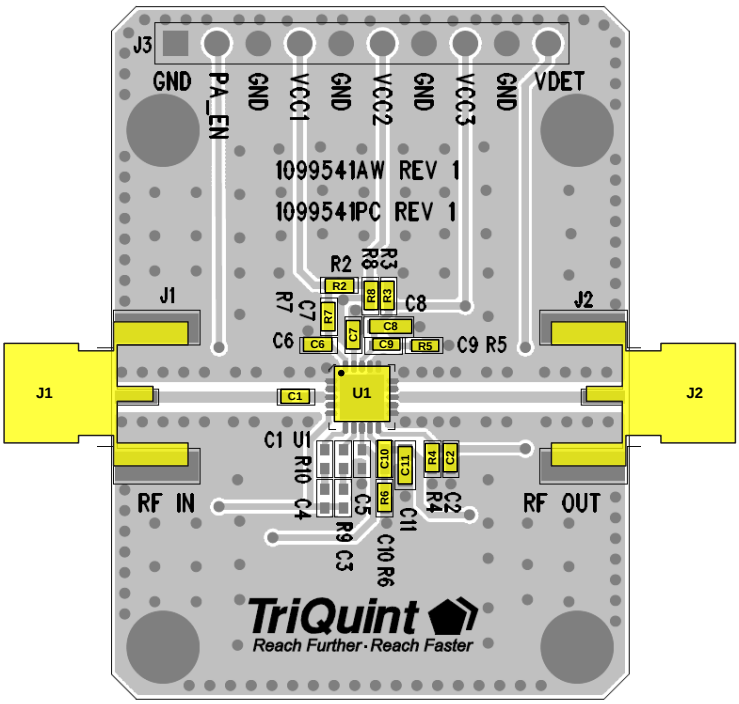
- Apply V_{CC} prior to turning on or pulsing PA enable.
- Turn off PA enable prior to turning off V_{CC}.

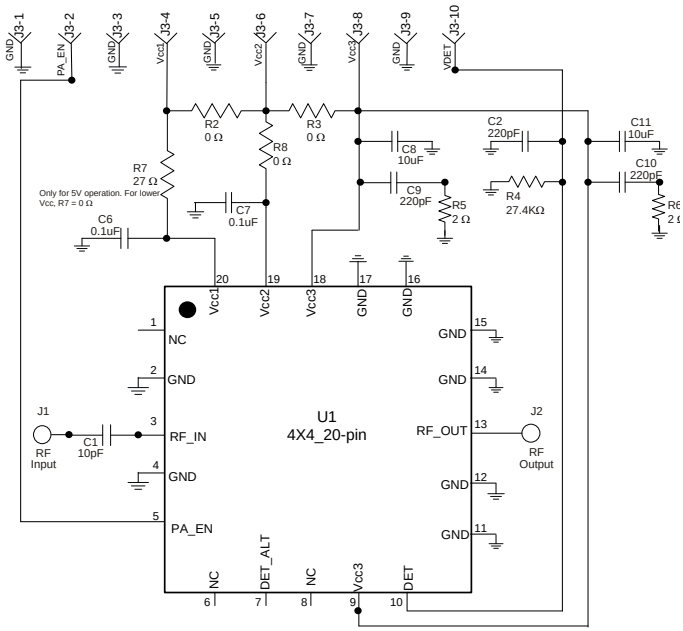
- Turn on PA enable prior to applying RF signal.
- Turn off RF signal prior to turning off PA enable.

Logic Truth Table

PA Mode	PA_EN
Disabled	Low
Enabled	High

Evaluation Board





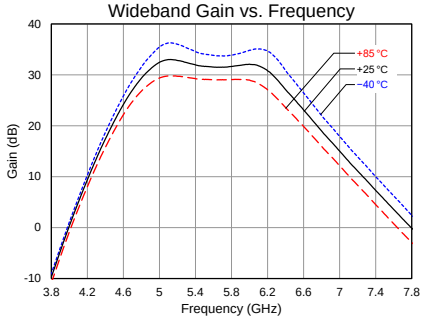
Bill of Material – QPA9501PCB401

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	1099541
U1	n/a	High Power 5GHz PA	Qorvo	QPA9501
R2, R8, R3	0 Ω	Resistor, Chip, 0402, 5%	various	
C1	10 pF	Capacitor, Chip, 0402, 5%	various	
C6, C7	0.1 uF	Capacitor, Chip, 0402, 10%	various	
C8, C11	10 uF	Capacitor, Chip, 0402, 10%	various	
C9, C10, C2	220 pF	Capacitor, Chip, 0402, 10%	various	
R7 (1)	0 to 27 Ω	Resistor, Chip, 0402, 5%, 1/10W	various	
R5, R6 (2)	2 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
R4	27.4 KΩ	Resistor, Chip, 0402, 5%, 1/16W	various	

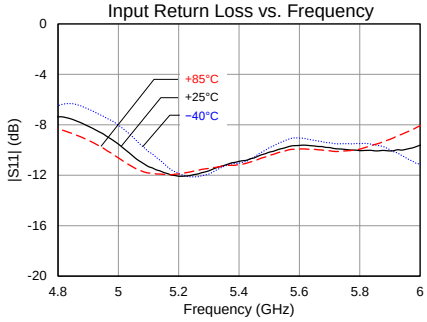
Performance Plots

$V_{CC1} = V_{CC2} = V_{CC3}$ = +5.0 V, PA_EN = +3.0V, Temp. = +25 °C

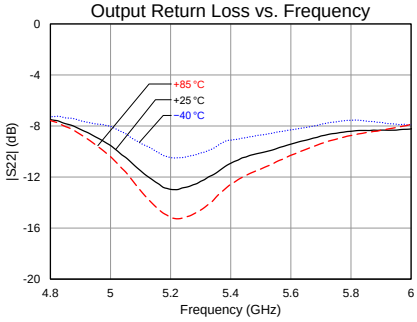
Wideband Gain vs. Frequency



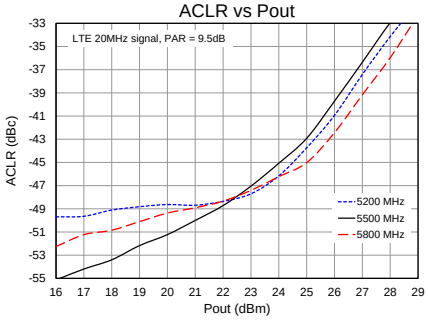
Input Return Loss vs. Frequency



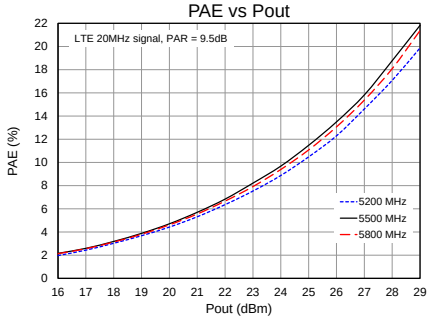
Output Return Loss vs. Frequency



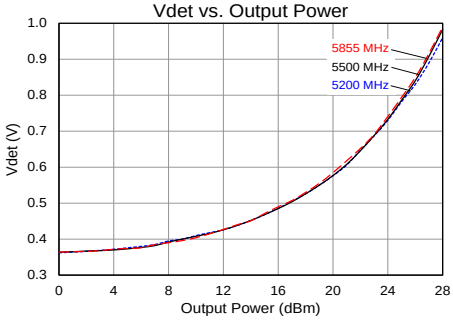
ACLR vs Pout



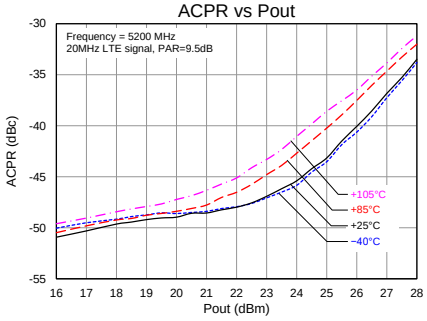
PAE vs Pout



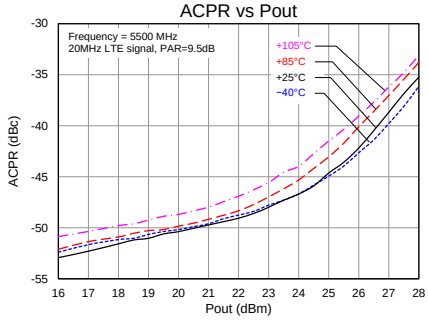
Vdet vs. Output Power



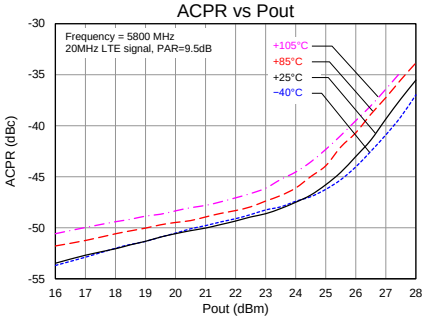
ACPR vs Pout



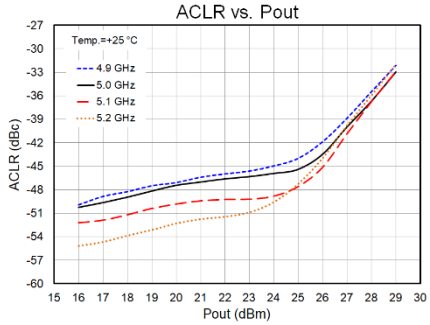
ACPR vs Pout



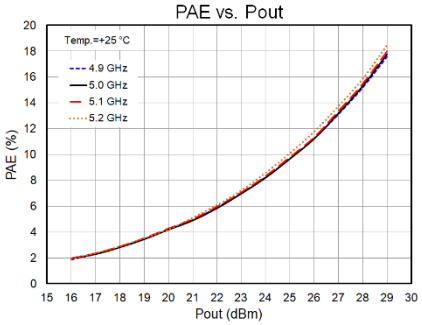
ACPR vs Pout



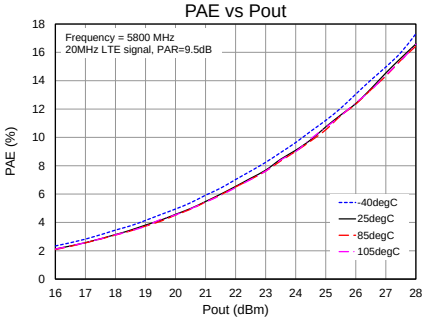
ACLR vs. Pout



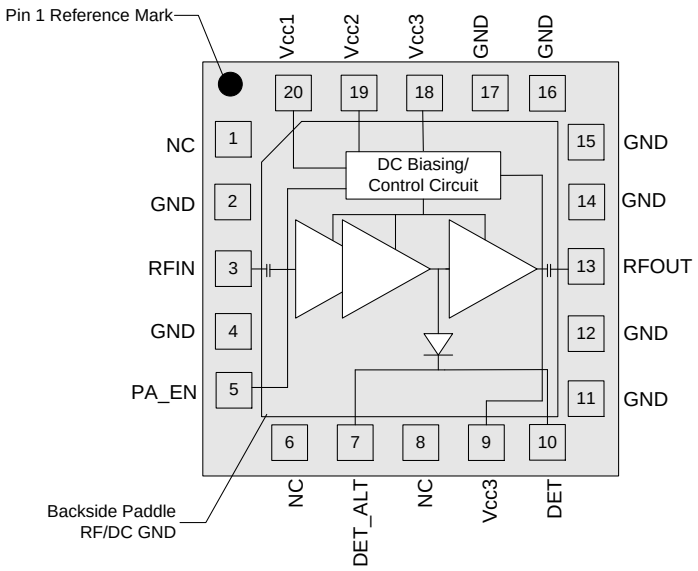
PAE vs. Pout



PAE vs Pout

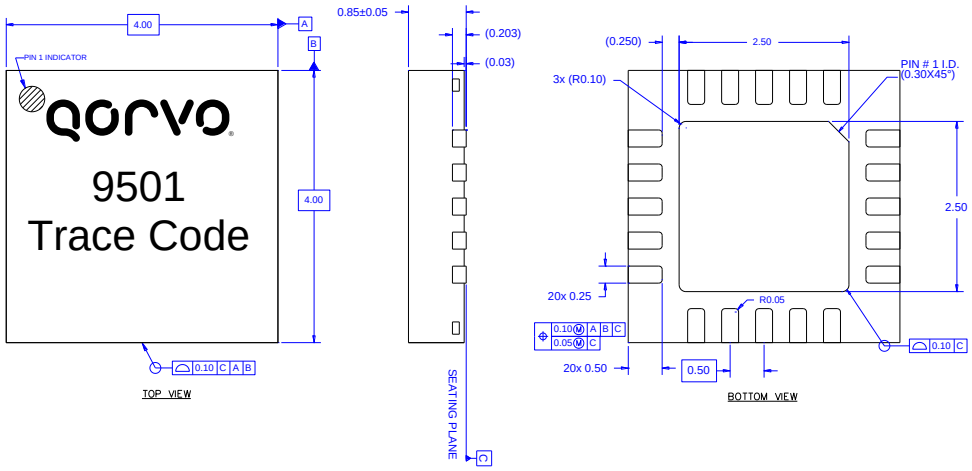


Pin Configuration and Description



Pin No.	Label	Description
1	NC	No internal connection. This pin can be grounded or N/C on PCB.
2	GND	Ground
3	RF_IN	RF Input
4	GND	Ground
5	PA_EN	PA Enable
6	NC	No internal connection. This pin can be grounded or N/C on PCB.
7	DET_ALT	Alternate Detector Output
8	NC	No internal connection. This pin can be grounded or N/C on PCB.
9	VCC3	Supply voltage for third stage PA
10	DET	Detector Output
11	GND	Ground
12	GND	Ground
13	RF_OUT	RF Output
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	VCC3	Supply voltage for third stage PA
19	VCC2	Supply voltage for second stage PA
20	VCC1	Supply voltage for first stage PA
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

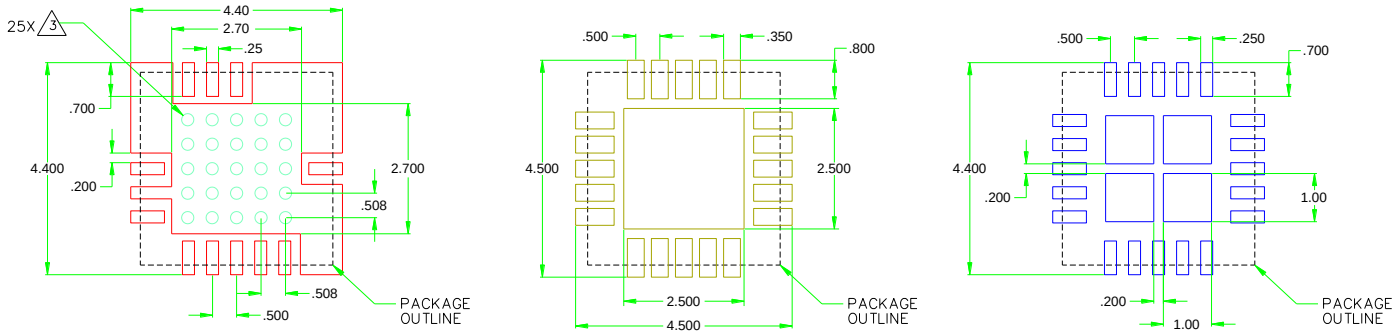
Package Marking and Dimensions



Notes:

1. All dimensions are in millimeters.

PCB Mounting Pattern



BOARD METAL & VIA PATTERN
TOP VIEW

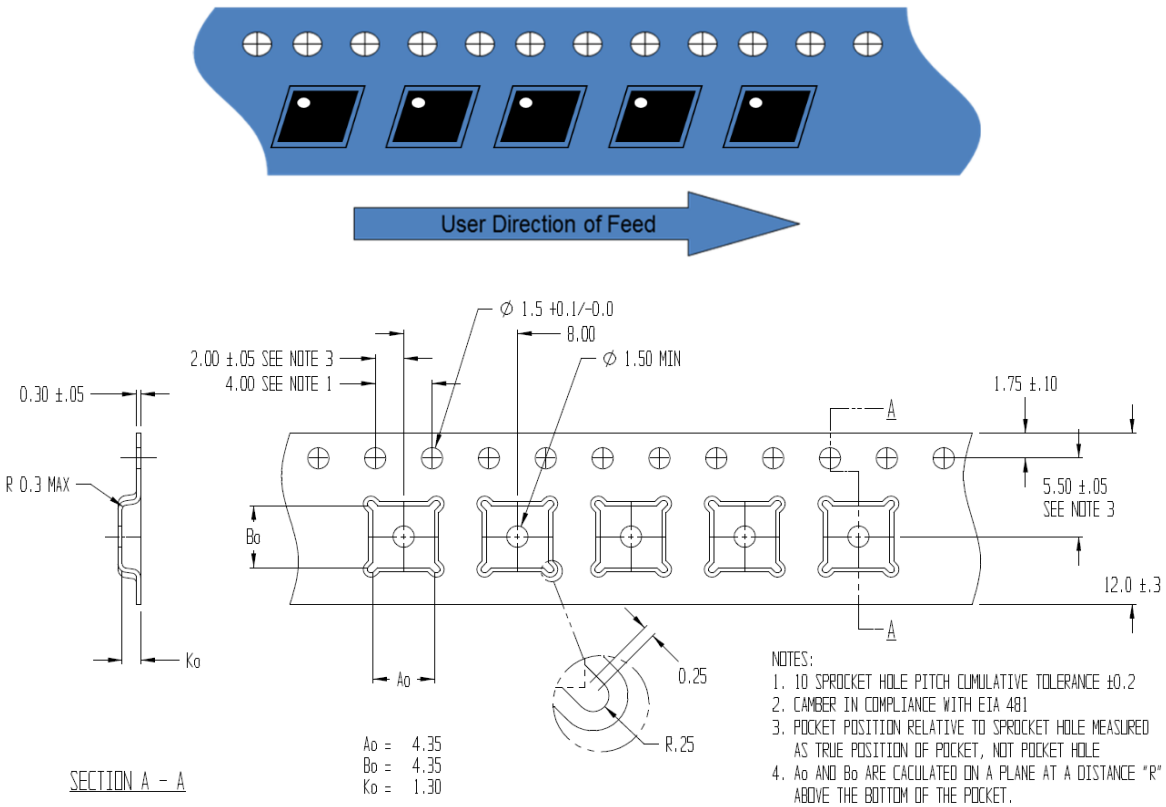
SOLDER MASK
TOP VIEW

STENCIL APERATURE
TOP VIEW (NOTE 4)

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

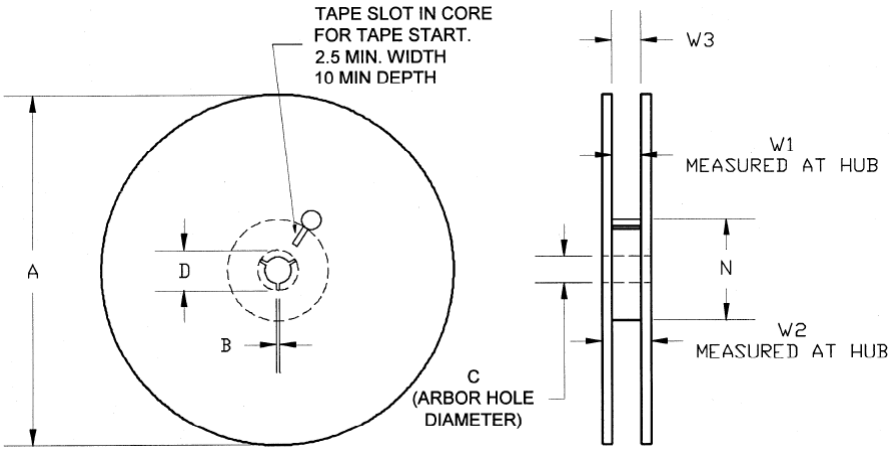
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.171	4.35
	Width	B0	0.171	4.35
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

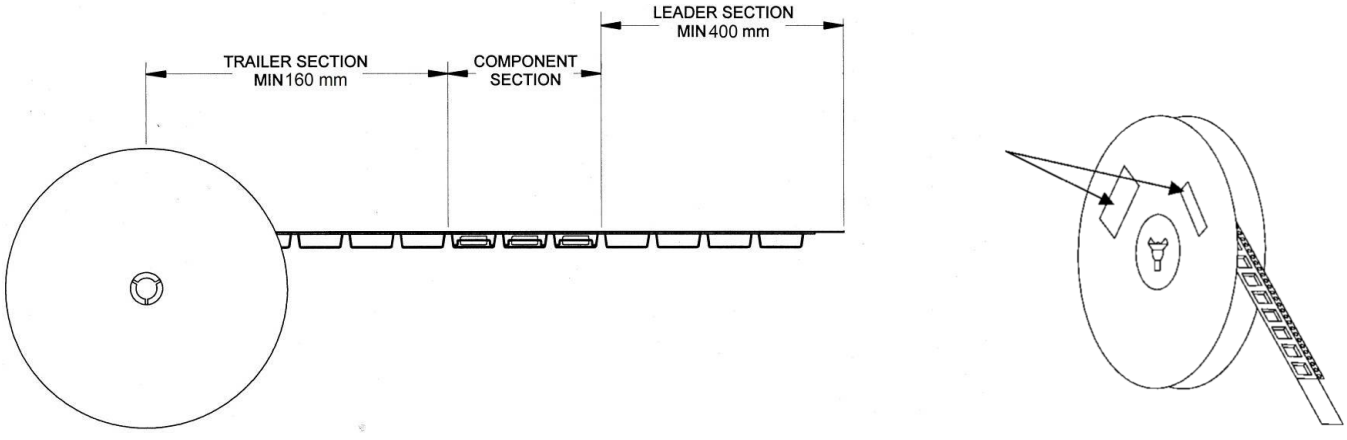
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.00
	Thickness	W2	0.717	18.20
	Space Between Flange	W1	0.504	12.80
Hub	Outer Diameter	N	4.016	102.00
	Arbor Hole Diameter	C	0.512	13.00
	Key Slit Width	B	0.079	2.00
	Key Slit Diameter	D	0.787	20.00

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Qorvo Green

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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