QPA9970D

4.3W GaN on SiC Power Amplifier Die

Product Overview

The QPA9970D is a 28 V, 4.3 W GaN on SiC high power discrete amplifier designed for commercial wireless infrastructure, cellular and WiMAX infrastructure, industrial / scientific / medical, and general purpose broadband amplifier applications. Using an advanced high power density Gallium Nitride (GaN) semiconductor process, the QPA9970D is able to achieve high efficiency and flat gain over a broad frequency range in a single amplifier design with proper heat sinking and assembly. The QPA9970D is an unmatched 0.5 µm gate, GaN transistor die suitable for many applications with > 36 dBm 3 dB – compressed power, >60 % 3 dB – compressed drain efficiency, and >21 dB small signal gain at 2 GHz.

0.448 x 0.825 x 0.1 mm die

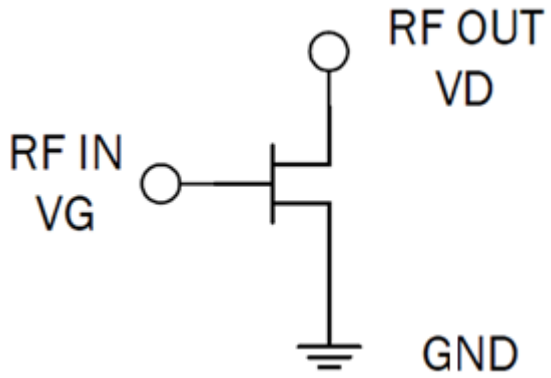
Key Features

- Broadband Operation DC to 10 GHz
- Advanced GaN HEMT Technology
- Small Signal Gain = 21.4 dB at 2.14 GHz
- 28 V Typical Performance
- Output Power 4.3 W at P3dB
- Drain Efficiency 60% at P3dB
- Dimensions:

  GaN Die: 0.448 x 0.825 x 0.1 mm

  Active Area Periphery: 2.22 mm

Functional Block Diagram



Applications

- Commercial Wireless Infrastructure
- Cellular and WiMAX Infrastructure
- Civilian and Military Radar
- General Purpose Broadband Amplifiers
- Public Mobile Radios
- Industrial, Scientific, and Medical

Ordering Information

Part Number	Description
QPA9970D	4.3 W GaN on SiC PA

Absolute Maximum Ratings[1]

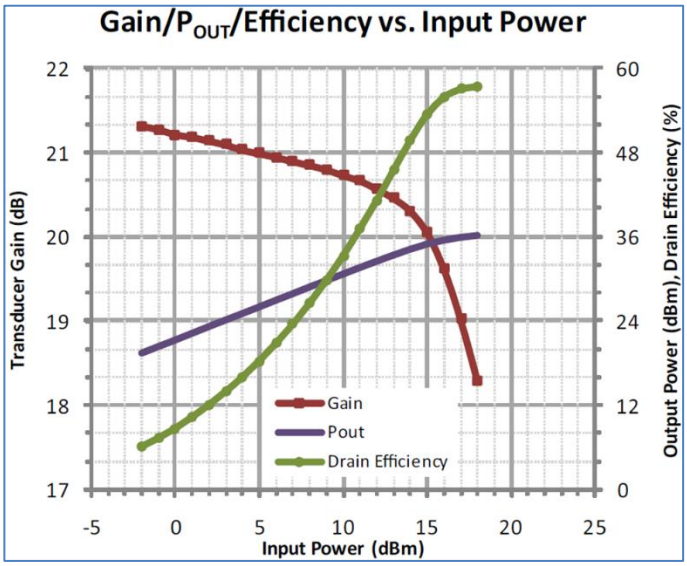
Parameter	Rating
Drain Voltage (V_D)	+155 V
Gate Voltage (V_G)	-6 to +2 V
Gate Current (I_G)	+2.2 mA
Operational Voltage	+28 V
Storage Temperature Range	-55 to +125 °C
Operational Junction Temperature (T_J)	200 °C
MTTF (T_J <200 °C, 95% Confidence Limits) [2]	1.8 x 10^7 Hours
Thermal Resistance (R_{TH}), Junction to die backside [3]	12.5 °C/W

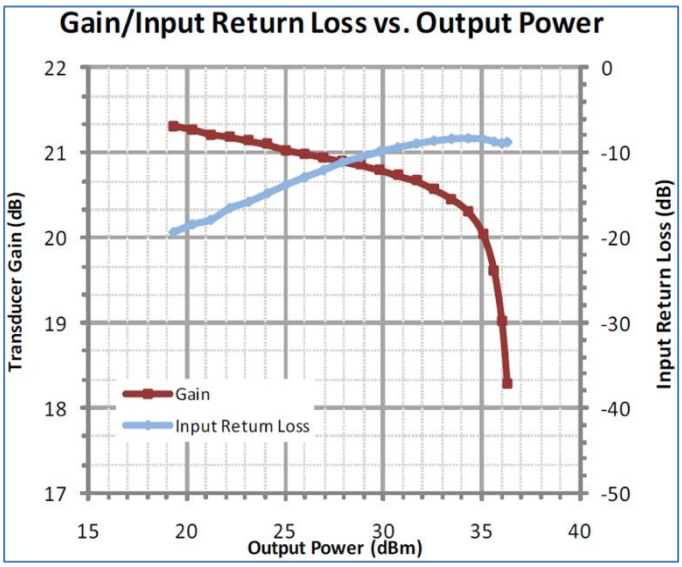
1. Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.
2. MTTF = Median Time to Failure for failure wear-out mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT (random) failure rate.
3. User will need to define this specification in the final application and ensure bias conditions satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH}$ J-C and $T_C = T_{DIE}$ to maintain maximum operating junction temperature and MTTF.

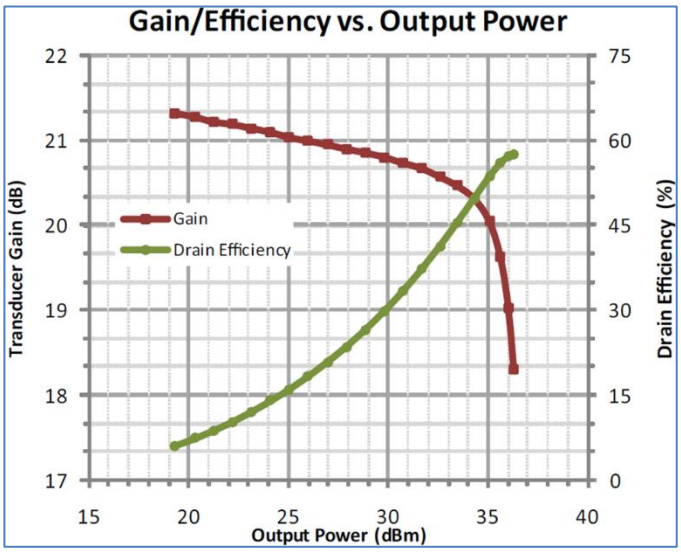
Electrical Specifications

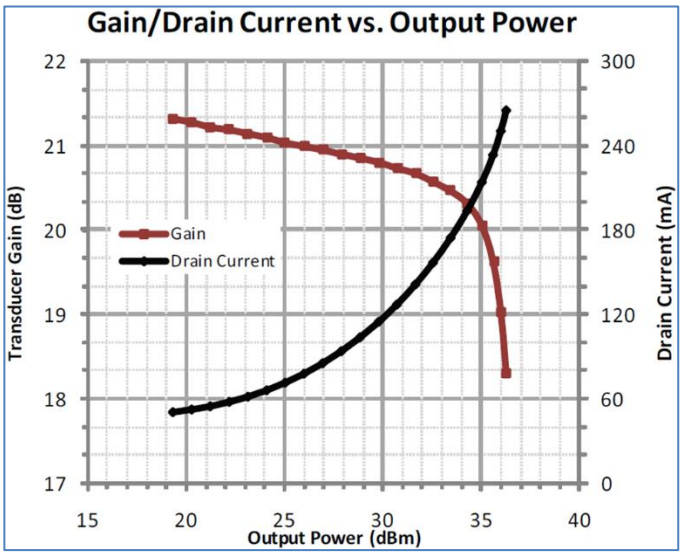
Parameter	Condition [1]	Min	Typ	Max	Unit
Drain Voltage (V_{DSQ})			28		V
Gate Voltage (V_{GSQ})	V_D = 28 V, I_D = 44 mA		-0.96		V
Drain Bias Current			44		mA
Frequency of Operation	Based on 10dB power gain, calculated from f_{MAX}	DC		10	GHz
DC Functional Test					
V_G (on) – Forward Bias Diode Gate Voltage	I_G = 2.22 mA, V_D = 0 V	0.4	0.95	1.2	V
BV (off) – Drain Breakdown Voltage	V_G = -4 V, I_D = 2.22 mA	100	>150		V
V_{PO-} Threshold Voltage	V_D = 20 V, I_D = 2 mA	-1.9	-1.48	-1.1	V
Die Capacitance from on-wafer CV measurements					
C_{RSS}	V_D = 28 V, I_D = 44 mA		60		f_F
C_{ISS}	V_D = 28 V, I_D = 44 mA		5460		f_F
C_{OSS}	V_D = 28 V, I_D = 44 mA		895		f_F
RF Small Signal Figures of Merit (On-wafer Test)					
F_T	V_D = 28 V, I_D = 170 mA		10		GHz
F_{MAX} (based on G_{TU})	V_D = 28 V, I_D = 170 mA		32		GHz
F_T	V_D = 28 V, I_D = 44 mA		7		GHz
F_{MAX} (based on G_{TU})	V_D = 28 V, I_D = 44 mA		27		GHz
RF Typical Load Pull Performance (On-wafer Tests)					
Gain	V_{DQ} = 28 V, I_{DQ} = 44 mA, CW, f = 2140MHz		21.4		dB
Gain	V_{DQ} = 28 V, I_{DQ} = 44 mA, CW, f = 2700MHz		19.4		dB
Output Power at P3dB	V_{DQ} = 28 V, I_{DQ} = 44 mA, CW, f = 2140MHz		36.3		dBm
Output Power at P3dB	V_{DQ} = 28 V, I_{DQ} = 44 mA, CW, f = 2700MHz		35.8		dBm
Drain Efficiency at P3dB	V_{DQ} = 28 V, I_{DQ} = 44 mA, CW, f = 2140MHz		60		%
Drain Efficiency at P3dB	V_{DQ} = 28 V, I_{DQ} = 44 mA, CW, f = 2700MHz		60		%

Performance Data – 2.14 GHz



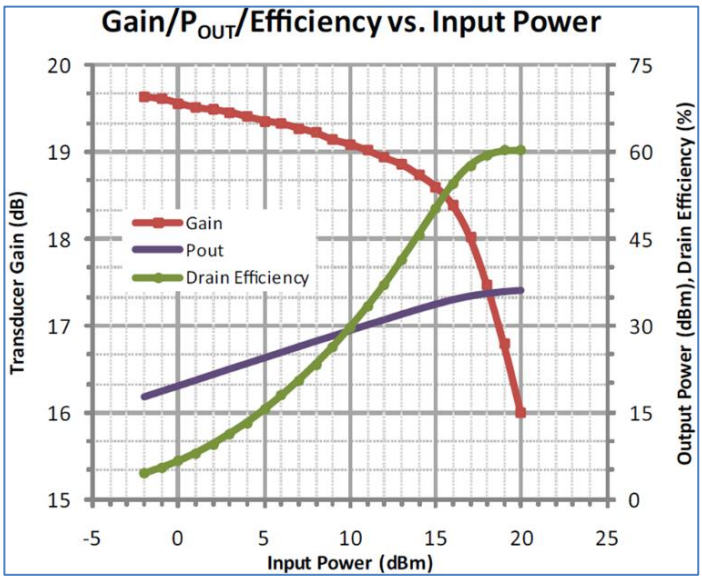


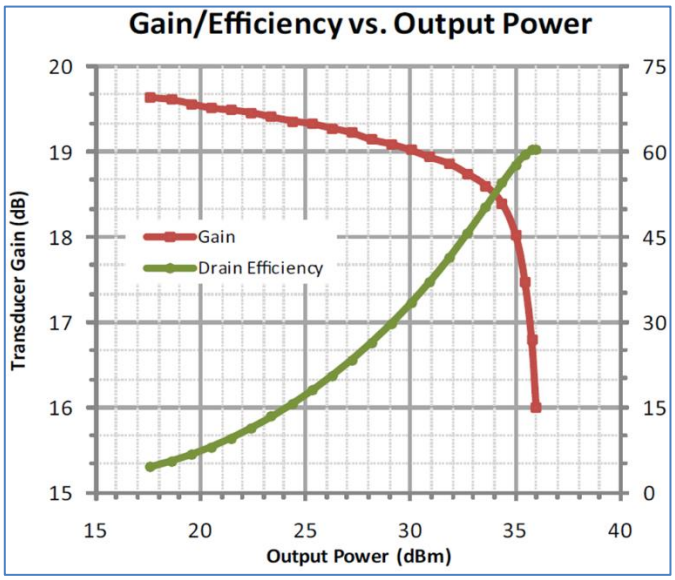


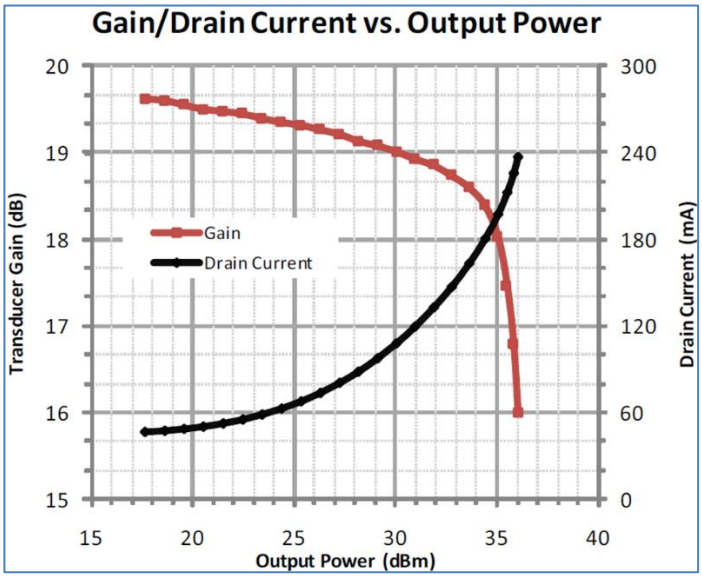


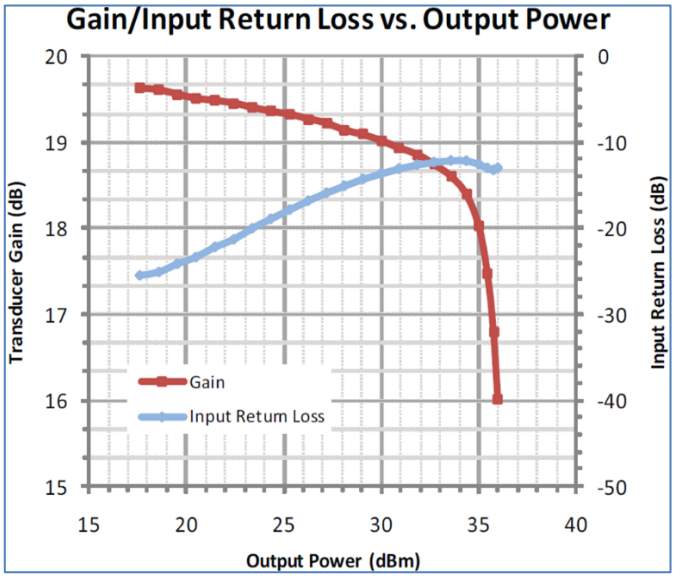
1. Typical performance at 2.14 GHz when matched to a match point located midway between points of maximum gain and maximum efficiency.
2. Test conditions: CW Operation, f = 2140 MHz, VDSQ = 28 V, IDQ = 44.4 mA, $T_{AMBIENT}$ = 25 °C measured with probes on-wafer, in Maury Microwave Load Pull Test System.

Performance Data – 2.7 GHz





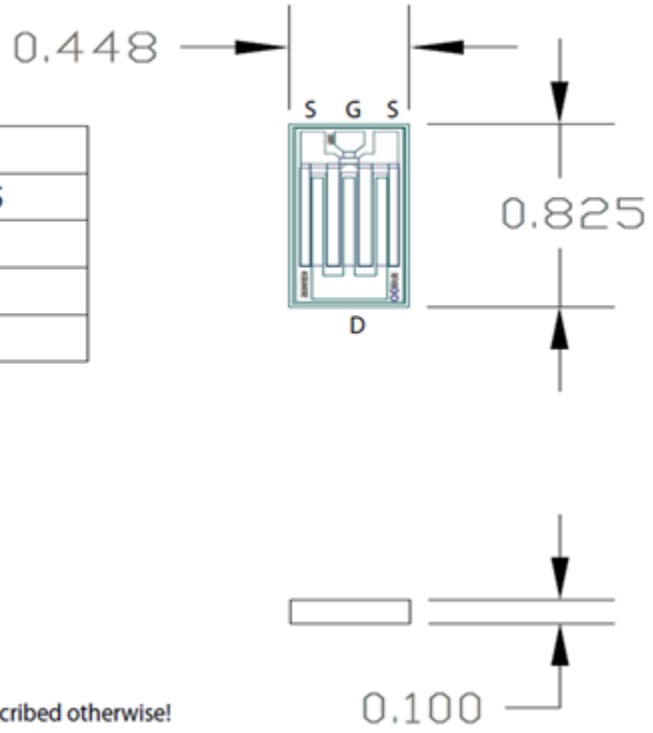




1. Typical performance at 2.7 GHz when matched to a match point located midway between points of maximum gain and maximum efficiency.
2. Test conditions: CW Operation, f = 2700 MHz, VDSQ = 28 V, IDQ = 44.4 mA, $T_{AMBIENT}$ = 25 °C measured with probes on-wafer, in Maury Microwave Load Pull Test System.

Package Drawing

Sizes (in um):	
Die:	448 x 825
Gate-Pad:	92 x 80
Source-Pad:	73 x 127
Drain-Pad:	230 x 92



All dimension in mm (metric), if not described otherwise!

Bias Instructions for the QPA9970D Die

ESD Sensitive Material. Please use proper ESD precautions when handling devices die.
Die must be mounted with minimal die attach voids for proper thermal dissipation. This device is a depletion mode HEMT and must have gate voltage applied for pinched off prior to applying drain voltage.

1. Mount device on carrier or package with minimal die attach voiding and applying proper heat removal techniques.
2. Connect ground to the ground supply terminal and ensure that both the V_G and V_D grounds are also connected to this ground terminal.
3. Apply -4 V to V_G.
4. Apply 28 V to V_D.
5. Increase V_G until drain current reaches desired bias point.
6. Turn on the RF input.

Assembly Notes

Die Storage:

- Individual bare die should be held in appropriately sized ESD waffle trays or ESD GEL packs.
- Die should be stored in CDA / N2 cabinets and in a controlled temperature and humidity environment.

Die Handling:

- Die should only be picked using an auto or semi-automated pick system and an appropriate pick tool.
- Pick parameters will need to be carefully defined so not to cause damage to either the top or bottom die surface.
- GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.
- Qorvo does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

Caution: The use of inappropriate or worn-out ejector needle and improper ejection parameter settings can cause die backside tool marks or micro-cracks that can eventually lead to die cracking.

Die Attach:

There are two commonly applied die attach processes: adhesive die attach and eutectic die attach. Both processes use special equipment and tooling to mount the die.

EUTECTIC ATTACH:

- 80 / 20 AµSn preform, 0.5 mil to 1 mil thickness, made from virgin melt gold.
- Pulsed heat or die scrub attach process using auto or semi-automatic equipment.
- Attach process carried out in an inert atmosphere.
- Custom die pick collets are required that match the outline of the die and the specific process employed using either pulsed, fixed heat, or scrub.
- Maximum temperature during die attach should be no greater than 320 °C and for less than 30 seconds.
- Key parameters that need to be considered include: die placement force, die scrub profile and heat profile.
- Minimal amount of voiding is desired to ensure maximum heat transfer to the carrier and no voids should be present under the active area of the die.
- Voiding can be measured using X-ray or Acoustic Microscopy.
- The acceptable level of voiding should be determined using thermal modeling analysis.

ADHESIVE ATTACH:

- High thermal silver filled epoxy is dispensed in a controlled manner and die is placed using an appropriate collet. Assembled parts are cured at temperatures between 150 °C and 180 °C.
- Always refer to epoxy manufacturer's data sheet.
- Industry recognized standards for epoxy die attach are clearly defined within MIL-883.

Early Life Screen Conditions:

Qorvo recommends an Early Life Screen test that subjects this die to T_J = 250 °C (junction temperature) for at least 1 hour prior to field deployment.

Mounting and Thermal Considerations:

The thermal resistance provided as R_{TH} (junction to die backside) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

Assembly Notes

Mounting and Thermal Considerations – continued

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200 °C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

DC Bias:

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. QORVO recommends applying V_{GS} = −5 V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

GaN HEMT Capacitances:

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. QORVO presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

Handling Precautions

GaN devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly, and test.

Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU .

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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