QPD0305

2x20 W, 48 V, 3.4 – 3.8 GHz, Dual GaN RF Transistor

Product Overview

The QPD0305 is a dual-path GaN power amplifier in a DFN package which operates from 3.4 to 3.8 GHz. In each path is a single-stage amplifier transistor capable of delivering P_{SAT} of 25.1 W at +48 V operation.

Lead-free and RoHS compliant.

6 Pin 7 x 6.5 mm DFN Package

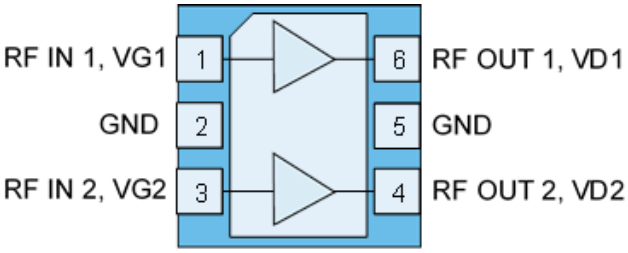
Key Features

- Operating Frequency Range: 3.4 – 3.8 GHz
- Operating Drain Voltage: +48 V
- Maximum Output Power (P_{3dB}): 25.1 W (1)
- Maximum Drain Efficiency: 79.4% (1)
- Efficiency-Tuned P3dB Gain: 18.9 dB (1)
- 7 x 6.5 mm DFN Package

Notes:

1. Single-path load pull data at 3.6 GHz.

Functional Block Diagram



Applications

- WCDMA / LTE
- Macrocell Base Station Driver
- Microcell Base Station
- Small Cell
- Active Antenna
- 5G Massive MIMO
- Symmetric Doherty Applications

Ordering Information

Part Number	Description
QPD0305S2	2 Pieces
QPD0305SB	5 Pieces
QPD0305SQ	25 Pieces
QPD0305SR	7” Reel – 100 Pieces
QPD0305TRX	Short Reel – 500 Pieces
QPD0305TR13	13” Reel – 2500 Pieces

Absolute Maximum Ratings

Parameter	Rating
Breakdown Voltage (BV_{DG})	+165 V
Gate Voltage Range ($V_{G1,2}$)	−7 to +2 V
Drain Voltage ($V_{D1,2}$)	+55 V
Peak RF Input Power	36 dBm
VSWR Mismatch, P1dB Pulse (20% Duty Cycle, 100 µs Width), T = +25°C	10:1
Storage Temperature	−65 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Gate Voltage ($V_{G1,2}$)		−2.7		V
Drain Voltage ($V_{D1,2}$)		+48		V
Quiescent Current (I_{DQ1})		32.5		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3400		3600	MHz
Quiescent Drain Current (I_{DQ})			32.5		mA
Gain	3 dB Compression		15.5		dB
Power (P_{SAT})	3 dB Compression		43.4		dBm
Drain Efficiency	3 dB Compression		63.8		%

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse CW (20% duty cycle, 100 µs width) signal at 3600 MHz on single-path of reference fixture tuned for 3400 – 3600 MHz.

Thermal Information

Parameter	Conditions	Values	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	T_{CASE} = +85°C, T_{CH} = 120°C CW: P_{DISS} = 4.7 W, P_{OUT} = 7.1 W	7.5	°C/W

Notes:

1. Based on expected carrier amplifier efficiency of Doherty.
2. P_{OUT} assumes 10% peaking amplifier contribution of total average Doherty rated power.
3. Thermal resistance is measured to package backside.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
3400	27.2 – j76.4	20.3 – j9.2	43.7	66.0	17.5
3600	103.7 – j25.8	20.0 – j10.7	44.0	71.4	17.4
3800	30.6 + j7.1	20.3 – j14.7	43.9	69.6	16.9

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width), single path.

Efficiency-Matched Load Pull Performance

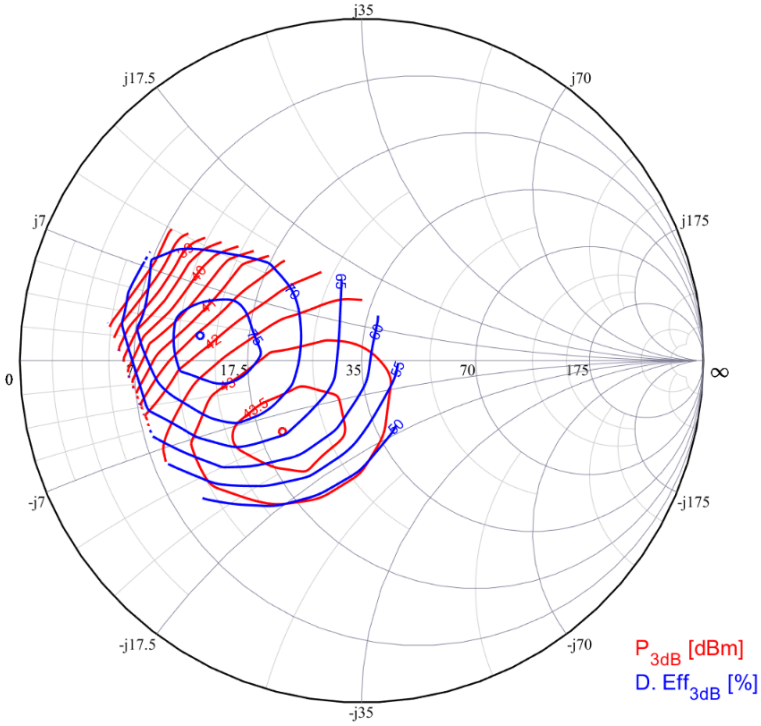
Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
3400	27.2 – j76.4	12.4 + j2.3	41.6	77.5	19.8
3600	103.7 – j25.8	15.2 – j2.0	42.8	79.4	18.9
3800	30.6 + j7.1	15.6 – j0.2	42.3	79.4	17.5

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width), single path.

Load Pull Contours

Test Conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width), single path.

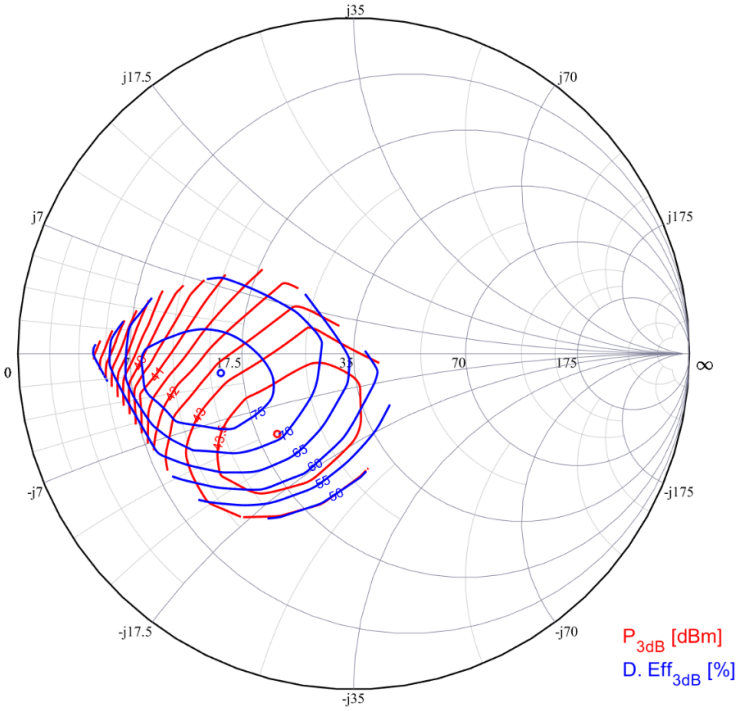
Load Pull at 3400 MHz



Power Match
$Z_{S(f0)}$ = 27.2-j76.4 Ohms
$Z_{S(2f0)}$ = 32.7+j1.1 Ohms
$Z_{L(f0)}$ = 20.3-j9.2 Ohms
$Z_{L(2f0)}$ = 7.7-j5.9 Ohms
P_{3dB} = 43.7 dBm
D_{Eff3dB} = 66.0 %
G_{3dB} = 17.5 dB

Efficiency Match
$Z_{S(f0)}$ = 27.2-j76.4 Ohms
$Z_{S(2f0)}$ = 32.7+j1.1 Ohms
$Z_{L(f0)}$ = 12.4+j2.3 Ohms
$Z_{L(2f0)}$ = 7.7-j5.9 Ohms
P_{3dB} = 41.6 dBm
D_{Eff3dB} = 77.5 %
G_{3dB} = 19.8 dB

Load Pull at 3600 MHz

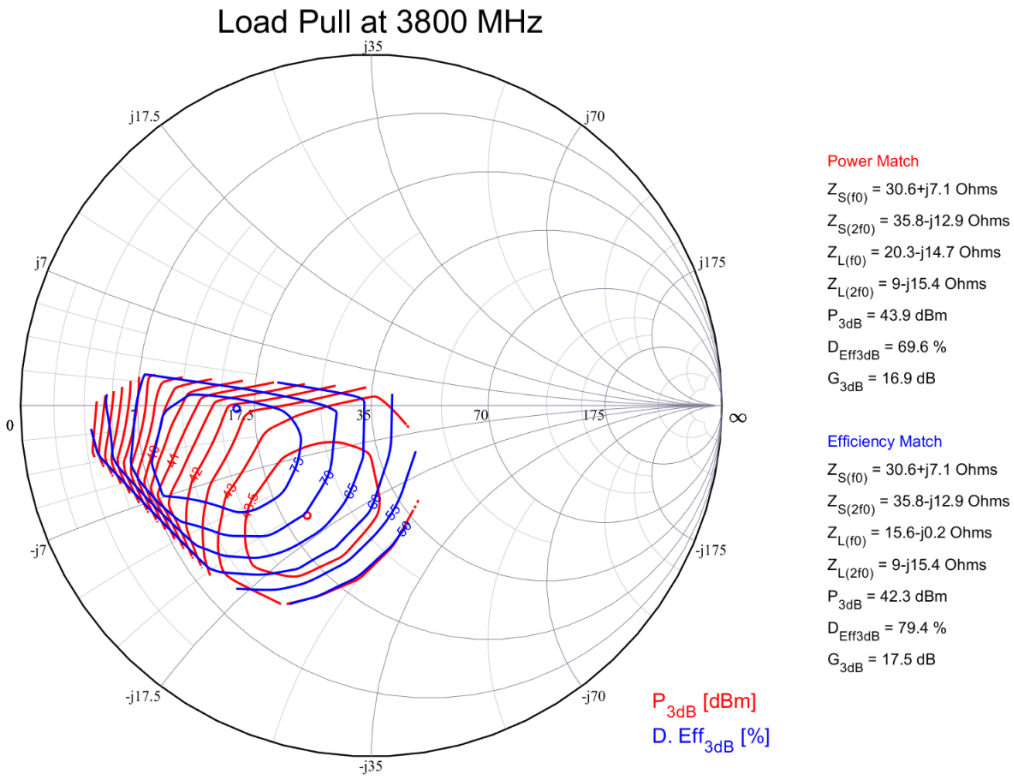


Power Match
$Z_{S(f0)}$ = 103.7-j25.8 Ohms
$Z_{S(2f0)}$ = 27.7-j1.2 Ohms
$Z_{L(f0)}$ = 20-j10.7 Ohms
$Z_{L(2f0)}$ = 7.5-j2.9 Ohms
P_{3dB} = 44.0 dBm
D_{Eff3dB} = 71.4 %
G_{3dB} = 17.4 dB

Efficiency Match
$Z_{S(f0)}$ = 103.7-j25.8 Ohms
$Z_{S(2f0)}$ = 27.7-j1.2 Ohms
$Z_{L(f0)}$ = 15.2-j2 Ohms
$Z_{L(2f0)}$ = 7.5-j2.9 Ohms
P_{3dB} = 42.8 dBm
D_{Eff3dB} = 79.4 %
G_{3dB} = 18.9 dB

Load Pull Contours

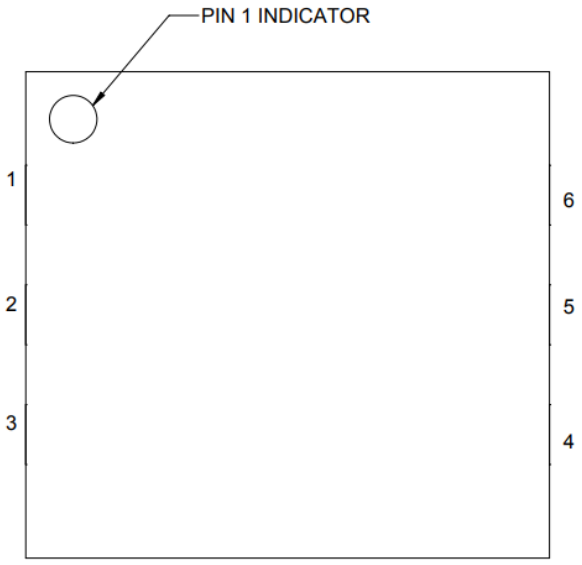
Test Conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 32.5 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width), single path.



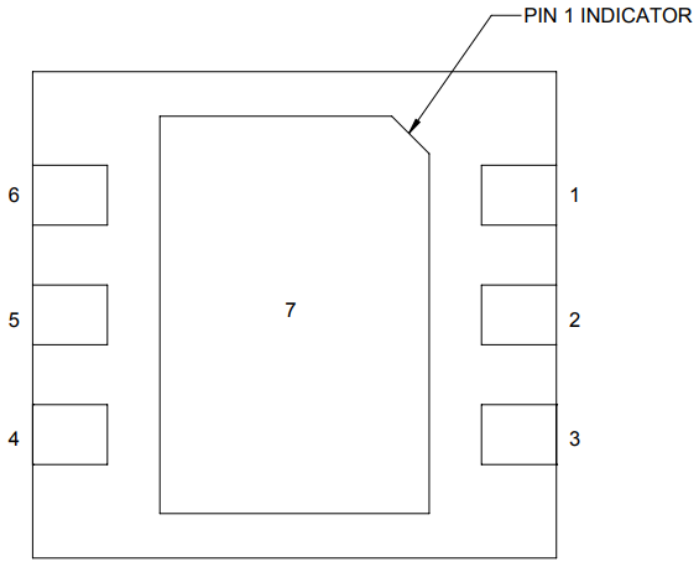
Power Match
$Z_{S(f0)}$ = 30.6+j7.1 Ohms
$Z_{S(2f0)}$ = 35.8-j12.9 Ohms
$Z_{L(f0)}$ = 20.3-j14.7 Ohms
$Z_{L(2f0)}$ = 9-j15.4 Ohms
P_{3dB} = 43.9 dBm
D_{Eff3dB} = 69.6 %
G_{3dB} = 16.9 dB

Efficiency Match
$Z_{S(f0)}$ = 30.6+j7.1 Ohms
$Z_{S(2f0)}$ = 35.8-j12.9 Ohms
$Z_{L(f0)}$ = 15.6-j0.2 Ohms
$Z_{L(2f0)}$ = 9-j15.4 Ohms
P_{3dB} = 42.3 dBm
D_{Eff3dB} = 79.4 %
G_{3dB} = 17.5 dB

Pin Configuration and Description



Top View

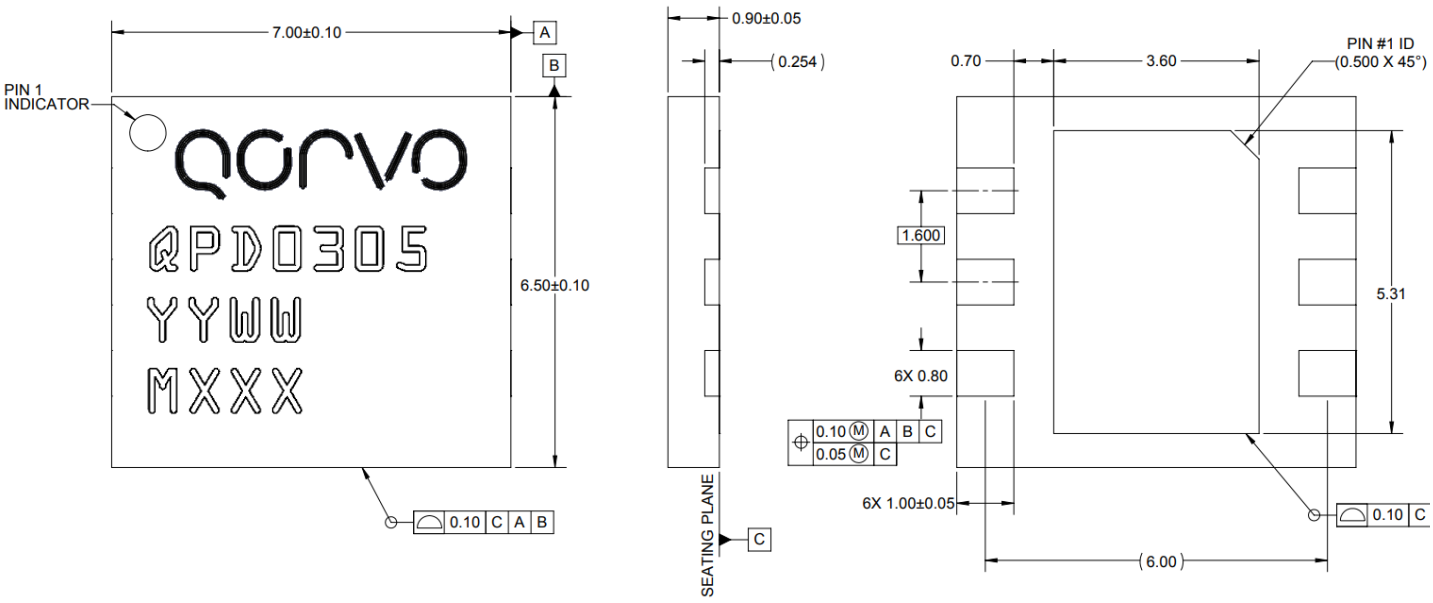


Bottom View

Pin Number	Label	Description
1	RF IN, VG1	RF Input, Gate Bias 1
2	GND	Ground
3	RF IN, VG2	RF Input, Gate Bias 2
4	RF OUT, VD2	RF Output, Drain Bias 2
5	GND	Ground
6	RF OUT, VD1	RF Output, Drain Bias 1
7 (Backside Paddle)	GND	Ground

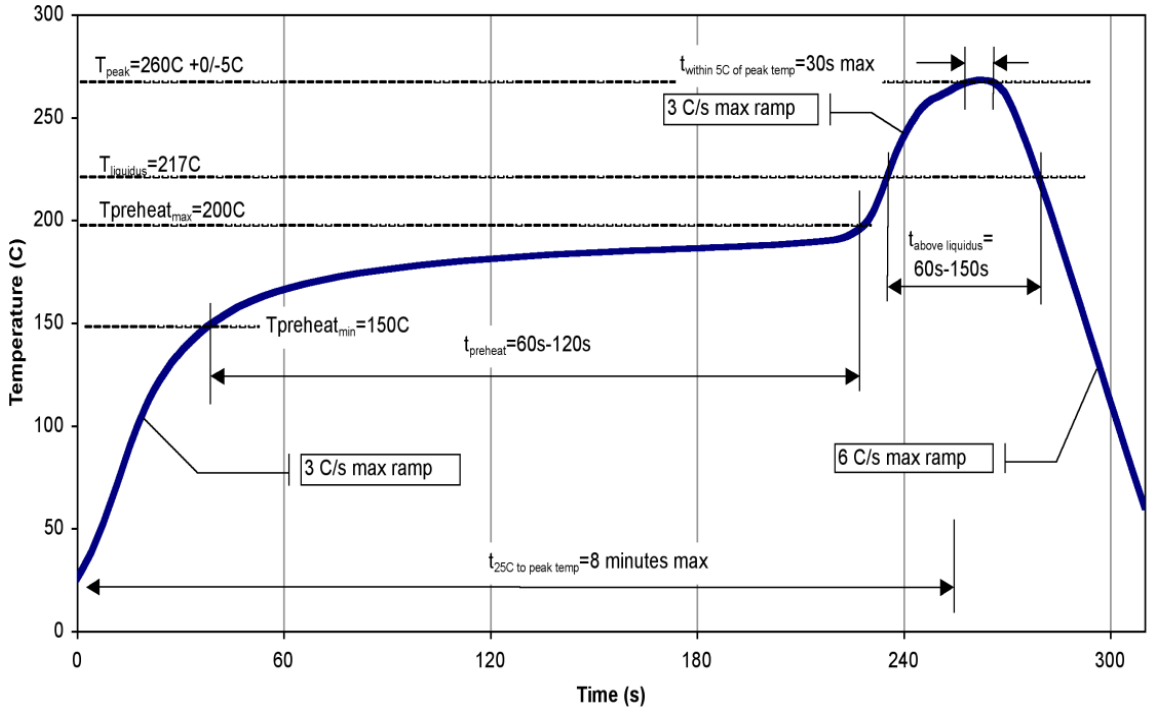
Package Marking and Dimensions

Marking: Qorvo Logo
Part Number – QPD0305
Date Code – YYWW
Lot Code – MXXX



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. General Tolerance is ±0.05.
3. Part is overmold encapsulated.
4. Contact plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A (250 V)	ANSI/ESDA/JEDEC Standard JS-001
ESD – Charged Device Model (CDM)	Class C2 (750 V)	ANSI/ESDA/JEDEC Standard JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC Standard J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering processes.

Package lead plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: BTSApplications@qorvo.com

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