

Product Overview

The Qorvo QPD1011 is a 7W (P_{3dB}), 50 Ω -input matched discrete GaN on SiC HEMT which operates from 30 MHz to 1.2 GHz. The integrated input matching network enables wideband gain and power performance, while the output can be matched on board to optimize power and efficiency for any region within the band.

The device is housed in a 5 x 6 mm leadless SMT package that saves real estate of already space-constrained handheld radios.

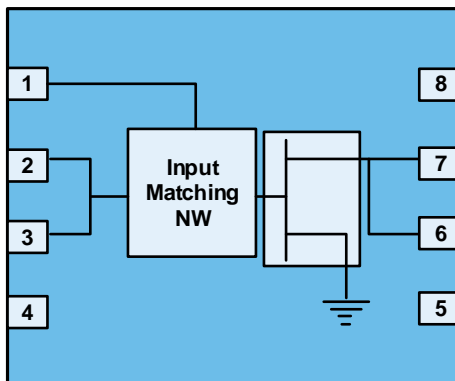
Lead-free and ROHS compliant.

Evaluation boards are available upon request.



5 x 6 x 0.85 mm Package

Functional Block Diagram



Key Features

- Frequency: 30 to 1200 MHz
 - Output Power (P_{3dB})¹: 8.7 W
 - Linear Gain¹: 21 dB
 - Typical PAE_{3dB}¹: 60 %
 - Operating Voltage: 50 V
 - CW and Pulse capable
- Note 1: @ 1 GHz Load Pull

Applications

- Military radar
- Civilian radar
- Land mobile and military radio communications
- Test instrumentation
- Wideband or narrowband amplifiers
- Jammers

Ordering Information

Part No.	Description
QPD1011SR	7" Short Reel – 100 Pieces
QPD1011EVB1	50 – 1000 MHz EVB

Absolute Maximum Ratings¹

Parameter	Rating	Units
Breakdown Voltage, V_{BDG}	+145	V
Gate Voltage Range, V_G	-7 to +2	V
Drain Current, $I_{D_{MAX}}$	1.46	A
Power Dissipation, P_{DISS}	14.7 ²	W
RF Input Power, Pulsed, 1.3 GHz, $T = 25\text{ }^\circ\text{C}^2$	+27	dBm
Mounting Temperature (30 Seconds)	320	$^\circ\text{C}$
Storage Temperature	-65 to +150	$^\circ\text{C}$

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Pulsed, 100 μS PW, 10% DC

Recommended Operating Conditions¹

Parameter	Min	Typ	Max	Units
Operating Temp. Range	-40	+25	+85	$^\circ\text{C}$
Drain Voltage Range, V_D	+32	+50	+55	V
Drain Bias Current, I_{DQ}		20		mA
Drain Current, I_D^4	-	300	-	mA
Gate Voltage, V_G^3	-	-2.8	-	V
Power Dissipation (P_D) ^{2,4}	-	-	13	W
Power Dissipation (P_D), CW ²	-	-	10	W

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85 $^\circ\text{C}$
3. To be adjusted to desired I_{DQ}
4. Pulsed, 100 μS PW, 10% DC

Measured Load Pull Performance – Power Tuned^{1, 2}

Parameter	Typical Values				Units
	0.6	0.8	1.0	1.2	
Frequency, F	0.6	0.8	1.0	1.2	GHz
Drain Voltage, V_D	50	50	50	50	V
Drain Bias Current, I_{DQ}	20	20	20	20	mA
Output Power at 3dB compression, P_{3dB}	39.7	39.4	39.4	39.1	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	59.4	58.7	49.3	49.1	%
Gain at 3dB compression, G_{3dB}	15.7	18	18.3	16.6	dB

Notes:

1. Pulsed, 100 μS Pulse Width, 10% Duty Cycle
2. Characteristic Impedance $Z_0 = 33.4\ \Omega$.

Measured Load Pull Performance – Efficiency Tuned^{1, 2}

Parameter	Typical Values				Units
	0.6	0.8	1.0	1.2	
Frequency, F	0.6	0.8	1.0	1.2	GHz
Drain Voltage, V_D	50	50	50	50	V
Drain Bias Current, I_{DQ}	20	20	20	20	mA
Output Power at 3dB compression, P_{3dB}	37.7	38.4	37.3	37.4	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	71.6	64.1	60.1	55.4	%
Gain at 3dB compression, G_{3dB}	17.9	19.2	19.5	19.1	dB

Notes:

1. Pulsed, 100 μS Pulse Width, 10% Duty Cycle
2. Characteristic Impedance $Z_0 = 33.4\ \Omega$.

50 – 1000 MHz EVB at 500 MHz Performance¹

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	17.8	–	dB
Output Power at 3dB compression point, P3dB	–	7.2	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	52.6	–	%
Gain at 3dB compression point, G3dB	–	14.8	–	dB

1. $V_D = +50$ V, $I_{DQ} = 20$ mA, Temp = +25 °C, CW

RF Characterization – Mismatch Ruggedness at 1000 MHz¹

Symbol	Parameter	Input Drive Level	Typical
VSWR	Impedance Mismatch Ruggedness	23 dBm	10:1

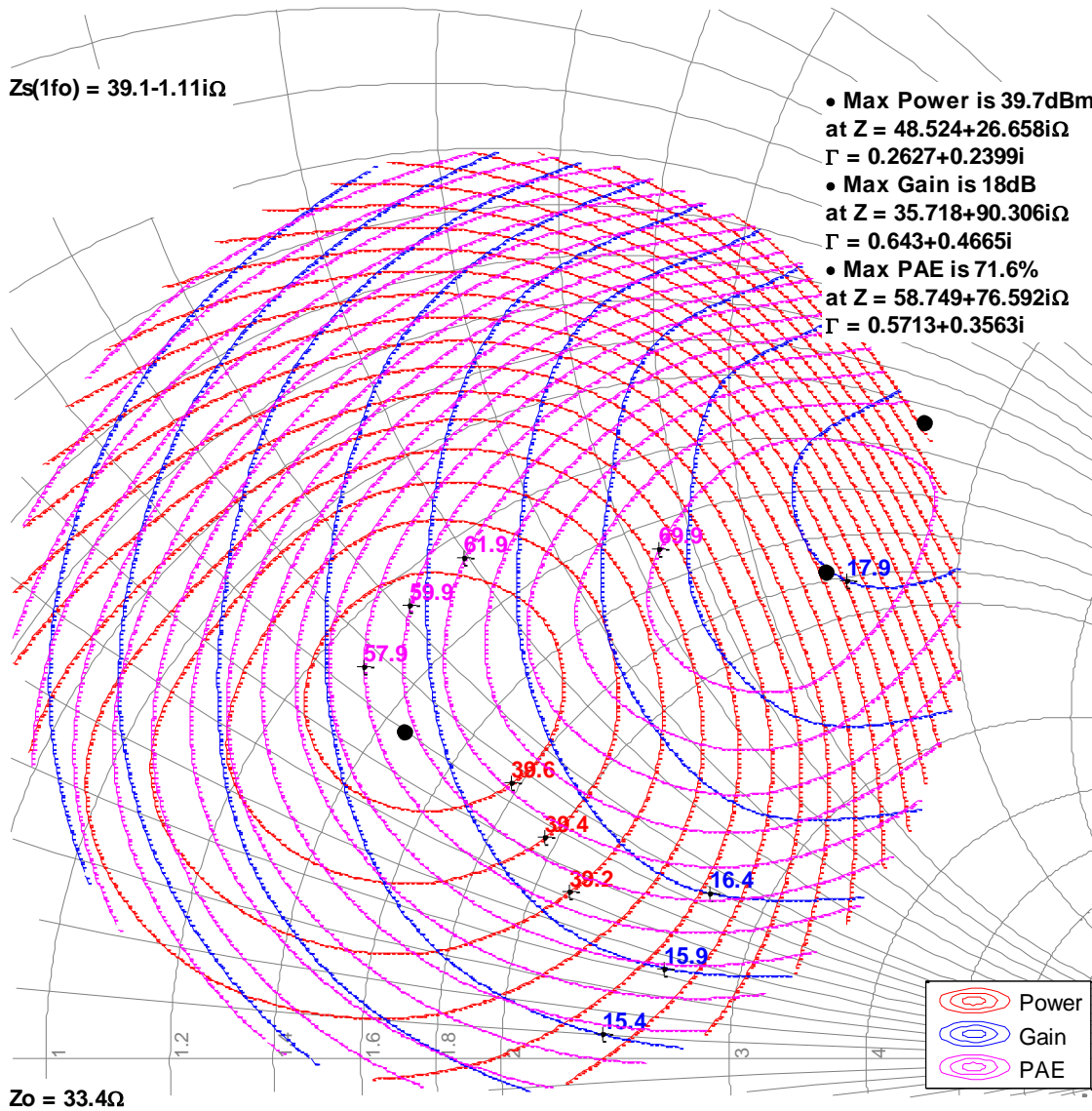
1. Test conditions unless otherwise noted: $T_A = 25$ °C, $V_D = 50$ V, $I_{DQ} = 20$ mA, CW

Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, 100 uS Pulse Width, 10% Duty Cycle
2. See page 18 for load pull reference planes where the performance was measured.

0.6GHz, Load-pull

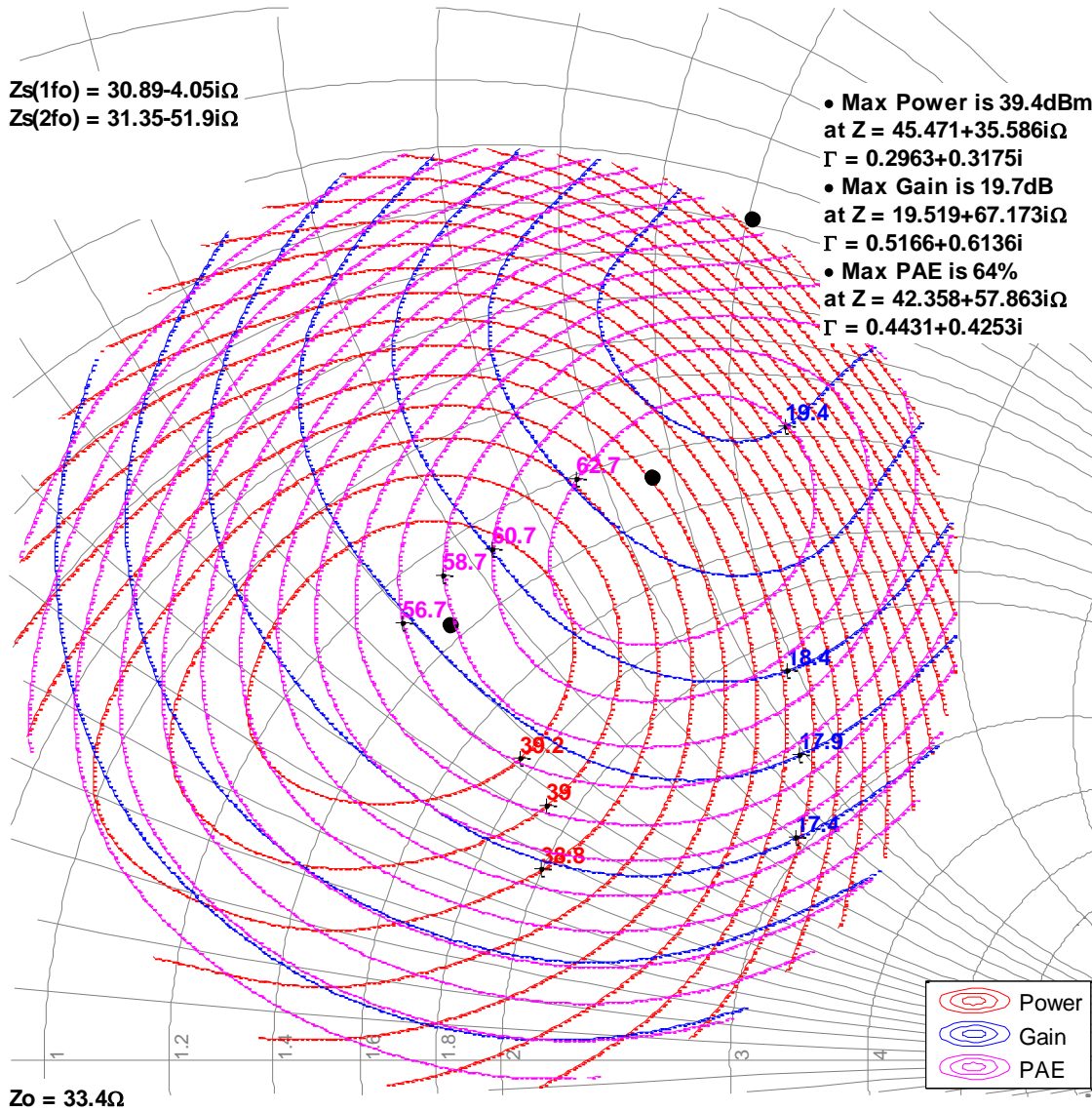


Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, 100 μs Pulse Width, 10% Duty Cycle
2. See page 18 for load pull reference planes where the performance was measured.

0.8GHz, Load-pull

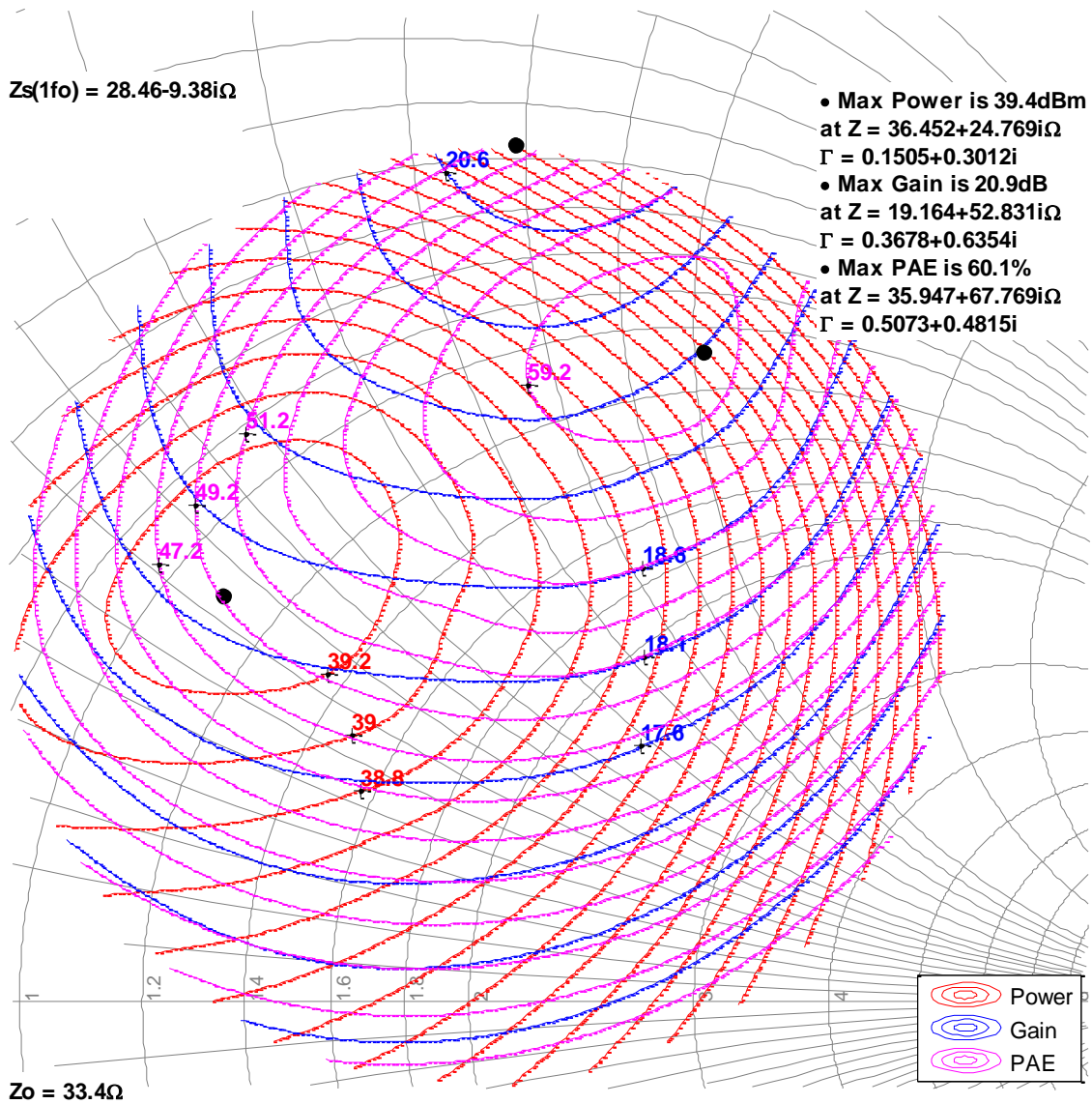


Measured Load-Pull Smith Charts^{1,2}

Notes:

1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, 100 μs Pulse Width, 10% Duty Cycle
2. See page 18 for load pull reference planes where the performance was measured.

1GHz, Load-pull

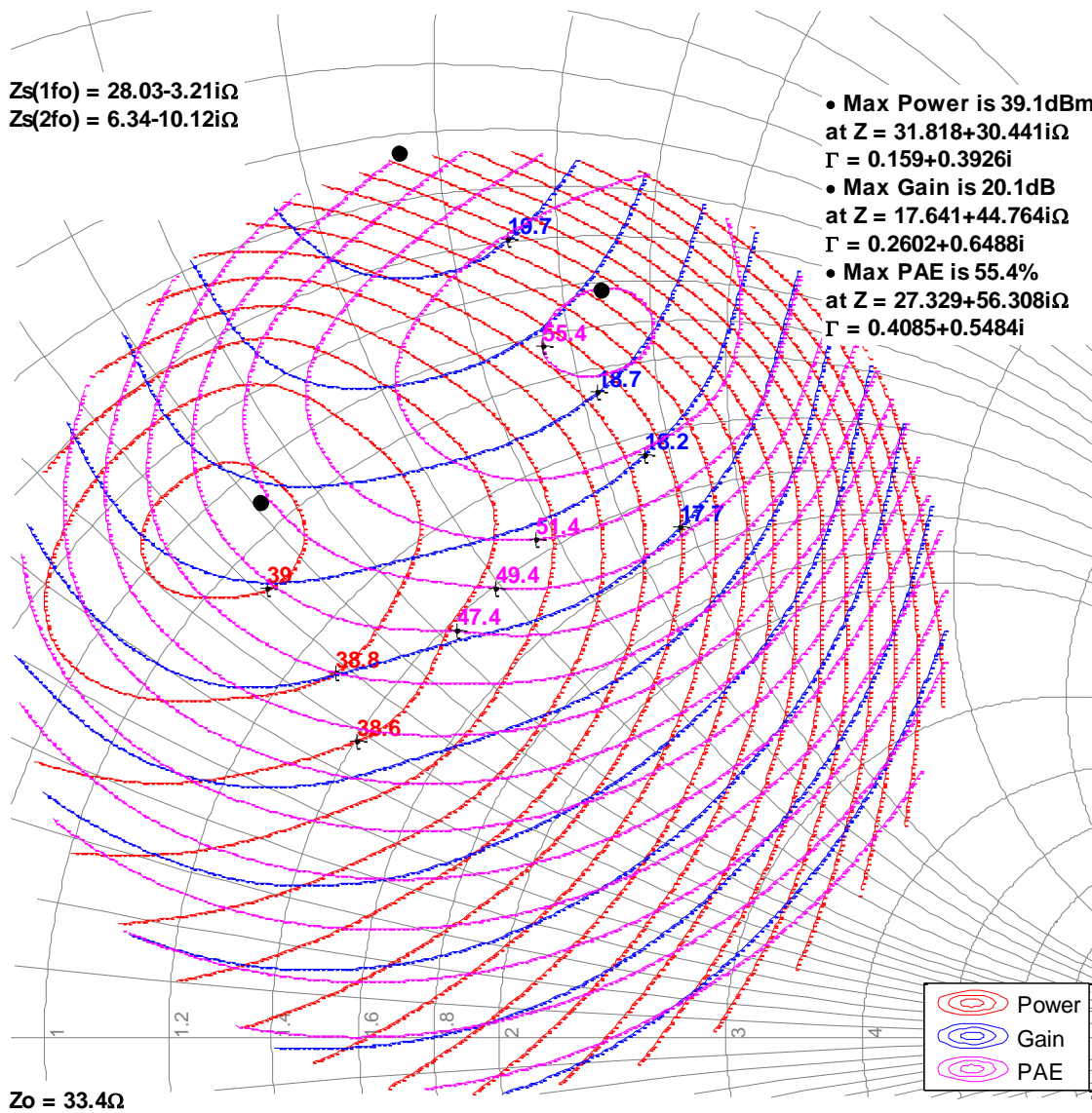


Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, 100 μs Pulse Width, 10% Duty Cycle
2. See page 18 for load pull reference planes where the performance was measured.

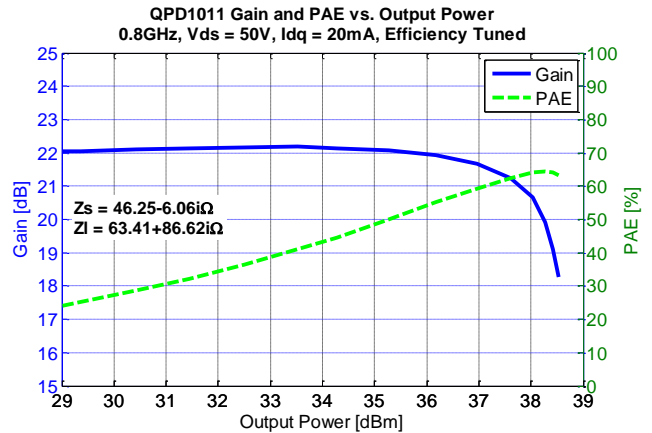
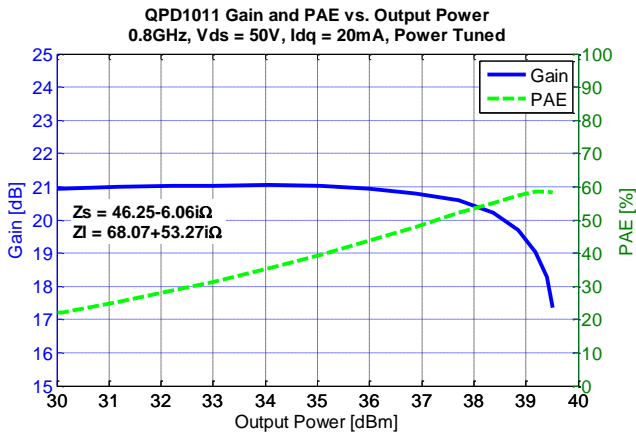
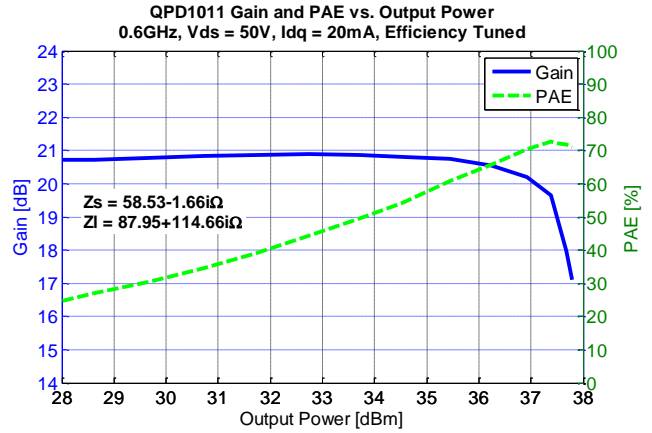
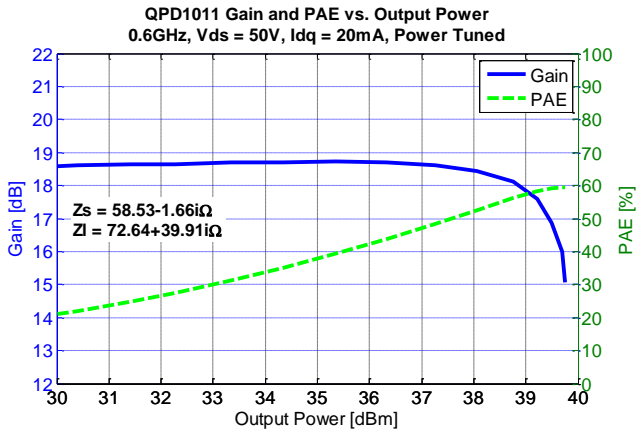
1.2GHz, Load-pull



Typical Measured Performance – Load-Pull Drive-up^{1, 2}

Notes:

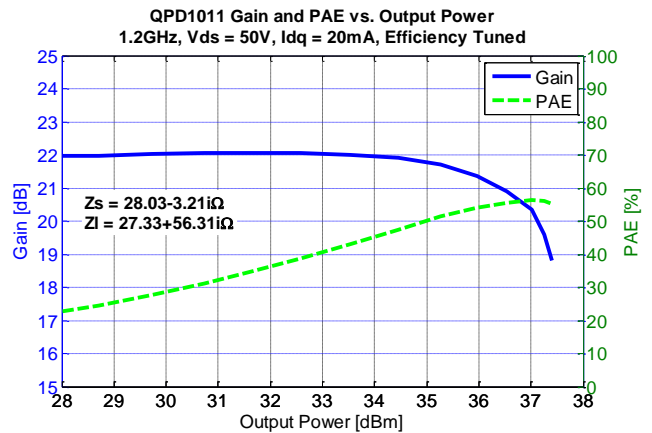
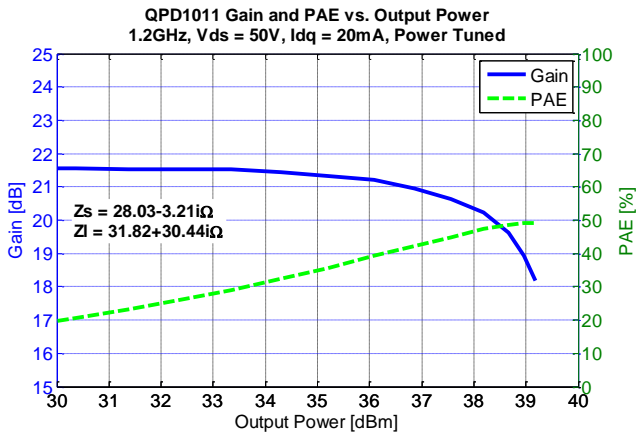
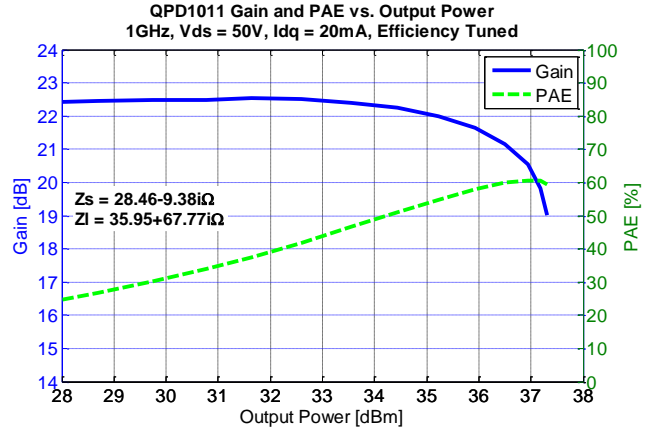
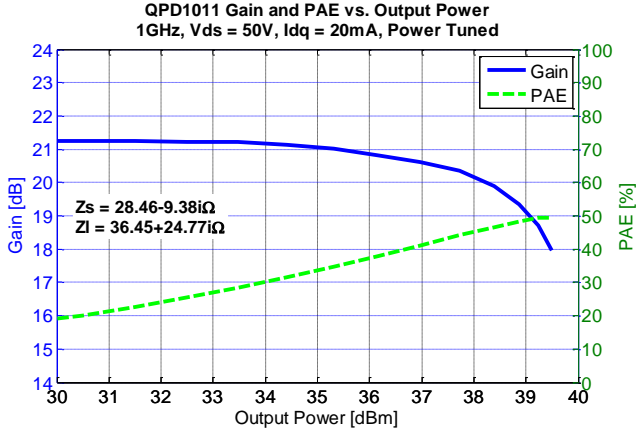
1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, 100 μs Pulse Width, 10% Duty Cycle
2. See page 18 for load-pull and source-pull reference planes where the performance was measured.



Typical Measured Performance – Load-Pull Drive-up^{1, 2}

Notes:

1. C Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, 100 μs Pulse Width, 10% Duty Cycle
2. See page 18 for load-pull and source-pull reference planes where the performance was measured.

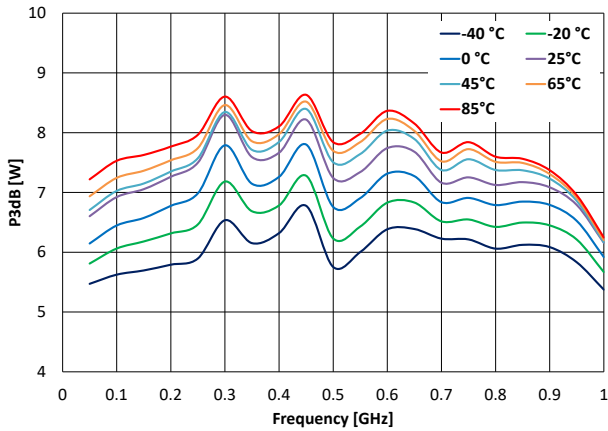


Power Driveup Performance Over Temperatures Of 50 – 1000 MHz EVB^{1,2}

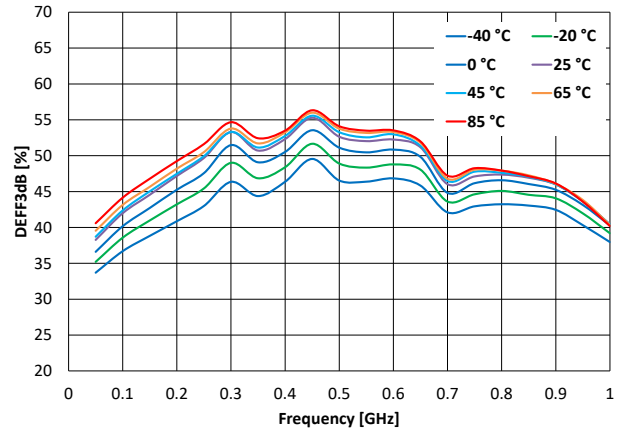
Notes:

1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW
2. The dissipation power is calculated at EVB level. The device dissipation power is lower due to input and output matching network losses.

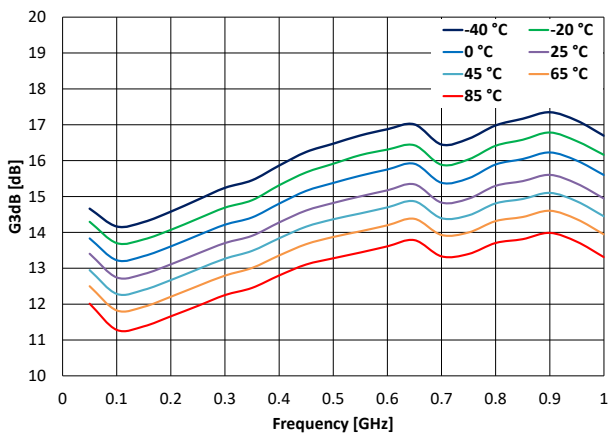
P3dB Over Temperatures



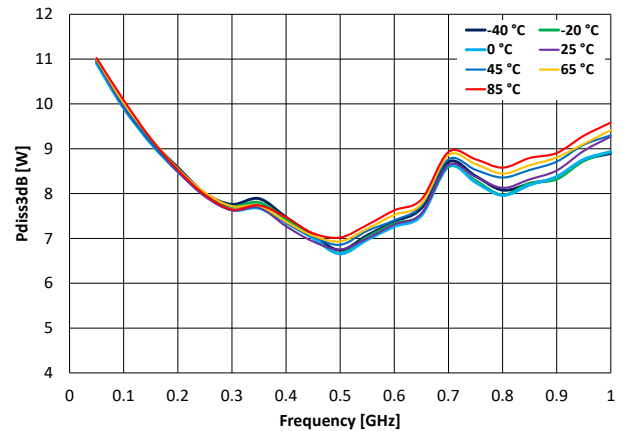
DEFF3dB Over Temperatures



G3dB Over Temperatures



Pdiss3dB Over Temperatures

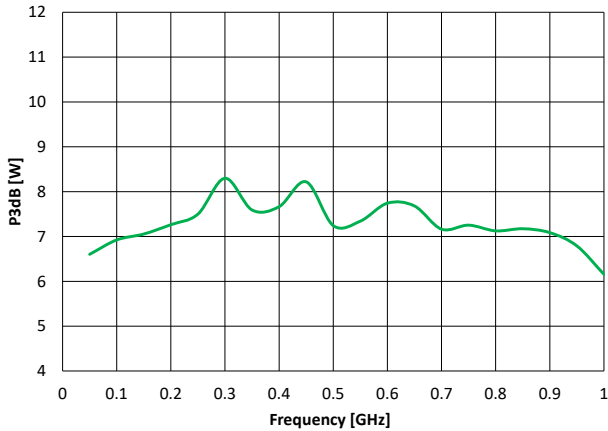


Power Driveup Performance At 25°C Of 50 – 1000 MHz EVB^{1,2}

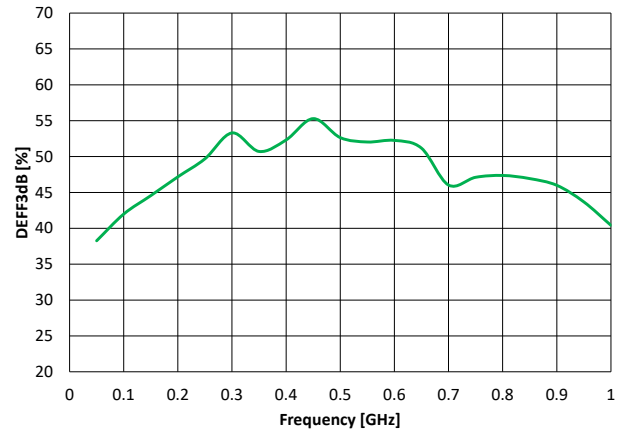
Notes:

1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$, CW
2. The dissipation power is calculated at EVB level. The device dissipation power is lower due to input and output matching network losses.

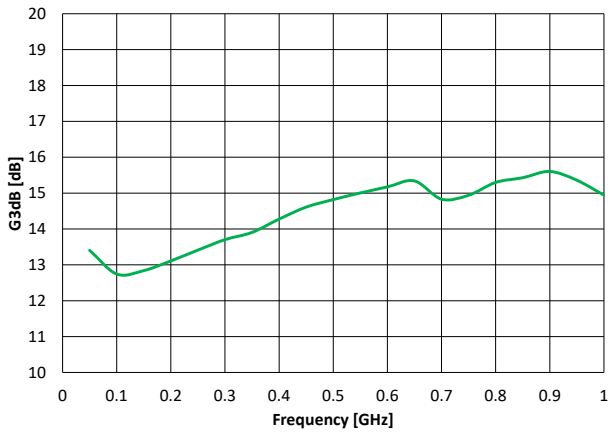
P3dB At 25 °C



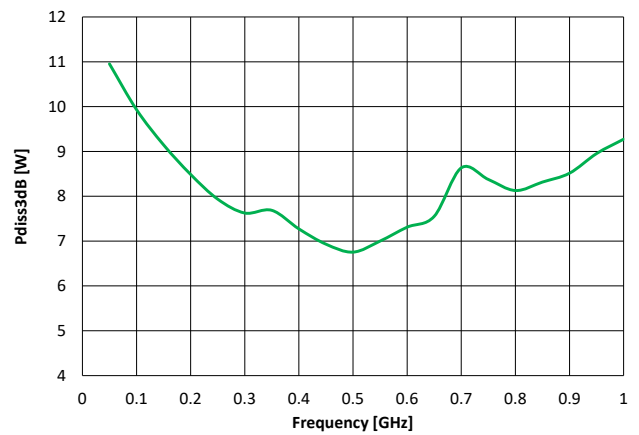
DEFF3dB At 25 °C



G3dB At 25 °C



Pdiss3dB At 25 °C

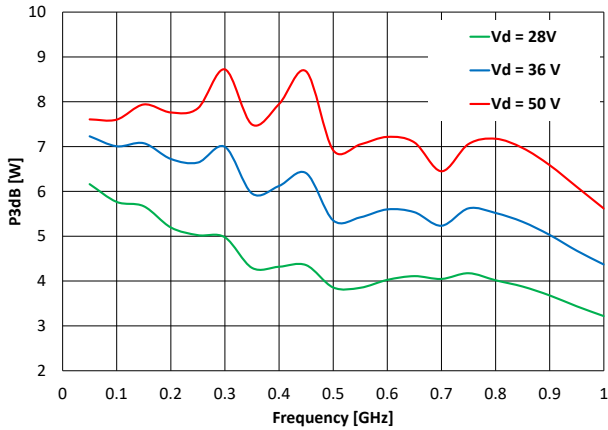


Power Driveup Performance At 25°C Over Drain Voltage Of 50 – 1000 MHz EVB^{1, 2}

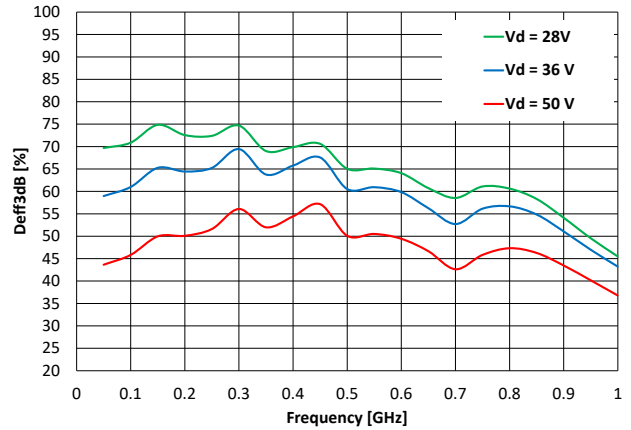
Notes:

1. Test Conditions: $I_{DQ} = 20 \text{ mA}$, CW
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network..

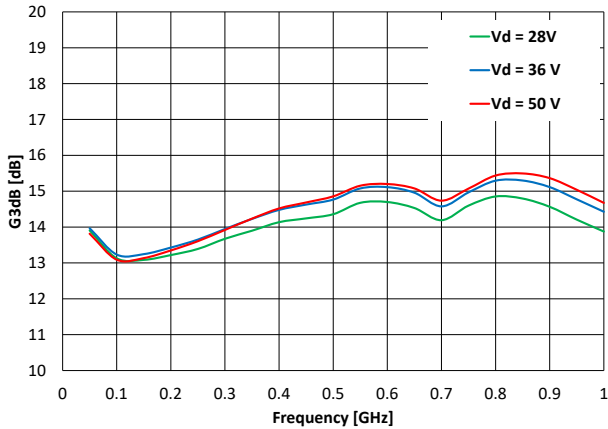
P3dB Over Drain Voltage



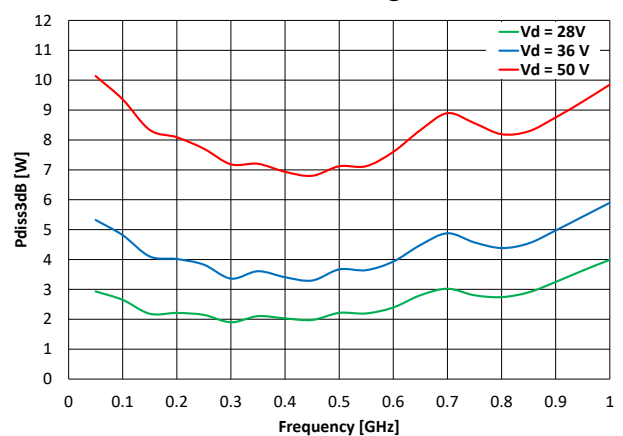
Deff3dB Over Drain Voltage



G3dB Over Drain Voltage



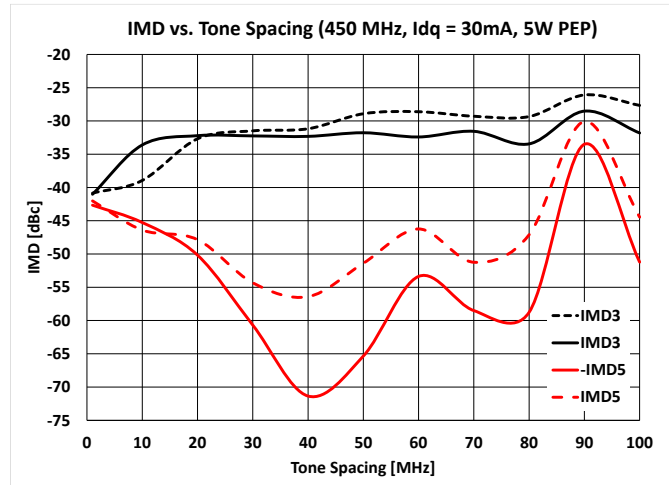
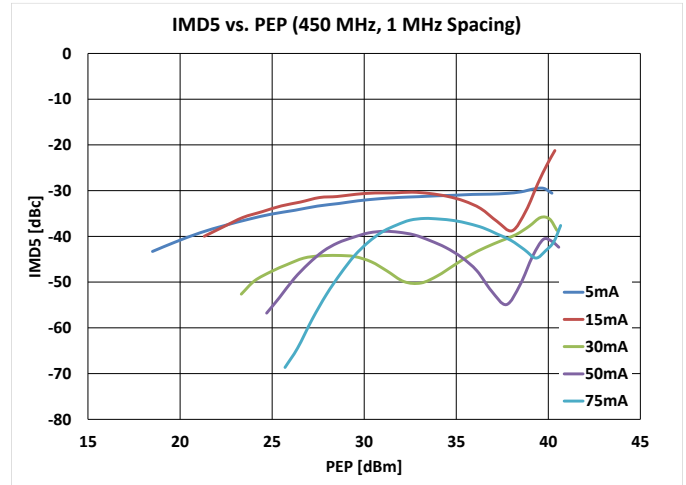
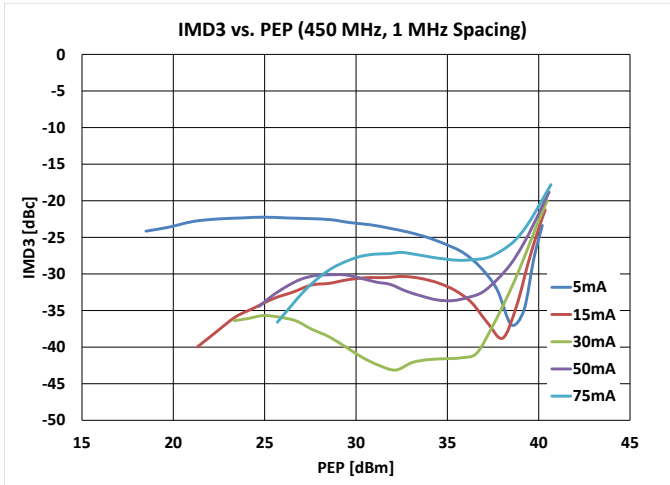
Pdiss3dB Over Drain Voltage, Tamb = 25 °C



2-Tone Performance At 25°C Of 50 – 1000 MHz EVB¹

Notes:

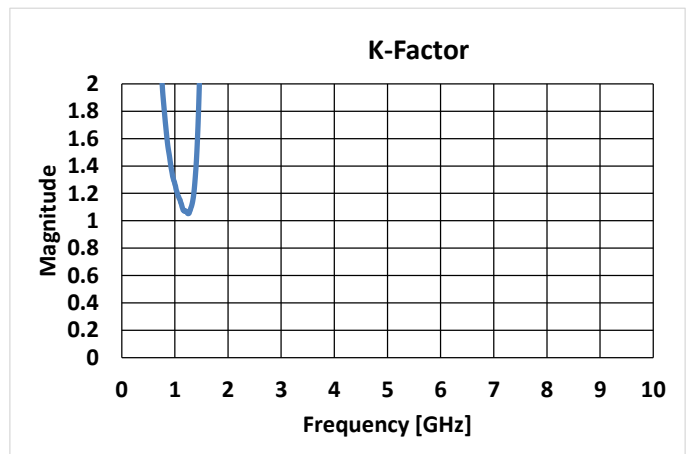
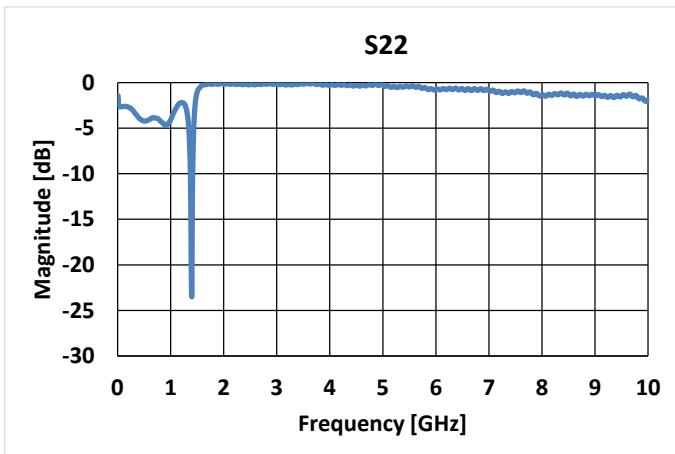
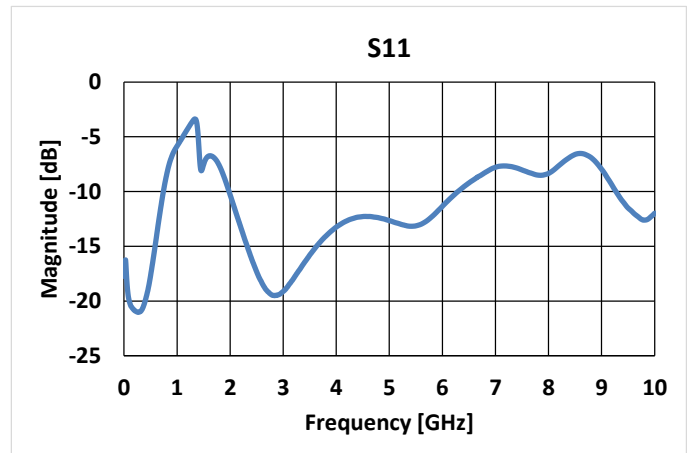
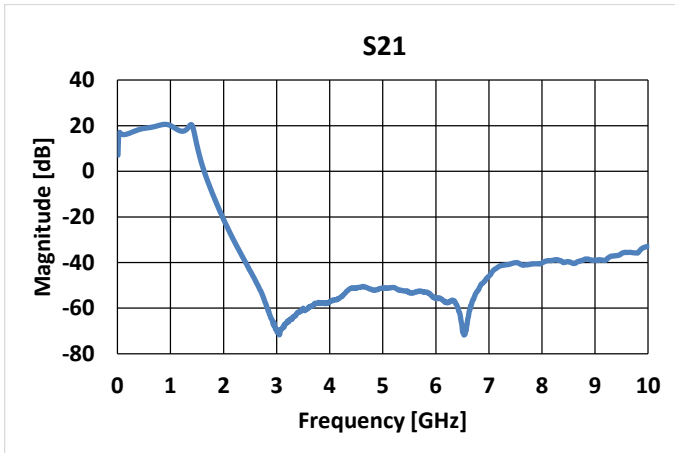
1. Test Conditions: $I_{DQ} = 20 \text{ mA}$, CW



S-Parameters At -40°C Of 50 – 1000 MHz EVB^{1, 2}

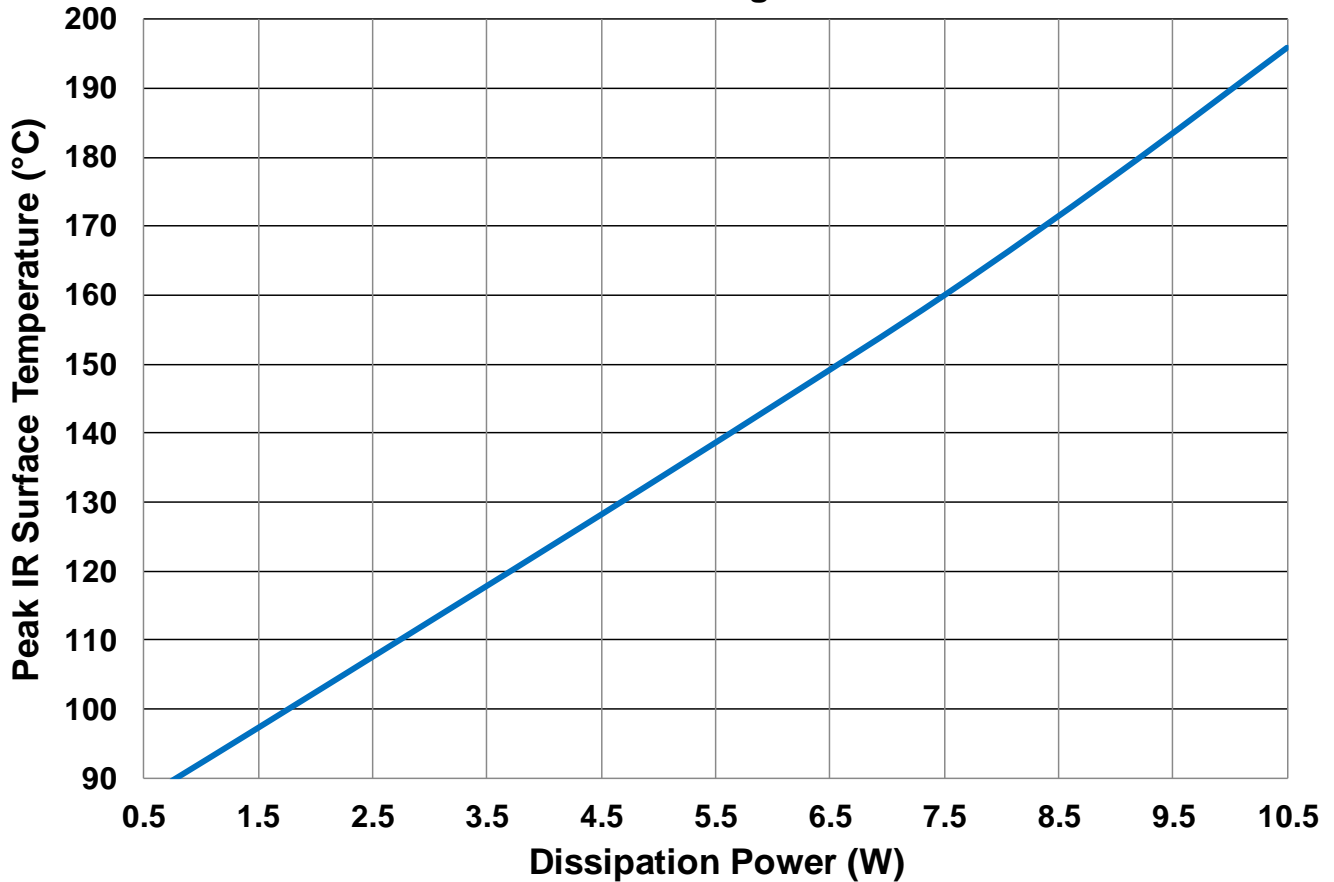
Notes:

1. Test Conditions: $V_D = 50\text{ V}$, $I_{DQ} = 20\text{ mA}$
2. K-factor > 1 indicates unconditional stability



Thermal and Reliability Information - CW

**Peak IR Surface Temperature vs. CW Dissipation Power
Base of DFN Package Fixed at 85 °C**

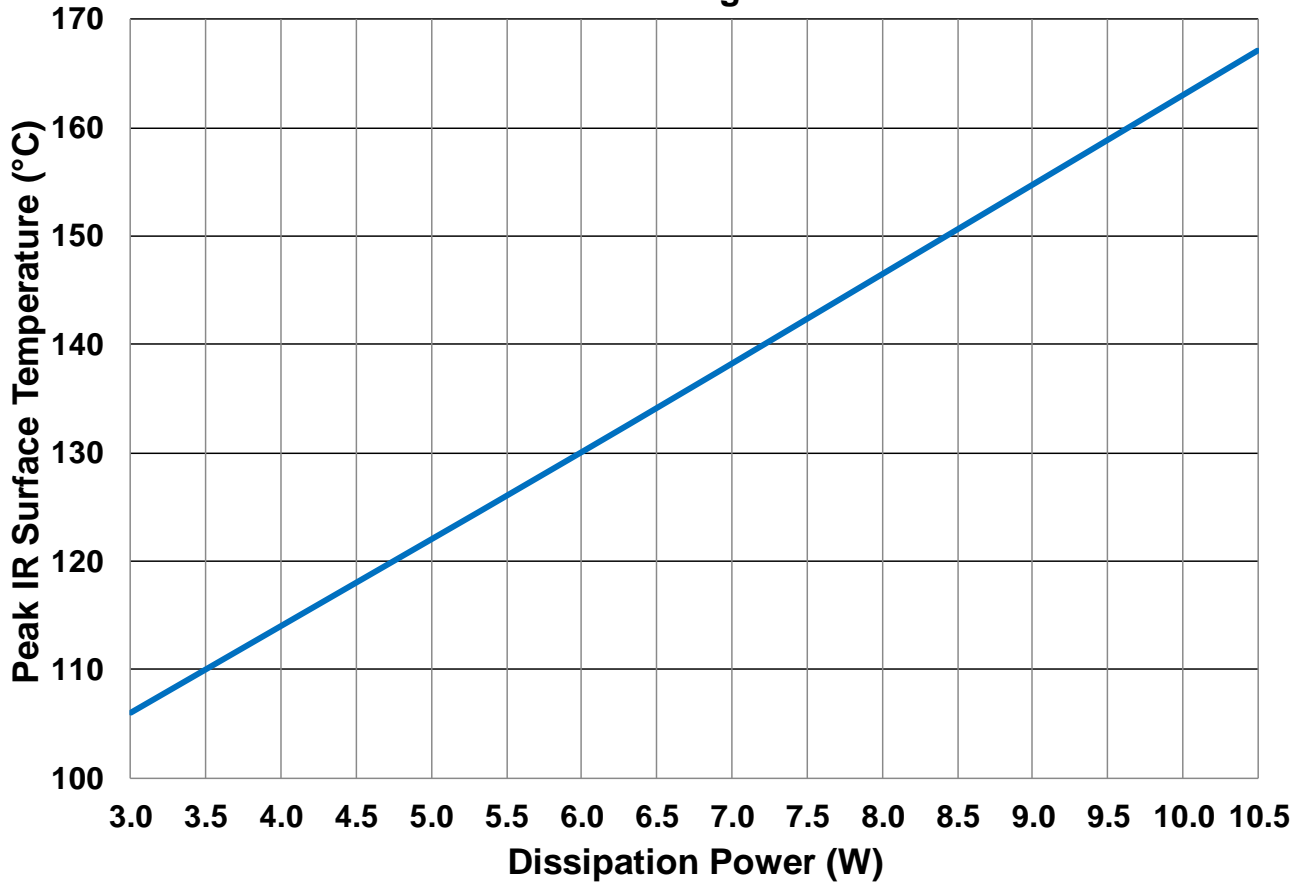


Parameter	Conditions	Values	Units
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	10.6	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	10.5 W Pdiss, CW	196	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	10.2	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	9.0 W Pdiss, CW	177	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	10.0	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	7.5 W Pdiss, CW	160	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	9.8	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	6.0 W Pdiss, CW	144	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	9.6	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	4.5 W Pdiss, CW	128	°C

¹Refer to the following document [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Thermal and Reliability Information - Pulsed

**Peak IR Surface Temperature vs. Dissipation Power
Base of DFN Package Fixed at 85 °C**

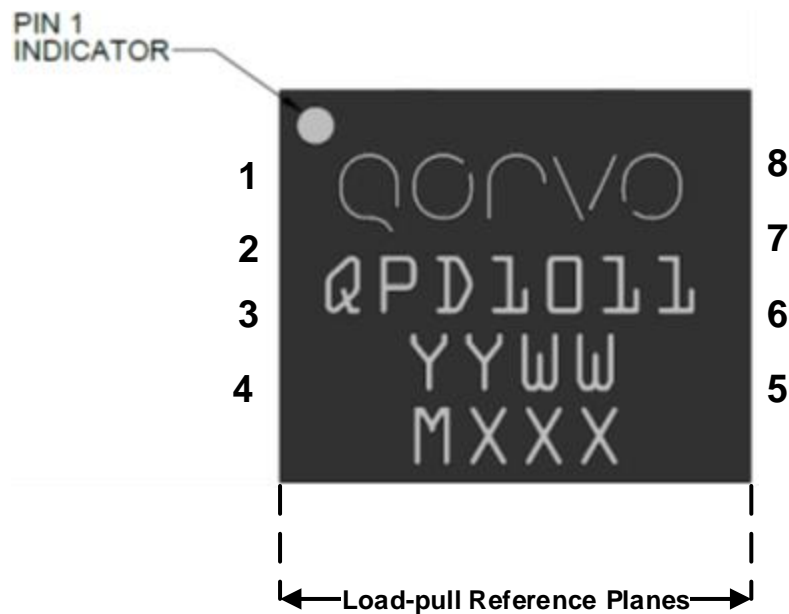


Parameter	Conditions	Values	Units
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	7.8	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	10.5 W Pdiss, 100 uS PW, 10% DC	167	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	7.7	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	8.3 W Pdiss, 100 uS PW, 10% DC	149	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	7.5	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	6.0 W Pdiss, 100 uS PW, 10% DC	130	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	7.0	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	3.0 W Pdiss, 100 uS PW, 10% DC	106	°C

¹Refer to the following document [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Pin Configuration and Description¹

Note 1: The QPD1011 will be marked with the “QPD1011” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the MXXX” is the production lot number.

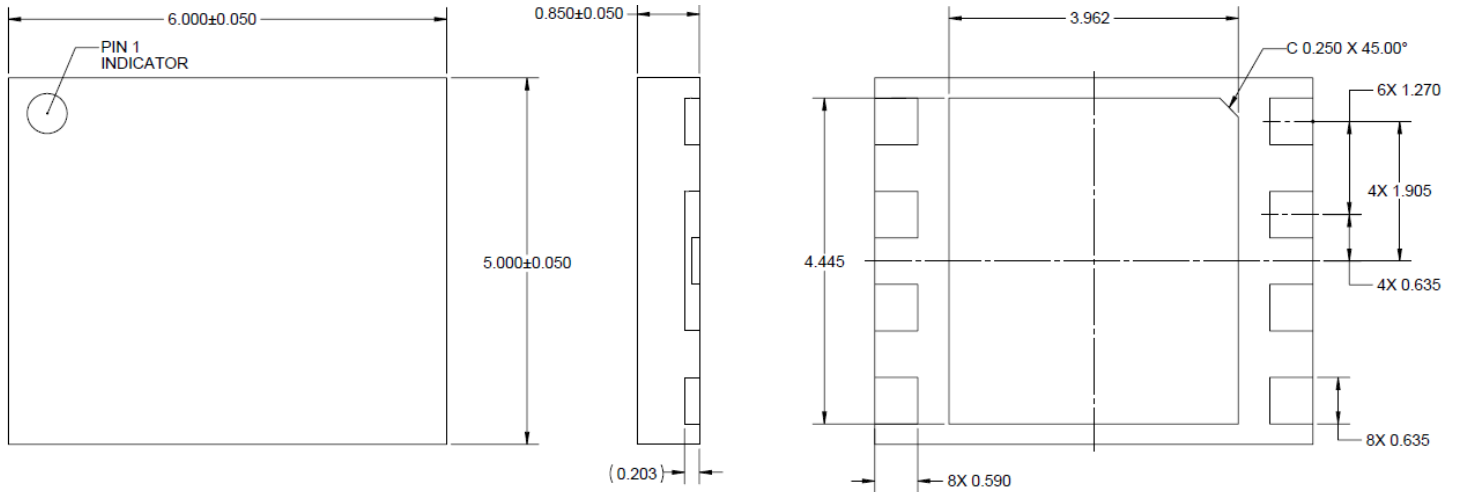


Pin	Symbol	Description
1	V_G	Gate Voltage
2, 3	RF INPUT	Gate
6, 7	RF OUTPUT / V_D	Drain
4, 5, 8	NC	No connection
9	Source	Source / Ground / Backside of part

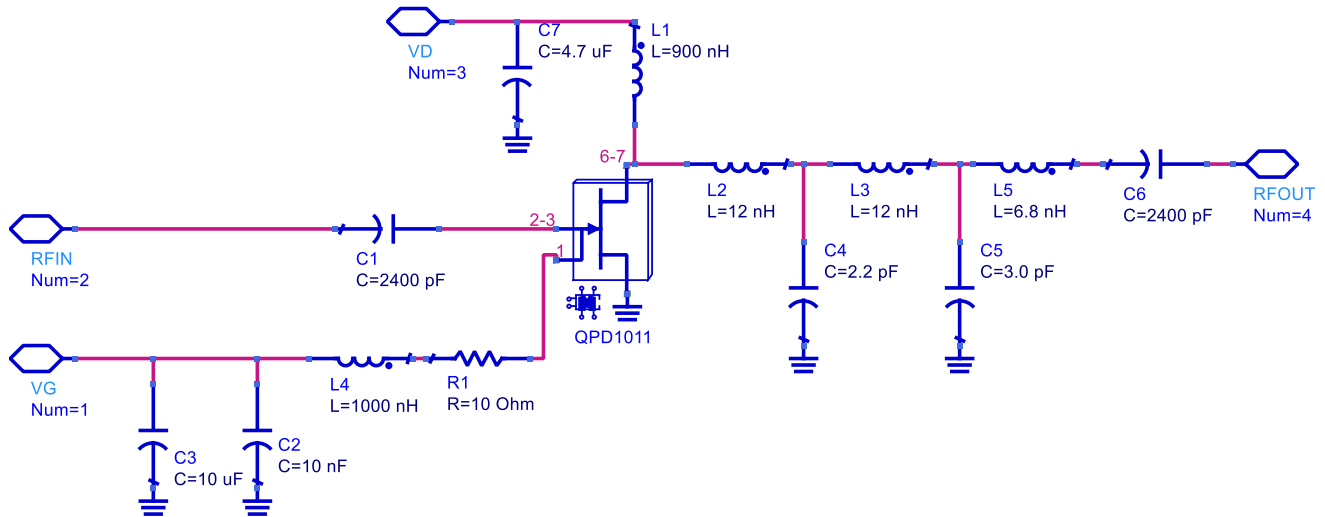
Mechanical Drawing^{1, 2, 3, 4}

Note

1. Dimensions are in mm.
2. Dimension tolerance is ± 0.1 mm, unless noted otherwise.
3. Package leads are gold plated.
4. Part is mold encapsulated.



50 – 1000 MHz Application Circuit - Schematic



Bias-up Procedure

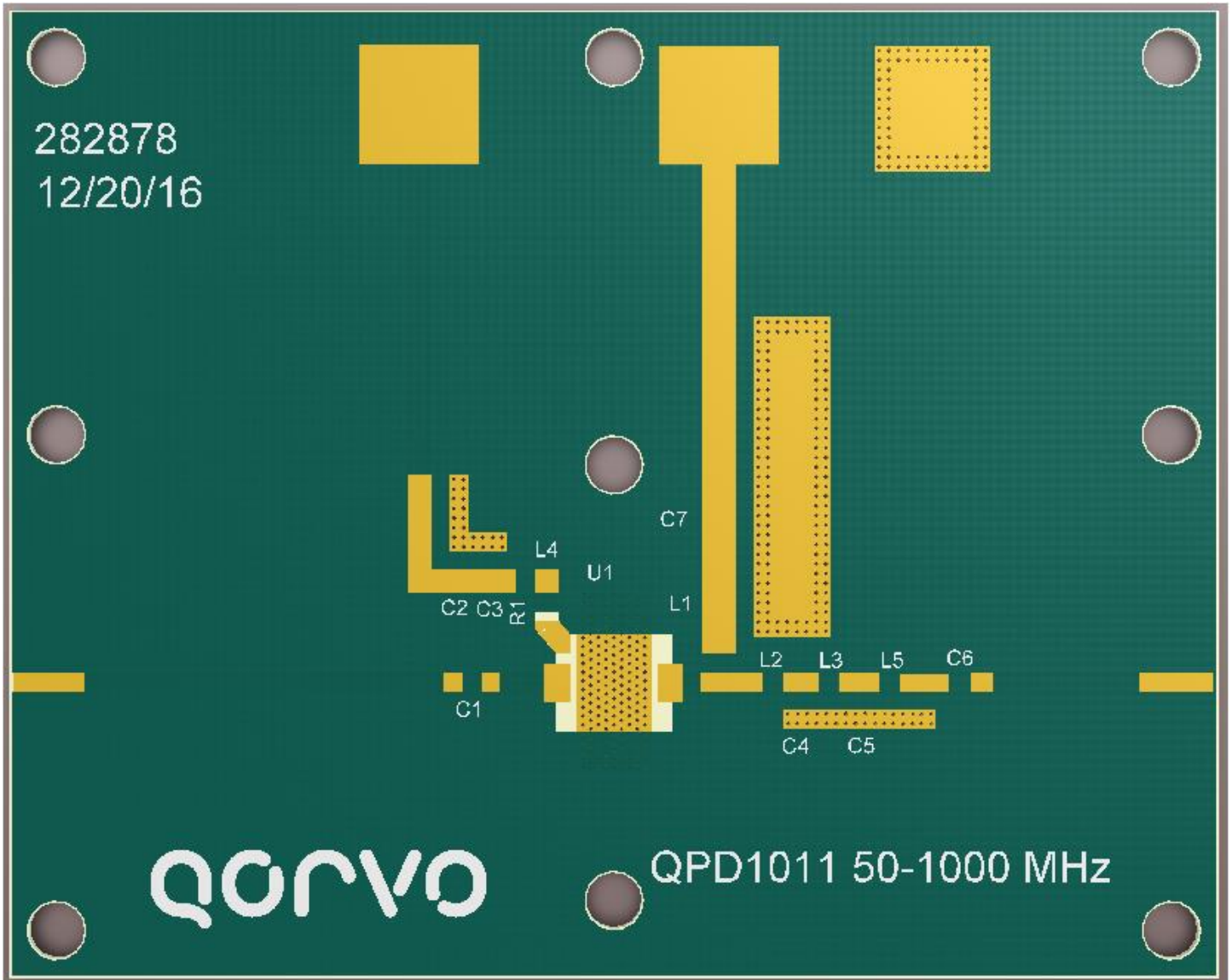
1. Set V_G to -3.5 V.
2. Set I_D current limit to 30 mA.
3. Apply 50 V V_D .
4. Slowly adjust V_G until I_D is set to 20 mA.
5. Set I_D current limit to 500 mA (CW operation)
6. Apply RF.

Bias-down Procedure

1. Turn off RF signal.
2. Turn off V_D
3. Wait 2 seconds to allow drain capacitor to discharge
4. Turn off V_G

50 – 1000 MHz Application Circuit - Layout

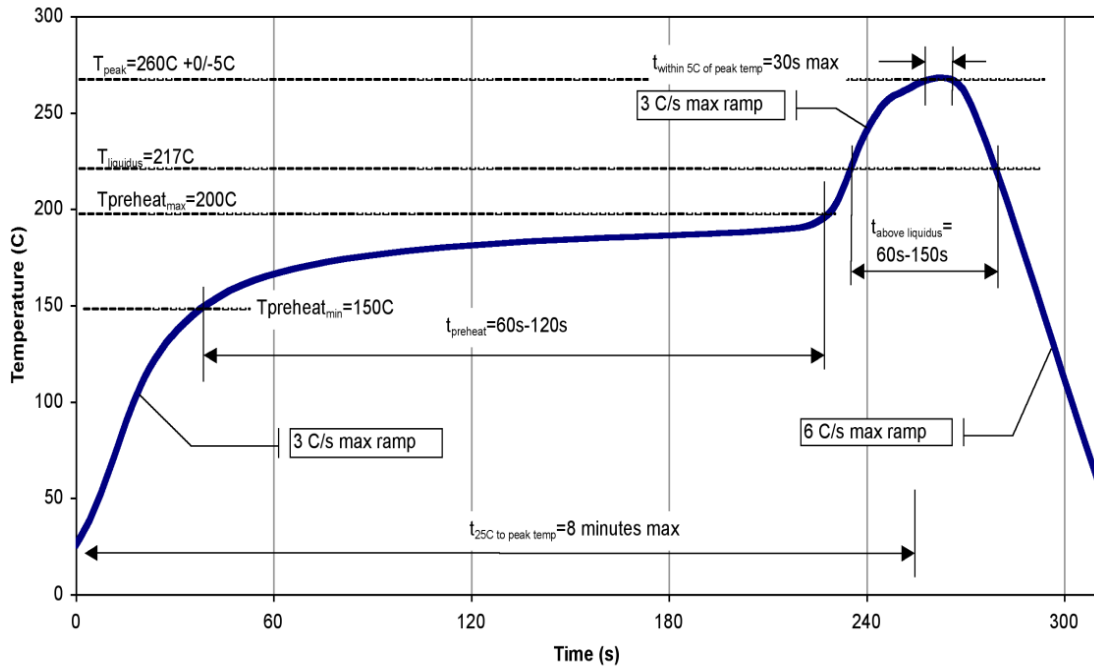
Board material is RO4350B 0.020" thickness with 2oz copper cladding. Overall EVB size is 3.98" x 3.98".



50 – 1000 MHz Application Circuit - Bill Of material

Description	Ref. Des.	Manufacturer	Part Number
CAP, SMT 0603 10nF	C2	AVX Corporation	0603YC103KAT2A
CAP, CER, SMD 10UF, 10%, 10V, 0805, X7R	C3	Murata	GRM21BR71A106KE51L
CAP MLCC 2400PF TC +/-15% 50V, 0805	C1, C6		C08BL242X-5UN-X0T
CAP CER 4.7UF 100V 10% X7R 2220	C7	Murata	GRM55ER72A475KA01L
CAP, 2.2pF, +/-0.1pF, 250V, HI-Q, 0603	C4	American Technical Ceramics	600S2R2BT250T
CAP, 3.0pF, +/-0.1pF, 250V, HI-Q, 0603	C5	American Technical Ceramics	600S3R0BT250XT
RES 10 OHM 1/10W +/-5% 0603	R1	TTI Inc.	CRCW060310R0JNEA
IND 1000nH 0603 2%	L4	Coilcraft Inc.	0603LS-102XGLC
IND 900nH 1008 5%	L1	Coilcraft Inc.	1008AF-901XJLC
IND, 6.8nH, 5%, W/W, 0603	L5	Coilcraft Inc.	0603HC-6N8XJLW
IND, 12nH, 5%, 0603, HC	L2, L3	Coilcraft Inc.	0603HC-12NXGLW

Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A, 250 V	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	750 V	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	JESD J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

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