

1 Product Overview

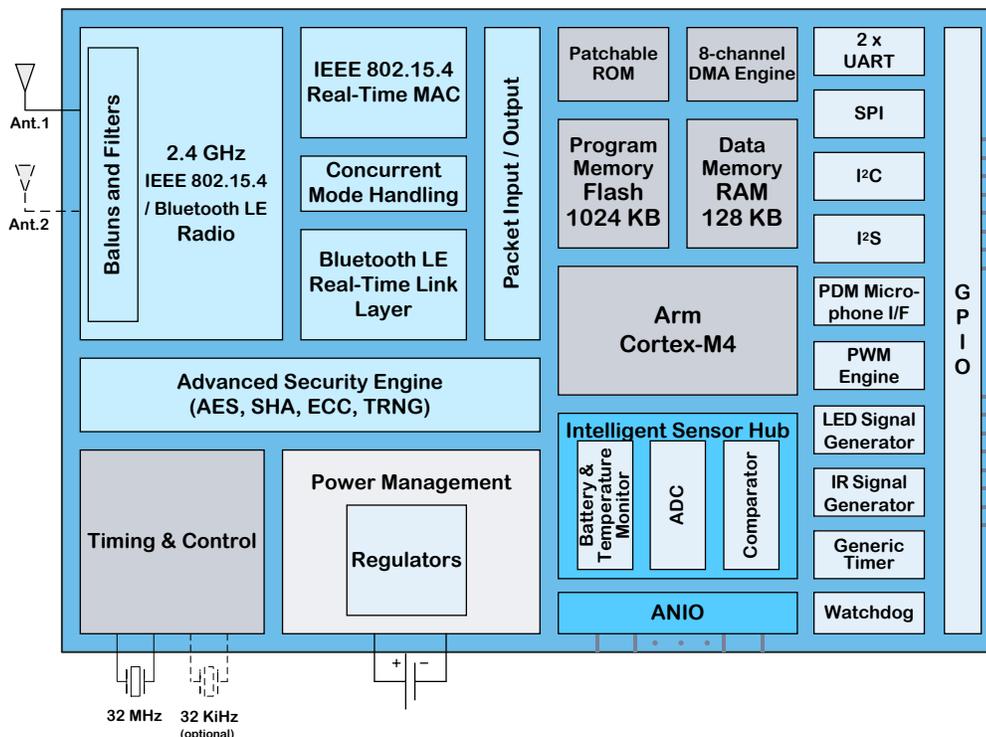
The QPG6105 is a multi-standard Smart Home communications controller supporting Zigbee, Thread, Matter™, Bluetooth® Low Energy and Bluetooth® Mesh, enabling greater interoperability and scalability.



It features ConcurrentConnect™ technology enabling multiple protocols to operate simultaneously, delivering improved capacity and enhanced interoperability with the leading low power standards.

- ConcurrentConnect **Multi-Radio** capability allows continuously scanning for incoming packets across Bluetooth Low Energy and IEEE 802.15.4 protocols with no observable blind spots.
- Patented ConcurrentConnect **Antenna Diversity** enables increased effective range.
- ConcurrentConnect **Multi-Channel** capability allows operating in up to 3 PANs on different channels.
- **Simplify Gateway** dependencies by bridging Zigbee, Thread and/or Bluetooth Mesh networks.
- **Enhanced security** capabilities enable highly secure solution with built in support for secure boot, secure OTA software upgrade and secure identity.
- **Optimized** connected lighting design **BOM**, reducing the number of components and PCBs in the design.
- Qorvo's turn-key **development kits** include complete software applications and hardware designs; enabling quick development of Connected Lighting and Smart Home products.
- Designed for low power IoT end node applications such as:
 - Connected Lighting
 - Sensors
 - Smart Plugs
 - Thermostats
 - Wearables

2 Functional Block Diagram



3 Key Features

Radio

- ✓ Operates in the worldwide 2.4 GHz ISM-band
- ✓ Integrated baluns and RF filters
- ✓ In 1 dB steps, programmable transmitter output power up to +10 dBm
- ✓ Targeting compliance with worldwide RF regulations: ETSI EN 300 328 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T-66 (Japan)

IEEE 802.15.4 compliant PHY and Real-Time MAC

- ✓ Preamble-based ConcurrentConnect Antenna Diversity
- ✓ Packet-in-Packet resynchronization
- ✓ ConcurrentConnect Multi-Channel capability, operating in up to 3 PANs on different channels

Bluetooth v 5.3 compliant Low Energy Controller

- ✓ Enhanced Data Rate (2 Mbits/s)
- ✓ Link Layer Privacy and Advertising Extensions
- ✓ Full connection utilization

Multi-Stack Support

- ✓ Multiple IEEE 802.15.4 based stacks MAC API
- ✓ Bluetooth Low Energy HCI

Dynamic Multi-Protocol

- ✓ Hardware accelerated Dynamic Multi-Protocol Bluetooth Low Energy and IEEE 802.15.4 communications
- ➔ Allows combining Bluetooth Low Energy Peripheral with any type of Zigbee/Matter-over-Thread device

ConcurrentConnect Multi-Radio capability

- ✓ Concurrent IEEE 802.15.4 and Bluetooth listening
- ➔ Allows combining Bluetooth Low Energy Central/Observer or Mesh Node with Zigbee/Matter-over-Thread router

Advanced Security Engine

- ✓ Hardware accelerated AES and CCM/CCM* encryption and decryption with 128, 192 and 256-bit keys
- ✓ Hashing engine: SHA-128, SHA-2 (SHA-256, SHA-512)
- ✓ Public Key Crypto: Elliptic Curve; support for ECDSA, ECDH, P256, Curve25519, J-Pake, ECMQV, EdDSA, etc.
- ✓ Cryptographic Random Number Generator

Built-in Security Features

- ✓ Secure boot
- ✓ Secure OTA software upgrades
- ✓ Secure identity

Integrated Microcontroller

- ✓ Arm® Cortex®-M4 processor with DSP functionality
- ✓ Up to 64 MHz clock speed

Memory

- ✓ 1 Mbyte Flash Program memory
- ✓ Patchable ROM for Flash offload
- ✓ 128 Kbyte Low Leakage Retention RAM
- ✓ 8-Channel DMA Engine

Peripherals and Interfaces

- ✓ Up to 23 Programmable GPIO lines
- ✓ Up to 4 Analog input lines
- ✓ Full internal IO pull-up / pull-down support during active and standby states
- ✓ Two UART interfaces
- ✓ SPI Master and Slave interfaces
- ✓ I²C Master and Slave interfaces
- ✓ I²S Master/Slave interface for digital audio devices
- ✓ PDM Microphone Interface
- ✓ PWM Engine (16-bit PWM) for 8 outputs
- ✓ LED Signal Generator (8-bit PWM) with fading support for 4 signaling LEDs
- ✓ IR Signal Generator
- ✓ 10/12-bit ADC to monitor the ANIO pins, the power supply level and the temperature
- ✓ Low power comparator

Power Management

- ✓ Operating voltage range: 1.8 ... 3.6V
- ✓ Integrated Regulators
- ✓ Low power standby modes:
 - Using internal LjRC oscillator: 0.9 μA
 - Using 32 MHz crystal oscillator: 765 μA
 - Using 32 KiHz crystal oscillator: 1.6 μA
- ✓ Data and state retention in all standby modes

Dimensions and Layout

- ✓ QFN32, 4x4 mm package (0.4 mm pitch)
- ✓ Supports direct interfacing with printed antennas
- ✓ No RF shielding required

Environmental Aspects

- ✓ RoHS compliant

4 Ordering Information

| Part Number | Chip Package | Flash | RAM | Packing | Unit Quantity (number of chips) | Box Dimensions |
|-------------|--------------|---------|-----------|-------------------|------------------------------------|----------------|
| QPG6105TR13 | QFN32 | 1 Mbyte | 128 Kbyte | 13" Tape and Reel | 4500 | 37 x 35 x 8 cm |
| QPG6105SR | | | | 7" Tape and Reel | 100 | |

Table of Contents

| | | |
|---------|---|----|
| 1 | Product Overview | 1 |
| 2 | Functional Block Diagram | 1 |
| 3 | Key Features | 2 |
| 4 | Ordering Information | 3 |
| 5 | Functional Description | 5 |
| 5.1 | 2.4 GHz Radio | 5 |
| 5.1.1 | RF Ports with Integrated Switch, Matching and Filters | 5 |
| 5.1.2 | Radio Configurations | 5 |
| 5.1.3 | RSSI | 5 |
| 5.1.4 | Transmit Power Control | 6 |
| 5.2 | IEEE 802.15.4 Communications | 6 |
| 5.2.1 | 2.4 GHz IEEE 802.15.4 Transceiver | 6 |
| 5.2.2 | ConcurrentConnect™ Antenna Diversity | 6 |
| 5.2.3 | Clear Channel Assessment (CCA) | 6 |
| 5.2.4 | Packet-in-Packet Resynchronization | 6 |
| 5.2.5 | Real-Time Medium Access Control (MAC) | 7 |
| 5.2.6 | Link Quality Indication | 7 |
| 5.2.7 | ConcurrentConnect™ Multi-Channel Capability | 7 |
| 5.3 | Bluetooth Communications | 7 |
| 5.3.1 | 2.4 GHz Bluetooth Low Energy PHY Layer | 7 |
| 5.3.2 | Real-Time Bluetooth Low Energy Link Layer | 7 |
| 5.3.3 | Full Connection Utilization | 8 |
| 5.4 | Multi-Stack Support | 8 |
| 5.5 | HW-Accelerated Dynamic Multi-Protocol Support | 8 |
| 5.6 | ConcurrentConnect™ Multi-Radio Capability | 8 |
| 5.7 | Advanced Security Engine | 8 |
| 5.8 | Built-in Security Features | 9 |
| 5.9 | Packet Input Output (PIO) | 9 |
| 5.10 | Memory Architecture | 9 |
| 5.11 | Internal Microcontroller | 10 |
| 5.12 | Peripherals | 10 |
| 5.12.1 | IO Pins | 10 |
| 5.12.2 | UARTs | 11 |
| 5.12.3 | SPI Master | 11 |
| 5.12.4 | SPI Slave | 11 |
| 5.12.5 | I ² C Master | 11 |
| 5.12.6 | I ² C Slave | 11 |
| 5.12.7 | I ² S Master/Slave | 12 |
| 5.12.8 | IR Signal Generator | 12 |
| 5.12.9 | LED Signal Generator | 12 |
| 5.12.10 | PDM Microphone Interface | 12 |
| 5.12.11 | PWM Engine | 12 |
| 5.12.12 | Generic Timer | 13 |

| | | |
|---------|---|----|
| 5.12.13 | Watchdog | 13 |
| 5.12.14 | Intelligent Sensor Hub | 13 |
| 5.12.15 | Clock Output | 14 |
| 5.13 | Timing and Control | 14 |
| 5.13.1 | Oscillator Settings | 15 |
| 5.13.2 | Standby Modes | 15 |
| 5.14 | Power Management | 16 |
| 5.14.1 | Low Voltage Behavior | 16 |
| 6 | Electrical Characteristics | 17 |
| 6.1 | Absolute Maximum Ratings | 18 |
| 6.2 | Recommended Operating Conditions | 18 |
| 6.3 | Current Consumption | 20 |
| 6.4 | Receiver Characteristics | 22 |
| 6.5 | Transmitter Characteristics | 24 |
| 6.6 | Digital Timing Characteristics | 26 |
| 6.7 | Reset, Wake up and Standby Timing Characteristics | 28 |
| 6.8 | Flash Memory Characteristics | 30 |
| 6.9 | Crystal Oscillator Specifications | 30 |
| 6.9.1 | The 32 MHz Crystal Oscillator | 30 |
| 6.9.2 | The 32 KiHz Crystal Oscillator (optional) | 31 |
| 6.10 | Internal Pull-up / Pull-down Characteristics | 31 |
| 6.11 | ADC Characteristics | 32 |
| 6.12 | Battery / Temperature Monitor Characteristics | 33 |
| 6.13 | Comparator Characteristics | 33 |
| 6.14 | 32 kHz LjRC Oscillator Characteristics | 33 |
| 7 | Application Circuit | 34 |
| 8 | Application Programming Information | 34 |
| 8.1 | Multi-Protocol Support | 34 |
| 9 | Flash Programming and Configuration | 35 |
| 9.1 | SPI Programming Interface | 35 |
| 9.2 | UART Programming Interface | 35 |
| 10 | Debug Mode | 36 |
| 11 | Device Information | 37 |
| 11.1 | QFN32 Package | 37 |
| 11.1.1 | QFN32 Pin Assignments | 37 |
| 11.1.2 | QFN32 Package Drawings | 42 |
| 11.1.3 | QFN32 Package Information | 44 |
| 11.1.4 | QFN32 Thermal Characteristics | 44 |
| 11.1.5 | QFN32 Tape and Reel Information | 45 |
| 11.2 | Moisture/Reflow Sensitivity | 47 |
| 11.3 | RoHS Compliance | 48 |
| 12 | Errata | 49 |
| 12.1 | Spurious External Event | 49 |
| | Abbreviations | 50 |
| | Important Notices | 51 |
| | Product Status | 51 |
| | Document History | 52 |

5 Functional Description

5.1 2.4 GHz Radio

The QPG6105 radio transceiver provides all the functionality for the Physical layer (PHY) for both the IEEE 802.15.4 and the Bluetooth communications.

This section describes the generic features; following sections describe the specific features for IEEE 802.15.4 and Bluetooth.

5.1.1 RF Ports with Integrated Switch, Matching and Filters

The QPG6105 has two antenna ports with integrated switch, matching and RF filters. The antenna ports output is 50 Ω single ended. Optionally the outputs can be combined to one 200 Ω differential output.

5.1.2 Radio Configurations

The QPG6105 supports several different radio configurations. It can be configured to use a different receive and transmit antenna, or for IEEE 802.15.4 communications it can use antenna diversity (see section 5.2.2). A few sample configurations are depicted below, but others are also possible.

Sample Configuration 1 (Figure 1):

- Single ended 50 Ω antenna
- Using antenna 1 (RF1 pin) for both RX and TX
- Antenna diversity disabled

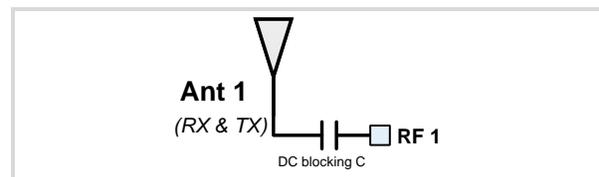


Figure 1: Single Antenna

Sample Configuration 2 (Figure 2):

- 2 Single ended 50 Ω antennas
- TX on same antenna as was selected best by RX
- Antenna diversity enabled (for IEEE 802.15.4)

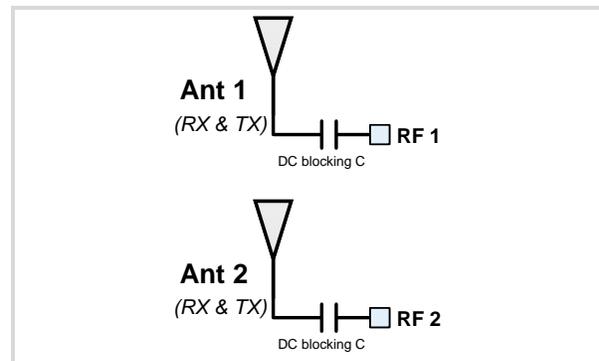


Figure 2: Two Antennas

Sample Configuration 3 (Figure 3):

- Symmetrical antenna
- Antenna diversity disabled

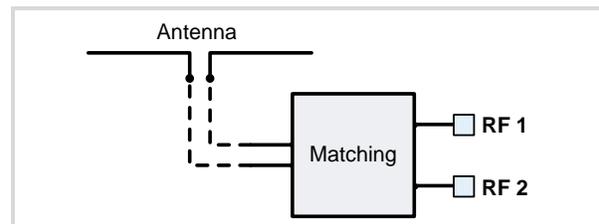


Figure 3: Symmetrical Antenna

5.1.3 RSSI

The PHY's RSSI circuitry measures the received signal energy level and this value is converted to dBm values in the Hardware Abstraction Layer (HAL). See Receiver Characteristics (6.4 below) for the range and accuracy.

5.1.4 Transmit Power Control

The QPG6105 can be configured for two transmitter output power modes:

- Low power mode; TX output power up to 7 dBm
- High power mode; TX output power up to 10 dBm

The transmitter output power is configured by software, in steps of 1 dB.

5.2 IEEE 802.15.4 Communications

5.2.1 2.4 GHz IEEE 802.15.4 Transceiver

The QPG6105 radio is compliant with the IEEE 802.15.4 standard as required for supporting Zigbee and Thread.

The QPG6105 supports all the IEEE Standard 802.15.4 defined channels in the 2.4 GHz ISM license-free frequency band (channels 11 .. 26).

The channel number (k) and center frequency (F_c) relate as follows: $F_c = 2405 + 5(k - 11)$ in MHz

5.2.2 ConcurrentConnect™ Antenna Diversity

IEEE 802.15.4 Preamble based Antenna Diversity enables the PHY to choose the optimal antenna for every individual packet, and increases the performance of the receiver in environments that are dominated by multipath fading effects and interference situations. In receive mode the PHY selects the antenna based on the best signal quality (signal-to-noise/interference ratio).

For typical indoor usage in an environment with 50 ns delay-spread and 2 MHz signal bandwidth using the Rayleigh fading model, antenna diversity with 2 antennas results in a ~8 dB improved link budget (at a 1% outage probability) compared to no antenna diversity. This translates into 70% more reliable range (using a log-distance breakpoint model¹ with path loss coefficients $g_1=2$ (free space propagation) and $g_2=3.5$ above the breakpoint at 10 m).

Unless configured otherwise, the QPG6105 will use the same antenna for transmission as the one that was used for the reception of the last packet.

¹ Refer to “T.S. Rappaport, Wireless Communications – Principles & Practice, Prentice Hall, 1996” for this model.

5.2.3 Clear Channel Assessment (CCA)

The PHY can perform a clear channel assessment (CCA) to avoid collisions. The IEEE 802.15.4 standard defines 3 CCA methods; the QPG6105 supports:

CCA mode 1, **Energy Detect (ED)** : The medium is considered busy when the measured energy in the selected channel is above a certain threshold. This CCA threshold is programmable.

CCA mode 3, **Energy Detect (ED) and Carrier Sense (CS)** : The medium is considered busy when a valid IEEE 802.15.4 carrier is detected in the selected channel and the measured energy in the selected channel is above the programmable threshold.

5.2.4 Packet-in-Packet Resynchronization

If the QPG6105 is receiving a packet from one node and is interrupted by the reception of another stronger packet from another node, the receiver will resynchronize to the latter and continue to receive and process this packet. This allows one packet (the strongest) to be received where otherwise both packets would have been lost. Packet-in-Packet collisions can occur in situations when neighbor network packets are received at a low level and in hidden node situations where not all nodes can see each other.

5.2.5 Real-Time Medium Access Control (MAC)

The QPG6105 implements all Zigbee and Thread-required MAC features of the IEEE Standard 802.15.4. The MAC provides a packet-level service to the protocol stack, and handles packet transmissions and receptions autonomously, including:

- Performing CSMA/CA to avoid collisions when transmitting packets;
- Adding CRC and Sequence number;
- Acknowledgement handling for transmitted packets, including automatic retransmissions;
- Option to spread retransmissions over different channels to natively support rf4ce multi-channel acknowledged transmission schemes
- Address recognition and packet filtering on received packets, including CRC checking;
- Acknowledgement handling for received packets, including automatic acknowledge transmission.

5.2.6 Link Quality Indication

In addition to the RSSI, there is also a link quality indication (LQI) determined for each received IEEE 802.15.4 data packet, for use at the network and application layers.

5.2.7 ConcurrentConnect™ Multi-Channel Capability

For the IEEE 802.15.4 communications, the QPG6105 can simultaneously listen for packets on three different PANs (Personal Area Networks) that may be on the same or on different RF channels.

In this way it can support the Zigbee Router role, concurrently with a Thread Router (REED) role, even if these networks run on different RF channels. Or alternatively, it can be used to serve a Zigbee coordinator for up to 3 different ZigBee networks at the same time, each network running on a potentially different RF channel.

5.3 Bluetooth Communications

The QPG6105 implements the Bluetooth Low Energy (LE) Controller functionality, including PHY, Link Layer and Host Controller Interface (HCI) according the Bluetooth Core Specification v 5.3 for Bluetooth Low Energy. When combined with a Bluetooth Low Energy protocol stack (see chapter 8), it supports all GATT-based profiles and services, and it can operate as a Broadcaster, Observer, Central and Peripheral device.

5.3.1 2.4 GHz Bluetooth Low Energy PHY Layer

The QPG6105 implements the Bluetooth LE PHY layer, supporting all the (40) Bluetooth defined frequency channels in the 2.4 GHz ISM license-free frequency band.

The Bluetooth LE Controller supports the following bit-rates:

| | |
|---------------------|-----------|
| Basic data rate: | 1 Mbit/s, |
| Enhanced data rate: | 2 Mbit/s. |

Note: The QPG6105 does not support the Long Range Coded PHY and Isochronous Channels (LE Audio).

5.3.2 Real-Time Bluetooth Low Energy Link Layer

The Real-Time Link Layer implements the real-time functions of the Bluetooth LE Link Layer (LL) protocol for the Advertising-, Scanning, Initiating and Connection States. Multi-state operation is supported: a multi-level priority mechanism ensures appropriate scheduling of Advertising, Scanning, Initiating and Connection- events.

In the Connection State, the Real-Time Link Layer maintains the LE Asynchronous Connection-oriented Logical (LE ACL) transport on master and/or slave connections, allowing transfer of control (LE-C) and user (LE-U) data. High-throughput applications are supported via a dedicated queue per (LE ACL) connection, thus ensuring efficient filling of Connection Events.

The QPG6105 supports the maximum PDU payload size of 255 bytes (including MIC), which is the maximum PDU payload size allowed by the Bluetooth Core Specification.

The QPG6105 supports the Link Layer Privacy and Advertising Extensions as defined in the Bluetooth Core Specification v 5.3.

5.3.3 Full Connection Utilization

The QPG6105 has been optimized for audio streaming over Bluetooth Low Energy with a full Bluetooth connection utilization under high CPU load conditions. This implies that the system can fill the complete connection with Bluetooth packets allowing to achieve the maximal bandwidth of the connection, even when the CPU is processing audio (decimation, equalizing, compressing), under a large variety of Bluetooth connection configurations (normal data and high data rate, short and long connection intervals, short and long Bluetooth packets).

5.4 Multi-Stack Support

The QPG6105 can support multiple protocol stacks. Multiple IEEE 802.15.4 based stacks (Zigbee, Thread, proprietary) can interface simultaneously with the QPG6105 MAC API through a MAC Dispatcher, while the Bluetooth Low Energy Stack can interface with the QPG6105 at the Host Controller Interface (HCI) level at the same time.

5.5 HW-Accelerated Dynamic Multi-Protocol Support

The QPG6105 has HW support to seamlessly interleave Bluetooth Low Energy communications (advertisements and Bluetooth connections) with IEEE 802.15.4 communications. The Dynamic Multi-Protocol Support lets the IEEE 802.15.4 MAC autonomously schedule and interleave IEEE 802.15.4 traffic to ensure that Bluetooth connection traffic is maintained without any connection drops.

For use cases where the airtime needs to be divided differently between Bluetooth and IEEE 802.15.4 data transfers, the following additional modes are supported:

- Best effort mode, for non-real-time (bulk) Bluetooth data transfers, where the Bluetooth LE controller frees up airtime in the connection when an IEEE 802.15.4 data packet is queued.
- Controlled bandwidth mode, for real-time (streaming) Bluetooth data transfers, where the Bluetooth LE controller reserves a portion of the connection for IEEE 802.15.4 communication.

This feature can be combined with Multi-Channel Support to support three IEEE 802.15.4 stacks, while simultaneously acting as a Bluetooth Low Energy peripheral and maintain a Bluetooth connection with a smartphone.

5.6 ConcurrentConnect™ Multi-Radio Capability

The QPG6105 can concurrently listen to one IEEE 802.15.4 RF channel, and one Bluetooth advertisement channel.

In this way it can combine a Zigbee Router role with Bluetooth Low Energy Central/Observer role. Another example would be the combination of a (Matter over) Thread Router role with a Bluetooth Low Energy Mesh Node.

Note: ConcurrentConnect listening mode applies to Bluetooth **advertisement** channels and hence to the 1 Mbit/s data rate. It does not apply to 2 Mbit/s data rate as that is not used for advertisement channels.

5.7 Advanced Security Engine

The QPG6105 is equipped with a low power Advanced Security Engine that can work independently from the PHY and MAC.

The Advanced Security Engine supports:

- Hardware accelerated AES and CCM/CCM* encryption and decryption with 128, 192 and 256-bit keys
Note: For Zigbee and Thread the 128-bit CCM* is used. For Bluetooth Low Energy the 128-bit CCM is used.
- Hashing: SHA-128, SHA-2 (SHA-256, SHA-512)
- Public Key Cryptography: Elliptic Curve
 - Support for ECDSA, ECDH, P256, Curve25519, J-Pake, ECMQV, EdDSA, etc.
- Cryptographic Random Number Generation, designed for compliance with NIST-800-90B

5.8 Built-in Security Features

The QPG6105 has the following built-in security features:

- Secure boot from ROM
- Secure OTA upgrade support
- Secure Debug provisions
- Secure Key Storage
 - Secure Key Load
 - Secure Symmetric Key Generation
 - Secure Public/Private Key Pair Generation
- Secure Identity support

5.9 Packet Input Output (PIO)

The Packet Input Output (PIO) controls the exchange of primitives and packets between the microcontroller and the 802.15.4 Real-Time MAC, as well as the exchange of (LE-C and LE-U) packets between the microcontroller and the Bluetooth LE Real-Time Link Layer. Information about a packet or other primitive parameters is stored in Packet Buffer Memory (PBM), a reserved region of the RAM that can hold information for up to 32 packets. The number of packets is software configurable; the application needs to make sure there are sufficient PBMs available to meet the requirements. These PBM entries are shared between the 802.15.4 MAC (RX & TX) and Bluetooth (RX & TX) functions.

5.10 Memory Architecture

The QPG6105 contains:

128 Kbyte RAM : Low Leakage Random Access Memory (RAM), for packet buffering and run-time data. This is split in:

32 Kbyte is System RAM, accessible to the internal microcontroller and other functional blocks, and 96 Kbyte is MCU RAM, accessible to the internal microcontroller only.

The contents of the RAM can be retained (or partially retained) during standby modes but is cleared when a Power-On-Reset (POR) occurs.

Table 1: RAM Retention Options

| RAM Block Size | RAM Block Type | Total RAM Retained | Retained RAM Type |
|----------------|----------------|--------------------|----------------------|
| 8 Kbyte | System RAM | 8 Kbyte | System RAM |
| 24 Kbyte | System RAM | 32 Kbyte | System RAM |
| 32 Kbyte | MCU RAM | 64 Kbyte | System RAM + MCU RAM |
| 32 Kbyte | MCU RAM | 96 Kbyte | System RAM + MCU RAM |
| 32 Kbyte | MCU RAM | 128 Kbyte | System RAM + MCU RAM |

1 Mbyte Flash : Flash memory, for program storage, calibration data and non-volatile storage of critical run-time data (e.g. pairing information and frame counters). The contents are retained under all circumstances (power-on-reset, standby).

ROM : Integrated patchable ROM (256 Kbyte) to provide off-load functionality to significantly reduce the Flash code footprint. Items included in ROM are:

- Security Primitives
- Core SW modules and functions: Scheduler; HAL; Bluetooth LE Controller; IEEE 802.15.4 MAC
- Matter-specific offload: Bluetooth LE Host; NVM SW module

DMA Engine : The QPG6105 has an 8-channel DMA Engine that relieves the microcontroller from transferring data internally between RAM and peripherals.

5.11 Internal Microcontroller

The internal microcontroller allows the QPG6105 to operate as a standalone system. It is a high performance 32-bit Arm Cortex-M4 processor with DSP functionality, optimized for low power consumption, performance, and code size.

It runs at up to 64 MHz clock speed, and can execute code from Flash as well as from RAM, with zero wait states.

Table 2: Memory Access Speeds

| Arm clock | MCU RAM access | System RAM access | ROM access | Flash Memory access |
|-----------|----------------|-------------------|------------|--|
| 32 MHz | 32 MHz | 32 MHz | 32 MHz | 32 MHz for linear code; 16 MHz worst case |
| 64 MHz | 64 MHz | 32 MHz | 32 MHz | 42 MHz for linear code; 16 MHz worst case |

5.12 Peripherals

The QPG6105 features a set of peripherals and allows configuration of the mapping between the IO signals needed by the peripherals and the available IO pins.

5.12.1 IO Pins

The QPG6105 features many IO pins that can be configured to predefined functional signals; see the Pin Assignments in chapter 11:

- 17 programmable General Purpose IO (GPIO) lines, plus
- 4 programmable Analog IO (ANIO) or GPIO lines (of which 2 input only), plus
- 2 pins for the optional 32 KHz crystal IO can alternatively be used as GPIO (input only) lines.

The whole pin configuration with associated settings is retained when going to standby.

5.12.1.1 GPIO

The QPG6105 features programmable GPIO lines that are mapped individually to functional signals, as specified in the Pin Assignments in chapter 11 (Table 30), with following settings:

Pin pull-up/down settings : Except for GPIO19 and GPIO20, the GPIO pins can be individually weakly pulled up or weakly pulled down during active as well as standby states.

Except for GPIO19, GPIO20, GPIO21 and GPIO22, the GPIO pins can be individually configured for bus-keeper.

Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

Drive strength : The drive strength of the GPIO output pins can be configured per group of 4 IO's (GPIO0 ... GPIO3, GPIO4 ... GPIO7, etc.; see also Table 30) to 4.5, 9, 13.5 or 18 mA.

Wake up : All GPIO pins can be configured as **wake-up** pin. Each of these can be configured to trigger a wake-up event on a rising edge, on a falling edge or on both edges seen on the pin.

5.12.1.2 ANIO

The QPG6105 features up to 4 ANIO lines for inputs to the ADC. ANIO0 and ANIO1 are the preferred ones as they are protected from potential interference by output signals. ANIO0 and ANIO1 can also be used for differential measurements.

5.12.2 UARTs

The QPG6105 contains two Universal Asynchronous Receiver and Transmitters (UARTs) for interfacing with additional peripheral devices and/or for terminal logging during (software) development. The UARTs support:

- Full-duplex operation.
- Baud rates from 488 Bd to 2 MBd.
- Serial frames with 5, 6, 7, 8 or 9 data bits and 1 or 2 stop bits, with framing error detection.
- Odd or even parity generation and checking.
- Buffer overflow detection.
- False start bit detection and digital low pass filter for robustness against noise.
- Separate interrupts on TX Complete, TX Data Register Empty and RX Complete.
- Configurable pin mappings; i.e. a RX pin and a TX pin can be made available on the pin-out.

5.12.3 SPI Master

The QPG6105 contains a Serial Peripheral Interface (SPI) for interfacing with additional peripheral devices. This SPI Master supports:

- Full-duplex synchronous transfers on three lines (MISO, MOSI, SCLK).
- Programmable clock polarity and phase, supports SPI mode 0, 1, 2 and 3.
- Programmable data order with MSb-first or LSb-first shifting.
- High speed clock generator supporting clock speeds up to 32 MHz.
- 4-bit to 16-bit transfer frame format selection.
- Three separate interrupts on TX Complete, TX Data Register Empty and RX Complete.

5.12.4 SPI Slave

The QPG6105 contains an SPI Slave interface. This SPI Slave supports:

- SPI mode 0
- SPI clock frequencies up to 16 MHz
- Limited to byte-based operation

5.12.5 I²C Master

The QPG6105 contains an I²C (Inter-Integrated Circuit) Master interface, also referred to as Two-Wire Interface (TWI), for interfacing with additional peripheral devices. This I²C Master supports:

- Standard mode and Fast mode
- Short (7-bit) and long (10-bit) addresses
- General call address (0x00)
- Clock stretching

5.12.6 I²C Slave

The QPG6105 contains an I²C Slave interface. This I²C Slave supports:

- Standard mode and Fast mode
- Short (7-bit) and long (10-bit) addresses
- Configurable Slave Address
- General call address (0x00)

5.12.7 I²S Master/Slave

The QPG6105 contains an I²S (Inter-IC Sound) Master/Slave interface for interfacing with digital audio devices. This I²S Master/Slave supports:

- Full duplex transfers
- Configurable word length
- Left justified. Right justified mode can be emulated
- Double buffered, DMA capable
- Master clock frequency selectable from 62.5 kHz up to 8 MHz
- External Slave clock input supporting speeds up to 4 MHz

5.12.8 IR Signal Generator

The QPG6105 has an InfraRed (IR) signal generator. The IR signal generator supports a wide range of common IR protocols.

The IR generator supports multiple modulation modes:

- Pattern based: input is a pattern of 0's and 1's in RAM.
- Time based: input is a sequence of ON and OFF times.
- Event based: modulation is controlled by scheduled actions.

5.12.9 LED Signal Generator

The QPG6105 supports up to 4 signaling LEDs, with configurable function and events. The LED signal generator supports:

- 8-bit Pulse-Width Modulation (PWM)
- Fade-in/Fade-out
- Duty cycling to adjust brightness and save power

5.12.10 PDM Microphone Interface

The QPG6105 contains a Pulse-Density Modulation (PDM) MEMS Microphone Interface, that supports:

- A Clock and Data pin for interfacing with a PDM MEMS microphone
- Optionally Capturing Data on the Rising and Falling Edge of the Clock for Stereo operations.
- Frequency of Clock signal: 2 MHz.
- HW CIC Decimation filter with programmable decimation factor (R=1...64) that converts 1-bit input samples to 16-bit output samples. HW CIC output can be connected to DMA, to allow this processing chain to be extended with further decimation, equalization, volume control and compression using the Cortex M4 DSP routines.

5.12.11 PWM Engine

The QPG6105 contains a Pulse-Width Modulation (PWM) engine, for e.g. the backlight of a display or for a speaker output, that supports:

- 16-bits real-time timer. (Note that the Event Scheduler contains a timer with a much longer time base; see section 5.13 below)
- 16-bit PWM
- Configuration of the modulation parameters
- Support for 8 PWM outputs.

5.12.12 Generic Timer

The Generic Timer supports:

- 16-bits real-time timer. (Note that the Event Scheduler contains a timer with a much longer time base; see section 5.13 below)
- The option to take a timestamp whenever a selected input pin changes state. This can typically be used for IR learning purposes.
 - Support for 4 timestamp inputs.
 - Input pin selection.
 - Hysteresis capable preprocessing.

5.12.13 Watchdog

The QPG6105 contains a Watchdog timer that serves to detect and resolve software failures and to trigger an interrupt, an internal microcontroller reset or a system reset when the timer reaches a certain timeout value. Timeout values are software configurable: 16-bit values in 16 μ s resolution.

5.12.14 Intelligent Sensor Hub

The QPG6105 supports an Intelligent Sensor Hub mode for ultra-short measurement cycles for battery operated sensors, ensuring minimal battery usage for these measurements. Upon wake up from standby mode (see also section 5.13 below) measurements and calculations can be performed running on the internal system clock to determine quickly whether the system should be fully woken up (e.g. for radio transmission, requiring the 32 MHz crystal oscillator) or can go back to standby. This whole cycle is intended to take less than 100 μ s.

Through software configuration, all analog input channels (ANIO, see section 5.12.1) can be connected to the ADC and to the Comparator. The battery and temperature monitor signals can also be connected to the ADC.

5.12.14.1 ADC

The QPG6105 has an integrated ADC module that can be used to monitor external analog signals via the ANIO pins (see section 5.12.1.2) as well as the power supply level and temperature.

- ANIO0 and ANIO1 can be used for differential measurements.
- The ADC runs on 4 MHz clock speed. A total of 16 cycles are needed to obtain a conversion result.

Table 22 in section 6.11 provides the ADC's accuracy and other characteristics.

5.12.14.2 Battery / Temperature Monitor

The ADC can be configured by software to monitor the power supply level and/or temperature internally; no external components are required. The power supply level and temperature are measured separate from the ANIO pins.

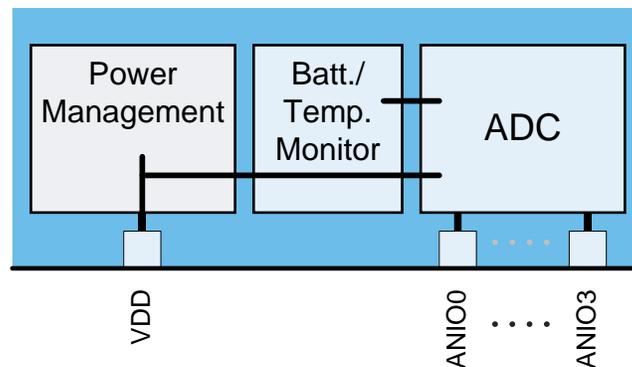


Figure 4: Battery / Temperature Monitor

5.12.14.3 Comparator

The QPG6105 features a low power comparator that can be used to trigger events to wake up the chip and/or trigger an action. The low power analog comparator can be connected to analog input(s). It supports 4 slots, allowing for time multiplexed measurements on different channels and with different threshold configurations. The comparator can be configured to combine such measurements to 'windowed' events (i.e. value is between two configurable levels).

5.12.15 Clock Output

The QPG6105 can provide a clock to peripheral devices (CLK_OUT). The clock frequency is derived from the 32 MHz crystal oscillator system clock. It can be configured for:

- 1, 2, 4, or 8 MHz clock with 50% duty cycle
- 16 MHz pulse blanked clock.

5.13 Timing and Control

The QPG6105 is designed to work in an environment where low power consumption is very important. To achieve the low power consumption in between receive and transmission cycles, the QPG6105 can be put in a standby (or sleep) state.

Following are the reasons for the QPG6105 to wake up:

- An event is detected on one of the IO lines (falling edge or rising edge).
- The voltage of an analog IO goes over or under a configurable threshold.
- It is time for a scheduled action.

The QPG6105 features a highly accurate and adaptive timing engine. The time base spans up to 30 minutes with a 1 μ s resolution and can be maintained during the standby modes. It can be used to autonomously and periodically schedule actions listed below in a just-in-time manner, improving the overall energy consumption of the system:

- Transmission of a packet from a TX queue.
- Enabling/disabling the receiver.
- Switch on/off IR modulation
- Trigger ADC measurement cycle
- Trigger analog measurements
- Interrupt and wake up the microcontroller.

5.13.1 Oscillator Settings

The QPG6105 includes the following oscillators:

32 MHz crystal oscillator, based on the required external 32 MHz crystal. This is used as main system clock and reference frequency to obtain the desired RF performance.

Internal system clock. This internal clock generator is used for fast start-up and initial processing. Its frequency is close to 32 MHz but its frequency accuracy is insufficient for RF performance. It can also be used for the Intelligent Sensor Hub, enabling minimum wake-up time to perform analog measurements.

32 kHz LjRC oscillator. This internal low jitter RC oscillator is designed to support applications needing an accurate time-base during standby, effectively removing the need for a 32 KiHz oscillator with external crystal. High accuracy is obtained through regular calibration of the LjRC oscillator using the 32 MHz crystal reference clock.

Optional **32 KiHz crystal oscillator**, based on the optional external 32 KiHz crystal. This oscillator can be used when more accurate timing during standby is needed. As a side effect of the more accurate timing, the power consumption can be improved as well for applications that implement synchronized wake up events (i.e. Bluetooth LE) as the more accurate timing results in a smaller guard band and more time spent in sleep mode.

5.13.2 Standby Modes

The QPG6105 supports the following standby modes (see section 6.3 Table 5 for the power consumption):

XT Standby mode : A low power mode that requires no reconfiguration (partial or full state retention). The time base for the Event Scheduler is delivered by the 32 MHz crystal oscillator.

RC Standby mode : A low power mode that requires no reconfiguration (partial or full state retention). The time base for the Event Scheduler is delivered by the internal 32 kHz LjRC oscillator.

32KiHz Standby mode : An optional low power mode that requires no reconfiguration (partial or full state retention). The time base for the Event Scheduler is delivered by the oscillator based on the optional 32 KiHz crystal.

In all standby modes, the QPG6105 can be programmed to also be woken up by an external event.

Note: During RC Standby and 32 KiHz Standby modes various amounts of RAM can be retained (see section 5.10). RC Standby mode and 32 KiHz Standby mode are only supported up to 85°C. Applications up to 125°C should use XT Standby mode.

5.14 Power Management

The QPG6105's integrated power management system includes a Global Low Dropout Regulator (GLDO). This generates an internal 1.8 V power supply rail that is used to supply separate local LDO regulators feeding RF/analog and digital blocks. The local LDOs used to supply RF/analog blocks are specially designed to have high power supply rejection ratio (PSRR) to suppress supply ripples.

5.14.1 Low Voltage Behavior

The QPG6105 contains following features that can be combined to implement the desired low voltage behavior:

VDD Brown-out Interrupt : Interrupt that can be software configured to trigger when VDD drops below the VDD Brown-out threshold while being active. This interrupt can be used to trigger the software to disable the radio and go into standby mode. A higher value gives the application more time for state cleanup. The VDD Brown-out threshold is software configurable: 1.80, 1.85, 1.90 or 1.95 V; default value is 1.80 V.

The VDD Brown-out detector is enabled and configured by software. In case that the Brown-out detector is not enabled, the Cut-Off detector is used to ensure reliable low voltage behavior.

VMT : Voltage Minimum Threshold (VMT), under which the chip will not wake up from standby mode.

VMT is software configurable; range = 1.6 ... 3.1 V; default value is 1.65 V.

VMT crossing detection time is software configurable; default is 125 μ s.

Power On Reset voltage level at which the chip will start up is determined by the VMT level; this is guaranteed to be ≤ 1.8 V at POR.

Cut-Off : A VDD threshold under which all functions are disabled, and current consumption is strictly limited.

The Cut-Off threshold changes with the configured Brown-out threshold as follows:

| Brown-out threshold | Cut-Off threshold |
|---------------------|-------------------|
| 1.80 V (default) | 1.65 V |
| 1.85 V | 1.69 V |
| 1.90 V | 1.72 V |
| 1.95 V | 1.76 V |

POR Circuit Timing : The Power On Reset circuit resets the chip before the VDD voltage reaches the minimal operating voltage. The chip embeds a Power On Reset circuit with internal and external triggers.

| Trigger Type | Trigger condition (Typ) | Response time (Typ) |
|-----------------------------------|--|---------------------|
| Internal (on chip VDD monitor) | $VDD \ll 1$ V | 1 ms |
| External (RESETn input) | $V_{\text{resetsn}} < \frac{1}{2} VDD$ | <10 ns |

Note: The internal reset trigger circuit samples VDD, the circuit behaves similar to a sample-based circuit at 1 kHz.

The external reset trigger uses an asynchronous (direct) input.

6 Electrical Characteristics

The QPG6105 characteristics are determined in a circuit like shown in Figure 5 below.

Note: The circuit shown is an evaluation circuit for measurement purposes and not a reference design.

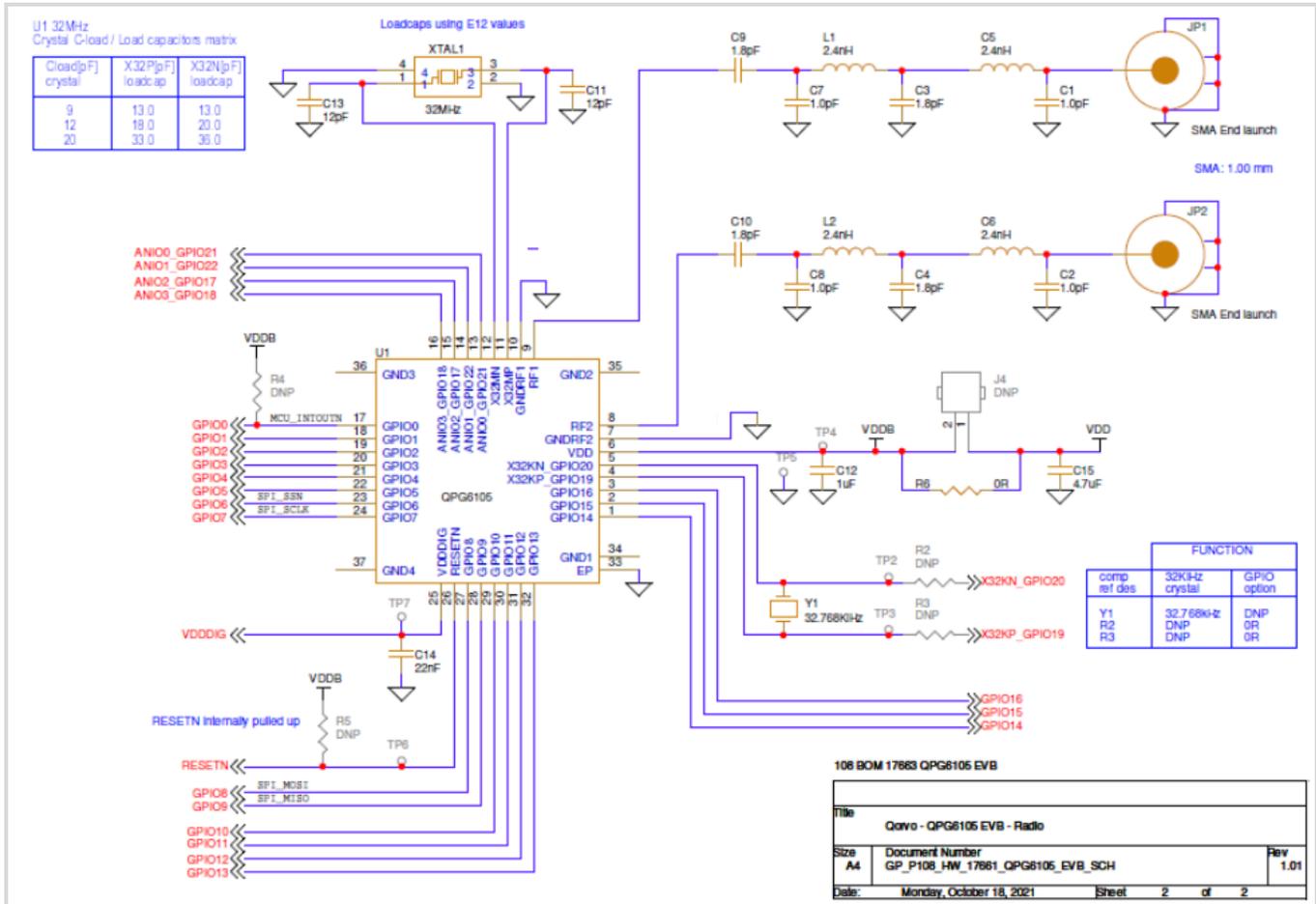


Figure 5: Parameter Evaluation Circuit

- Transmit as well as receive behavior is measured in accordance with the IEEE 802.15.4 specification and the Bluetooth Test Specification (RF-PHY.TS.5.0.1).
- All parameters are measured at VDD = 3.0 V and T_A = 25 °C, unless otherwise specified.
- IEEE 802.15.4 channel rejection is measured with the QPG6105 reference design system as interferer.

6.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|---|--|---------------------------------|------|
| VDD | Supply Input Voltage | -0.3 to +3.6 | V |
| All Digital pins, including "Analog or Digital" pins (see Table 29) | Digital IO Voltage | -0.3 to VDD+0.3 (Max = +3.6) | V |
| All Analog pins (see Table 29) | Analog IO Voltage | -0.3 to +1.32 | V |
| VDDDIG | Decoupling Voltage | -0.3 to +1.32 | V |
| RF1, RF2 | RF IO Voltage | -0.3 to +0.3 | V |
| P _{MAX} | Input RF level | +10 | dBm |
| T _J | Junction Temperature | +125 | °C |
| T _{stg} | Storage Temperature | -50 to +150 | °C |
| T _{sol} | Reflow Soldering Temperature | +260 (10 s max.) | °C |
| | ESD HBM (ANSI/ESDA/JEDEC JS-001-2017 Human Body Model) | Class 1C | |
| | RF pins: | (1000 V to < 2000 V) | |
| | non-RF pins: | (2000 V to < 4000 V) | |
| | ESD CDM (ANSI/ESDA/JEDEC JS-002-2018 Charged Device Model) | Class C2a (500 V to < 750 V) | |

6.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|---|-------------|------------|------|------|
| VDD | Power Supply Voltage | | 1.8 | 3.0 | 3.6 | V |
| T _A | Ambient Temperature | | -40 | +25 | +125 | °C |
| F _{ref} | Reference Crystal Oscillation Frequency | | | 32 | | MHz |
| V _{IL} | Input Low Voltage for all GPIO lines | Logical value (functional) | VDD = 1.8 V | | 0.6 | V |
| | | | VDD = 3.0 V | | 1.0 | |
| | | | VDD = 3.6 V | | 1.3 | |
| | | Analogue value (prevents leakage current) | | | 0.25 | V |
| V _{IH} | Input High Voltage for all GPIO lines | Logical value (functional) | VDD = 1.8 V | 1.0 | | V |
| | | | VDD = 3.0 V | 1.6 | | |
| | | | VDD = 3.6 V | 2.0 | | |
| | | Analogue value (prevents leakage current) | | VDD – 0.25 | | V |

| Symbol | Parameter | Conditions | | | Min | Typ | Max | Unit | | | | | |
|------------------|---|-----------------|--|----------------------|-------------------|----------------------|-----|------|-------|---------|----------|-----|-----|
| V _{OL} | Output Low Voltage for all GPIO lines | VDD | Drive Strength(*) | I _{OL} (**) | | | | | | | | | |
| | | | | | | | | | 1.8 V | 4.5 mA | 3 mA | 0.4 | 0.6 |
| | | | | | | | | | | 9 mA | 7 mA | 0.4 | 0.6 |
| | | | | | | | | | | 13.5 mA | 11 mA | 0.5 | 0.6 |
| | | 3.0 V | 18 mA | 15 mA | 0.5 | 0.6 | | | | | | | |
| | | | 4.5 mA | 4.5 mA | 0.25 | 0.40 | | | | | | | |
| | | | 9 mA | 9 mA | 0.25 | 0.40 | | | | | | | |
| | | 3.6 V | 13.5 mA | 13.5 mA | 0.30 | 0.45 | | | | | | | |
| | | | 18 mA | 18 mA | 0.30 | 0.45 | | | | | | | |
| | | | 4.5 mA | 4.5 mA | 0.20 | 0.35 | | | | | | | |
| | | | 9 mA | 9 mA | 0.20 | 0.35 | | | | | | | |
| | | V _{OH} | Output High Voltage for all GPIO lines | VDD | Drive Strength(*) | I _{OH} (**) | | | | | | | |
| 1.8 V | 4.5 mA | | | | | | | | | | -4.5 mA | 1.1 | 1.3 |
| | 9 mA | | | | | | | | | | -9 mA | 1.1 | 1.3 |
| | 13.5 mA | | | | | | | | | | -13.5 mA | 1.0 | 1.2 |
| 3.0 V | 18 mA | | | -18 mA | 1.0 | 1.2 | | | | | | | |
| | 4.5 mA | | | -4.5 mA | 2.45 | 2.7 | | | | | | | |
| | 9 mA | | | -9 mA | 2.45 | 2.7 | | | | | | | |
| | 13.5 mA | | | -13.5 mA | 2.35 | 2.6 | | | | | | | |
| 3.6 V | 18 mA | -18 mA | 2.35 | 2.6 | | | | | | | | | |
| | 4.5 mA | -4.5 mA | 3.1 | 3.4 | | | | | | | | | |
| | 9 mA | -9 mA | 3.1 | 3.4 | | | | | | | | | |
| | 13.5 mA | -13.5 mA | 3.0 | 3.3 | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | 18 mA | -18 mA | 3.0 | 3.3 | |
| | | | | | | | | | 18 mA | -18 mA | 3.0 | 3.3 | |
| | | | | | | | | | 18 mA | -18 mA | 3.0 | 3.3 | |
| notes: | * Refer to section 5.12.1.1 for applicability. | | | | | | | | | | | | |
| | ** I _{OL} / I _{OH} : positive value: pin is sinking current; negative value: pin is sourcing current. | | | | | | | | | | | | |
| I _{OH} | Total sourced current for all GPIO output lines combined | | | | | | 100 | mA | | | | | |
| T _{INT} | Pulse width for GPIO interrupts | | | | 250 | | | ns | | | | | |

6.3 Current Consumption

Table 5: Current Consumption - Common

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--|--|--|-----|------|-----|------|--|
| I _{idle} | Idle Modes (running CoreMark reference program.) (typical XTAL 32 MHz running) | Arm asleep | | 2.0 | | mA | |
| | | Arm running from RAM | | | | | |
| | | @ 32 MHz | | 3.6 | | | |
| | | @ 64 MHz | | 5.0 | | | |
| | | Arm running from Flash | | | | | |
| | | @ 32 MHz | | 5.5 | | | |
| | | @ 64 MHz | | 6.9 | | | |
| I _{standby} | Standby Modes | RC Standby mode; T_A ≤ 85°C(*) | | | | μA | |
| | | 8 Kbyte RAM retained (see 5.10) | | 0.9 | | | |
| | | 32 Kbyte RAM retained | | 1.3 | | | |
| | | 64 Kbyte RAM retained | | 2.3 | | | |
| | | 96 Kbyte RAM retained | | 3.1 | | | |
| | | 128 Kbyte RAM retained | | 4.0 | | | |
| | | 32 KiHz Standby mode; T_A ≤ 85°C(*) | | | | | |
| | | 8 Kbyte RAM retained (see 5.10) | | 1.6 | | | |
| | | 32 Kbyte RAM retained | | 2.0 | | | |
| | | 64 Kbyte RAM retained | | 3.0 | | | |
| 96 Kbyte RAM retained | | 3.8 | | | | | |
| 128 Kbyte RAM retained | | 4.7 | | | | | |
| | (Current consumption depends on crystal specification and load capacitance, see section 6.9 below) | XT Standby mode | | 765 | | | |
| | Current increase by activated comparator (measurement frequency dependent) | Measurement frequency = 32 kHz | | 0.23 | | | |
| I _{reset} | Reset Mode | | | 50 | | μA | |
| note: * RC Standby mode and 32 KiHz Standby mode are only supported up to 85°C. Applications up to 125°C should use XT Standby mode. | | | | | | | |

Table 6: Current Consumption - IEEE 802.15.4

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|--|-----|------|-----|------|
| I _{active} | Active Modes (Operating in IEEE 802.15.4 channel 20) | RX listening*, single antenna | | 5.6 | | mA |
| | | RX listening, single channel, with antenna diversity | | 7.4 | | |
| | | RX listening, multi-channel, with antenna diversity | | 11.5 | | |
| | | RX receiving packet | | 10.2 | | |
| | | TX @ 0 dBm | | 16.7 | | |
| | | TX @ 7 dBm, low power mode | | 26.4 | | |
| | | TX @ 10 dBm, high power mode | | 38.8 | | |

Note: * “RX listening” is defined as receive mode during preamble hunt.

Table 7: Current Consumption - Bluetooth Low Energy

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--------------|---|-----|------|-----|------|
| I _{active} | Active Modes | RX listening* 1 Mbit/s | | 10.4 | | mA |
| | | RX listening 2 Mbit/s | | 10.7 | | |
| | | RX receiving packet (1 Mbit/s or 2 Mbit/s) | | 12.4 | | |
| | | TX @ 0 dBm | | 16.7 | | |
| | | TX @ 7 dBm, low power mode | | 26.4 | | |
| | | TX @ 10 dBm, high power mode | | 38.8 | | |

Notes: * “RX listening” is defined as receive mode during preamble hunt.

Table 8: Current Consumption – ConcurrentConnect Mode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--------------|--|-----|------|-----|------|
| I _{active} | Active Modes | RX listening* concurrent IEEE 802.15.4 and Bluetooth LE | | 11.6 | | mA |

Note: * “RX listening” is defined as receive mode during preamble hunt.

6.4 Receiver Characteristics

Table 9: Receiver Characteristics - Common

| Parameter | Conditions | Min | Typ | Max | Unit | |
|--|---------------|-------------------|-----|------|------|-----|
| RSSI range (assuming the HAL is used, see sections 5.1.3 and 8.1) | 5 dB accuracy | AGC activated | | -101 | -33 | dBm |
| | | AGC not activated | | -101 | -50 | |
| | Resolution | | | 1 | | dB |
| LO leakage | 2.4 GHz | | | | -47 | dBm |
| | 4.8 GHz | | | | -47 | |

Table 10: Receiver Characteristics - IEEE 802.15.4

| Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------------|---|------------------------|------|------|--------|
| RF channels | Programmable in 5 MHz steps as defined by IEEE 802.15.4 | 2405 | | 2480 | MHz |
| Bit rate | | | 250 | | kbit/s |
| Receiver sensitivity | as defined in IEEE 802.15.4 (Measured in IEEE 802.15.4 channel 20) | | | | dBm |
| | Single channel listening | | -101 | | |
| | Multi-channel listening (signal at both antenna ports) | | -100 | | |
| | IEEE 802.15.4 / Bluetooth LE concurrent listening Sensitivity for 2480 MHz may be up to 3 dB worse. For 2415 and 2465 MHz sensitivity may be up to 1 dB worse. | | -98 | | |
| | Antenna Diversity Gain (refer to section 5.2.2 for the channel model) | | 8 | | dB |
| RX carrier frequency offset range | Sensitivity loss < 2 dB | -200 | | +215 | kHz |
| Maximum receive level | 1% PER as defined in IEEE 802.15.4 | +10 | | | dBm |
| IIP3 | RX mode, AGC enabled | | +1 | | dBm |
| P-1dB RF front-end | RX mode, AGC enabled | | -11 | | dBm |
| Co-Channel rejection | Packet in Packet collision | | -10 | | dB |
| | Non-IEEE 802.15.4 Interference (noise) | single antenna | | -3 | dB |
| | | with antenna diversity | | -1 | |
| Adjacent channel rejection | as defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 5 MHz | | 35 | | dB |
| Alternate adjacent channel rejection | as defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 10 MHz | | 47 | | dB |
| Far away channel rejection | wanted signal at -82 dBm. IEEE 802.15.4 interferer, +/- 15 MHz | | 52 | | dB |
| Wi-Fi IEEE 802.11ax rejection | wanted signal at -82 dBm. Wi-Fi centered at +12 MHz / -13 MHz or higher offset frequency | | 37 | | dB |

| Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|-----|-----|-----|------|
| Bluetooth rejection (fixed carrier, rejection of FSK modulated signal with frequency deviation +/- 160 kHz, BT=0.5) | wanted signal at -82 dBm, Bluetooth carrier at: +/-4 MHz | | 36 | | dB |
| | +/-6 MHz | | 51 | | |
| Blocking / desensitization (e.g. mobile phone signal rejection) | (Measured according to ETSI EN 300 440-1 V1.6.1; 2010-08). | | | | dBm |
| | -100 MHz from lower band edge | | -10 | | |
| | -40 MHz from lower band edge | | -12 | | |
| | -20 MHz from lower band edge | | -12 | | |
| | +20 MHz from upper band edge | | -12 | | |
| | +40 MHz from upper band edge | | -11 | | |
| | +100 MHz from upper band edge | | -9 | | |

Table 11: Receiver Characteristics - Bluetooth Low Energy

| Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|--|------|-------|------|--------|
| RF channels | Channel spacing in 2 MHz steps | 2402 | | 2480 | MHz |
| Frequency error tolerance | | -250 | | 250 | kHz |
| Bit rates | (LE 1M) | | 1 | | Mbit/s |
| | (LE 2M) | | 2 | | Mbit/s |
| Data rate error tolerance | | -500 | | +500 | ppm |
| Receiver sensitivity | * (RF-PHY/RCV-LE/CA/BV-01-C); BER = 10 ⁻³ (Measured in Bluetooth channel 0 = 2402 MHz) | | | | dBm |
| | At 2 Mbit/s | | -94.5 | | |
| | At 1 Mbit/s | | -97 | | |
| | Sensitivity at these frequencies may be up to 3 dB worse; 2416 + n*16 (n= 0..4) [in MHz] | | | | |
| Receiver saturation | * (RF-PHY/RCV-LE/CA/BV-06-C); BER = 10 ⁻³ | | >+10 | | dBm |
| Co-Channel rejection | Wanted signal at -67 dBm, modulated interferer in channel, BER = 10 ⁻³ | | -6.5 | | dB |
| Selectivity | * (RF-PHY/RCV-LE/CA/BV-03-C); BER = 10 ⁻³ , modulated interferer at: | | | | dB |
| | -5 MHz or more | | 43 | | |
| | -4 MHz | | 40 | | |
| | -3 MHz | | 36 | | |
| | -2 MHz | | 28 | | |
| | -1 MHz | | 8 | | |
| | +1 MHz | | 5 | | |
| | +2 MHz | | 27 | | |
| | +3 MHz = image frequency -1 MHz | | 36 | | |
| | +4 MHz = image frequency | | 27 | | |
| | +5 MHz or more = image frequency +1 MHz | | 39 | | |

| Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---|-----|-----|-----|------|
| Out-of-band blocking | * (TP/RCV-LE/CA/BV-04-C); 30 ... 2000 MHz | | 3 | | dBm |
| | 2003 ... 2399 MHz | | -5 | | |
| | 2484 ... 2997 MHz | | -3 | | |
| | 3000 MHz ... 12.75 GHz | | 3 | | |
| Intermodulation | * (RF-PHY/RCV-LE/CA/BV-04-C); Wanted signal at 2402 MHz, at -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level. | | -29 | | dBm |

Note: * As defined in Bluetooth Test Specification RF-PHY.TS.5.0.1, and for 1 Mbit/s bit rate.

6.5 Transmitter Characteristics

Table 12: Transmitter Characteristics - Common

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|-----|---------|-------|------|
| Maximum TX output power | High power mode | | 10 | | dBm |
| | Low power mode | | 7 | | |
| Minimum TX output power | Active TX | | -27 | | dBm |
| TX output power variation | Over temperature range | | +/- 1 | | dB |
| | Part to part variation (+/-3 σ) | | +/- 1.5 | | |
| Note: Device does not require any TX power calibration. | | | | | |
| TX Harmonics | Measured at 10 dBm output power in 1 MHz bandwidth | | | | dBm |
| | FCC regulations, radiated, average power | | | -41.2 | |
| | ETSI regulations, radiated | | | -30 | |
| | China regulations, conducted | | | -30 | |
| TX out of band emissions | Measured at 10 dBm output power, modulated signal, on all IEEE 802.15.4 and Bluetooth channels. (1 MHz resolution bandwidth, average power) | | | | dBm |
| | < 2390 MHz | | | -42 | |
| | > 2483.5 MHz | | | -42 | |

Table 13: Transmitter Characteristics - IEEE 802.15.4

| Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--|------|-----|------|---------|
| RF channels | Programmable in 5 MHz steps as defined by IEEE 802.15.4 | 2405 | | 2480 | MHz |
| Bit rate | | | 250 | | kbit/s |
| Chip rate | | | 2.0 | | Mchip/s |
| EVM | | | 14 | 22 | % |

Table 14: Transmitter Characteristics - Bluetooth Low Energy

| Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|------|------|------|--------|
| RF channels | Channel spacing in 2 MHz steps | 2402 | | 2480 | MHz |
| Bit rates (LE 1M) | | | 1 | | Mbit/s |
| (LE 2M) | | | 2 | | Mbit/s |
| In-band emissions | * (RF-PHY/TRM-LE/CA/BV-03-C) +/-2 MHz | | -46 | | dBm |
| | +/(3+n) MHz (n=0,1,2...) | | -54 | | |
| Frequency deviation | * (RF-PHY/TRM-LE/CA/BV-06-C) | | | | |
| | Δf_{avg} 1 Mbit/s | | 254 | | kHz |
| | $\Delta f_{2avg} / \Delta f_{avg}$ | | 0.94 | | |
| | Δf_{avg} 2 Mbit/s | | 500 | | kHz |
| | $\Delta f_{2avg} / \Delta f_{avg}$ | | 0.98 | | |

Note: * As defined in Bluetooth Test Specification RF-PHY.TS.5.0.1, and for 1 Mbit/s bit rate unless specified otherwise.

6.6 Digital Timing Characteristics

Table 15: SPI Slave Timing Characteristics

| Symbol | Parameter | Reference (Figure 6) | Min | Typ | Max | Unit |
|-------------------|--|----------------------|-------|-----|-------|------|
| F _{SCLK} | SCLK frequency | t1 | 0 | | 16 | MHz |
| | SCLK duty cycle clock | | | 50 | | % |
| | MOSI setup time | t2 | 10 | | | ns |
| | MOSI hold time | t3 | 10 | | | ns |
| | SCLK low to MISO valid time | t4 | | | 16 | ns |
| | SSn setup time | t5 | 31.25 | | | ns |
| | SSn high to MISO tri-state | t6 | | | 31.25 | ns |
| | Required time between accesses (from SSn gone high to SSn going low next) | t7 | 200 | | | ns |

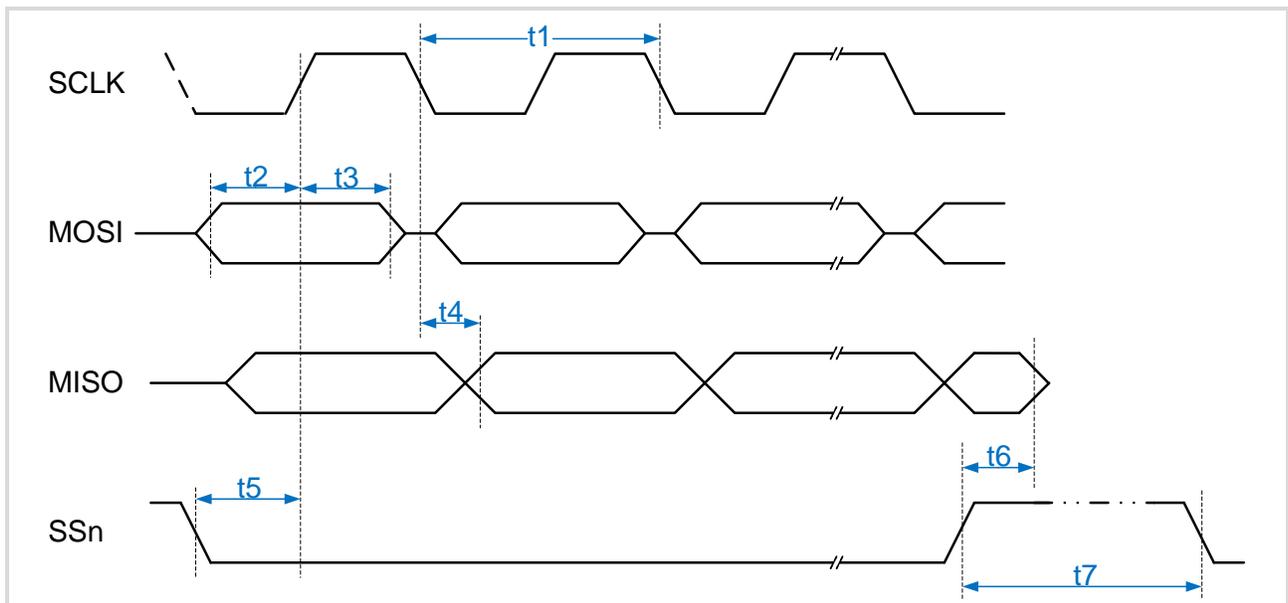


Figure 6: SPI Slave Signaling Timing Diagram

Table 16: I²C Timing Characteristics

| Symbol | Parameter | Reference (Figure 7) | Standard Mode | | Fast Mode | | Unit |
|---------------------|--|-------------------------|---------------|-----|-----------|-----|------|
| | | | Min | Max | Min | Max | |
| F _{SCL} | SCL frequency | t1 | | 100 | | 400 | kHz |
| t _{HIGH} | Clock High Time | t2 | 4 | | 0.6 | | μs |
| t _{LOW} | Clock Low Time | t3 | 4.7 | | 1.3 | | μs |
| t _{SU;STA} | START condition setup time | t4 | 4 | | 0.6 | | μs |
| t _{HD;STA} | START condition hold time | t5 | 4.7 | | 0.6 | | μs |
| t _{HD;DAT} | Data hold time | t6 | 0 | | 0 | | μs |
| t _{SU;DAT} | Data setup time | t7 | 0.25 | | 0.1 | | μs |
| t _{SU;STO} | STOP condition setup time | t8 | 4 | | 0.6 | | μs |
| t _{BUF} | Bus free time between a STOP and a START condition | t9 | 4.7 | | 1.3 | | μs |

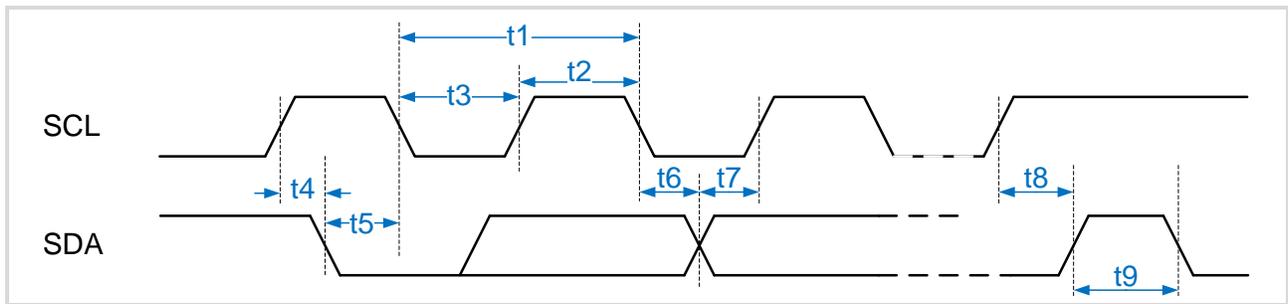


Figure 7: I²C Signaling Timing Diagram

6.7 Reset, Wake up and Standby Timing Characteristics

Table 17: Reset, Wake up and Standby Timings

| Application use cases | Remarks | Min | Typ | Max | Unit |
|--|--|-----|-----|-----|------|
| Power on detect | See Figure 8 below. | | 0.5 | 20 | ms |
| From Power on detect, until Program starts running (*) (**) | See Figure 8 below. | | 520 | | µs |
| External Reset, until Program starts running (*) (**) | See Figure 9 below. | | 520 | | µs |
| RESETN pulse width | See Figure 9 below. The RESETN is asynchronous. A practical minimum is 10 ns. | | | | |
| Go to RC Standby mode, from application command (*) | 8 Kbyte RAM retained | | 120 | | µs |
| Go to XT Standby mode, from application command | | | | 1 | µs |
| Go to 32KiHz Standby mode, from application command | Value is dominated by the startup time of the 32 KiHz crystal oscillator (see section 6.9.2). Typically, this can go up to 500 ms. | | 150 | | ms |
| Wake up from RC or 32KiHz Standby mode, until Program starts running (*) (**) | 8 Kbyte RAM retained; other RAM not re-initialized. | | 180 | | µs |
| Wake up from XT Standby mode, until Program starts running (*) | | | | 1 | µs |
| Note * : The Program is responsible for backup/restore of operational data as required by the application. The time required for this is not included in the values specified above. | backup: | | 40 | | µs |
| | restore: | | 40 | | |
| Note ** : To enable RF reception or transmission, the 32 MHz crystal oscillator has to be started: | | | | | |
| Prepare for RX/TX, when 32 MHz crystal oscillator is not yet running | See Figure 8 and Figure 9 below. Value is dominated by the startup time of the 32 MHz crystal oscillator (see section 6.9.1) | | 2 | | ms |

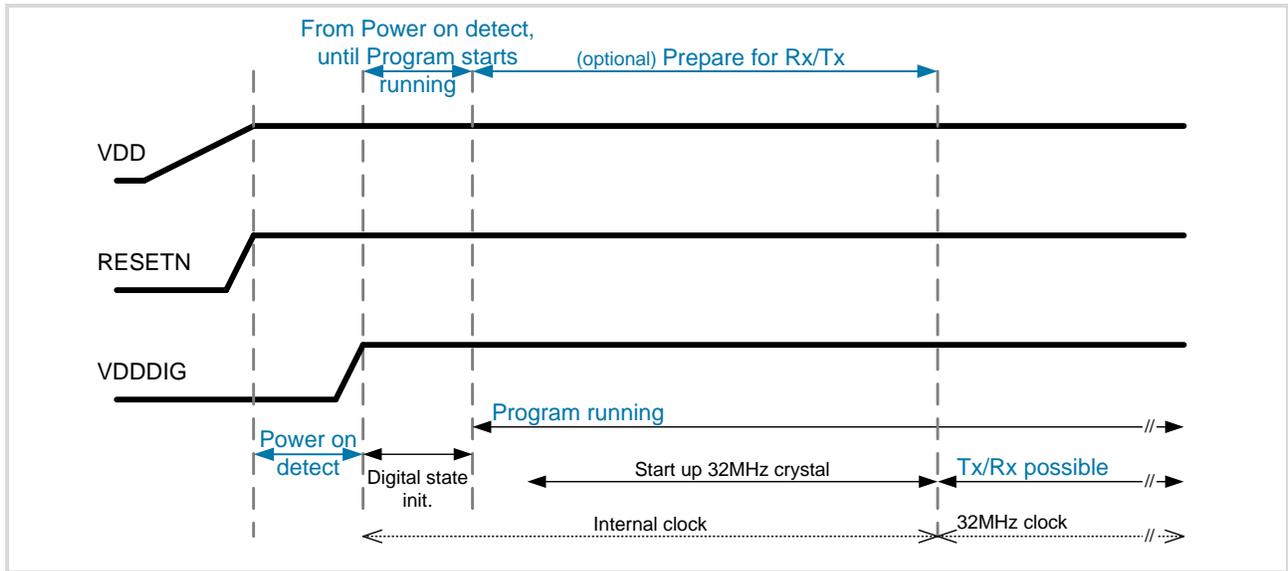


Figure 8: Power On Timing (not to scale)

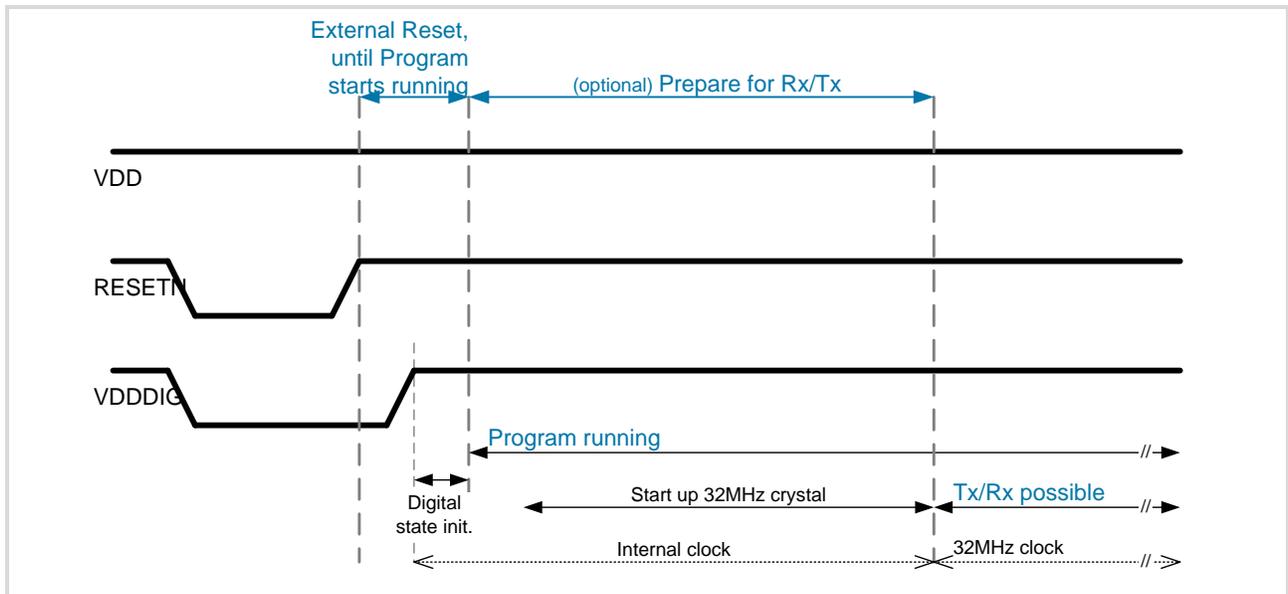


Figure 9: External Reset Timing (not to scale)

6.8 Flash Memory Characteristics

Table 18: Flash Memory Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------|--|------|------|-----|------|
| | Retention period | As specified in the QPG6105 Qualification Report | 10 | | | year |
| | Number of ERASE cycles | | 100k | | | |
| | VDD for programming | Zero source resistance | 1.8 | | 3.6 | V |
| | Sector size | | | 1024 | | byte |
| T _{WR} | Write time (512 bytes) | Physical operations, so excluding software overhead and transmission times | | | 2 | ms |
| T _{PE} | Sector Erase time | | | 3.5 | | |
| T _{BE} | Bulk Erase time | | | 8.5 | | |
| I _{WR} | Write current | | | 6.6 | | |
| I _{PE} | Sector Erase current | Average delta current | | 2.3 | | mA |
| I _{BE} | Bulk Erase current | | | 2.3 | | |

6.9 Crystal Oscillator Specifications

6.9.1 The 32 MHz Crystal Oscillator

The 32 MHz crystal oscillator is an AGC controlled oscillator that provides a high gain at start-up, to assure fast start-up times, and low gain when running, to minimize current consumption. It generates the system clock for the QPG6105 and can also be used as time base generation.

Some QPG6105 characteristics are crystal dependent. For reliable operation and to meet the specified standby current and startup time the crystal should comply with the Qorvo Procurement Specifications for the crystal. These Specifications are available from Qorvo upon request; see Table 19 below. Note that these Procurement Specifications specify limited operating temperature range; for crystals with extended operating temperature range, please contact Qorvo support. Qorvo can also provide service to evaluate other crystals.

Table 19: 32 MHz Crystal Specifications

| Package | Size | Type | Procurement Specification |
|------------------|--------------|----------------|---------------------------|
| Thru-Hole or SMD | Metal can | HC-49S 2 leads | GP_P007_PS_06541 |
| SMD | 3.2 x 2.5 mm | 4 pads SMD | GP_P007_PS_06542 |
| SMD | 2.5 x 2.0 mm | 4 pads SMD | GP_P007_PS_06544 |
| SMD | 2.0 x 1.6 mm | 4 pads SMD | GP_P007_PS_06543 |

Figure 10 shows the typical configuration of the oscillator. The values of the external load capacitors (Cx, Cy) are crystal type dependent.

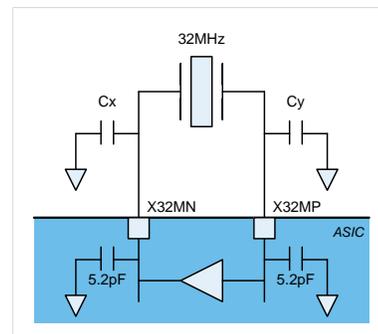


Figure 10: Typical 32 MHz Crystal Configuration

6.9.2 The 32 KiHz Crystal Oscillator (optional)

The 32.768 kHz (in short: 32 KiHz) crystal oscillator is optional and can be used for ultra-low power time base generation for the Event Scheduler with high accuracy. A side effect of this low power consumption is that the start-up time of the 32 KiHz oscillator is very dependent on the crystal and the capacitive load on the X32K oscillator pins. Within the operational temperature range, the 32 KiHz oscillator will always start within one second (At 25°C the start-up time is less than 0.5 s). The application must make sure that the QPG6105 does not enter the 32 KiHz standby mode before the 32 KiHz oscillator is stable.

For reliable operation and to meet the specified characteristics the crystal should comply with the Qorvo Procurement Specifications; see Table 20 below. These Specifications are available from Qorvo upon request. Qorvo can also provide service to evaluate other crystals.

Figure 11 shows the application circuit of this oscillator.

Table 20: 32 KiHz Crystal Specifications

| Procurement Specification |
|--|
| GP_P008_PS_13494 (Version 2.00 or higher) |

Note: The crystal load capacitors are integrated in the chip.

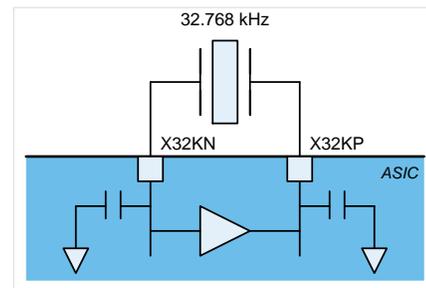


Figure 11: Typical 32 KiHz Crystal Configuration

6.10 Internal Pull-up / Pull-down Characteristics

Table 21: Internal Pull-up / Pull-down Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-------------------------------|---|-----|-----|-----|------|
| | Internal pull-up resistance | VDD=3.3V, T _A =25°C, Input is grounded. | | 41 | | kΩ |
| | | VDD=1.8V, T _A =25°C, Input is grounded. | | 95 | | |
| | Internal pull-down resistance | VDD=3.3V, T _A =25°C, Input is VDD level. | | 42 | | |
| | | VDD=1.8V, T _A =25°C, Input is VDD level. | | 110 | | |

6.11 ADC Characteristics

Table 22: ADC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---|-------------|------|-----|------|
| | Resolution | Sample rate up to 250 000 sample/s | | 10 | | bits |
| | | Integration factor 16, sample rate up to 15 625 sample/s | | 12 | | bits |
| V _{IN} | Measurement range | At the ANIO pin | 0 | | 3.6 | V |
| Note 1: When the ANIO pin driver is not low-ohmic, or high accuracy is needed, it is highly recommended to use the on-chip buffer(s), which limits the input range from 0 to VDD - 1V. Note 2: The ADC contains a scaler, which allows several measurement ranges. | | | | | | |
| | Channel switching time | (The ADC uses 16 clock cycles for a conversion) | | 4 | | μs |
| | Conversion time | | | 4 | | μs |
| | Reference variation (over temperature range) | Single ended | -40...85°C | 12 | | LSb |
| | | | -40...125°C | 24 | | |
| | | Differential | -40...85°C | 6 | | |
| | | | -40...125°C | 12 | | |
| INL | Integral Nonlinearity | Single ended, Scaler gain=1x, V _{in} > 100 mV | | 2 | | LSb |
| | | Differential measurement, 4% V _{ref} < V _{in_diff} < 96% V _{ref} | | 1 | | |
| DNL | Differential Nonlinearity | Differential measurement | | > -1 | | LSb |

6.12 Battery / Temperature Monitor Characteristics

Table 23: Battery / Temperature Monitor Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|---|---|-----|-----|------|------|
| | Battery level range | | 1.8 | | 3.6 | V |
| | Resolution of battery level measurement | At 3.6 V | | 10 | | mV |
| | Accuracy of battery level measurement | Typ at 3.6 V. Max over process, voltage and temperature. | | 25 | 60 | mV |
| | temperature measurement range | | -40 | | +125 | °C |
| | Resolution of temperature measurement | | | 1.4 | | °C |
| | Accuracy of temperature measurement | | | | | |

6.13 Comparator Characteristics

Table 24: Comparator Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|---|--------------------------------|-----|--------|-----|------|
| | Resolution | | | VDD/64 | | V |
| | Threshold level error | | | | 1 | LSb |
| | Increase of current consumption in Standby Mode | Measurement frequency = 32 kHz | | 0.23 | | µA |

6.14 32 kHz LjRC Oscillator Characteristics

Table 25: 32 kHz LjRC Oscillator Characteristics

| Symbol | Parameter | Remarks | Min | Typ | Max | Unit |
|-----------------|-------------------------|---|-----|----------|-----|-------|
| 32kRC-tolerance | Frequency stability | 1σ value, TA=25°C, calibration performed at least every 2.5 s for an averaging period >1 ms | | +/-100 | | ppm |
| 32kRC-Tc | Temperature coefficient | | | < +/-100 | | ppm/K |

7 Application Circuit

Qorvo provides reference designs for typical applications, suitable for systems targeting compliance with EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan). Please contact Qorvo Support.

8 Application Programming Information

Arm Programming Information:

Available from Arm:

- Generic User Guide, Cortex™-M4 Devices (document DUI 0553A), http://infocenter.arm.com/help/topic/com.arm.doc.dui0553a/DUI0553A_cortex_m4_dgug.pdf.

Available from Qorvo:

- Software Development Kit, including amongst others:
 - QPG6105 User Manual, describing the various peripherals and interfaces.
 - API Manuals for the various Qorvo-provided software layers.
 - Programming Guides for selected functions and features.
 - Sample applications.

Development System:

A development system for the development of QPG6105 software is available from Qorvo upon request.

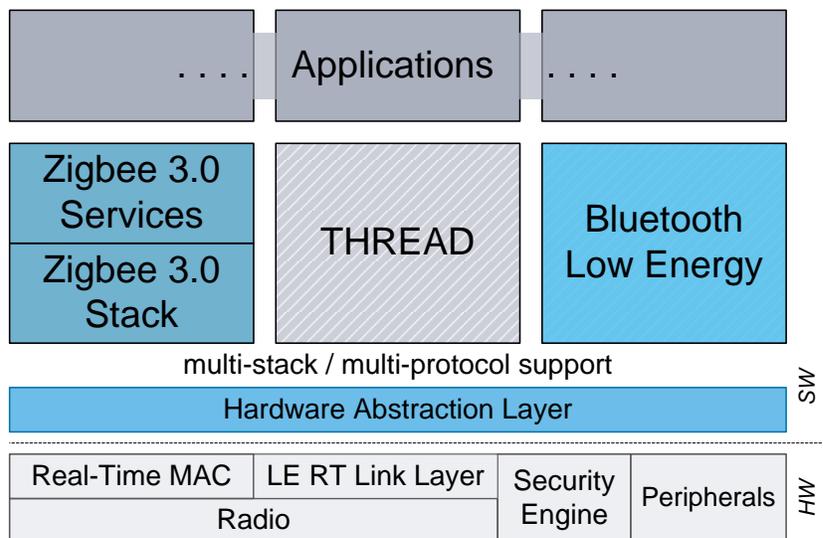
8.1 Multi-Protocol Support

The QPG6105 can run the full stack and applications for

- Zigbee 3.0
 - including Green Power,
- Thread
 - the OpenThread implementation
- Bluetooth Low Energy devices.

Integrated multi-stack, multi-protocol support enables different protocol stacks to operate concurrently, and on different channels.

The Hardware Abstraction Layer (HAL) provides an easy-to-use interface abstracting all features of the chip.



9 Flash Programming and Configuration

The Flash program and configuration memory is not programmed when the chips are shipped by Qorvo. To enable the functionality, the Flash must be programmed through a dedicated programming protocol. Please contact Qorvo Support for details of available programming solutions. If programming takes place on the target PCB, the Program Port signals need to be accessible on the PCB.

9.1 SPI Programming Interface

The primary programming interface for (production) programming of the Flash memory is the SPI Slave interface (section 5.12.4). For this the signals shown in Table 26 shall be made available for the Program Port.

Table 26: Mapping Signals to Program Port (SPI)

| QPG6105 | Program Port | Notes |
|---------|----------------------|--|
| EP | GND | Ground |
| VDD | VCC_DUT | The recommended supply voltage is: 3.3 V |
| RESETN | RESETn | The reset signal |
| GPIO6 | PROG_SS _n | Slave select signal |
| GPIO7 | PROG_SCLK | Clock provided by the Programmer |
| GPIO8 | PROG_MOSI | Data from Programmer to device |
| GPIO9 | PROG_MISO | Data from device to Programmer |
| GPIO5 | PROG_EN _n | Low (stable) enables programming mode at startup/reset. Should be kept low at least until the first SPI access in programming mode. The time between Reset and the first SPI access must be at least 50 ms. If no command has been received within 4 s, the chip will enter normal application mode. |

Following characteristics apply to the SPI programming interface:

- maximum SCLK frequency: **4 MHz**
- minimum SS_n high time: **2 μs**
- minimum last SCLK to SS_n high time: **2 μs**

9.2 UART Programming Interface

The Flash memory can also be programmed via the UART interface (section 5.12.2). For this the signals shown in Table 27 shall be made available for the Program Port.

Table 27: Mapping Signals to Program Port (UART)

| QPG6105 | Program Port | Notes |
|---------|----------------------|--|
| EP | GND | Ground |
| VDD | VCC_DUT | The recommended supply voltage is: 3.3 V |
| RESETN | RESETn | The reset signal |
| GPIO10 | UART_TX | Data from device to Programmer |
| GPIO11 | UART_RX | Data from Programmer to device |
| GPIO5 | PROG_EN _n | Low (stable) enables programming mode at startup/reset. Should be kept low at least until the first UART access in programming mode. The time between Reset and the first UART access must be at least 50 ms. If no command has been received within 4 s, the chip will enter normal application mode. |

Following characteristics apply to the UART programming interface:

- Default baud rate: **57600 Bd** (the baud rate can be changed via the programming protocol after initial setup)

- 1 start bit, 8 data bits, 1 stop bit, no parity

10 Debug Mode

During startup/reset the QPG6105 can be triggered to come up in debug mode. The SWD/JTAG signals shown in Table 28 will then be available.

Table 28: Debug Mode Signals

| QPG6105 | SWD/JTAG | Notes |
|---------|-------------|---|
| GPIO6 | SWIO/TMS_b | |
| GPIO7 | SWCLK/TCK_b | |
| GPIO8 | TDI_b | |
| GPIO9 | SWV/TDO_b | |
| GPIO5 | PROG_ENn | Low for about 1 s after Reset, then high, enables debug mode. |

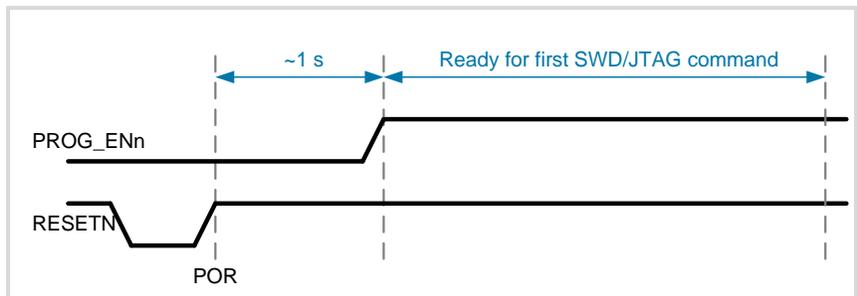


Figure 12: Entering Debug Mode

While PROG_ENn is asserted low, no transaction should be started on SPI or UART (otherwise programming mode will be entered; see chapter 9).

The QPG6105 will be ready for the first SWD/JTAG command for a period of 32 s. If then no command has been received, the chip will enter normal application mode.

11 Device Information

11.1 QFN32 Package

11.1.1 QFN32 Pin Assignments

Figure 13 below shows the pin connections top view, and Table 29 lists the pin assignments. Table 30 provides GPIO assignment options for various functions. For the software configuration options of the GPIO pins, please refer to section 5.12.1. Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

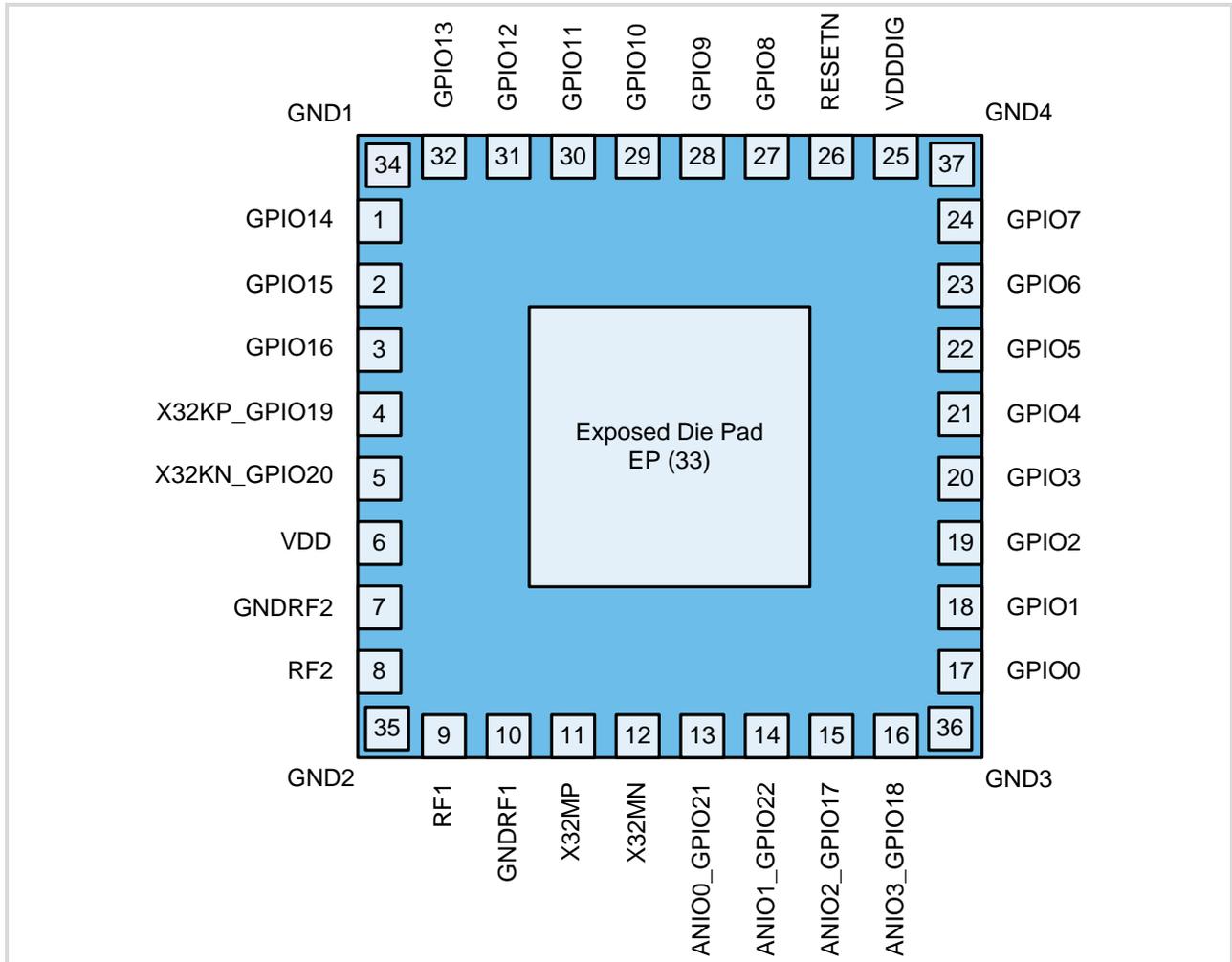


Figure 13: Pin Connections (QFN32) – Top View

Table 29: Pin Assignments (QFN32)

| Pin # | Name | Type | Description | Notes |
|-------|--------------|-------------------|--|---|
| 1 | GPIO14 | Digital | Configurable GPIO | |
| 2 | GPIO15 | Digital | Configurable GPIO | |
| 3 | GPIO16 | Digital | Configurable GPIO | |
| 4 | X32KP_GPIO19 | Analog or Digital | Optional 32 KiHz crystal output, or Configurable GPIO (input only) | Both pins should either be used for the 32 KiHz reference crystal (analog mode) or defined as GPIO (digital mode – input only). If a pin is not used, it must be connected to the exposed die pad (GND) or software should disable the input buffer, to prevent leakage current. If defined as GPIO, apply external pull up or pull down to avoid floating input. (See also section 5.12.1.1) |
| 5 | X32KN_GPIO20 | Analog or Digital | Optional 32 KiHz crystal input, or Configurable GPIO (input only) | |
| 6 | VDD | Power | Power supply input | |
| 7 | GNDRF2 | RF | RF ground return path RF2 | Must be connected to the exposed die pad (GND). |
| 8 | RF2 | RF | RF port for antenna 2 | In all cases the RF pins should be isolated from ground or VDD. A DC path between RF1 and RF2 is only permitted when used in differential mode. |
| 9 | RF1 | RF | RF port for antenna 1 | |
| 10 | GNDRF1 | RF | RF ground return path RF1 | Must be connected to the exposed die pad (GND). |
| 11 | X32MP | Analog | 32 MHz reference crystal input | The QPG6105 does not support an external clock. |
| 12 | X32MN | Analog | 32 MHz reference crystal output | |
| 13 | ANIO0_GPIO21 | Analog or Digital | Preferred ADC input, or Configurable GPIO (input only). | ANIO pins that are not used, are recommended to be connected to the exposed die pad (GND). |
| 14 | ANIO1_GPIO22 | Analog or Digital | Preferred ADC input, or Configurable GPIO (input only) | |
| 15 | ANIO2_GPIO17 | Analog or Digital | Optional ADC input, or Configurable GPIO | |
| 16 | ANIO3_GPIO18 | Analog or Digital | Optional ADC input, or Configurable GPIO | |
| 17 | GPIO0 | Digital | Configurable GPIO | |
| 18 | GPIO1 | Digital | Configurable GPIO | |
| 19 | GPIO2 | Digital | Configurable GPIO | |
| 20 | GPIO3 | Digital | Configurable GPIO | |
| 21 | GPIO4 | Digital | Configurable GPIO | |
| 22 | GPIO5 | Digital | Configurable GPIO | This pin shall be available for optional Flash programming, see chapter 9. At start-up/reset, the QPG6105 bootloader enables a temporary weak internal pull-up to prevent the QPG6105 entering programming mode in normal operation. |

| Pin # | Name | Type | Description | Notes |
|--------------|--------|---------|--|---|
| 23 | GPIO6 | Digital | Configurable GPIO | These pins shall be available for optional Flash programming via SPI, see chapter 9. |
| 24 | GPIO7 | Digital | Configurable GPIO | |
| 25 | VDDDIG | Power | Power supply output for decoupling | Decoupling to ground. This pin requires a 22 nF decoupling capacitor to ground. |
| 26 | RESETN | Digital | Active-low reset circuit | Internally pulled up, so no external pull up is required. This pin shall be available for optional Flash programming, see chapter 9. |
| 27 | GPIO8 | Digital | Configurable GPIO | These pins shall be available for optional Flash programming via SPI, see chapter 9. |
| 28 | GPIO9 | Digital | Configurable GPIO | |
| 29 | GPIO10 | Digital | Configurable GPIO | These pins shall be available for optional Flash programming via UART, see chapter 9. |
| 30 | GPIO11 | Digital | Configurable GPIO | |
| 31 | GPIO12 | Digital | Configurable GPIO | |
| 32 | GPIO13 | Digital | Configurable GPIO | |
| Die pad (33) | EP | Ground | Exposed die pad; analog chip ground | RF ground (GND) |
| (34) | GND1 | Ground | Additional ground connections, internally connected to the die pad via the lead frame. | Available for easier ground routing, e.g. on single layer designs. |
| (35) | GND2 | Ground | | |
| (36) | GND3 | Ground | | |
| (37) | GND4 | Ground | | |

For the software configuration options of the GPIO pins, please refer to section 5.12.1. Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

Table 30: GPIO Assignment Options (QFN32)

| # | Pin Name | Wake Up | Drive Strength group | SPI Master | SPI Slave | I ² C Master | I ² C Slave | I ² S Master / Slave ¹ | UART 0 | UART 1 | IR | PWM | Time-stamp | PDM (Voice) | LED | SWD / JTAG ² | Clock Output | |
|----|----------|---------|----------------------|---------------------------|--------------|-------------------------|------------------------|--|----------|--------|-----|--------------|--------------|-------------|-------------|-------------------------|------------------|---------|
| | | | | | | | | | | | | | | | | | | |
| 17 | GPIO0 | WKUP | 0..3 | MISO ³ | SSn | SDA ⁴ | SDA ⁴ | SDI | RX | TX | OUT | PWM0 PWM6 | Tstmp0 | DATA CLK | LED0 | SWIO/TMS | | |
| 18 | GPIO1 | WKUP | | SSn MISO ³ | MISO SCLK | SCL ⁴ | SCL ⁴ | WS WS_IN | TX | RX | | | PWM1 PWM7 | Tstmp1 | CLK DATA | LED1 | SWV/TDO | |
| 19 | GPIO2 | WKUP | | SCLK | MOSI SSn | SDA ⁴ | SDA ⁴ | SCK SCK_IN | RX | TX | OUT | | PWM2 PWM5 | Tstmp2 | DATA CLK | LED2 | TDI | |
| 20 | GPIO3 | WKUP | | MOSI | SCLK MISO | SCL ⁴ | SCL ⁴ | SDO | TX | RX | | | PWM3 PWM4 | Tstmp3 | CLK DATA | LED3 | SWCLK/TCK | |
| 21 | GPIO4 | WKUP | 4..7 | MISO ³ | SSn MOSI | | | SDI | RX | | | PWM0 | Tstmp0 | | LED0 | SWIO/TMS | | |
| 22 | GPIO5 | WKUP | | SSn | MISO | | | WS WS_IN | TX | | | | PWM1 | Tstmp1 | | LED1 | SWV/TDO | |
| 23 | GPIO6 | WKUP | | MOSI MISO ³ | SSn | | | SDO | RX | TX | | | PWM4 PWM6 | | | LED0 | SWIO/TMS | |
| 24 | GPIO7 | WKUP | | | SCLK | SCL ⁴ | SCL ⁴ | | TX | RX | | | PWM5 PWM7 | | | LED1 | SWCLK/TCK | |
| 27 | GPIO8 | WKUP | 8..11 | | MOSI | SDA ⁴ | SDA ⁴ | | RX | TX | | PWM4 PWM6 | | | LED2 | TDI | | |
| 28 | GPIO9 | WKUP | | | MISO | | | | TX | RX | | | PWM5 PWM7 | | | LED3 | SWV/TDO | |
| 29 | GPIO10 | WKUP | | SCLK | SSn | | | WS WS_IN | RX TX | TX | OUT | | PWM0 | Tstmp0 | DATA | LED0 | SWIO/TMS | CLK_OUT |
| 30 | GPIO11 | WKUP | | MOSI | SCLK | | | SCK SCK_IN | TX RX | RX | | | PWM1 | Tstmp1 | CLK | LED1 | SWCLK/TCK | |

¹ I²S Master uses SDO, SDI, SCK, WS and optionally REF_CLK. I²S Slave uses SDO, SDI, SCK_IN, WS_IN and optionally REF_CLK. WS_IN and SCK_IN may require external pull down to prevent floating input signals, depending on the behavior of the master device (e.g. during sleep state).

² Options printed in bold are the ones used by the Debug Mode (see chapter 10).

³ SPI MISO signal may require external pull down to prevent floating input signal, depending on the behavior of the slave device (e.g. during sleep state, or when not selected).

⁴ I²C bus signals (SCL, SDA) require external pull up.

| Pin | | Wake Up | Drive Strength group | SPI Master | SPI Slave | I ² C Master | I ² C Slave | I ² S Master / Slave ¹ | UART 0 | UART 1 | IR | PWM | Time-stamp | PDM (Voice) | LED | SWD / JTAG ² | Clock Output |
|-----|--------|---------|----------------------|---------------------------|--------------|-------------------------|------------------------|--|--------------|----------|-----|--------------|------------|-------------|------|-------------------------|--------------|
| # | Name | | | MISO ³ SCLK | MOSI SSn | | | SDO | RX TX | TX RX | | PWM2 PWM7 | Tstmp2 | DATA | LED2 | TDI | |
| 31 | GPIO12 | WKUP | 12..15 | MISO ³ SCLK | MOSI SSn | | | SDO | RX TX | TX RX | OUT | PWM2 PWM7 | Tstmp2 | DATA | LED2 | TDI | |
| 32 | GPIO13 | WKUP | | SSn MOSI | MISO SCLK | SDA ⁴ | SDA ⁴ | WS SDI WS_IN | TX RX | RX TX | OUT | PWM3 PWM6 | Tstmp3 | CLK | LED3 | SWV/TDO | |
| 1 | GPIO14 | WKUP | | SCLK | MOSI | SCL ⁴ | SCL ⁴ | SCK SCK_IN | RX | TX | | PWM0 PWM4 | Tstmp0 | DATA CLK | LED0 | TDI | |
| 2 | GPIO15 | WKUP | | MOSI MISO ³ | MISO | SDA ⁴ | SDA ⁴ | SDO | TX | RX | | PWM1 PWM5 | Tstmp1 | CLK DATA | LED1 | SWV/TDO | |
| 3 | GPIO16 | WKUP | 16..19 | MISO ³ SSn | SSn | SCL ⁴ | SCL ⁴ | WS SDI WS_IN | RX | TX | OUT | PWM2 PWM6 | Tstmp2 | DATA CLK | LED2 | SWIO/TMS | |
| 15 | GPIO17 | WKUP | | SCLK | SSn | SDA ⁴ | SDA ⁴ | SCK SCK_IN | RX TX | RX | | PWM4 | Tstmp2 | CLK DATA | LED2 | SWIO/TMS | |
| 16 | GPIO18 | WKUP | | MOSI | MISO | SCL ⁴ | SCL ⁴ | SDO | TX RX | TX | OUT | PWM5 | Tstmp3 | DATA CLK | LED3 | SWV/TDO | |
| 4 | GPIO19 | WKUP | input only | | | | | | | RX | | | Tstmp2 | DATA | | | |
| 5 | GPIO20 | WKUP | | | | | | | | | | | Tstmp3 | | | | |
| 13 | GPIO21 | WKUP | | | MOSI | | | | SCK_IN | RX | | | | Tstmp0 | | | |
| 14 | GPIO22 | WKUP | | MISO ³ | SCLK | | | | SDI WS_IN | RX | | | | Tstmp1 | DATA | | |

11.1.2 QFN32 Package Drawings

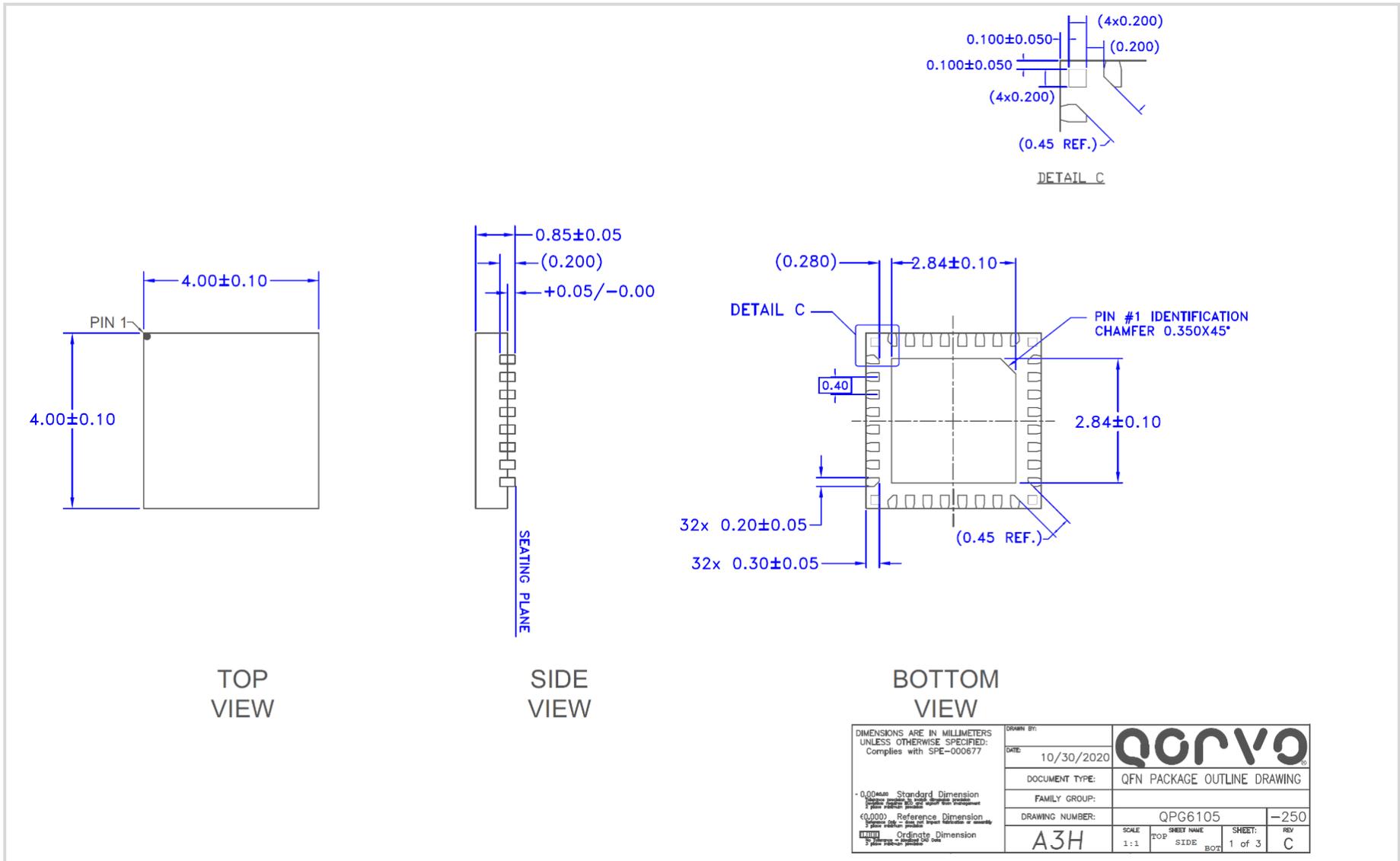


Figure 14: QFN32 Package Drawings and Dimensions (Refer to Product Change Notification # 22-0072)

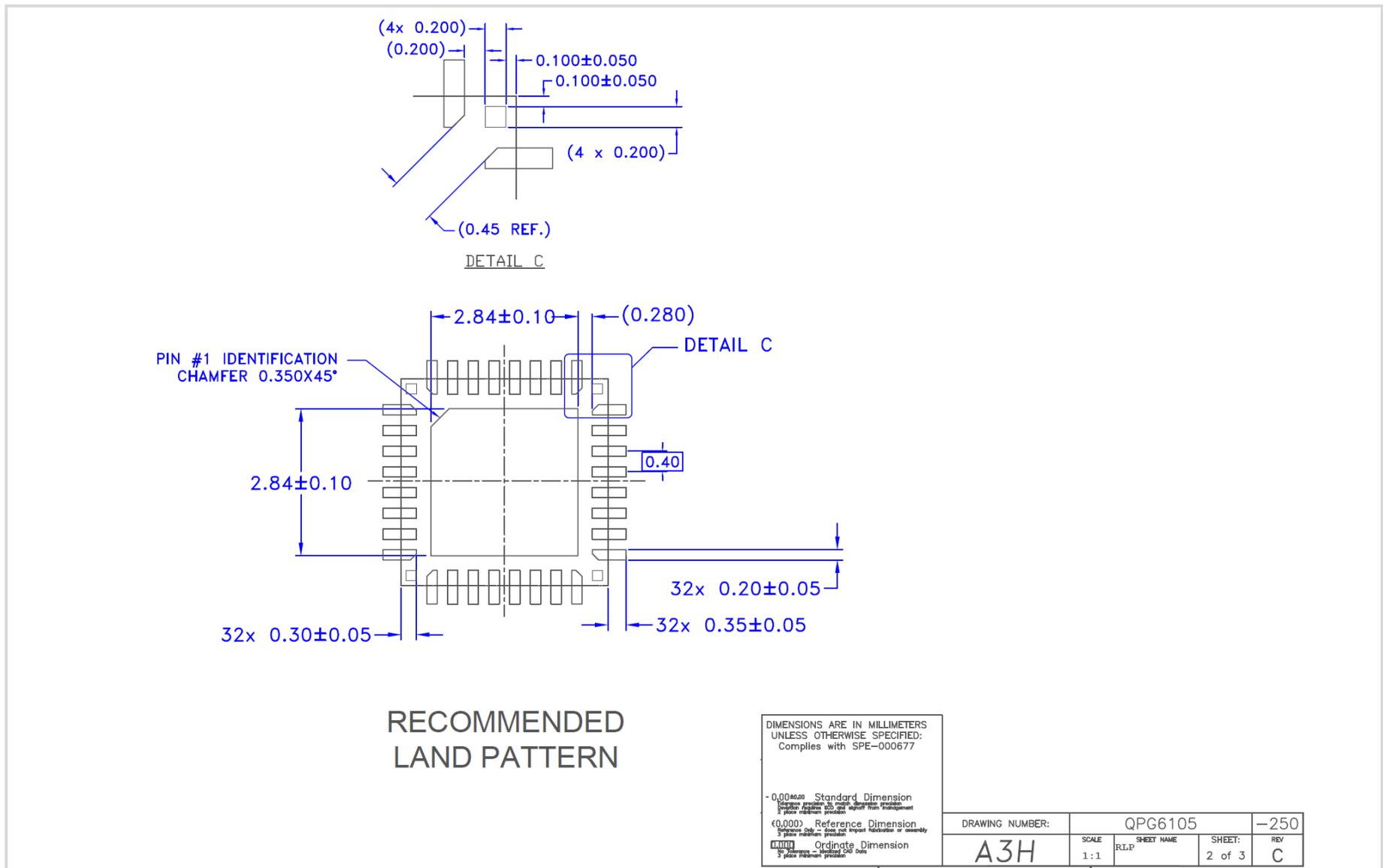


Figure 15: QFN32 Recommended Land Pattern

11.1.3 QFN32 Package Information

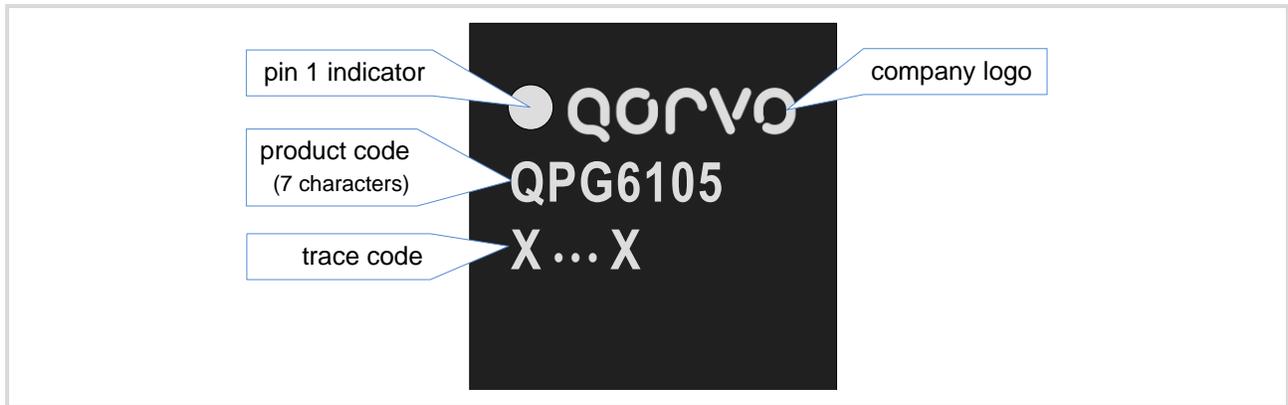


Figure 16: Information on the QFN32 Package

Note: Product code = first 7 characters of the part number (see chapter 4).

11.1.4 QFN32 Thermal Characteristics

Table 31: QFN32 Thermal Characteristics

| Symbol | Parameter | Conditions | QFN32 value | Unit |
|---------------------------------|--|---|-------------|------|
| Theta JA ($R_{\theta JA}$) | Thermal resistance from junction to ambient | JEDEC JESD 51-2; JEDEC 2S2P (4L) board as per JESD 51-7 | 30 | K/W |
| Psi-JT (Ψ_{JT}) | Junction-to-Top thermal characterization parameter | JEDEC JESD 51-12 | 15 | K/W |

11.1.5 QFN32 Tape and Reel Information

11.1.5.1 Carrier and Cover Tape Dimensions

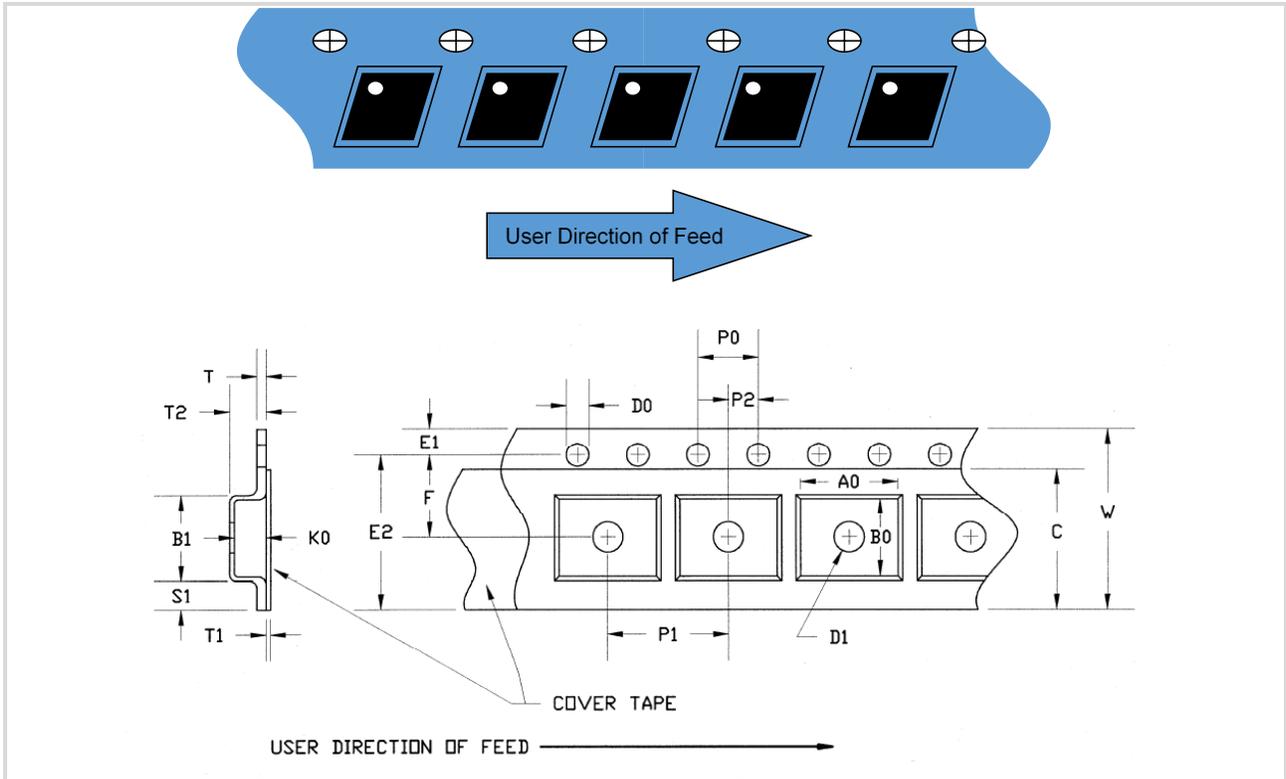


Figure 17: Carrier and Cover Tape Dimensions

Table 32: Carrier and Cover Tape Dimensions

| Feature | Measure | Symbol | Size (in) | Size (mm) |
|---------------------|--|--------|-----------|-----------|
| Cavity | Length | A0 | 0.170 | 4.3 |
| | Width | B0 | 0.170 | 4.3 |
| | Depth | K0 | 0.049 | 1.25 |
| | Pitch | P1 | 0.315 | 8.0 |
| Centerline Distance | Cavity to Perforation - Length Direction | P2 | 0.079 | 2.0 |
| | Cavity to Perforation - Width Direction | F | 0.217 | 5.50 |
| Cover Tape | Width | C | 0.362 | 9.20 |
| Carrier Tape | Width | W | 0.472 | 12.0 |

11.1.5.2 Reel Dimensions

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter (7" for samples). The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.

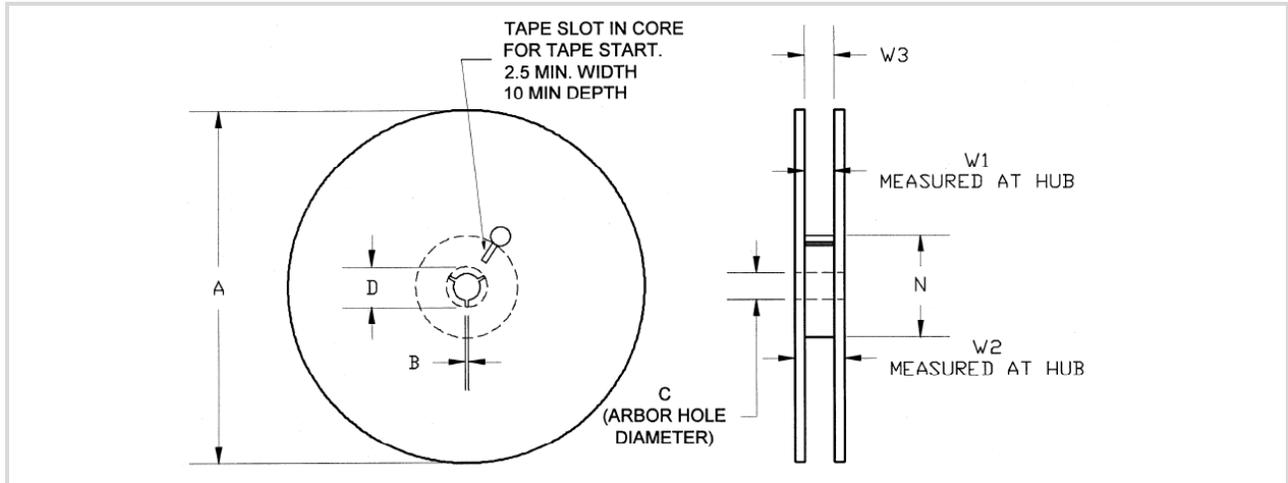


Figure 18: Reel Dimensions

Table 33: 13" Reel Dimensions

| Feature | Measure | Symbol | Size (in) | Size (mm) |
|---------|----------------------|--------|-----------|-----------|
| Flange | Diameter | A | 12.992 | 330 |
| | Thickness | W2 | 0.874 | 22.2 |
| | Space Between Flange | W1 | 0.661 | 16.8 |
| Hub | Outer Diameter | N | 4.016 | 102.0 |
| | Arbor Hole Diameter | C | 0.512 | 13.0 |
| | Key Slit Width | B | 0.079 | 2.0 |
| | Key Slit Diameter | D | 0.795 | 20.2 |

Table 34: 7" Reel Dimensions

| Feature | Measure | Symbol | Size (in) | Size (mm) |
|---------|----------------------|--------|-----------|-----------|
| Flange | Diameter | A | 6.969 | 177.0 |
| | Thickness | W2 | 0.717 | 18.2 |
| | Space Between Flange | W1 | 0.504 | 12.8 |
| Hub | Outer Diameter | N | 2.283 | 58.0 |
| | Arbor Hole Diameter | C | 0.512 | 13.0 |
| | Key Slit Width | B | 0.079 | 2.0 |
| | Key Slit Diameter | D | 0.787 | 20.0 |

11.1.5.3 Tape Info and Label Placement

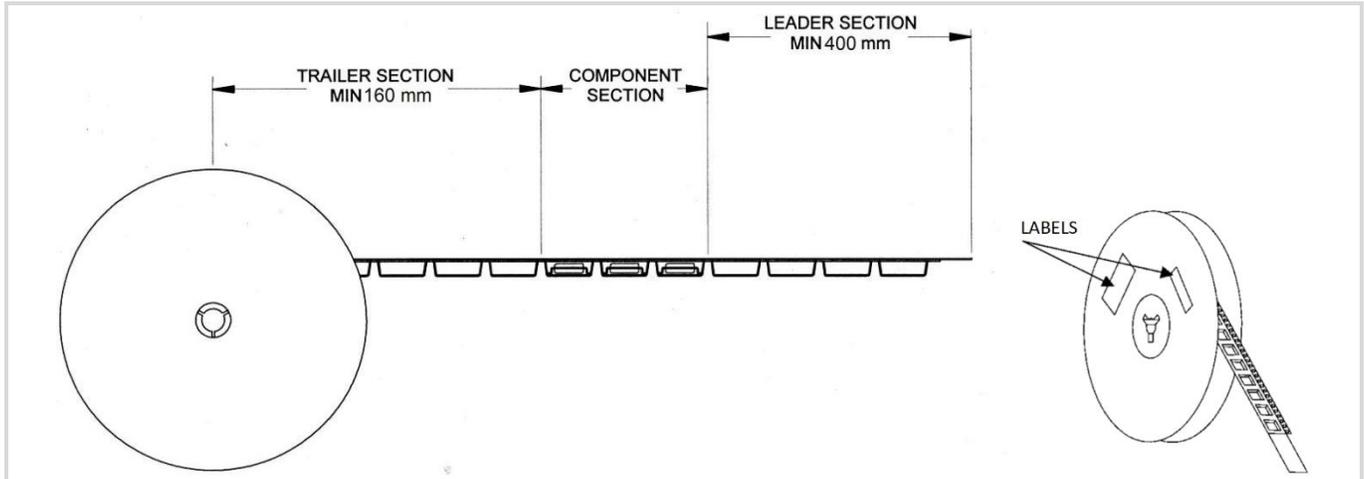


Figure 19: Tape and Labels

Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

11.2 Moisture/Reflow Sensitivity

Table 35: Moisture/Reflow Sensitivity

| Symbol | Parameter | Conditions | Value | Unit |
|--|----------------------------|------------|---------|------|
| | Soldering Process | | Pb-free | |
| T _c | Peak reflow temperature | 10 s max. | 260 | °C |
| MSL | Moisture Sensitivity Level | | 3 | |
| The Moisture/Reflow Sensitivity is classified according to: IPC/JEDEC J-STD-020D.1 (March 2008) Joint Industry Standard; Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. | | | | |

11.3 RoHS Compliance

Table 36: RoHS Compliance

| Symbol | Attribute | Compliant |
|---|--|-----------|
| RoHS | Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment; Directives 2011/65/EU and 2015/863/EU. | ✓ |
|  | Lead Free | ✓ |
| | Halogen Free (Chlorine, Bromine) | ✓ |
| | Antimony Free | ✓ |
| | TBBP-A (C ₁₅ H ₁₂ Br ₄ O ₂) Free | ✓ |
| | PFOS Free | ✓ |
| | SVHC Free | ✓ |

12 Errata

12.1 Spurious External Event

A spurious 'external event' interrupt may be triggered in the following case:

- A timer event is triggered that wakes up the device from RC Standby Mode or 32KiHz Standby Mode, AND
- a GPIO with wake-up capability (WKUP) has been configured to trigger on 'falling edge' (using internal or external pull-up)

This issue will never lead to spurious wake-ups, i.e. the issue is triggered as part of the wake-up resulting from the timer event. The spurious external event can be safely ignored in the external event handler in this case; example: external wake-up line is not low on wake-up. In practice, external event handlers incorporate the robustness against this spurious event by default. Processing overhead of the spurious event will be negligible. In addition, there are handles in the chip that can help working around this issue.

Abbreviations

| | | | |
|------------------|---|-------|---|
| ACL | Asynchronous Connection Logical transport | ISM | Industrial, Scientific, and Medical (license-free frequency band) |
| ADC | Analog-to-Digital Converter | LDO | Low Drop-Out voltage regulator |
| AEC | Automotive Electronics Council | LE | (Bluetooth) Low Energy |
| AES | Advanced Encryption Standard | LED | Light Emitting Diode |
| AGC | Automatic Gain Control | LL | (Bluetooth) Link Layer |
| ANIO | Analog Input/Output | LQI | Link Quality Indication |
| API | Application Program(ming) Interface | LSb | Least-Significant bit |
| ARIB | (Japan) Association of Radio Industries and Businesses | MAC | Medium Access Control layer |
| CCA | Clear Channel Assessment | MCU | MicroController Unit |
| CCM | Counter with CBC-MAC (ciphering), where CBC-MAC = cipher block chaining message authentication code | MEMS | Micro-Electro-Mechanical Systems |
| CCM* | extension of CCM | MOQ | Minimum Order Quantity |
| CDM | (ESD) Charged Device Model | MSb | Most-Significant bit |
| CSMA/CA | Carrier Sense Multiple Access with Collision Avoidance | NVM | Non-Volatile Memory |
| DNL | Differential Nonlinearity | OTA | Over the Air |
| ESD | Electrostatic Discharge | PCB | Printed Circuit Board |
| ETSI | European Telecommunication Standardization Institute | PDM | Pulse-Density Modulation |
| EVM | Error Vector Magnitude | PER | Packet Error Rate |
| FCC | (US) Federal Communications Commission | PHY | Physical layer |
| GATT | Generic Attribute Protocol | POR | Power On Reset |
| GLDO | Global Low Drop-Out voltage regulator | PSRR | Power Supply Rejection Ratio |
| GND | Ground | PWM | Pulse-Width Modulation |
| GPIO | General Purpose Input / Output | QFN | Quad Flat No leads (package) |
| HAL | Hardware Abstraction Layer | RAM | Random-Access Memory |
| HBM | (ESD) Human Body Model | RC | resistor–capacitor (circuit) |
| HCI | Host Controller Interface | RF | Radio Frequency |
| IC | Integrated Circuit | rf4ce | (Zigbee) Radio Frequency for Consumer Electronics |
| IEEE | Institute of Electrical and Electronics Engineers | RSSI | Received Signal Strength Indication |
| INL | Integral Nonlinearity | RoHS | Restriction of Hazardous Substances (Directive) |
| I ² C | Inter-Integrated Circuit | ROM | Read-Only Memory |
| I ² S | Inter-IC Sound | RX | Receive |
| IIP3 | Third Order Input Intercept Point | SPI | Serial Peripheral Interface |
| IO | Input/Output | TWI | Two-Wire Interface |
| IR | InfraRed | TX | Transmit |
| | | UART | Universal Asynchronous Receiver and Transmitter |
| | | VDD | Voltage Drain Drain (i.e. Positive voltage supply) |
| | | VMT | Voltage Minimum Threshold |

Important Notices

The information contained in this Data Sheet and any associated documents (“Data Sheet Information”) is believed to be reliable; however, Qorvo makes no warranties regarding the Data Sheet Information and assumes no responsibility or liability whatsoever for the use of said information. All Data Sheet Information is subject to change without notice. Customers should obtain and verify the latest relevant Data Sheet Information before placing orders for Qorvo® products. Data Sheet Information or the use thereof does not grant, explicitly, implicitly or otherwise any rights or licenses to any third party with respect to patents or any other intellectual property whether with regard to such Data Sheet Information itself or anything described by such information.

DATA SHEET INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. Applications described in the Data Sheet Information are for illustrative purposes only. Customers are responsible for validating that a particular product described in the Data Sheet Information is suitable for use in a particular application.

© 2021-2023 Qorvo, Inc. All rights reserved. This document is subject to copyright laws in various jurisdictions worldwide and may not be reproduced or distributed, in whole or in part, without the express written consent of Qorvo, Inc. | QORVO® is a registered trademark of Qorvo, Inc. | ConcurrentConnect™ technology is a trademark of Qorvo, Inc.

The Bluetooth® word mark and logos are registered trademarks owned by Bluetooth SIG, Inc. and any use of such marks by Qorvo is under license. Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. This device contains Packetcraft Open Source protocol software; Copyright (c) 2019 Packetcraft, Inc. | Licensed under the Apache License, Version 2.0. All other trademarks, trade names, product or service names are those of their respective owners.

Product Status

| Marking | Product Status | Definition |
|--------------|-----------------------|---|
| ADVANCE INFO | Formative / In Design | Datasheet contains design specifications for product development. Specifications may change in any manner without notice. |
| PRELIMINARY | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Qorvo reserves the right to make changes at any time without notice to improve the design. |
| (none) | Full Production | Datasheet contains final specifications. Qorvo reserves the right to make changes at any time without notice to improve the design. |
| OBSOLETE | Not in Production | Datasheet contains specifications on a product that is discontinued. The datasheet is for reference information only. |

Document History

| Version | Date | Section | Changes |
|---------|-------------|------------------------------|---|
| 1.00 | 9 Jun 2022 | | FINAL Release. |
| 1.01 | 13 Sep 2022 | 1, 3, 5.2.2, 5.2.7, 5.4, 5.6 | Updated text on ConcurrentConnect. |
| | | 5.14.1 | Added POR Detector. |
| | | 6.12 | Updated accuracy of temperature measurement. |
| | | 11.1.1 | Corrected GPIO18 PDM pin assignment. |
| | | 11.1.2 | Updated package outline drawings according to PCN#22-0072. |
| 1.02 | 4 Oct 2022 | | Document classification changed to Unrestricted. Format changed to Letter. |
| | | 1 | Added bullet for ConcurrentConnect Multi-Channel. |
| 1.03 | 10 Oct 2023 | Table 10 | Desense information added for IEEE 802.15.4 communication. |
| | | Table 22 | Supported ADC input range updated. |
| 1.04 | 15 Nov 2023 | Table 10 | IEEE 802.15.4 sensitivity updated. Channel numbers replaced by frequencies. |
| | | Table 11 | BLE channels with reduced sensitivity expressed as frequencies. |