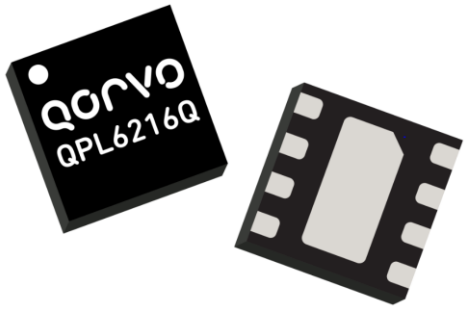
QPL6216Q

High-Linearity SDARS LNA

Product Description

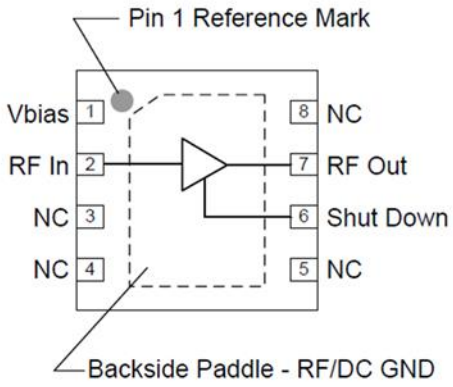
The QPL6216Q is a high linearity, ultra-low noise gain block amplifier in a small 2x2 mm surface-mount package. At 2332 MHz, the amplifier typically provides +36 dBm OIP3. The amplifier does not require any negative supplies for operation and can be biased from positive supply rails from 3.3 to 5.25 V. The device is housed in a lead- free/green/RoHS-compliant industry-standard 2x2 mm package.

The QPL6216Q uses a high performance E-pHEMT process. The low noise amplifier contains an internal active bias to maintain high performance over temperature.



Package: DFN, 8-pin
2.0mm x 2.0mm x 0.85mm

Functional Block Diagram



Feature Overview

- Tested in accordance with AEC-Q100 Grade 2
- High Gain device – Typical value 15.1dB
- Ultra-low noise figure, 0.45 dB NF at 2332 MHz
- High linearity, +36 dBm Output IP3
- Unconditionally stable
- Externally controlled Icq with Vbias
- Integrated shutdown control pin
- 3.3-5.25 V positive supply voltage: −Vgg not required

Applications

- SDARS Active Antenna

Ordering Information

PART NUMBER	DESCRIPTION
QPL6216QSB	5 PIECE SAMPLE BAG
QPL6216QSQ	25 PIECE SAMPLE BAG
QPL6216QSR	100 PIECE 7” REEL
QPL6216QTR7	2500 PIECE 7” REEL
QPL6216QPCK-01	EVALUATION BOARD + 5 PC SAMPLE BAG

Standard T/R Size = 2500 pieces on a reel

Absolute Maximum Ratings

PARAMETER	RATING	UNITS
Storage Temperature	-65 to 150°	C
Supply Voltage (V_{DD})	+7	V
RF Input Power, CW, 50Ω, T = 25°C	+22	dBm

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage (V_{DD})	+3.3	+4.5	+5.25	V
Bias Voltage (V_{bias})	+3.3	+3.6	+5.25	V
TCASE	−40		+105	°C
TJ (for >10^6 hours MTTF)			+190	°C

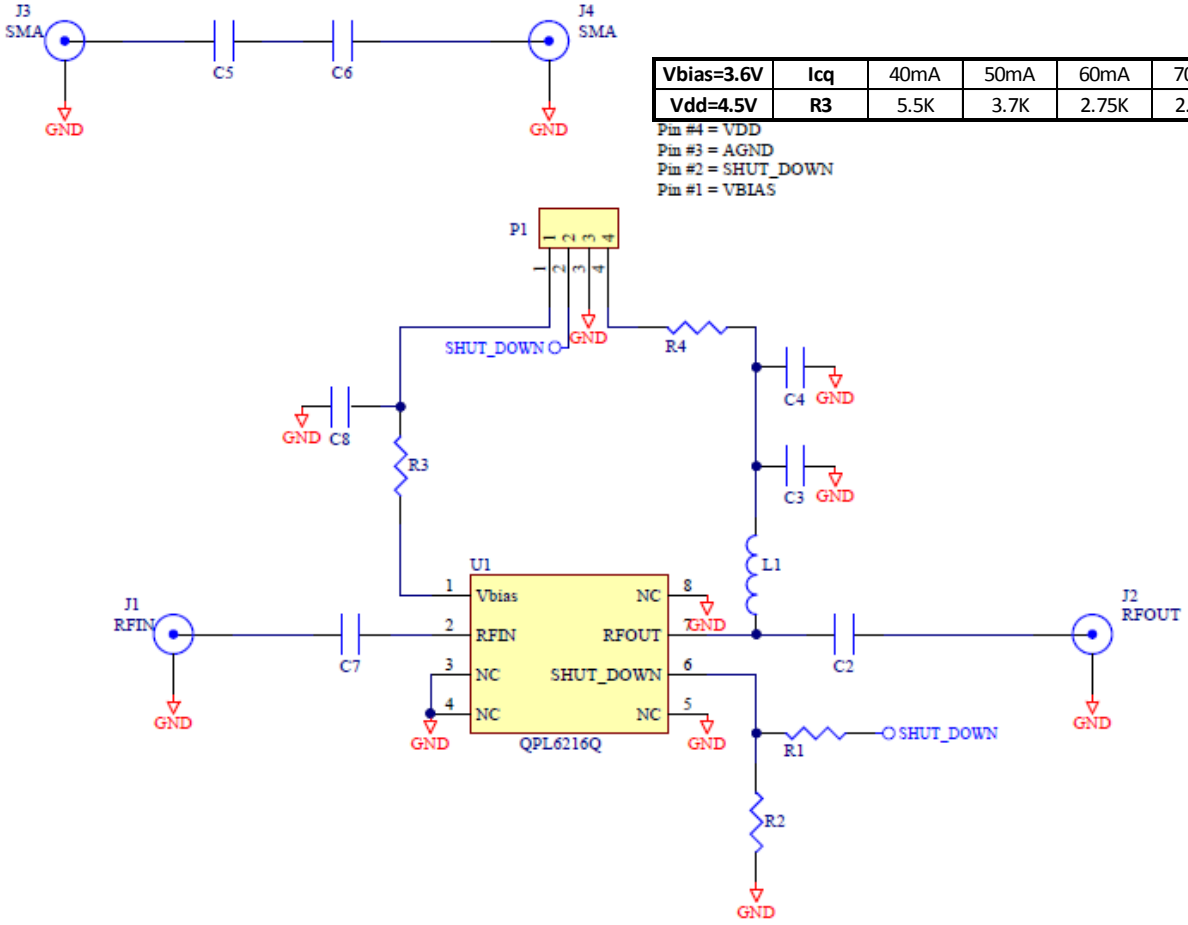
Electrical Specifications at +25˚C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operational Frequency Range		2320	2332	2345	MHz
Test Frequency			2330		MHz
Gain		14.3	15.1	15.6	dB
Input Return Loss			9		dB
Output Return Loss			15		dB
Output P1dB		+18.0	+22.5		dBm
Output IP3	Pout=+2 dBm/tone, Δf=1 MHz	+30	+36		dBm
Noise Figure[1]			0.45	0.65	dB
Power Shutdown Control (Pin 6)	On state	0		0.63	V
	Off state (Power down)	1.17	1.8	V_{DD}	V
Current, I_{DD}[2]	On state	45	60	75	mA
	Off state (Power down)		3	5	mA
Shutdown pin current, ISD	VPD ≥ 1.17 V		140		µA
Thermal Resistance, θjc	channel to case		62		°C/W

Test conditions unless otherwise noted: V_{DD} = +4.5V, V_{bias} = +3.6V, Temp =+25°C, 50 Ω system

Note: 1) Noise Figure data has input trace loss de-embedded
2) Icq set by external 2.75K resistor

Application Schematic

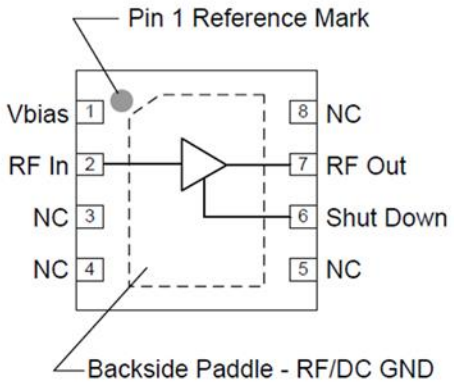


Vbias=3.6V	Icq	40mA	50mA	60mA	70mA	80mA
Vdd=4.5V	R3	5.5K	3.7K	2.75K	2.13K	1.73K

Pin #4 = VDD
Pin #3 = AGND
Pin #2 = SHUT_DOWN
Pin #1 = VBIAS

Qty	Ref Des	Description
1		High Linearity, SDARs LNA
1		PCB, QPL6216Q
4	"C2, C5, C6, C7"	CAP, 100pF, 5%, 50V, C0G, 0402
1	C3	CAP, 1000pF, 10%, 50V, X7R, 0402
1	C4	CAP, 1uF, 10%, 6.3V, X7R, 0402
1	R1	RES, 0 OHM, 5%, 1/10W, 0402
1	R4	RES, 3.3 OHM, 5%, 1/16W, 0402
1	R3	RES, 2.7K, 5%, 1/16W, 0402
1	R2	RES, 20K, 5%, 1/16W, 0402
1	L1	IND, 18nH, 5%, M/L, 0402
4	J1,J2,J3,J4	862000-422 CONN .062 RF SMA F STRT FLANG
1	P1	CONN, HDR, ST, PLRZD, 4-PIN, 0.100"

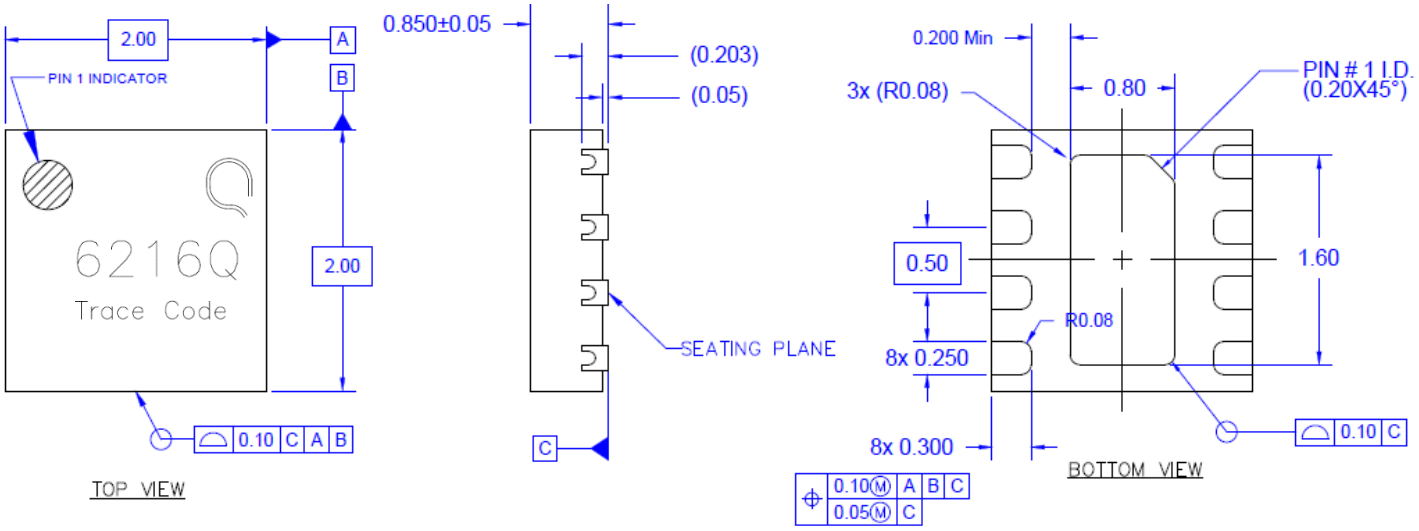
Pin Configuration and Description



Pin No.	Label	Description
1	Vbias	Sets the Icq bias point for the device.
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Mechanical Information

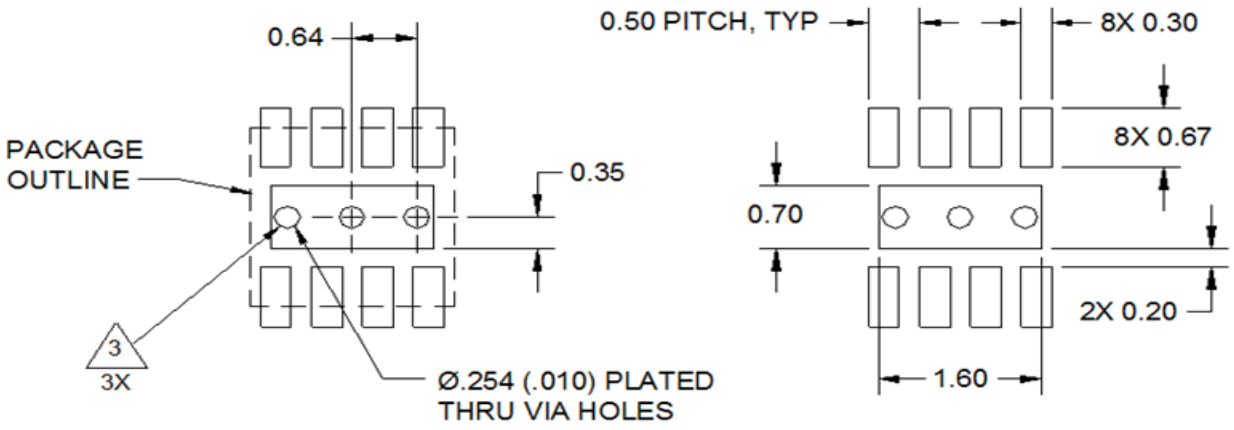
Marking: Part number – 6216Q
Trace Code – XXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1B

Value: Passes ≥ 500 V to < 1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class C3

Value: Passes ≥1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

RoHs Compliance

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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