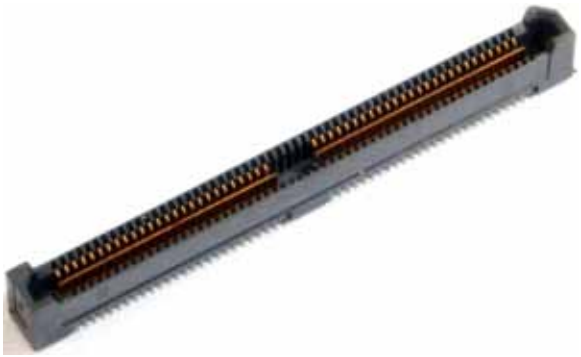
Q Rate® QRM8/QRF8 Series in 28 Gbps per Channel (OIF CEI-28G-SR) Applications

QRM8-052-02.0-S-D-A

Mates with

QRF8-052-05.0-S-D-A



SIG@samtec.com
+1-800-726-8329

COPYRIGHTS, TRADEMARKS, and PATENTS

Final Inch® and QRate® are trademarks of Samtec, Inc. Other product names used herein are trademarks of their respective owners. All information and material in this publication are property of Samtec, Inc. All related rights are reserved. Samtec, Inc. does not authorize customers to make copies of the content for any use.

Terms of Use

Use of this publication is limited to viewing the pages for evaluation or purchase. No permission is granted to the user to copy, print, distribute, transmit, display in public, or modify the contents of this document in any way.

Disclaimer

The information in this publication may change without notice. All materials published here are "As Is" and without implied or expressed warranties. Samtec, Inc. does not warrant this publication will be without error, or that defects will be corrected. Samtec, Inc. makes every effort to present our customers an excellent and useful publication, but we do not warrant or represent the use of the materials here in terms of their accuracy, reliability or otherwise. Therefore, you agree that all access and use of this publication's content is at your own risk.

NEITHER SAMTEC, INC. NOR ANY PARTY INVOLVED IN CREATING, PRODUCING, OR DELIVERING THIS PUBLICATION SHALL BE LIABLE FOR ANY DIRECT, INCIDENTAL, CONSEQUENTIAL, INDIRECT, OR PUNITIVE DAMAGES ARISING OUT OF YOUR ACCESS, USE OR INABILITY TO ACCESS OR USE THIS PUBLICATION, OR ANY ERRORS OR OMISSIONS IN ITS CONTENT.

Abstract

Several industry standards are developing higher speed serial data interfaces with the purpose of increased data flow. These standards include 100 Gigabit Ethernet (100 GbE) and the Optical Internetworking Forum (OIF). As these standards are finalized, the requisite technology will be deployed in workstations, servers, and communication platforms.

These standards will have serial channels operating in the 19-28 Gbps (giga-bits/second) regime depending on the number of parallel paths which aggregate the data to 100 Gbps. At these data rates, the physical layer needs to be designed as a microwave channel since the data stream can easily have frequency content up to 50 GHz. The technology used to achieve these data rates are a combination of enhanced physical media (connectors, cables, PCBs) and improved transceiver technology.

This Technical Note describes a statistical simulation method applied to proven Samtec Final Inch® designs and is intended to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors.

Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds up to 28 Gbps. To demonstrate the feasibility of using Samtec Q Rate® QRM8/QRF8 Series connectors in 28Gbps applications with PCBs, full S-parameter modeling of the channel, along with statistical simulation techniques, will be used to sweep various trace lengths across the design space to show a maximum trace length the channel can support.

The vast majority of Samtec customers use industry standards as a starting point in their design. Customers may not be using a non-compliant transmitter, or they may be using much shorter, low loss channel with minimal equalization. Samtec recognizes this and has taken the approach of assuming typical driver and receiver equalization to show how our products perform in OIF or other 28Gbps applications.

OIF-CEI-03.0

The Optical Internetworking Forum (OIF) has done considerable work to define practical usage models which enable long haul optical communications. This work by OIF at the physical layer is necessary for hardware providers to develop highly reliable electrical platforms operating at next generation data rates.

The usage models include -LR (long reach), -SR (short reach), and VSR (very short reach). LR models target traditional rack mounted backplane systems with removable line cards. SR models focus on board-to-board (BTB) scenarios where circuit boards are in a stackable configurable. VSR models are chip-to-chip connections within a module. This Technical Note will leverage work from the OIF SR usage model (board-to-board) shown in Figure 1.

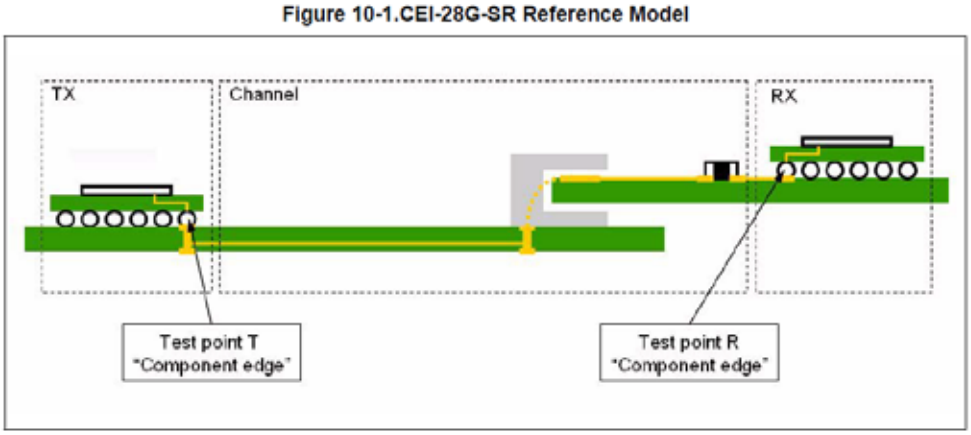


Figure 1. SR Usage Scenario from OIF-CEI-03.0

The approach taken by OIF is to define transmitter and channel characteristics but leave the receiver definition open for creative equalization implementations. At 28 Gbps data rates, practical low BER data transmission is only possible using sophisticated receiver equalization. This usually takes the form of continuous time linear equalization (CTLE) and decision feedback equalization (DFE). By leaving the receiver equalization undefined, the OIF specification allows flexibility and creativity in design. Transmitters are assumed to use some form of more simplistic de-emphasis or finite impulse response (FIR) equalization, and OIF provides guidance here.

Simulation Model

Figure 2 shows the mated Samtec Q Rate® QRM8/QRF8 Series connectors used in a typical multi-segment channel with a source adapter residing on a motherboard and a target adapter residing on an add-in card. The test circuit includes:

- Tx (transmitter) and Rx (receiver) models that include IC packaging effects. These package effected are modeled using Ansys HFSS.
- A variable length interconnect trace segment on the Tx side of the connector. This is shown as Segment #1 on the source adapter in Figure 2.
- A fixed length interconnect trace on the Rx side of the connector. This is shown as Segment #2 on the target adapter in Figure 2.
- A mated Samtec Q Rate® QRM8/QRF8 Series connector touchstone S-parameter model developed with CST Microwave Studio
- Asynchronous crosstalk aggressors on highest coupled channels

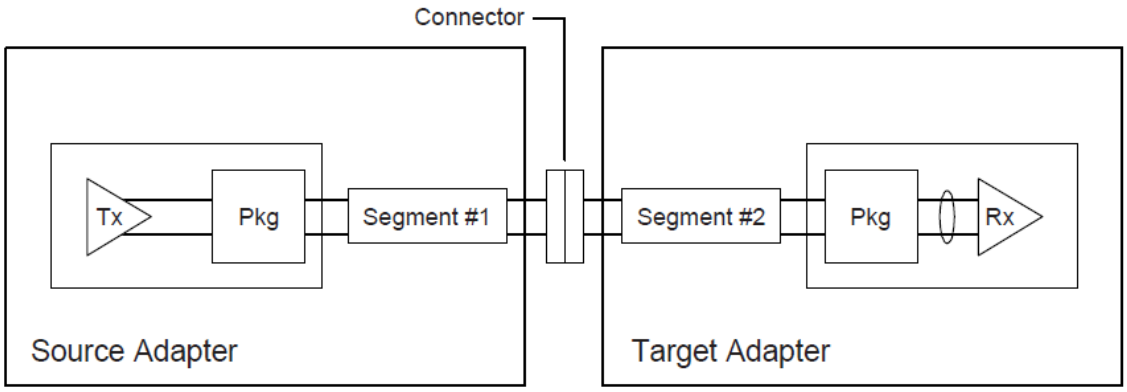


Figure 2. Simulation Model

Segment topology of the source and target adapters were swept to determine the limits of compliant channel operation. The source length is swept from 2" to 18" with the target length set at 2".

All traces were modeled as microstrip on Nelco 4000-13 SI with the following parameters:

- The board material is modeled using a Svensson/Djordjevic causal model that has a broadband response that is faithful to measured results from DC to greater than 20 GHz, using the following parameters:
  - Er = 3.5 @ 1 GHz
  - Loss Tangent = 0.008 @ 1 GHz

- Copper is modeled as follows to reflect the reduced conductivity of copper foil used in PCB fabrication:
  - Conductivity = 4.5 E+7 S-m
  - Surface roughness = 0.6 micron

- Traces are differential microstrip with the following geometry:
  - 100 ohm differential impedance
  - 7 mil trace width
  - 1.4 mil trace copper thickness
  - 9 mil spacing between differential traces
  - 4 mil dielectric thickness
  - 30 mil spacing between differential pairs

These parameters reflect typical trace geometries and material parameters used in 28 Gbps applications. Other trace geometries or materials will lead to different results than shown here. However, if reasonable care is made to stay well within the design space and guidelines provided in this document, it is possible to build robust 28 Gbps channels with limited additional simulation verification.

Transmitter Model

OIF-CEI-03.0 is helpful in developing a representative transmitter model. For our simulation model, we will use a driver amplitude of 800mVpp differential with 8 pS (20-80%) rise and fall times as per table 10-6 of OIF-CEI-03.0 (Figure 3)

Table 10-6. Transmitter Electrical Output Specification.

Characteristic	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Baud Rate	T_Baud		19.90		28.05	Gsym/s
Output Differential Voltage	T_Vdiff	Emphasis off. See Note 4	800		1200	mVppd
Differential Resistance	T_Rd		80	100	120	Ω
Differential Termination Resistance Mismatch (see Table 1-2)	T_Rdm				10	%
Output Rise and Fall Time (20% to 80%)	T_tr, T_tf	Emphasis off. See Note 2	8			ps
Common Mode Noise	T_Ncm	Note 3			12	mVrms
Differential Output Return Loss	T_SDD22	See Section 10.3.1.3				dB
Common Mode Output Return Loss	T_SCC22	Below 10 GHz			-6	dB
		10 GHz to baud rate			-4	
Output Common Mode Voltage	T_Vcm	Load Type 0 See Note 1	-100		1700	mV

NOTES:
1. Load Type 0 with min. T_Vdiff, AC-Coupling or floating load.
2. The transmitter under test is preset such that C0 is its maximum value (C0_max) and all other coefficients are zero. The 20% and 80% values are of the steady state one and zero. The max value is limited by the linear fit pulse peak value in Table 10-11.
3. Measurement procedure is defined in Section 12.3.
4. T_Vdiff is two times the steady-state value V_f as defined in Section 10.3.1.6.2. The value is given as differential p-p voltage.

Figure 3. Transmitter Characteristics from OIF-CEI-03.0

Transmitter jitter is not defined at 28 Gbps in OIF-CEI-03.0. Work done by OIF on the VSR spec can be leveraged which defines the total transmitter jitter to be 0.28UI. With these parameters, a representative transmitter model can be constructed. Figure 4 shows the transmitter waveform prior to pre-emphasis.

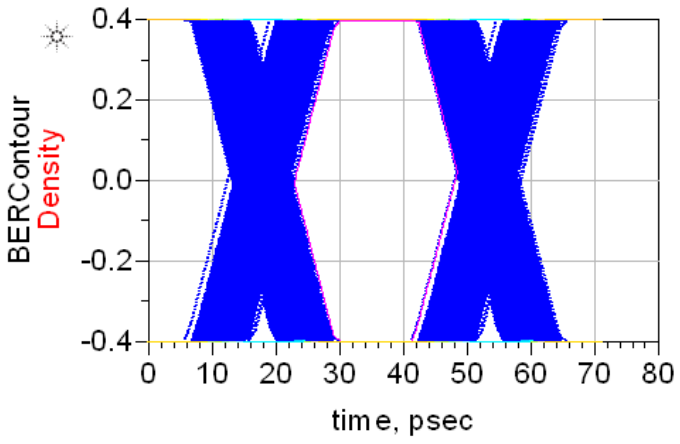


Figure 4. Transmitter Waveform

Package Model

OIF-CEI-03.0 does not provide a model or insight into the driver/receiver package effects; however, it is important to include the package discontinuities in a 28 Gbps channel simulation. Samtec has some experience with flip chip IC packaging and a representative geometric model was created using practical package design criteria.

The model was simulated using Ansys HFSS and a 12 port coupled S-parameter model was extracted. The differential insertion loss and return loss from this extracted model is shown in Figure 5.

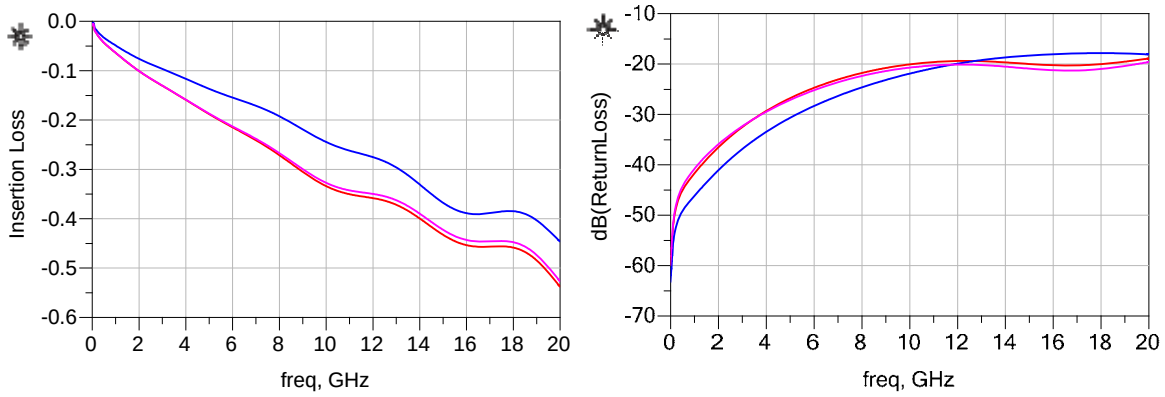


Figure 5. Insertion Loss (left) and Return Loss (right) of Tx/Rx Package Model

Receiver Model

Channels operating at 28 Gbps rely on sophisticated equalization embedded in the receiver. Unfortunately, the OIF specification does not directly specify receiver equalization parameters. In other high speed serial standards (PCIe G3), receiver equalization is defined to include a 2 pole CTLE and 3 tap DFE. This equalization approach will be used and can be readily implemented in the simulation environment.

In addition to equalization, receiver sensitivity in the form of an eye mask is required. This will serve as "good to" metric meaning the PCB trace lengths will be increased until the eye contour at a BER of 10^{-12} violates the eye mask. In other high speed serial standards (PCIe G3), receiver sensitivities of 25 mVpp are defined. It is recognized that other sources of noise are not included in this simulation, notably driver and receiver impedance mismatch outside of the package model. To provide margin for effects not included in the channel model, the receiver threshold will be increased from 25 mVpp to 50 mVpp. The mask width will be 0.25 UI consistent with the mask width defined in PCIe G3.

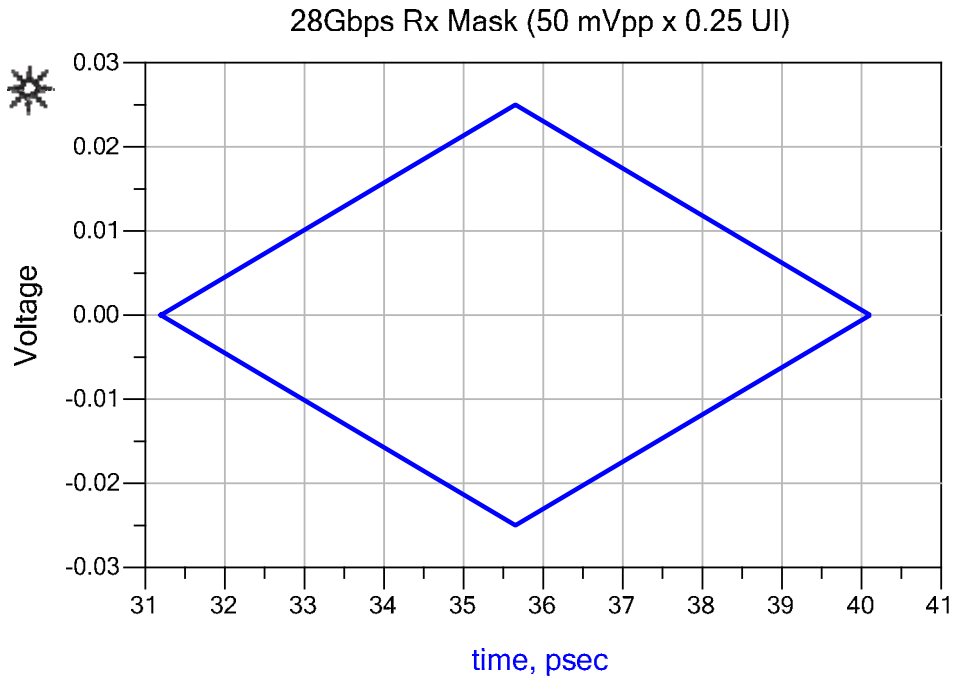


Figure 6. Receiver Mask

Simulation Environment

For this Technical Document, Agilent's Advanced Designed System 2013 (ADS) software simulation tool is used to accomplish the simulation tasks. Templates were developed within ADS to automate the analysis so that channel components can be easily replaced. The ADS templates require the following channel definitions:

- Definition of input S-parameter files to be used in the simulations.
  - Tx Package
  - Rx Package
  - Samtec Q Rate® QRM8/QRF8 Series 7mm mated connector on recommended PCB footprint
  - Nelco 4000-13 SI Microstrip Differential Trace
- Definition of Tx segment 1 and Rx segment 2 trace lengths to be simulated.
- Iterative processing of the transmitter trace length (trace length A) using the ADS2013 batch simulation mode. The receiver trace length (trace length B) is fixed at 2".

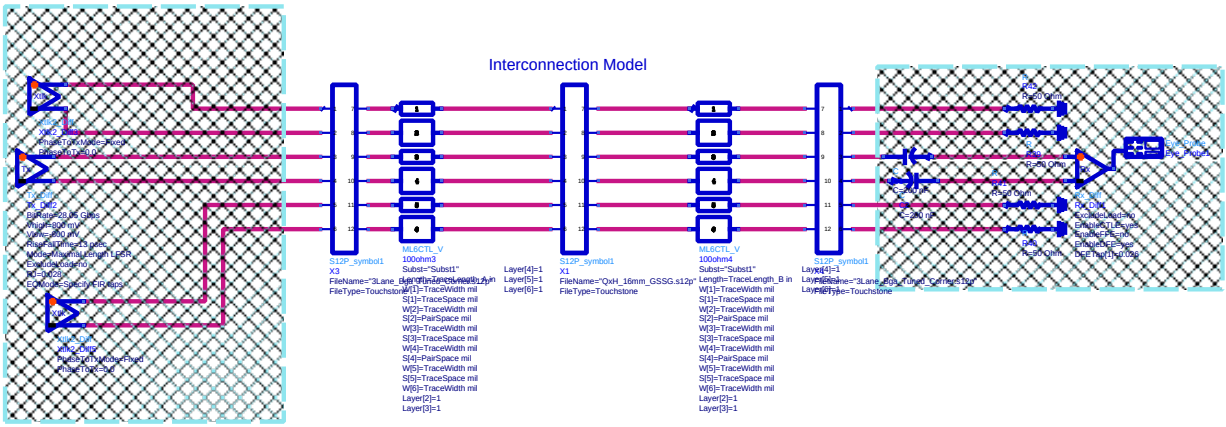


Figure 7. ADS Channel Simulation Environment

Simulation Results

Figures 8 display a graph of the measured inner eye height for each simulated transmitter trace length. This simulation includes all channel, jitter, crosstalk effects, and 2" of receiver trace length. Our chosen compliance limit of 50 mV P-P is shown on the chart as a red line. With the trace models and material parameters that we are using, a total channel reach of 11" (9" on Tx side, 2" on Rx side) is possible. Longer channels will have higher loss, with lower eye openings; however, we generally do not advise using longer channels without detailed channel modeling.

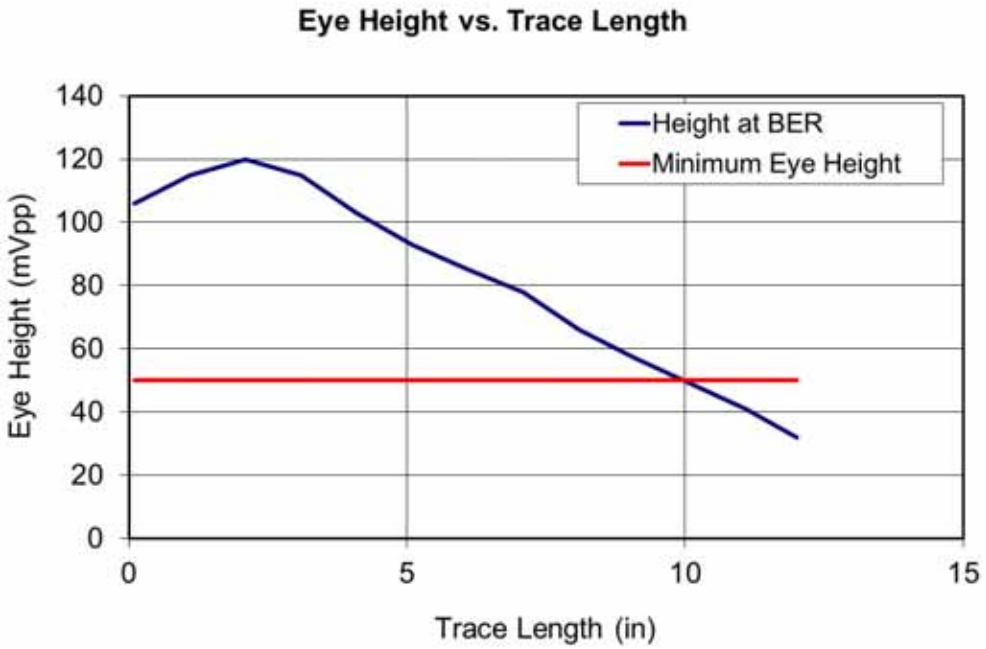


Figure 8. Eye Height vs. Transmitter Trace Length
7 mm QRM8/QRF8

Figure 9 displays a graph of the measured inner eye width for the aforementioned simulation deck. The 0.25 UI eye width compliance limit is shown as a red line on the chart. The simulations show that the eye height limit is reached before the eye width.

Figure 9. Eye Width vs. Channel Length
7 mm QRM8/QRF8

The simulated eye for 11" of interconnect (9" Tx board trace, 2" Rx board trace) is shown in Figure 10. For these statistical simulations, the eye boundary is defined for a statistical confidence interval with a bit error rate (BER) of 10^{-12}. A 57.0 mV inner eye opening was measured by the simulator; this is just above our established compliance limit for this study. The measured inner eye width of 0.27 UI is above our 0.25 UI limit. By providing 32 mV of additional amplitude margin over the specified 25 mV limit, we provide a guard against additional issues that may be unforeseen by the designer.

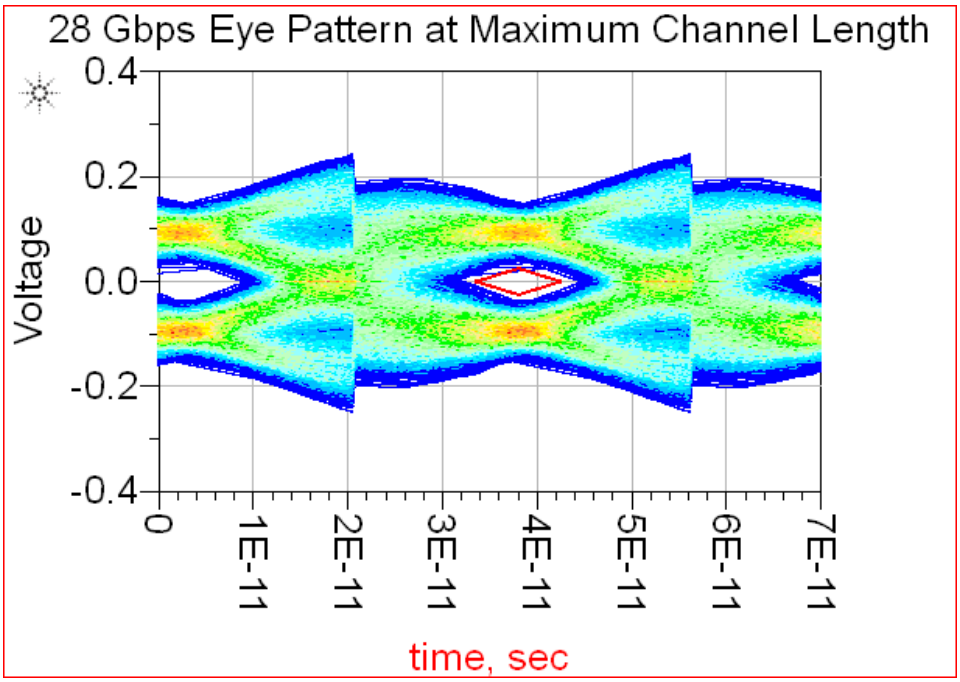


Figure 10. Eye Pattern at Maximum Channel Length using Equalization (3 tap FIR, CTLE and DFE) 7 mm QRM8/QRF8

Conclusion

A single Samtec 7 mm stack height Q Rate® QRM8/QRF8 Series connector in a board-to-board configuration can be used in 100 ohm 28.0 Gbps systems with total trace lengths not to exceed 11 total inches when used with Samtec's Final Inch® routing, breakout, and trace width solutions as modeled and simulated in this document.

Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, sub optimal routing solutions with higher pair-to-pair coupling, and additional vias will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum trace length limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.