1. General Description

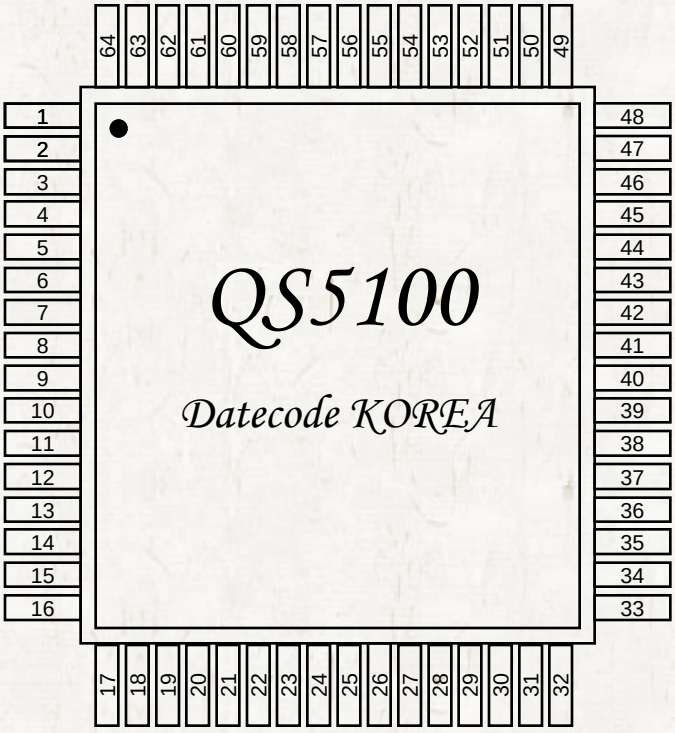
The QS5100 is a high quality Effect processor LSI that can produce the effects of reverb, chorus, echo, vibrato, tremolo, wahwah, and flanger with a 5 band-equalizer.

All functions can be controlled by an external 8bit MCU, making it possible for the QS5100 to be applied to a wide variety of applications.

Making the QS5100 the best solution for external guitar effectors, car audio, PA and hardware effect modules.

2. Features

- High resolution of up to 32k ~ 48kHz sampling rate
- Supports 8 bit MCU or Serial EEPROM interface for stand alone mode.
- 5 band EQ on digital output
- Supports 256k words EDO DRAM for delay.
- Low power operation 2.7V ~ 3.6V
- Support for 16/18/20/22/24 bits Codec I/F
- Supports reverb, chorus, echo, wah wah, flanger, tremolo, vibrato
- Compact thin package 64 LQFP (10 X 10mm)
- f = 8.192 ~ 12.288 MHz
- Low power consumption under 10uA in power down mode
- IDD_{OP} < 50 mA
- Can be assign CODEC I/F (Left or Right Justified)



64P LQFP
10 X 10mm 0.5 pitch

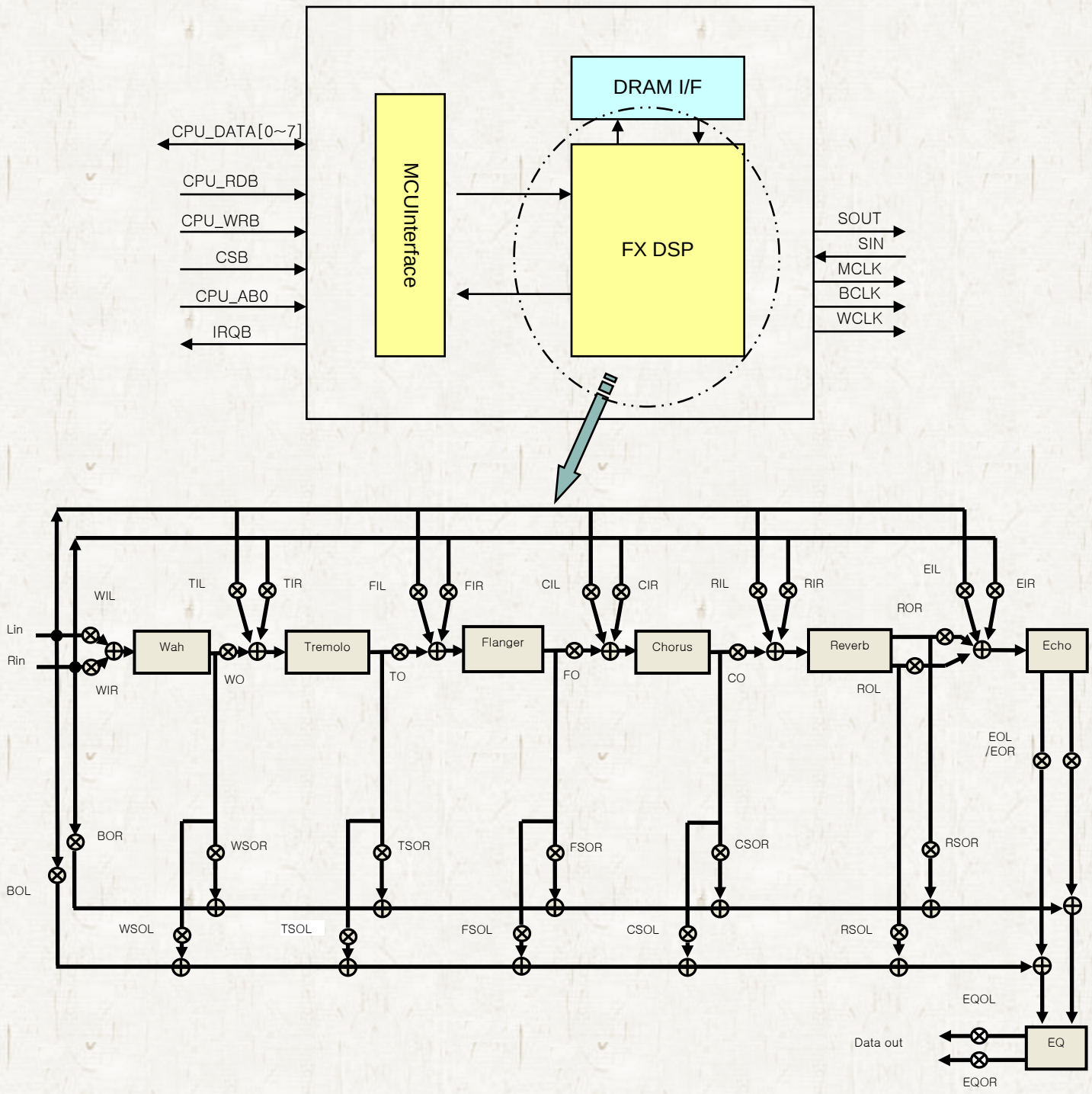
3. Pin Description

PIN NO	PAD NAME	PAD TYPE	I/O	DESCRIPTION
P1	CPU_DATA[0]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Serial EEPROM Data I/O for Stand Alone Mode.
P2	CPU_DATA[1]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Serial EEPROM Clock for Stand Alone Mode.
P3	CPU_DATA[2]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Set[0] for Stand Alone Mode.
P4	CPU_DATA[3]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Set[1] for Stand Alone Mode.
P5	CPU_DATA[4]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Set[2] for Stand Alone Mode.
P6	CPU_DATA[5]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Set[3] for Stand Alone Mode.
P7	VDD	PVDF	P	Power
P8	VSS	PV0F	P	Ground
P9	CPU_DATA[6]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Set[4] for Stand Alone Mode.
P10	CPU_DATA[7]	PC3B03U	I/O	CPU Data I/O for Normal Mode. Set[5] for Stand Alone Mode.
P11	CPU_REB	PC3B03U	I/O	Data Read Enable for Normal Mode. Used for external data read operation, functions on active low. First Serial Peripheral Interface CS $\overline{\text{for}}$ Stand Alone Mode.
P12	CPU_WEB	PC3B03U	I/O	Data Write Enable for Normal Mode. Used for external data write operation, functions on active low. First Serial Peripheral Interface Clock for Stand Alone Mode.
P13	CPU_AB0	PC3B03U	I/O	Address Data Select for Normal Mode. Used to distinguish between Address and Data. Low for Address, High for Data. First Serial Peripheral Interface Data for Stand Alone Mode
P14	CSB	PC3D21	I	QS5100 Chip Select. Data Read/Write operation possible when '0'. Cannot when '1'.
P15	IRQB	PC3B03U	I/O	CPU Interrrupt for Normal Mode. Second Serial Peripheral Interface CS $\overline{\text{for}}$ Stand Alone Mode.
P16	SPI2_CLK	PC3B03U	I/O	Second Serial Peripheral Interface Clock for Stand Alone Mode.
P17	SPI2_OUT	PC3B03U	I/O	Second Serial Peripheral Interface Data for Stand Alone Mode.
P18	MODE0	PC3D21	I	System Clock Mode 2X clock is used in System Clock when '0', 1X clock when '1'
P19	MODE1	PC3D21	I	System Select Mode Normal Mode when '0', Stand Alone Mode when '1'
P20	MODE2	PC3D21	I	Clock 2X Test Mode Normal mode when '0', Clock 2X test mode when '1'

PIN NO	PAD NAME	PAD TYPE	I/O	DESCRIPTION
P21	MRSTB	PC3D21U	I	Master Reset Operates on active low.
P22	XOUT	PC3X11	O	Crystal Output
P23	XIN	PC3X11	I	Crystal Input (f = 8.192 ~ 12.288 Mhz)
P24	VDD	PVDF	P	Power
P25	VSS	PV0F	P	Ground
P26	SIN	PC3D21	I	Serial Data Input
P27	MCLK	PC3O03	O	Serial Data System Clock
P28	WCLK	PC3O03	O	Serial Data Sample Rate Clock
P29	BCLK	PC3O03	O	Serial Data Bit Clock
P30	SOUT	PC3O03	O	Serial Data Output
P31	DRAM_ADDR[4]	PC3O03	O	DRAM Address
P32	DRAM_ADDR[5]	PC3O03	O	DRAM Address
P33	DRAM_ADDR[6]	PC3O03	O	DRAM Address
P34	DRAM_ADDR[7]	PC3O03	O	DRAM Address
P35	DRAM_ADDR[8]	PC3O03	O	DRAM Address
P36	DRAM_OEB	PC3O03	O	DRAM Output Enable
P37	DRAM_UCASB	PC3O03	O	DRAM Upper Column Address Strobe
P38	DRAM_LCASB	PC3O03	O	DRAM Lower Column Address Strobe
P39	VDD	PVDF	P	Power
P40	VSS	PV0F	P	Ground
P41	DRAM_ADDR[3]	PC3O03	O	DRAM Address
P42	DRAM_ADDR[2]	PC3O03	O	DRAM Address
P43	DRAM_ADDR[1]	PC3O03	O	DRAM Address
P44	DRAM_ADDR[0]	PC3O03	O	DRAM Address
P45	DRAM_RASB	PC3O03	O	DRAM Row Address strobe
P46	DRAM_WEB	PC3O03	O	DRAM Write Enable
P47	DRAM_DATA[3]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P48	DRAM_DATA[2]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P49	DRAM_DATA[1]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P50	DRAM_DATA[0]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P51	DRAM_DATA[4]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P52	DRAM_DATA[5]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P53	DRAM_DATA[6]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P54	DRAM_DATA[7]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P55	DRAM_DATA[8]	PC3B03U	I/O	DRAM Data Inputs/Outputs

PIN NO	PAD NAME	PAD TYPE	I/O	DESCRIPTION
P56	VDD	PVDF	P	Power
P57	VSS	PV0F	P	Ground
P58	DRAM_DATA[9]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P59	DRAM_DATA[10]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P60	DRAM_DATA[11]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P61	DRAM_DATA[15]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P62	DRAM_DATA[14]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P63	DRAM_DATA[13]	PC3B03U	I/O	DRAM Data Inputs/Outputs
P64	DRAM_DATA[12]	PC3B03U	I/O	DRAM Data Inputs/Outputs

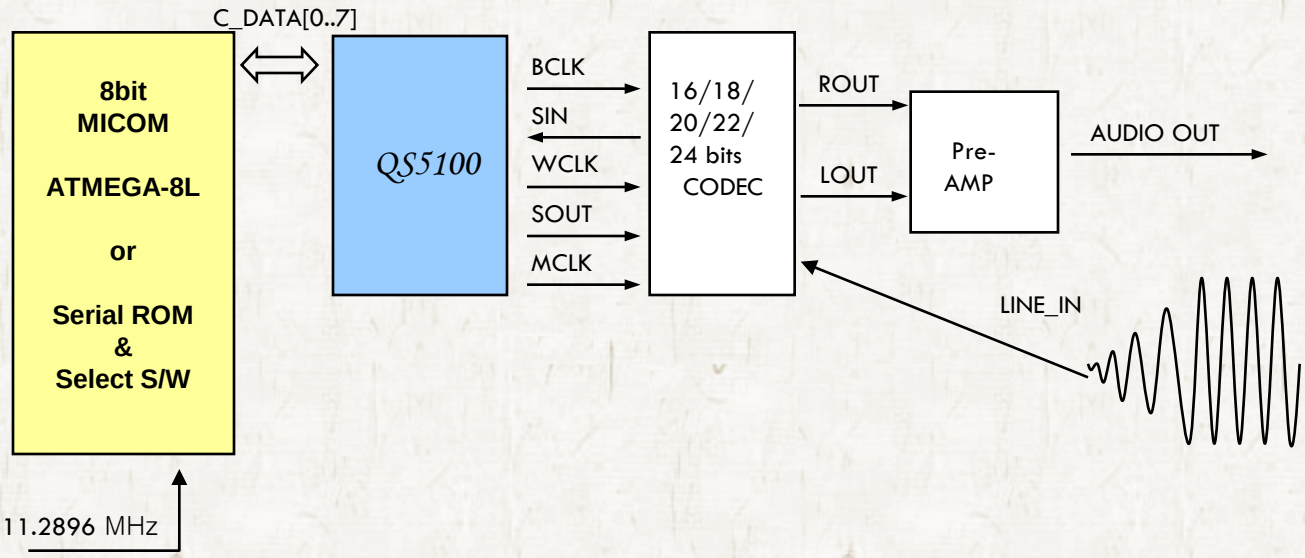
4. Block Diagram



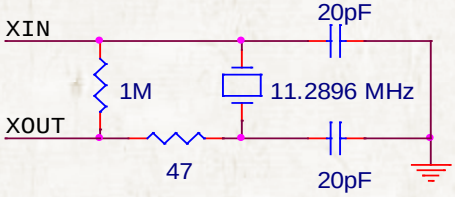
5. Application

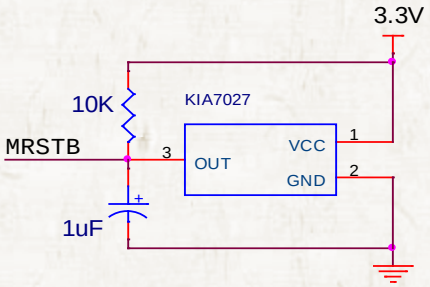
5-1. Typical Hardware Configuration

5-1-1. Using with CODEC Interface



5-2. Recommended System Reset Circuit and Clock circuit





* KIA7027 is Voltage Detector made by KEC

6. Electrical Characteristics

6-1. DC Characteristics

Absolute Maximum range

ITEMS	Symbol	Min	Max	Unit	Note
VDD terminal power supply voltage	**V**DD	2.7	3.6	V	
Operating ambient temperature	**T**AOP	-20	85	˚C	Industrial
Carrier temperature	**T**CA	-40	125	˚C	

Recommended operating condition

ITEMS	Symbol	Min	Max	Unit
VDD terminal power supply voltage	**V**DD	2.7	3.6	V
Digital input voltage	**V**IND	-0.3	VDD+0.3	V
Operating ambient temperature	**T**AOP	0	70	˚C
Carrier temperature	**T**ACA	-20	125	˚C

DC Characteristics

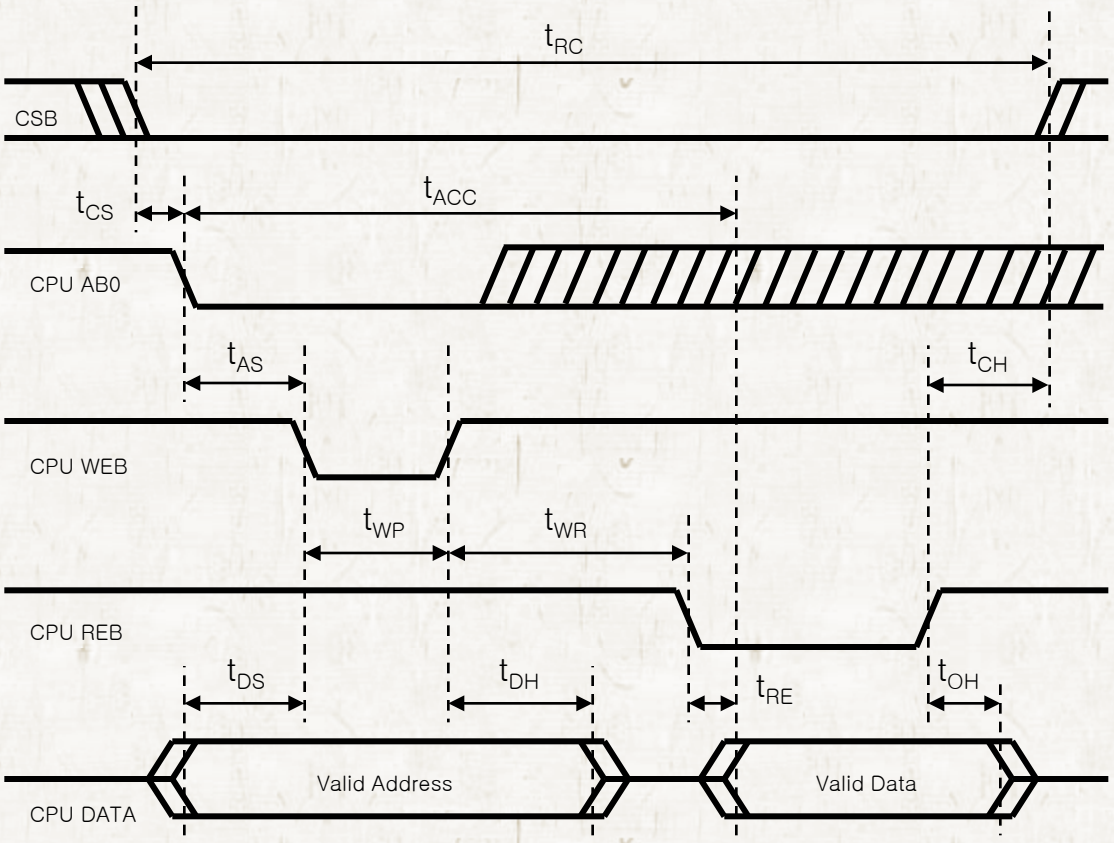
ITEMS	Symbol	Min	Typ	Max	Unit
INPUT Voltage “H” Level	**V**IH	VDD*0.7		VDD + 0.5V	V
INPUT Voltage “L” Level	**V**IL	-0.5V		VDD*0.3	V
OUTPUT Voltage “H” Level	**V**OH	VDD - 0.1V			V
OUTPUT Voltage “L” Level	**V**OL			VSS + 0.1V	V
Input Leakage current	**I**L		1	1000	uA
Input capacity	**C**I			10	pF

6-2. AC Characteristics

모든 Timing Condition은 내부 System Clock이 24MHz (출력 Sample Frequency는 48 KHz)로 동작한다고 가정하였다.

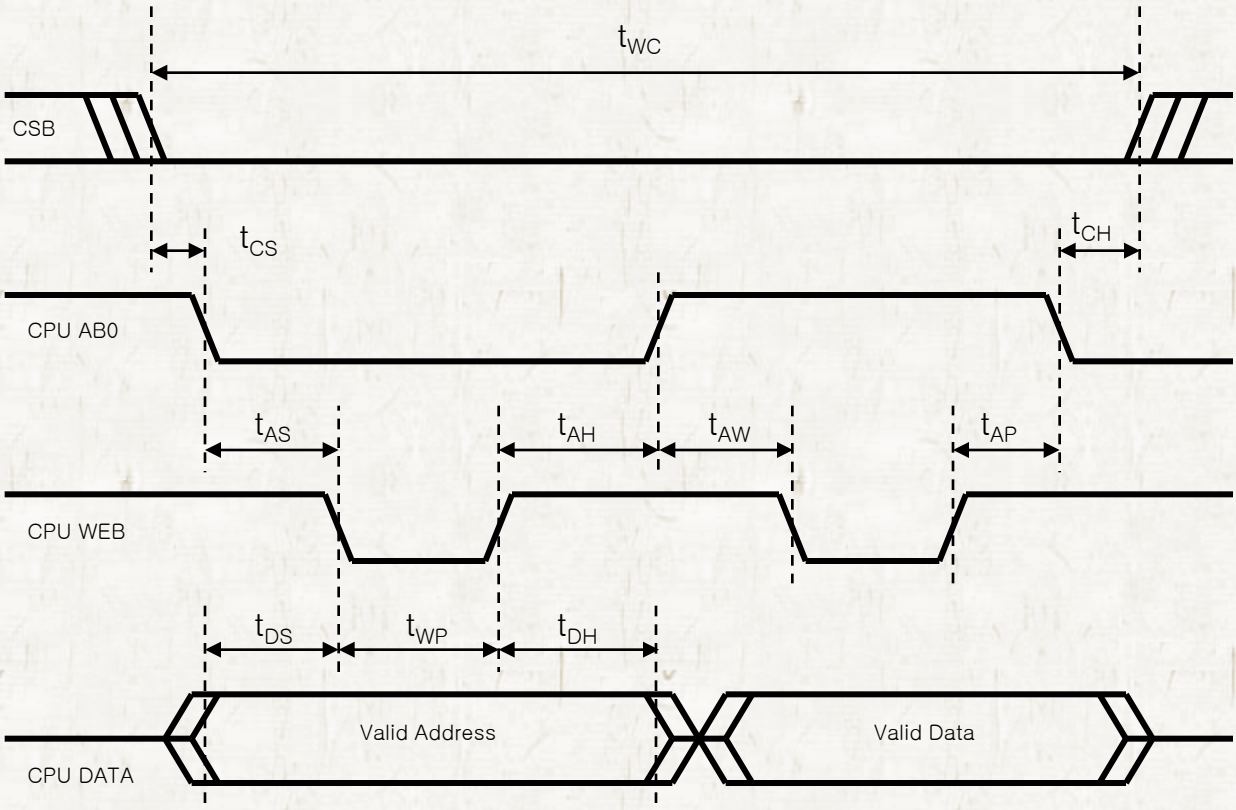
6-2-1. External CPU Interface Timing

6-2-1-1. READ Operation



ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Read Cycle Time	t_{RC}	136			ns
Access Time from AB0	t_{ACC}			113	ns
Chip Enable Setup Time	t_{CS}	0			ns
Chip Enable Hold Time	t_{CH}	0			ns
AB0 Setup Time	t_{AS}	0			ns
Write Pulse Width	t_{WP}	42			ns
Write Enable to Read Enable Delay	t_{WR}	85			ns
Data Setup Time	t_{DS}	5			ns
Data Hold Time	t_{DH}	0			ns
Read Enable to Data setup time	t_{RE}	5			ns
Hold Time from rising edge of CPU_RDB	t_{OH}	5			ns

6-2-1-2. WRITE Operation



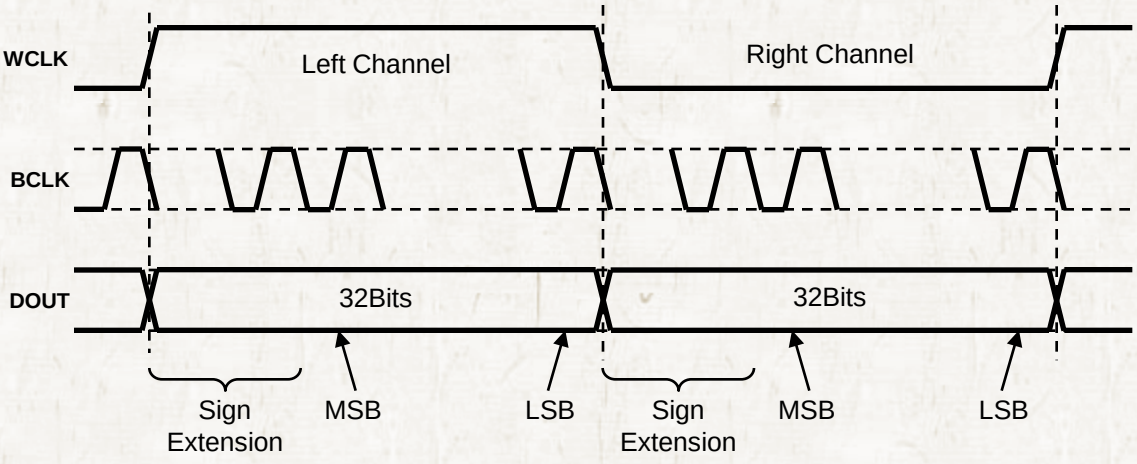
ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Write Cycle Time	t_{WC}	173			ns
Chip Enable Setup Time	t_{CS}	0			ns
Chip Enable Hold Time	t_{CH}	0			ns
AB0 Setup Time	t_{AS}	0			ns
AB0 Hold Time	t_{AH}	0			ns
Write Pulse Width	t_{WP}	42			ns
AB0 High to Write Enable Delay	t_{AW}	42			ns
AB0 Preset Time	t_{AP}	42			Ns
Data Setup Time	t_{DS}	5			ns
Data Hold Time	t_{DH}	0			ns

6-2-2. CODEC Interface Timing

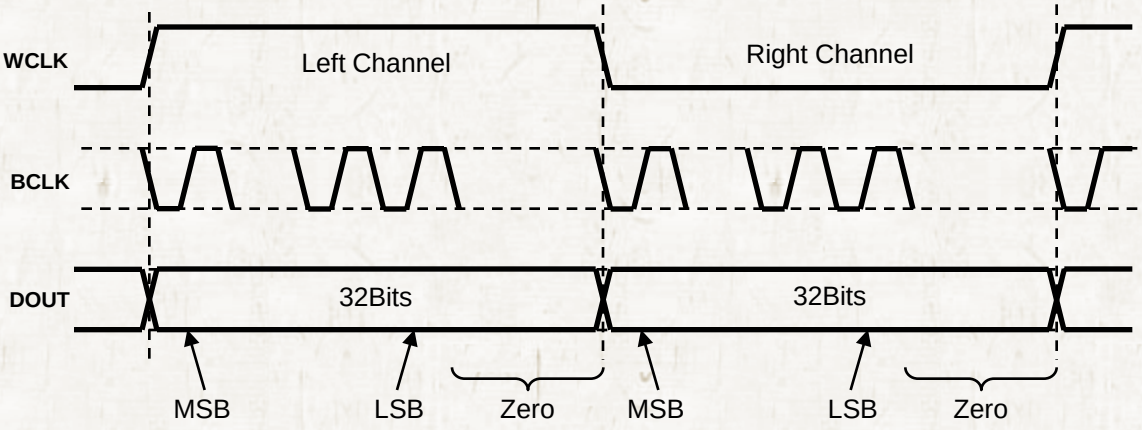
6-2-2-1. Clock Characteristics

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Left/Right Clock Input	WCLK	32		48	KHz
Bit Clock Input	BCLK	2.048		3.072	MHz

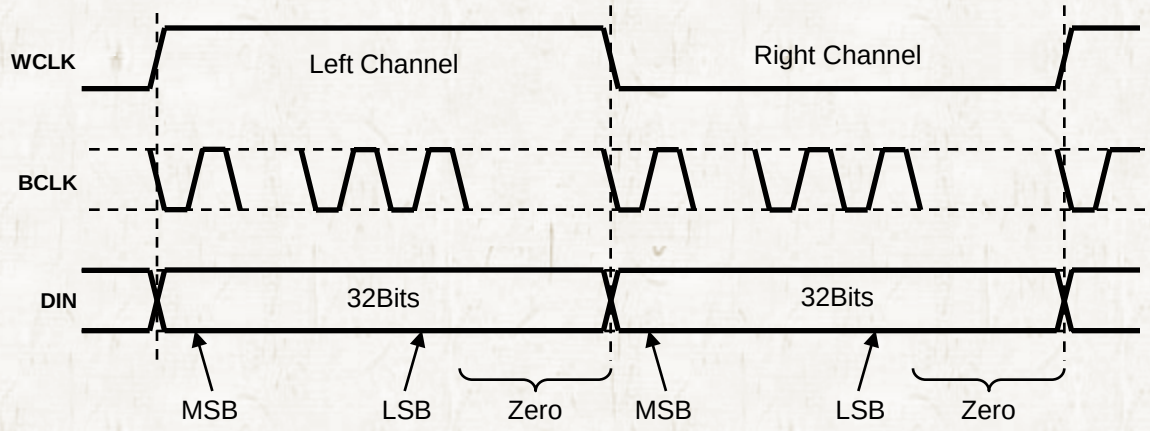
6-2-2-2. CODEC Interface Timing in Mode0 (DAC: MSB-First, Right Justified)



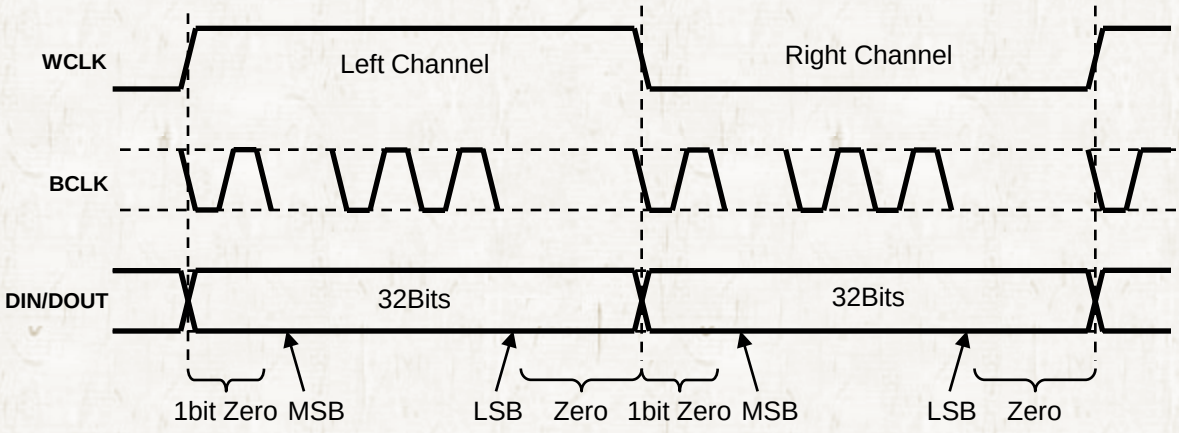
6-2-2-3. CODEC Interface Timing in Mode1 (DAC: MSB-First, Left Justified)



6-2-2-3. CODEC Interface Timing in Mode0/1 (ADC: MSB-First, Left Justified)



6-2-2-4. CODEC Interface Timing in Mode2 (DAC/ADC: MSB-First, I^2S)

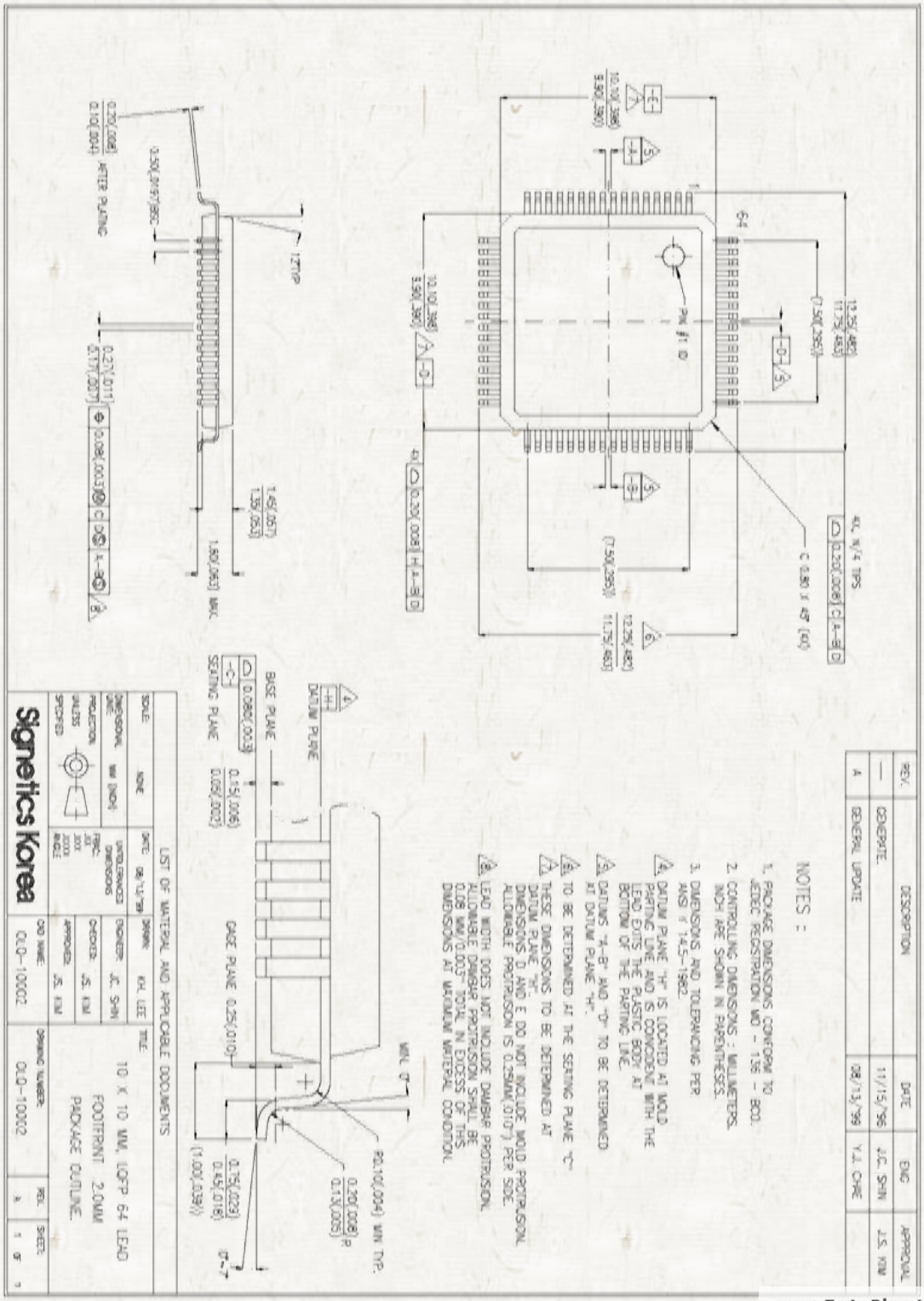


6-3. Power Consumption

Xin = 11.2896 MHz

Items	Symbol	3.0V	3.3V	Unit
Standby IDD & Operating	**ICC**ST/ **ICC**OP	45	50	mA
Power Down Mode	**ICC**PD	Max 10		uA

7. Package Dimension



A. APPENDIX

A-1. DFX Module Solution

A-1-1. DFX Module Overview

	DFX-MA4	DFX-MA16
Digital FX Presets	4 Presets	16 Presets
ADJUST Control	Rotary Linear Volume	Rotary Encoder, Gray Encoder
Level Control	FX Level, Reverb Level	
DSP arithmetic	24bit	
Ext.DRAM	MAX 256KWORD	
AD Converter	AK4554VT(AK)	
DA Converter		
S/N(A-weight)	90dB	
Dynamic range	90dB	
Frequency passband	20Hz ~ 20KHz	
Sampling Frequency	32 ~ 48KHz	
Max.Input voltage	1 Vrms (Normal 300mVrms)	
Max.Output voltage	1 Vrms	
Input Impedance	12KOhm	
Analog Input	Mono/Stereo	
Analog Output	Stereo	
Power Supply	DC 5V	
Power Consumption	160mA (DC IN = 9V,VDD =3.6V Fs = 48Khz)	

	1. Delay; Delay Time	1	Vibratone	9	Fast Chorus
	2. Chorus: Speed	2	Delay – 150ms	10	Deep Chorus
	3. Flange: Speed	3	Delay – 300ms	11	Chorus + Delay
	4. Reverb; Volume	4	Delay – 500ms	12	Chorus + Reverb
		5	Reverb – Room	13	Flange 1 (Fast)
		6	Reverb – Hall	14	Flange 2 (Slow)
		7	Reverb – Spring	15	Flange + Reverb
		8	Reverb + Delay2	16	Flange + Chorus + Delay + Reverb

Dimensions	50 x 45mm

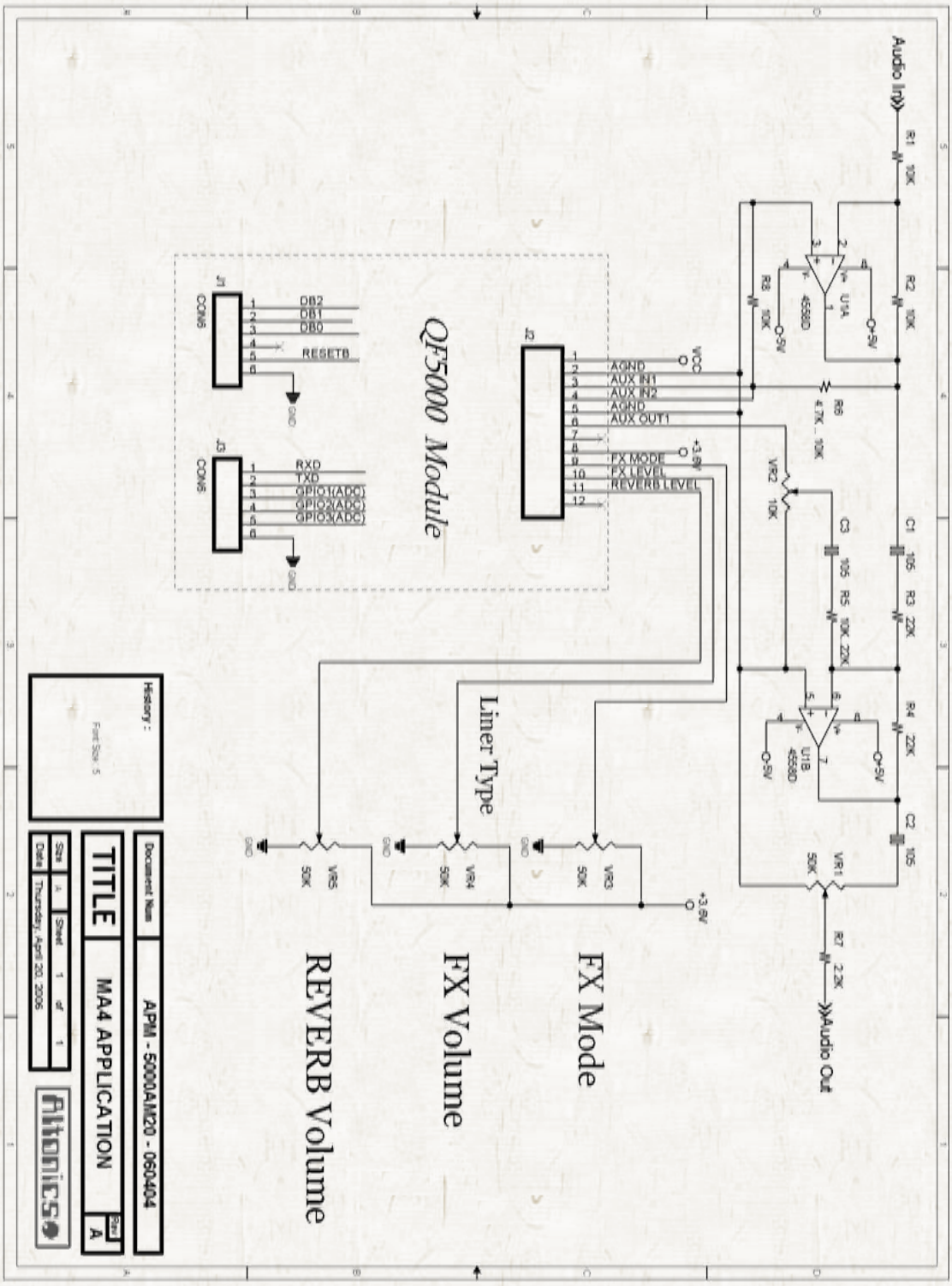
*A-1 preliminary rev 1.1 – module specs may change without notice!

A-1-2. Pin Descriptions

Part_Name/ Pin_No		PIN NAME	MA4 FUNCTION	MA16 FUNCTION
J2	PIN1	VCC + 5V	+5V POWER SUPPLY	←
	PIN2	AGND	ANALOG GROUND	←
	PIN3	AUX IN1	AUDIO INPUT,SINGLE ENDED MODE	←
	PIN4	AUX IN2	AUDIO INPUT,SINGLE ENDED MODE	←
	PIN5	AGND	ANALOG GROUND	←
	PIN6	AUX OUT1	AUDIO OUTPUT,SINGLE ENDED MODE	←
	PIN7	AUX OUT1	AUDIO OUTPUT,SINGLE ENDED MODE	←
	PIN8	3.6VREF	CONTROL PORT REFERENCE VOLTAGE OUT, 3.6V	←
	PIN9	FX MODE	FX MODE CONTROL	←
	PIN10	FX LEVEL	FX VOLUME	←
	PIN11	REV LEVEL	REVERB LEVEL	N.C (Control Port /ADC IN)
	PIN12	N.C		
J1	PIN1	SCK	SPI BUS MASTER CLOCK INPUT	
	PIN2	MISO	SPI BUS MASTER INPUT	
	PIN3	MOSI	SPI BUS MASTER OUTPUT	
	PIN4	NC		
	PIN5	RESETB	SPI RESET	
	PIN6	GND	Ground	
J3	PIN1	GPIO5/RXD	Reserve Control Port/USART INPUT	
	PIN2	GPIO6/TXD	Reserve Control Port/USART OUTPUT	
	PIN3	GPIO7/ADC_IN6	Reserve Control Port/ADC IN	
	PIN4	GPIO8/ADC_IN7	Reserve Control Port/ADC IN	
	PIN5	GPIO9/ADC_IN8	Reserve Control Port/ADC IN	
	PIN6	GND	Ground	

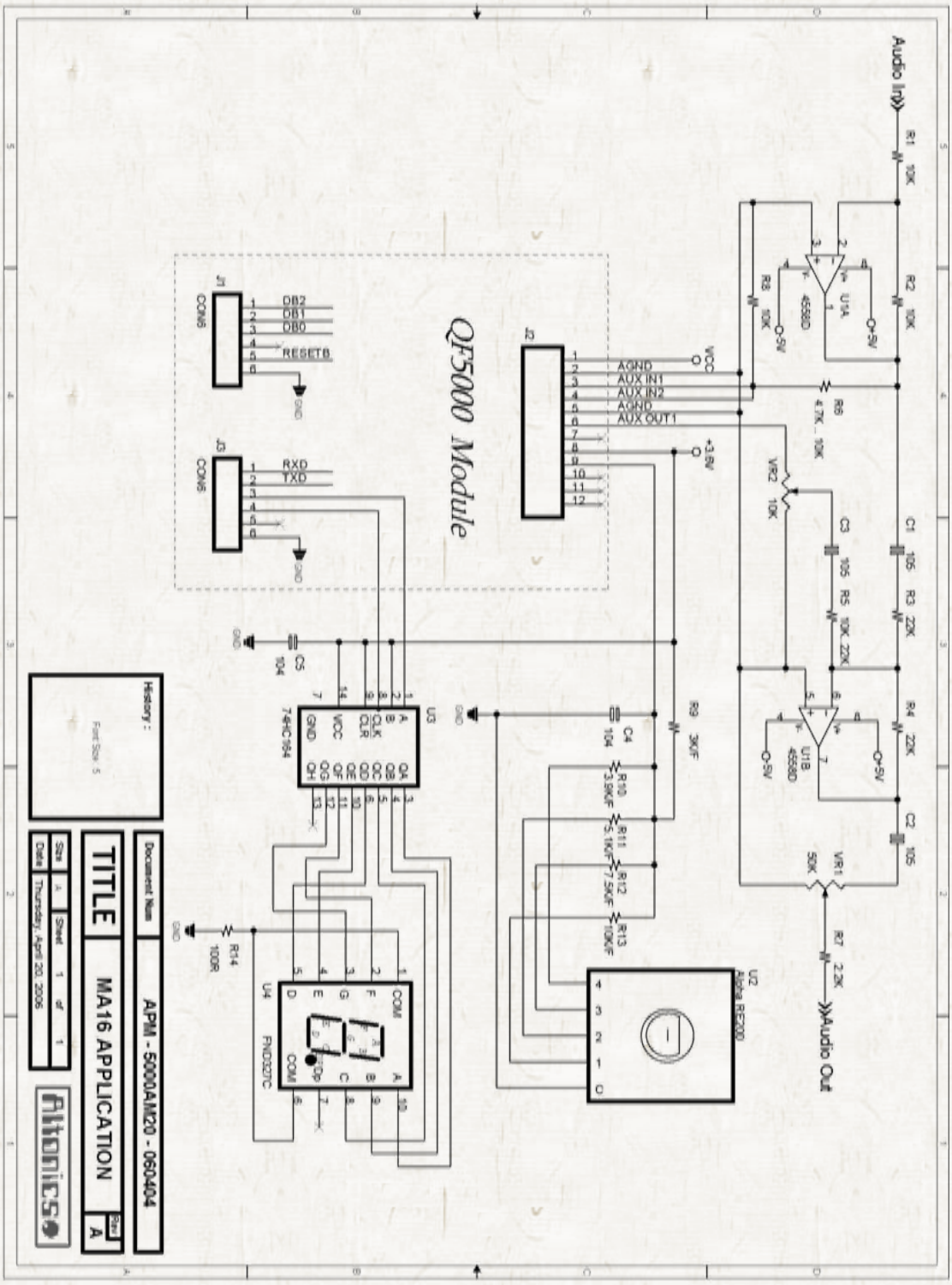
*A-1-2 preliminary rev 1.1 – module specs may change without notice!

A-1-3 DFX Module Application Schematic (DFX MA4 Type)



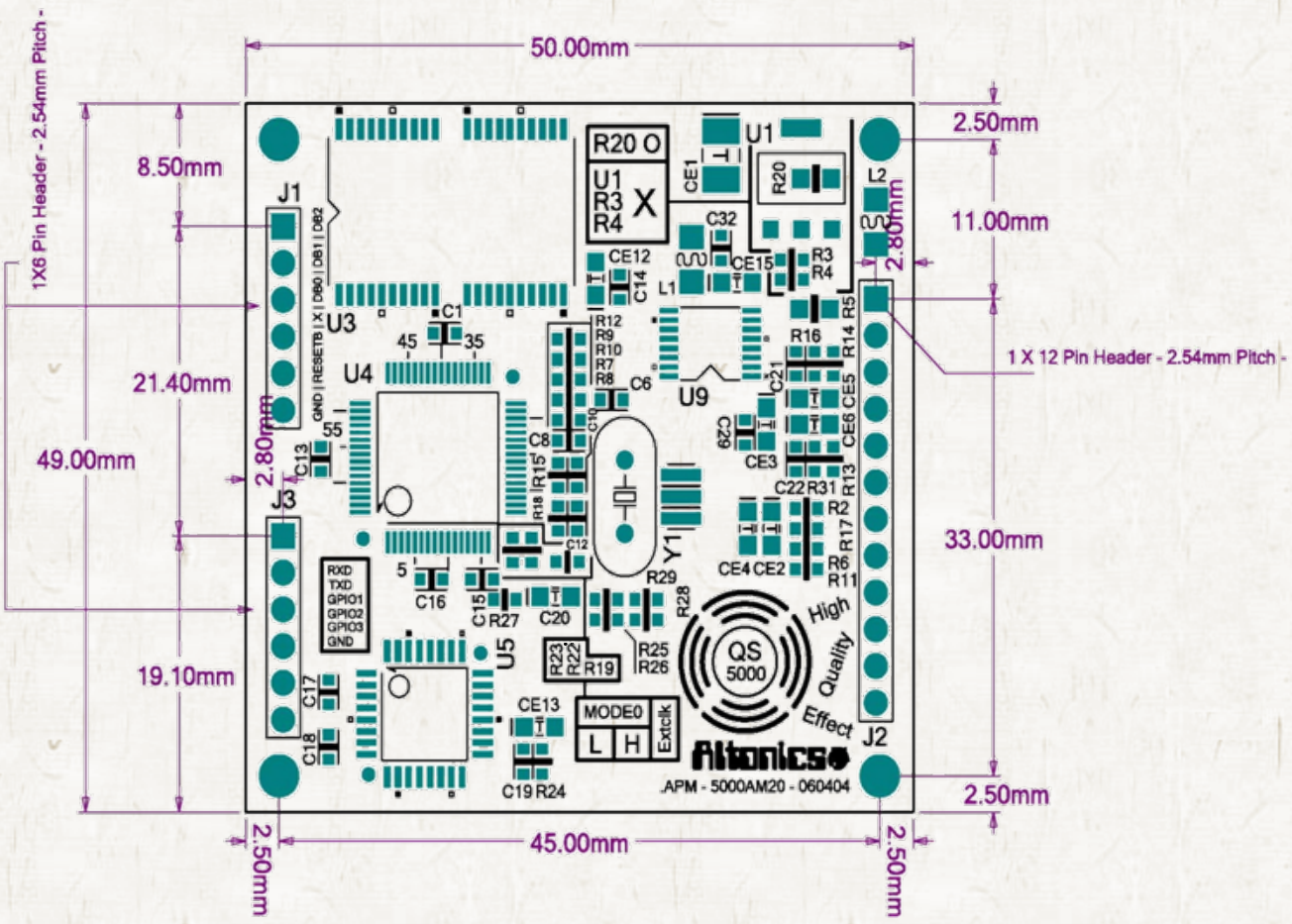
*A-1-3 preliminary rev 1.1 – module specs may change without notice!

A-1-4 DFX Module Application Schematic (DFX MA16 Type)



*A-1-4 preliminary rev 1.1 – module specs may change without notice!

A-1-5 MA16 Module Dimension



A-2. Revision History

Date	Description
2005/8/15	First edition
2006/3/6	Rev 1.1: Appendix A-1
2006/4/13	Changed 6-3 and Added to A-1-5 MA16 module dimension (Ver 1.2)