QT117L QProx™ IC OVERVIEW

The QT117L is is designed to output raw data over a master-mode SPI port. The SPI port allows a host MCU to separately process signal data without any pre-processing by the QT117L. The data is 16-bits; actual binary values depend on both signal load (Cx) and sampling capacitor value (Cs); As Cx rises, the SPI signal value will *drop*. As Cs rises, the SPI signal will also rise.

The pinouts of the device are as follows:

PIN	FUNCTION
1	Vcc: +3 to +5
2	SPI Data
3	SPI Clock
4	Sync
5	SPI Frame
6	SNS1
7	SNS2
8	Gnd

SPI DATA The SPI port outputs 16 bit data, and sends the MSB first. The bitfields are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

S0..S15 S0..S15 are signal bits which can have a value from 0 to 0xffff (in unsigned binary). *The less signal from an object, the higher this value will be*. Data is proportional to burst length which is inversely proportional to capacitance. Further, the signal exhibits a logarithmic response: For every doubling of Cx, the signal decreases by approximately 50%. The SPI output value is not compensated for drift.

SPI Clock The SPI clock has 16 positive-going clock edges that should be used to clock the serial data into a shift register. The data is valid before and after the rising edge of Clock, so the receiving SPI port should be set for 'positive edge clocking'. If a standard CMOS or TTL shift register is used, the shift register clock input should trigger on rising edges.

SPI Frame Frame is a negative-going signal that brackets or 'frames' the SPI datastream. The first, falling edge occurs before any data is shifted out or clocked. The second, rising edge of Frame can be used to latch the serial data into a parallel latch, or trigger an interrupt in a host device. Frame is required in SPI systems that need an enable line. In some systems Frame is referred to as /SS (Slave Select).

SPI Timing: Timing of all signals is 50us from any edge to any other edge among the 3 SPI signals. The Frame signal falls 100us ahead of the first Data bit shifted out, or 150us ahead of the first rising edge of Clock. Frame rises again 100us after Clock terminally falls to zero on bit S15, or 150us after the last rising edge of Clock.

Sync: If this pin is tied high, the part will repeatedly acquire and send SPI data every 70-100ms. If this pin is held low, the part is kept in a quiescent mode and consumes only a few microamps. When the line is raised high again, the part immediately acquires and then sends out the result of the acquire via the SPI lines. This line can be used to sync the device to a master, permitting arbitrary acquire rates. Further, the Frame line can be used to daisy-chain sync pulses to additional QT117L's. Daisy-chaining prevents devices from

bursting at the same time, thus preventing cross interference effects if the electrodes are close together.

The device goes into low-power quiescent mode automatically after the SPI is sent out regardless of the state of the Sync pin, until the next burst. A negative-going pulse on the pin will bring the part out of quiescence on the rising edge of the pulse.

SPI During Quiescent State: During quiescence all 3 SPI lines are held in a 3-state mode. This happens about 50us after Frame goes high following an SPI transmission. This allows multiple QT117L's to coexist on the same SPI bus, with a master MCU coordinating the activities of the slave QT117L's. This operation also works if several devices are daisy-chained together using the Frame and Sync lines, thus requiring only a single master pulse to initiate the entire chain via the first device in the chain.

SNS1, SNS2 These are the signal sampling pins. Connect the Cs capacitor across them. The signal lead is normally connected to SNS2.

The QT117L is a derivative of the QT110 and QT113. Please refer to the QT110 and QT11x datasheets for additional information.