奇美電子 CHIMEI INNOLUX

PRODUCT SPECIFICATION

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: R196U2
SUFFIX: L02

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

核准時間	部門	審核	角色	投票
2011-01-25 11:38:08	APPL 產品管理處	yuhsiang.chang (張喻翔)	Director	Accept

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REVISION HISTORY

Version	Date	Section	Description
Ver 0.0	May, 05, '09	All	R196U2 -L02 Specification was first issued.
Ver 1.0	Oct, 21. '09	All	Update
Ver.1.1	May, 16. '10	3.2	Lamp current, 5.3mA changed to 4.2mA
		3.3	Inverter Electrical Characteristic modified
		7.1	Modify min. value of center luminance of white, 700nits changed to 600nits
			Modify min. value of contrast ratio 600:1 change to 560:1
			Modify response time value
		7.2	Remove Image Retention Spec.
	Jun, 1. '10	2.2.1	Modify the max. spec of the Power Supply Voltage, 16.5 changed to 14.4
			Modify the max. spec of the Logic Input Voltage, 4.3 changed to 4
		3.1.1	Vcc Power Dip Condition modify the VCC to 12
		6.1	Modify the max. spec of the LVDS clock frequency, 97.63 changed to 85.1
			Modify the min. spec of the LVDS clock period, 10.24 changed to 11.7
Ver. 2.0	July 10,'10	ALL	Approval Specification was first issued.
Ver. 2.1	Jan.18,'11	7.1	Modify the Optical Specification

1. GENERAL DESCRIPTION

1.1 OVERVIEW

R196U2 -L02 is a 19.6" TFT Liquid Crystal Display module with 16 CCFL Backlight unit and two port 20 pins 2ch-LVDS interface. This module supports 1600 x 1200 UXGA screen and can display 16.7M colors driven by 8bit drivers. The LCD module includes built-in inverter for Backlight.

1.2 FEATURES

- This specification applies to the 19.6" Color TFT LCD Module.
- This module includes an inverter card for the backlight.
- The screen format is intended to support UXGA 1600(H) x 1200(V) resolution.
- Supported colors are native 16M (8-bits data per R, G, B each).
- All input signals are LVDS (Low Voltage Differential Signaling) interface.
- The contrast was enhanced to enable gray scale application

1.3 APPLICATION

-This module is design for a TFT LCD Monitor style display unit.

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	398.4 (H) x 298.8 (V) (19.6" diagonal)	mm	(1)
Bezel Opening Area	402.4 (H) x 302.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1600 x R.G.B. x 1200	pixel	-
Pixel Pitch	0.249 (H) x 0.249 (V)	mm	-
Pixel Arrangement	RGB vertical stripe (at landscape position)	-	-
Display Colors	16.7M (8-bits data per R, G, B each)	color	-
Transmissive Mode	Normally Black		
Surface Treatment	Hard coating (3H), Anti-glare (Haze 25)	-	-
Module Power Consumption	66	Watt	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	426.5	427	427.5	mm	(1)
	Vertical(V)	321.9	322.4	322.9	mm	
	Depth(D)	-	37.8	38.3	mm	
Weight		-	1940	1990	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1)
Shock (Non-Operating)	S_{NOP}	-	50	G	(2), (4)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(3), (4)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

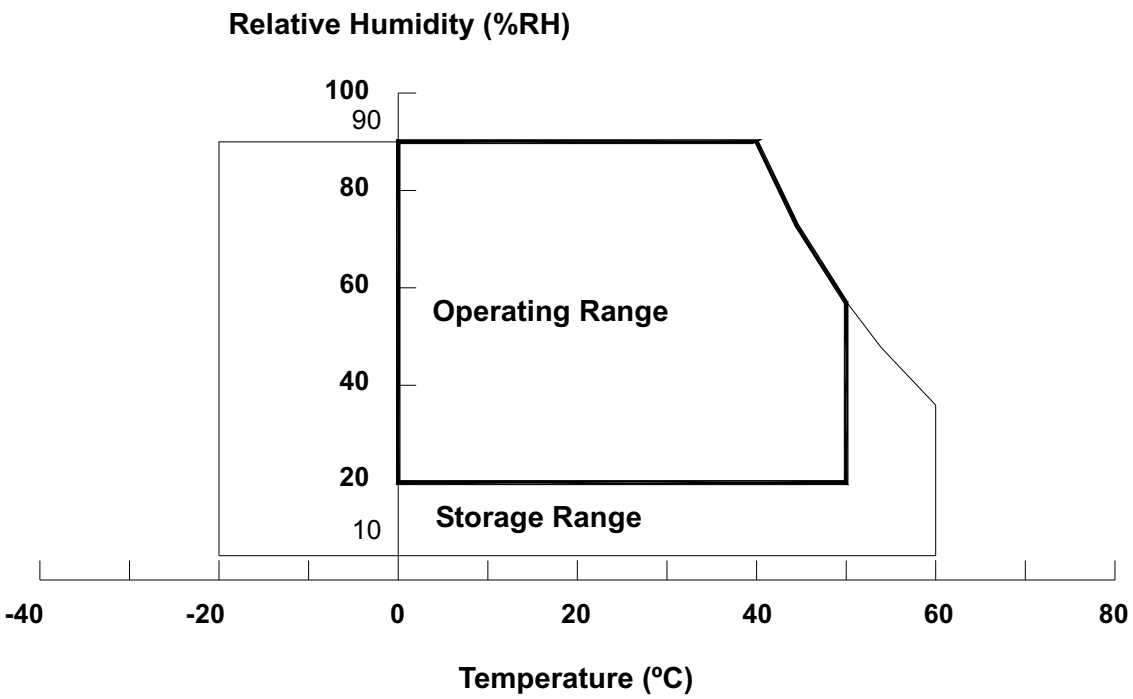
(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) 11ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (3) 10 ~ 200 Hz, 30min/cycle, 1 cycles each X, Y, Z.

Note (4) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	+14.4	V	(1)
Logic Input Voltage	V_{logic}	-0.3	+4	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Brightness control	VDIM	-0.3	+5.3	V	(1)
Backlight on signal	BLON.IN	-0.3	+5.3	V	
Power Supply Voltage	V_{in}	0	15	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

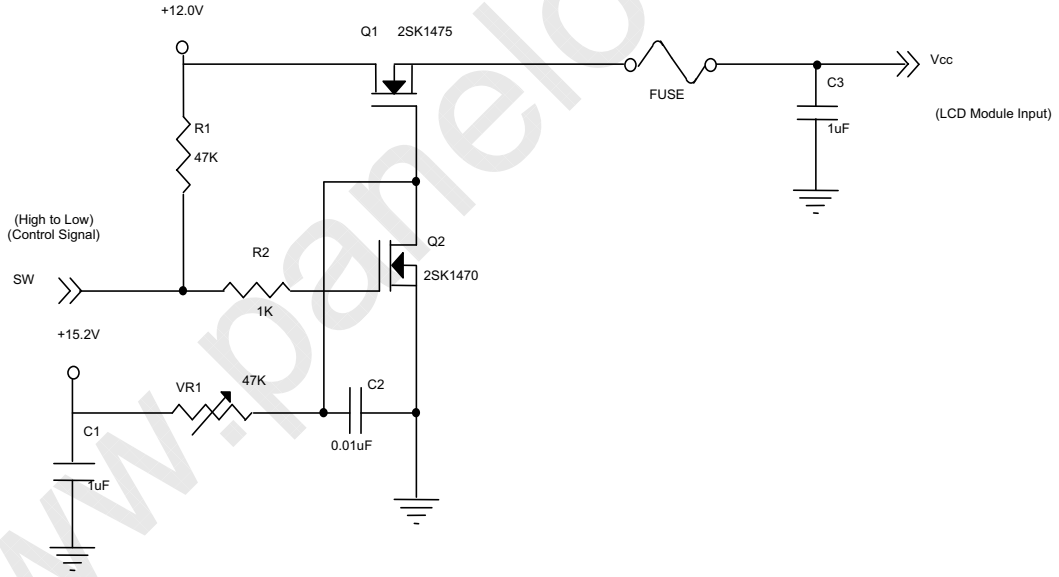
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

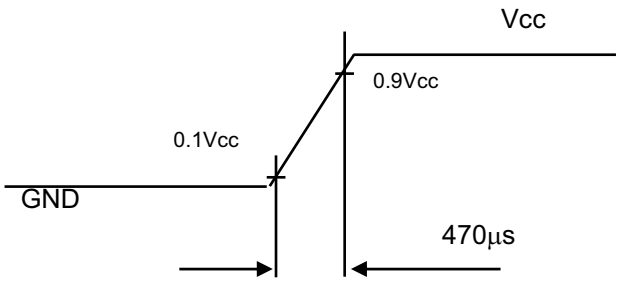
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	11.4	12.0	12.6	V	-
Ripple Voltage		V_{RP}	-	-	300	mV	-
Rush Current		I_{RUSH}	-	-	3.8	A	(2)
Power Supply Current	White	-	-	510	612	mA	(3)a
	Black	-	-	270	324	mA	(3)b
	Vertical Stripe	-	-	460	552	mA	(3)c
Power Consumption		P_{LCD}	-	6.12	7.71	watt	(4)
Magnitude LVDS differential input voltage		|Vid|	100	-	600	mV	
LVDS common input voltage		Vic	1.0	1.2	1.4	V	
Logic high input voltage		V_{IH}	2.64	-	-	V	
Logic low input voltage		V_{IL}	-	-	0.66	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:

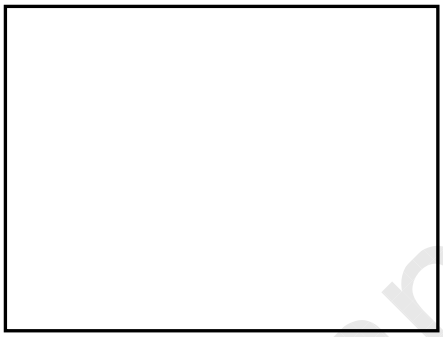


Vcc rising time is 470μs



Note (3) The specified power supply current is under the conditions at Vcc = 12.0 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

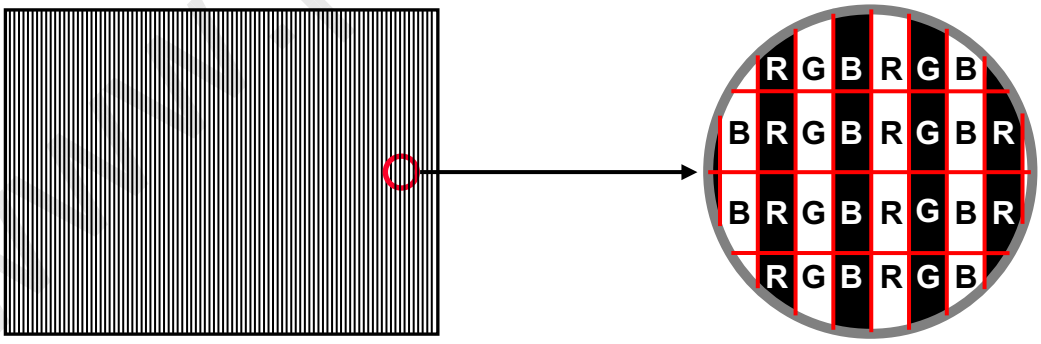


Active Area

b. Black Pattern

Active Area

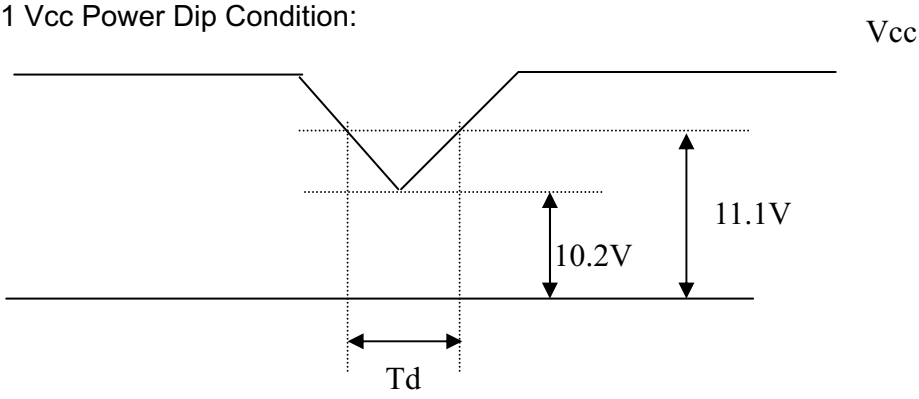
c. Vertical Stripe Pattern



Active Area

Note(4) The power consumption is specified at the pattern with the maximum current.

3.1.1 Vcc Power Dip Condition:



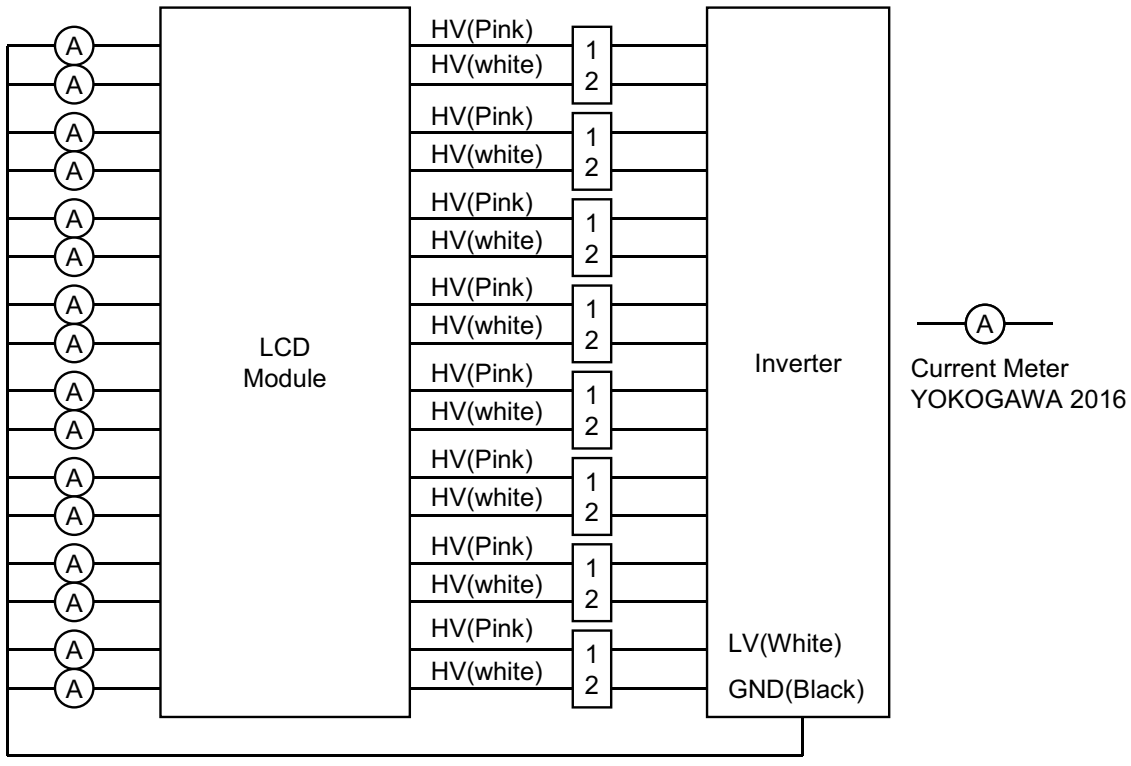
Dip condition: $10.2V \le Vcc \le 11.1V, Td \le 20ms$

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	---	740	---	V_{RMS}	
Lamp Current	I_L	---	4.2	---	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	---	---	1470 (25 °C)	V_{RMS}	(2)
		---	---	1570 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	40		80	KHz	(3)
Lamp Life Time	L_{BL}	50,000	---	---	Hrs	(5)

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L \times$ 16 CCFLs

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 5.3 mArms until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

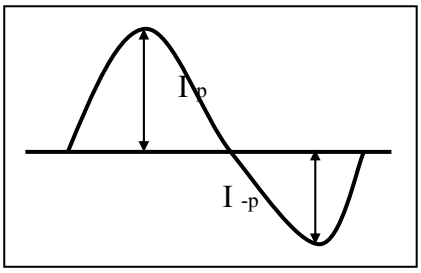
The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within $\sqrt{2}$ ± 10%;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

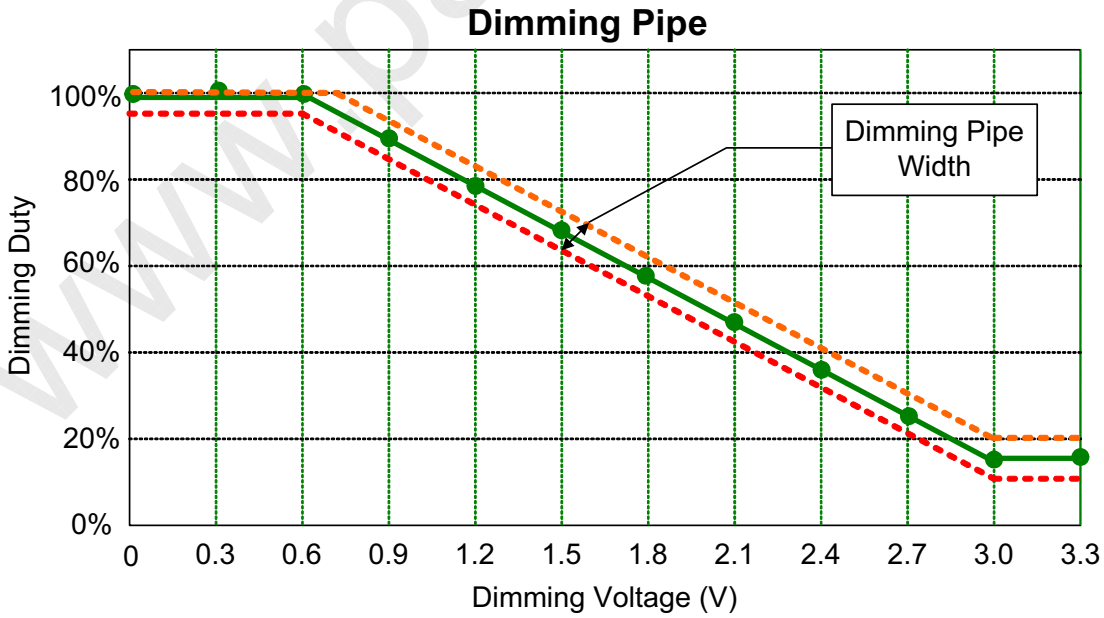
I_p (or I_{-p}) / I_{rms}

3.3 Inverter Electrical characteristic

Item	Symbol	Description	Min.	Typ.	Max.	Unit
1	V_{cc}	Inverter Input voltage	11.4	12	12.6	V
2	I_{in}	Inverter Input current (@V_{in}=12V)	---	5	---	A
3	P_{in}	Inverter Input power consumption	---	60		W
4	BLON	Input Backlight On/Off control: OFF	0	---	0.8	V
		Input Backlight On/Off control: ON	2	3.3	6	V
5	VDIM	Input Internal Brightness Control VDIM: 0V, maximum brightness VDIM: 3V, minimum brightness	0	---	3	V
6	F_b	Burst Mode Frequency	150	160	170	Hz
7	Freq.	Operating frequency	47	50	53	KHz
8	I_{out}	Output current, VDIM=0V	3.7	4.2	4.7	mA
		Output current, VDIM=3.3V (See item 6.2.7)	15	17.5	20	%

3.4 Backlight Dimming Range vs VDIM voltage

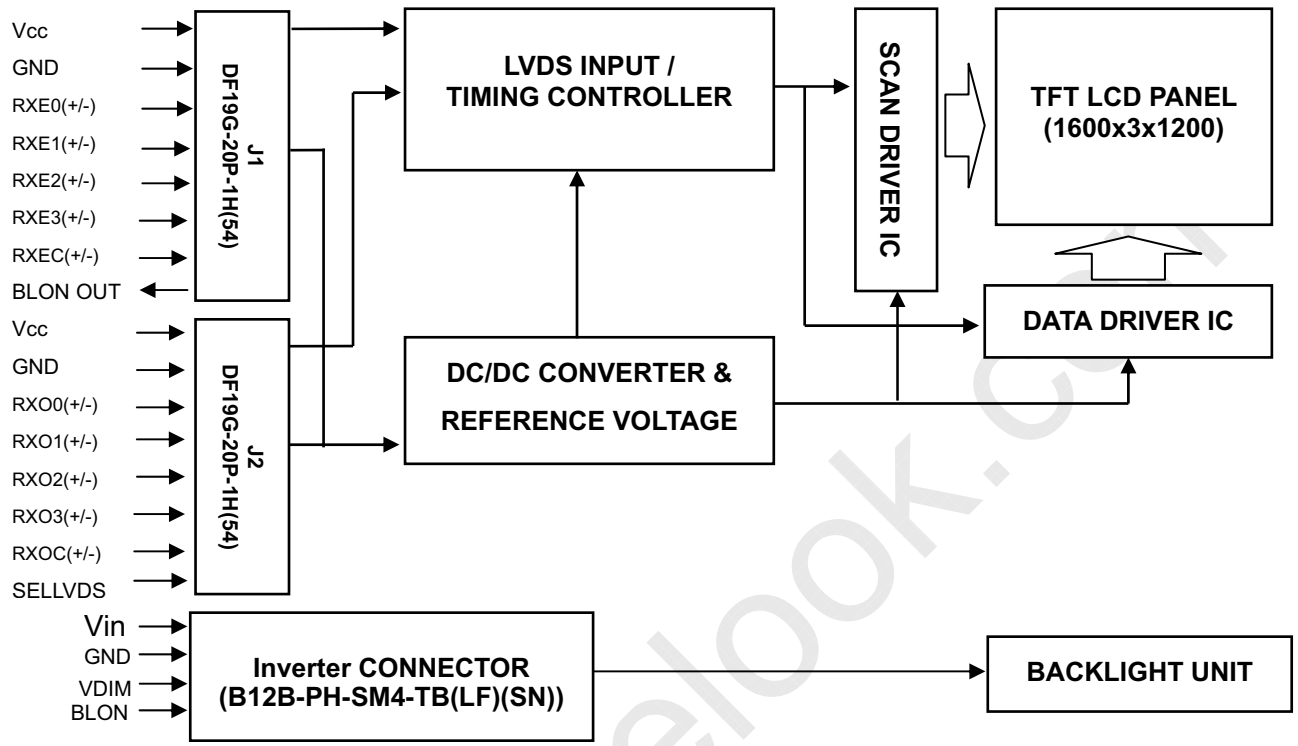
The following indicates the Dimming range vs VDIM voltage



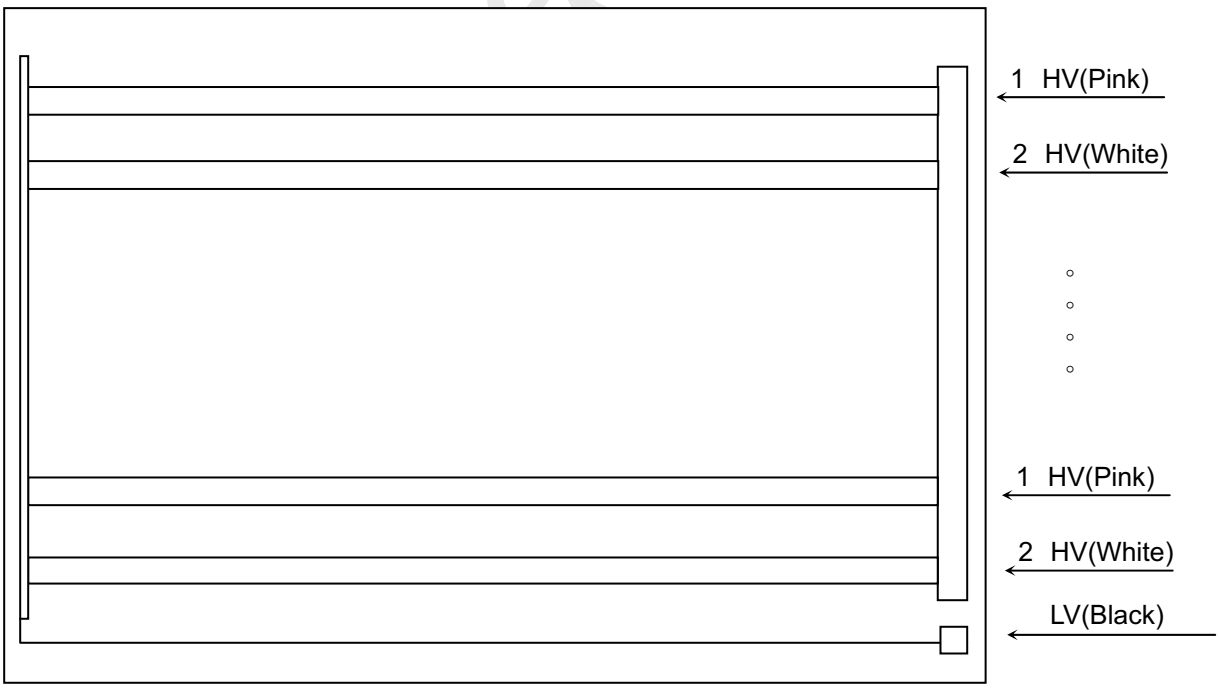
Note (1): This curve depends on the temperature and total running time of the backlight

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 LVDS Input Signal

J1(Master) : Right side(Front View)

Signal Description (J1)

Pin	Name	Description
1	VCC	+12.0V power supply
2	VCC	+12.0V power supply
3	GND	Ground
4	GND	Ground
5	RXE0-	Negative LVDS differential data input. Channel E0 (even)
6	RXE0+	Positive LVDS differential data input. Channel E0 (even)
7	GND	Ground
8	RXE1-	Negative LVDS differential data input. Channel E1 (even)
9	RXE1+	Positive LVDS differential data input. Channel E1 (even)
10	GND	Ground
11	RXE2-	Negative LVDS differential data input. Channel E2 (even)
12	RXE2+	Positive LVDS differential data input. Channel E2 (even)
13	GND	Ground
14	RXEC-	Negative LVDS differential clock input. (even)
15	RXEC+	Positive LVDS differential clock input. (even)
16	GND	Ground
17	RXE3-	Negative LVDS differential data input. Channel E3 (even)
18	RXE3+	Positive LVDS differential data input. Channel E3 (even)
19	GND	Ground
20	BLON OUT	Back-Light ON signal. 3.3V CMOS Output. This signal turns high at 50-80 ms after VCC applied.

J2(Slave) : Left side(Front View)

Signal Description (J2)

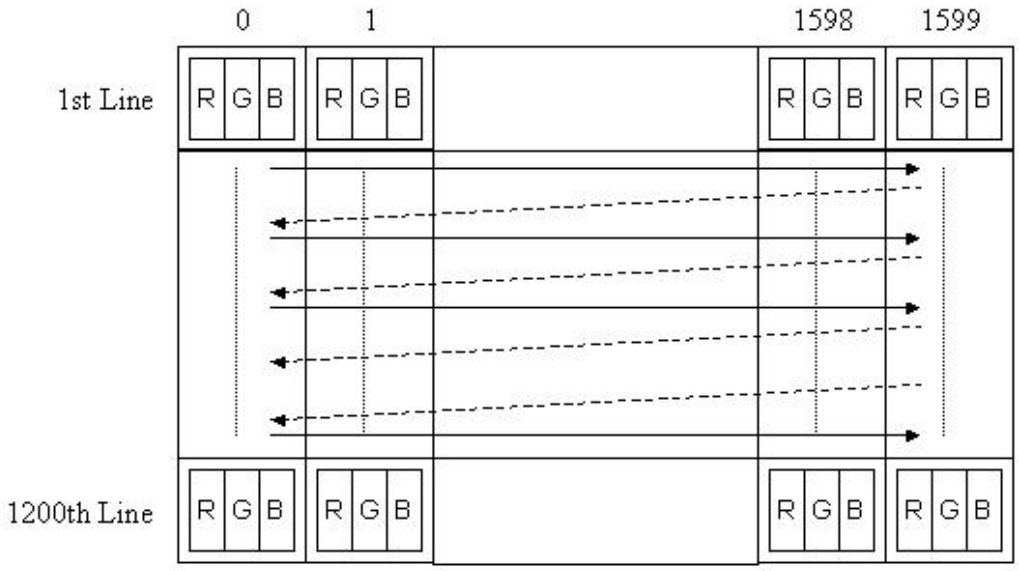
Pin	Name	Description
1	VCC	+12.0V power supply
2	VCC	+12.0V power supply
3	GND	Ground
4	GND	Ground
5	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
6	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
7	GND	Ground
8	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
9	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
10	GND	Ground
11	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
12	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
13	GND	Ground
14	RXOC-	Negative LVDS differential clock input. (odd)
15	RXOC+	Positive LVDS differential clock input. (odd)
16	GND	Ground
17	RXO3-	Negative LVDS differential data input. Channel O3 (odd)
18	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
19	GND	Ground
20	SELLVDS	Tie to GND:VESA Mode; Tie to 3.3V :JEITA Mode

Note (1) Connector Part No.: DF19G-20P-1H (54) or equivalent.

Note (2) The first pixel is even

Note (3) Input signal of even and odd clock should be the same timing.

Note (4) The module uses a 100-ohm resistor between positive and negative data lines of each receiver input.



5.2 LVDS Input Data Order

5.2.1 VESA mode

LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6

5.2.2 JEITA mode

LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG2	ER7	ER6	ER5	ER4	ER3	ER2
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB3	EB2	EG7	EG6	EG5	EG4	EG3
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB7	EB6	EB5	EB4
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB1	EB0	EG1	EG0	ER1	ER0
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG2	OR7	OR6	OR5	OR4	OR3	OR2
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB3	OB2	OG7	OG6	OG5	OG4	OG3
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB7	OB6	OB5	OB4
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB1	OB0	OG1	OG0	OR1	OR0

-5.3 Inverter Input Signal (1)

Pin No.	Symbol	Description
1	Vin	Inverter voltage
2	Vin	Inverter voltage
3	Vin	Inverter voltage
4	Vin	Inverter voltage
5	Vin	Inverter voltage
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	VDIM	Brightness control (0~3V)
12	BLON	Inverter On/Off control (0/3.3V)

Note (1) Connector Part No.: B12B-PH-SM4-TB(LF)(SN) (JST) or equivalent

Note (2) User's connector Part No.: PHR-12 (JST)

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

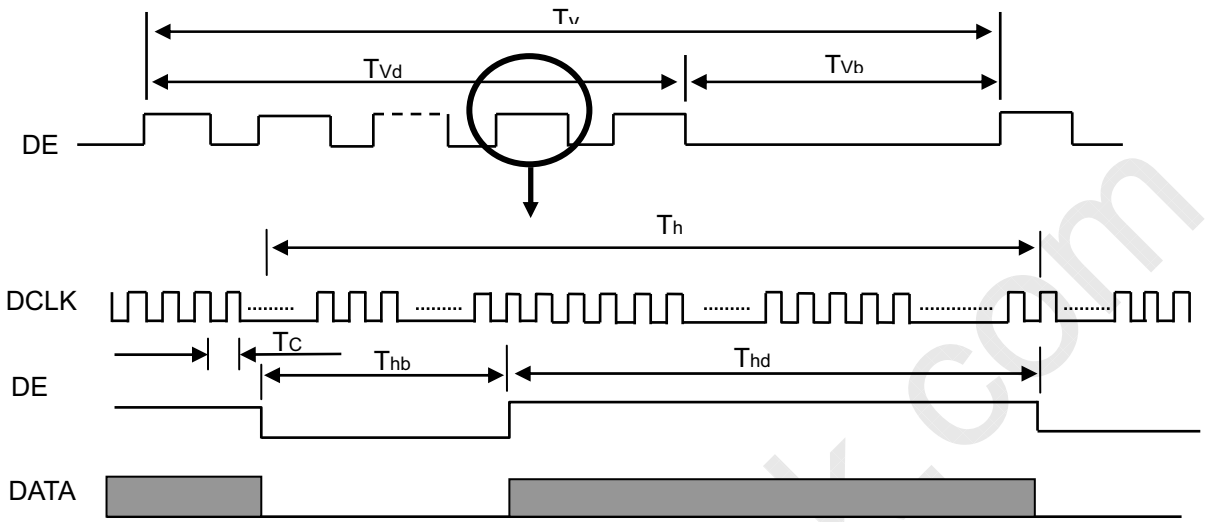
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

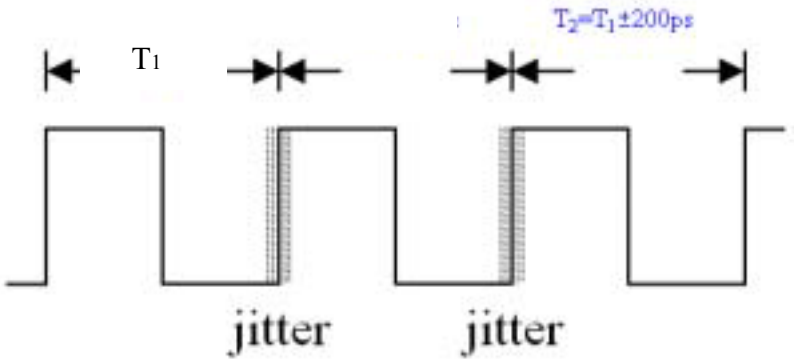
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	62.3	81	85.1	MHz	-
	Period	Tc	11.7	12.35	16.05	ns	
	Input cycle to cycle jitter	T_{rcl}	---	---	200	ps	(1)
	Spread spectrum modulation range	F_{clkin_mod}	---	---	1.02*Fc	MHz	(2)
	Spread spectrum modulation frequency	F_{SSM}	---	---	200	KHz	
	High Time	Tch	-	4/7	-	Tc	-
	Low Time	Tcl	-	3/7	-	Tc	-
LVDS Data	Setup Time	Tlvs	600	-	-	ps	(3)
	Hold Time	Tlvh	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr	-	60	-	Hz	Tv=Tvd+Tvb
	Total	Tv	1208	1250	1440	Th	-
	Display	Tvd	1200	1200	1200	Th	-
	Blank	Tvb	Tv-Tvd	50	Tv-Tvd	Th	-
Horizontal Active Display Term	Total	Th	860	1080	1130	Tc	Th=Thd+Thb (4)
	Display	Thd	800	800	800	Tc	-
	Blank	Thb	Th-Thd	280	Th-Thd	Tc	-

Note: Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

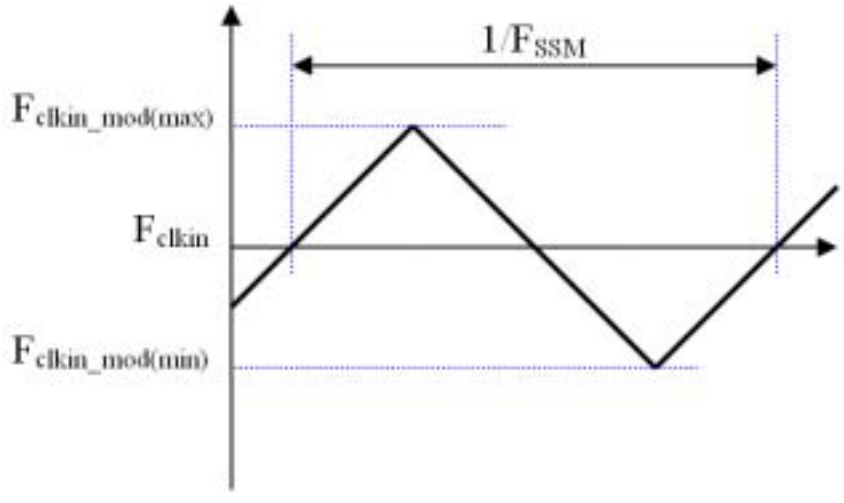
INPUT SIGNAL TIMING DIAGRAM



Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

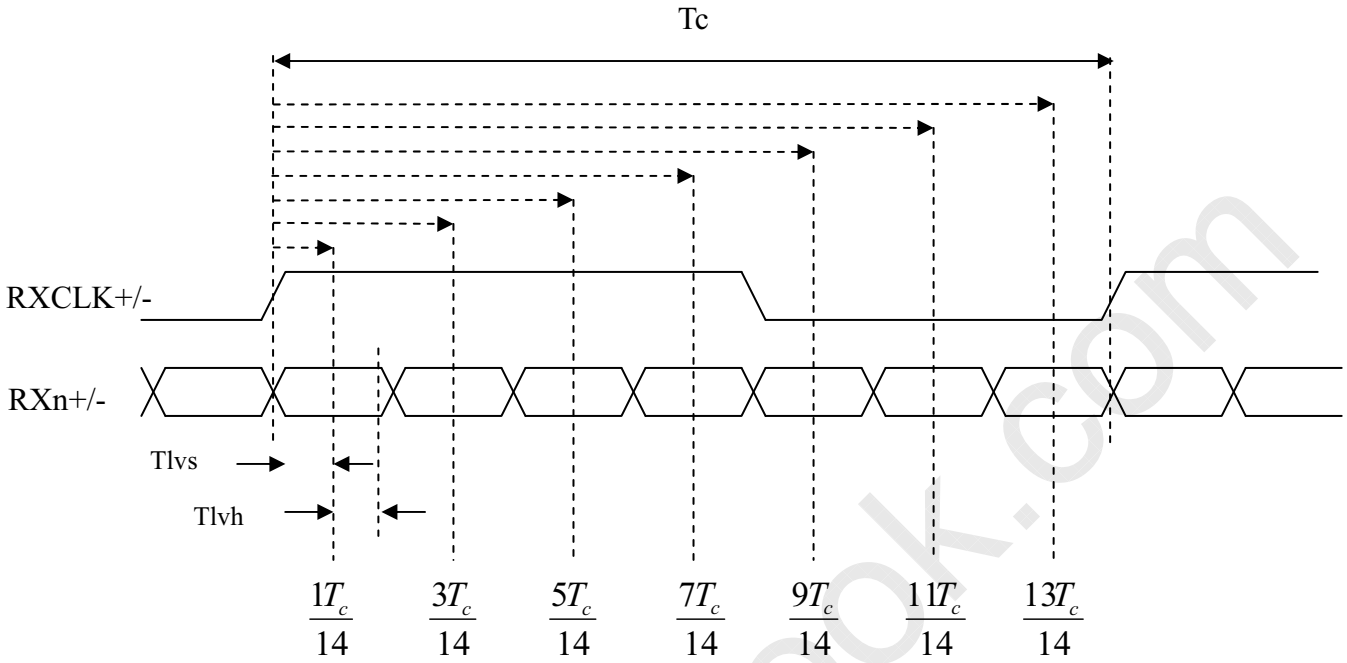


Note (2) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (3) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

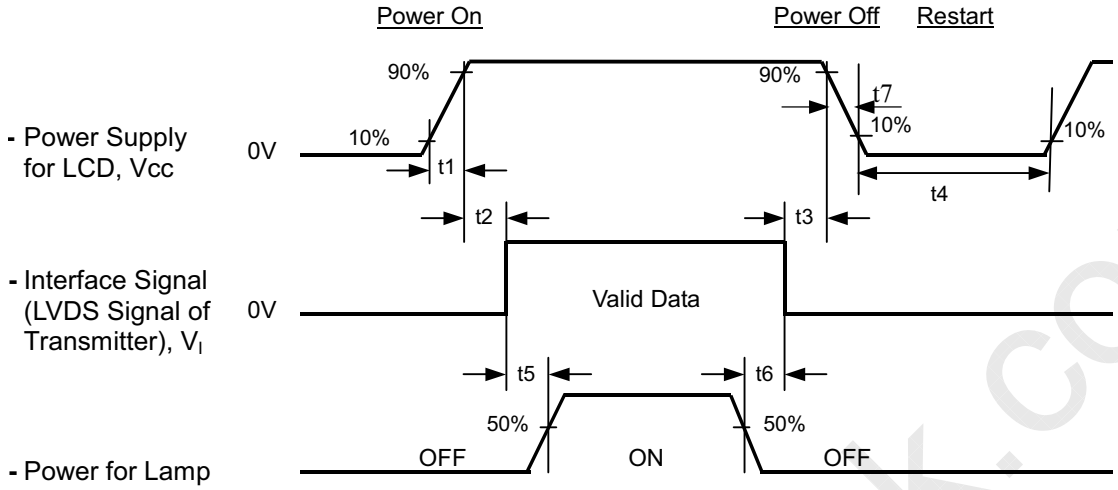
LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (4) Max value of H-total period is not applicable to last one line of a frame while Refresh Rate is in spec.

6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the inverter power on and signal power on/off sequence should be as the diagram below.



Timing Specifications:

0.5< t1 ≦ 10 msec

0 < t2 ≦ 50 msec

0 < t3 ≦ 50 msec

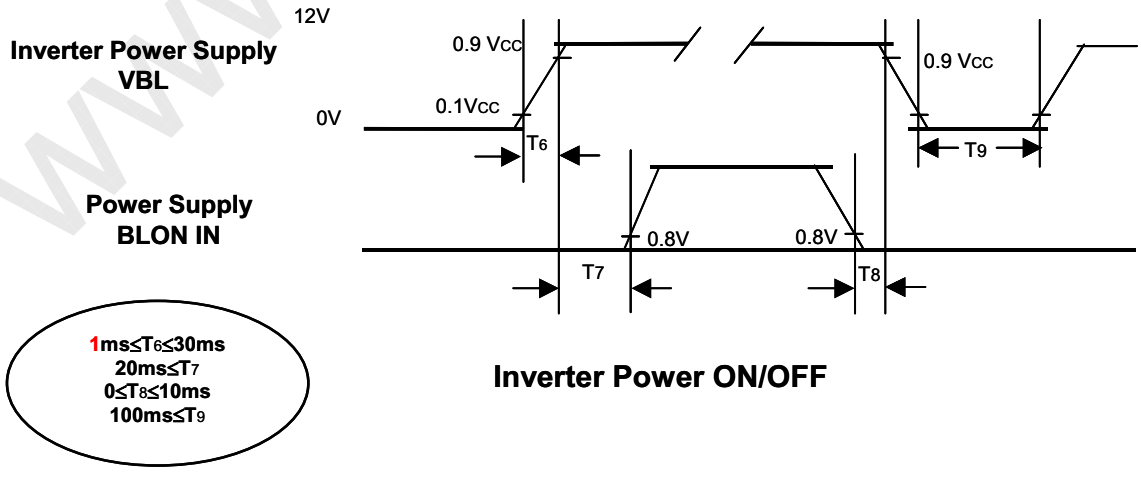
t4 ≧ 500 msec

t5 ≧ 450 msec

t6 ≧ 90 msec

5 ≦ t7 ≦ 100 msec (note6)

Power ON/OFF



Inverter Power ON/OFF

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power of and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

(6) The inverter power sequence and control signal timing must follow the figure above. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

(7) It is suggested that Vcc falling time follows t7 specification; else slight noise is likely to occur when LCD is turned off (even backlight is already off).

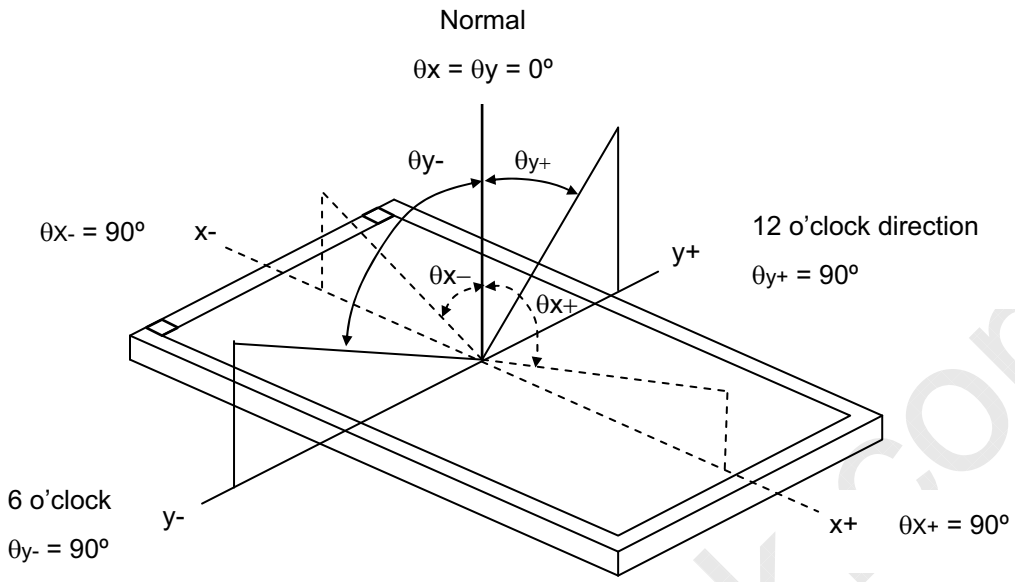
7. OPTICAL CHARACTERISTICS

7.1 OPTICAL SPECIFICATIONS

The optical characteristics are measured under stable environment shown in Note (6) and under 25 degree C condition.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y =0° CS-1000	Typ – 0.03	0.645	Typ + 0.03		(1), (5)
		Ry			0.324			
	Green	Gx			0.294			
		Gy			0.613			
	Blue	Bx			0.143			
		By			0.085			
	White	Wx			0.294			
		Wy			0.309			
Center Luminance of White		L_C		550		-	cd/m^2	(4), (5)
Contrast Ratio		CR		500		-	-	(2), (5)
Response Time		T_R	θ_x=0°, θ_Y =0°	-	25		ms	(3)
		T_F		-	25		ms	
White Variation		δW	θ_x=0°, θ_Y =0° USB2000	-	1.25	1.4	-	(5), (6)
Viewing Angle	Horizontal	θ_x+	CR ≧ 10 USB2000	80	85	-	Deg.	(1), (5)
		θ_x-		80	85	-		
	Vertical	θ_Y+		80	85	-		
		θ_Y-		80	85	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

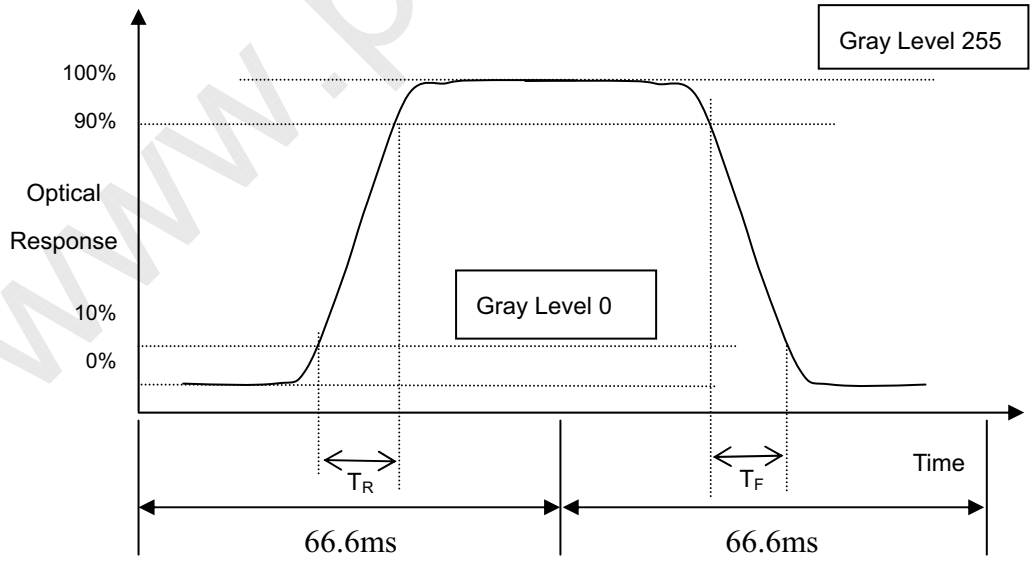
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

.

Note (3) Definition of Response Time (T_R, T_F):



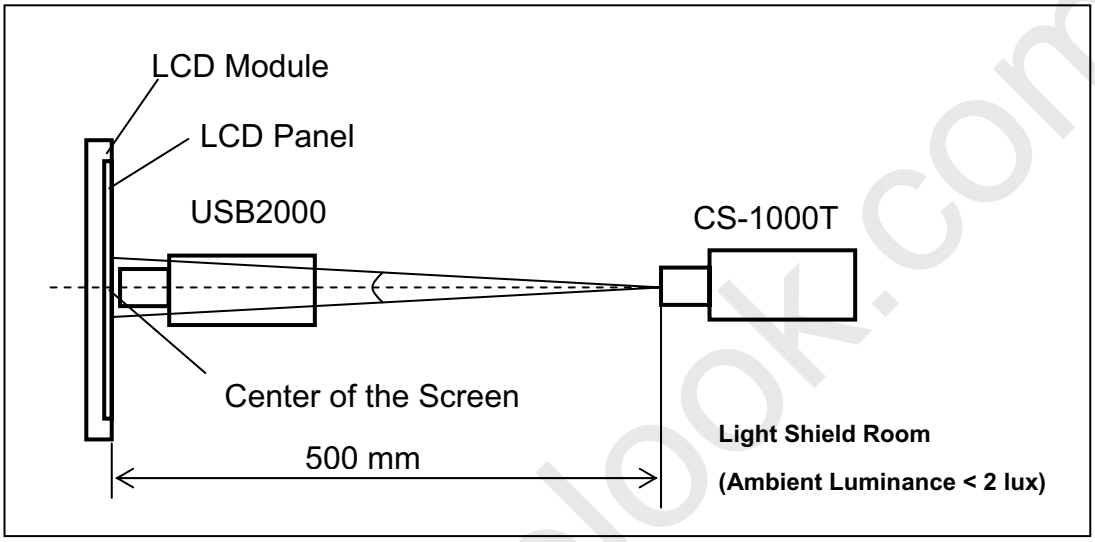
Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point

L_C = L (5)

Note (5) Measurement Setup:

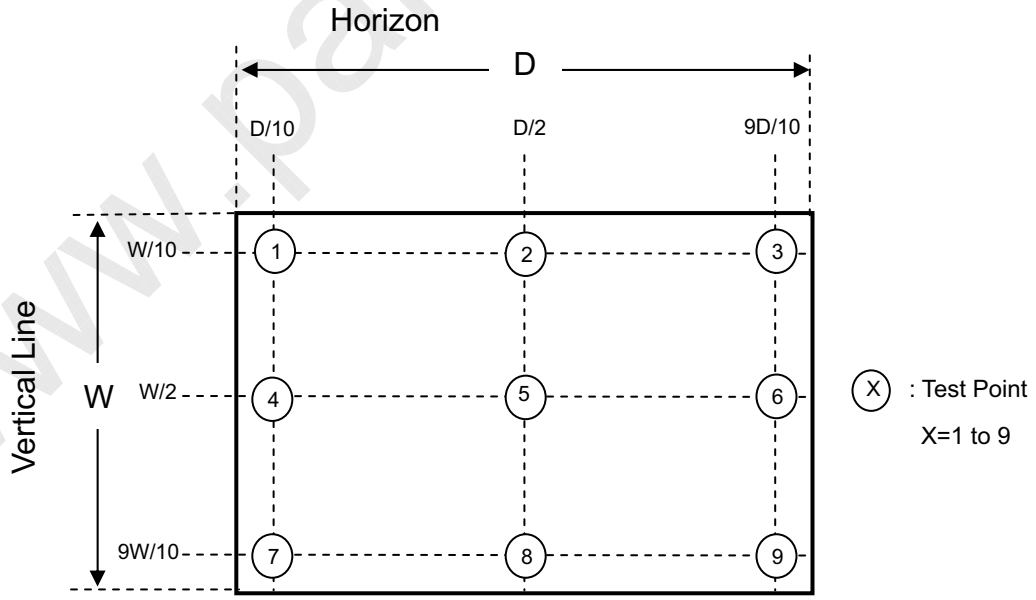
The LCD module should be stabilized at given temperature for 60 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 60 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2) ……L (4), L (9)] / Minimum [L (1), L (2) …… L (4), L (9)]



8. PACKAGING

8.1 PACKING SPECIFICATIONS

(1) 5 LCD modules / 1 Box

(2) Box dimensions: 442(L)*402(W)*558(H) mm

(3) Weight: approximately 15Kg (5 modules per box)

8.2 PACKING METHOD

(1) Carton Packing should have no failure in the following reliability test items.

Test Item	Test Conditions	Note
Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Dropping Test	1 Angle, 3 Edge, 6 Face, 60cm	Non Operation

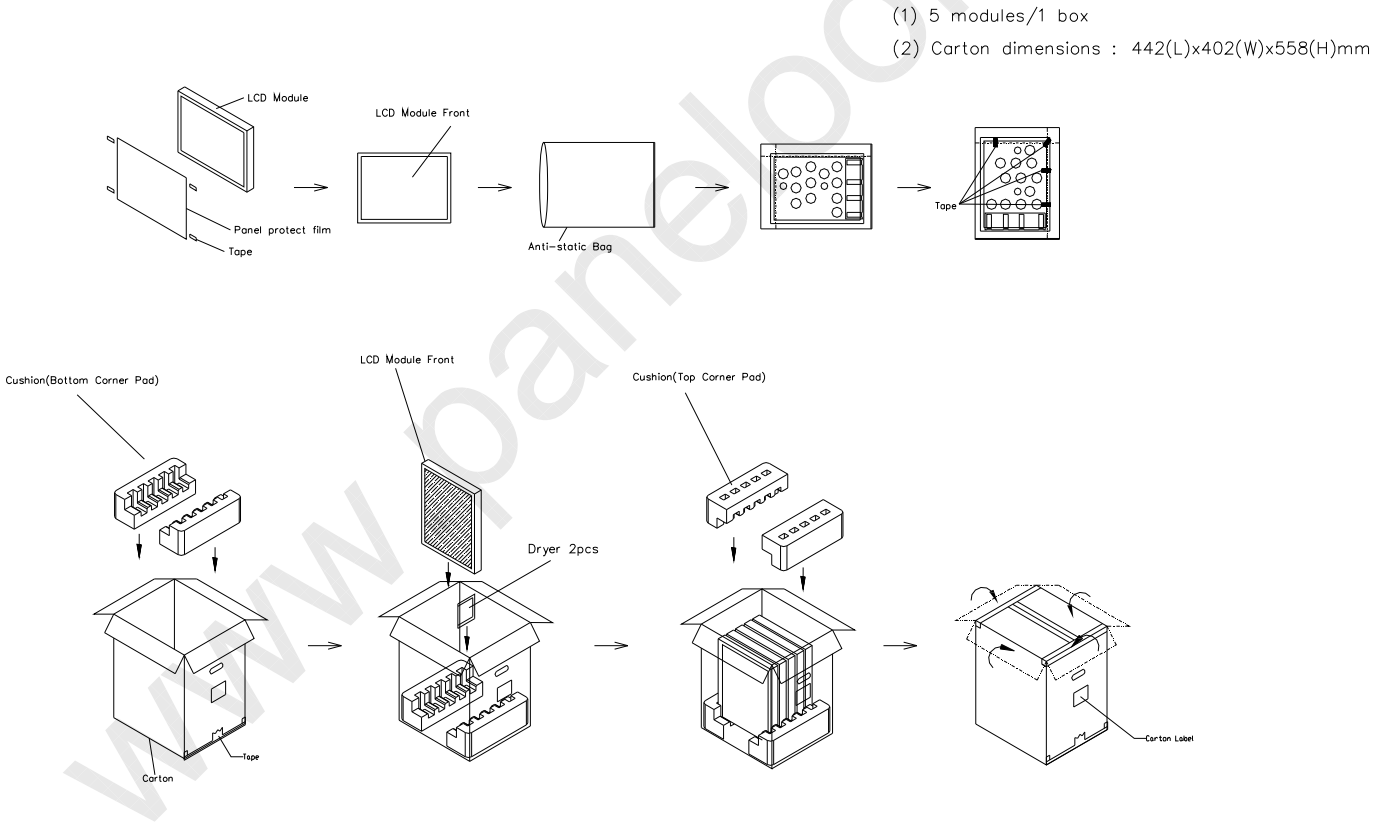


Figure. 8-1 Packing method

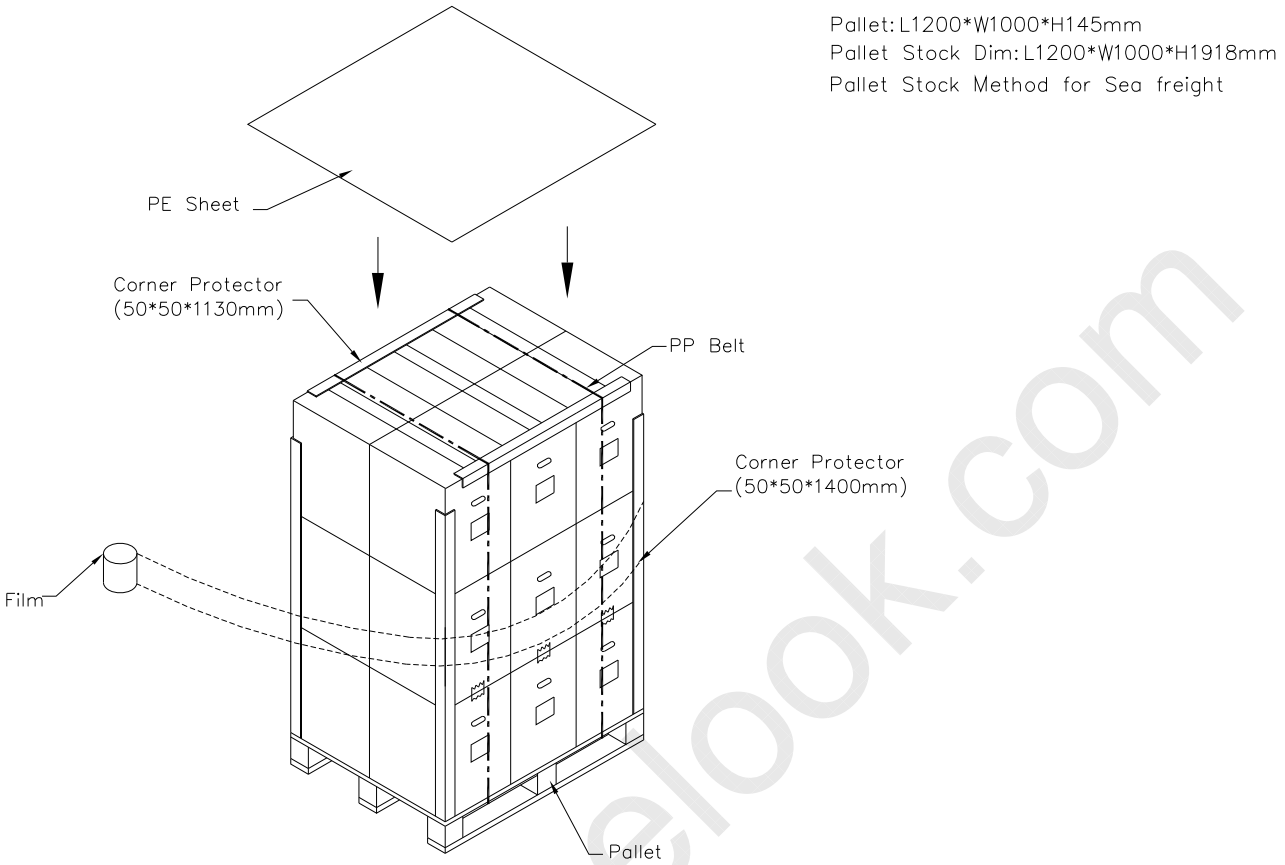


Figure. 8-2 Packing method

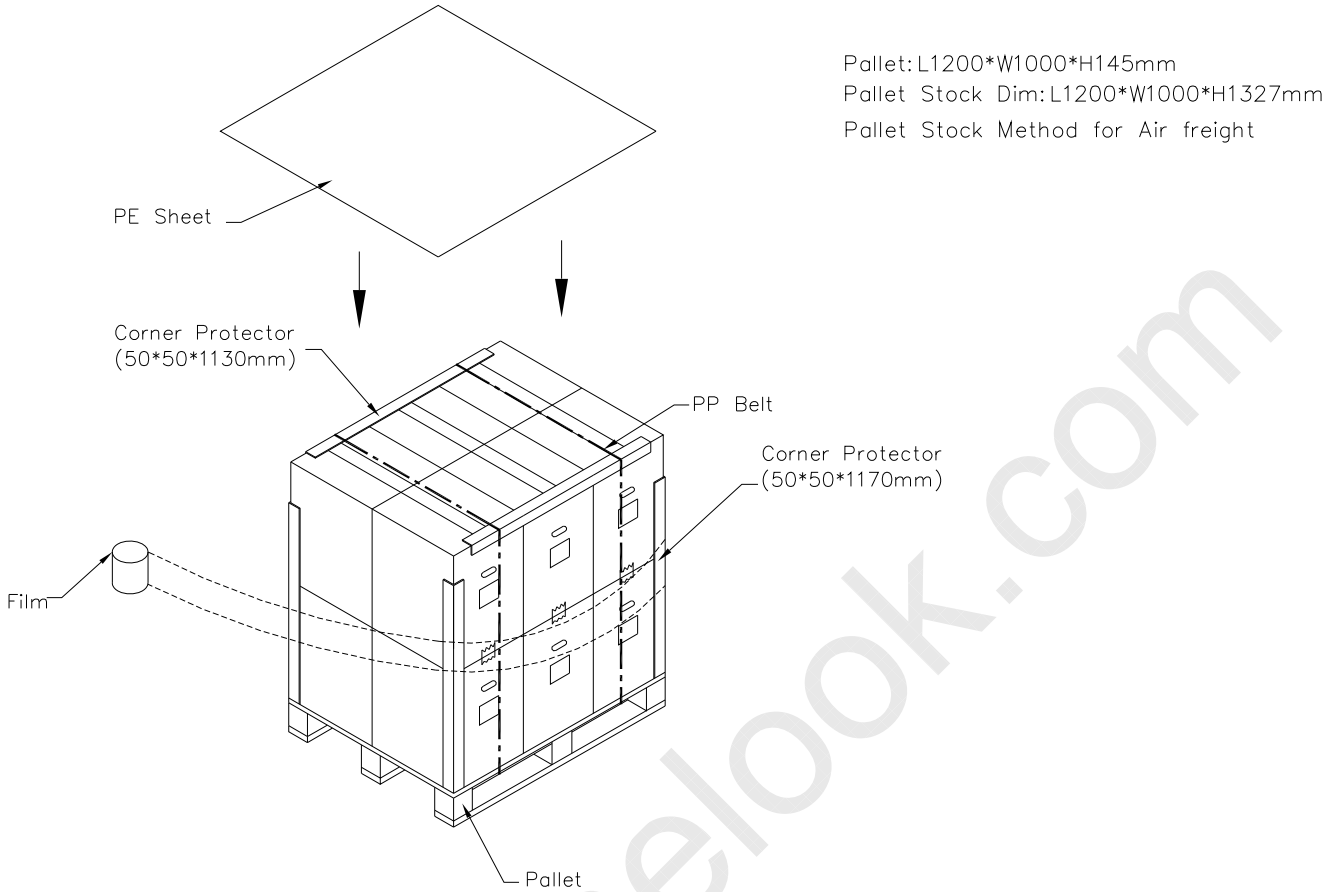
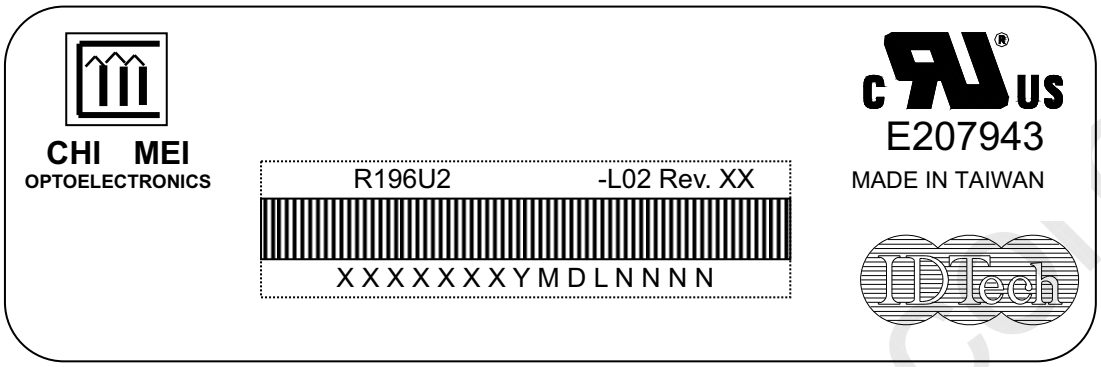


Figure. 8-3 Packing method

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

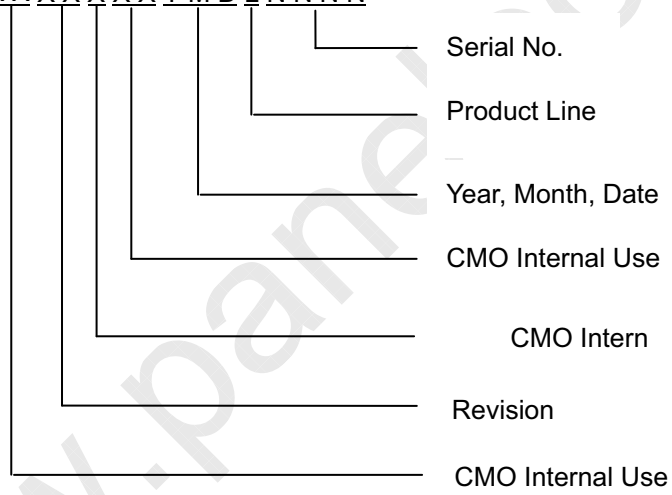
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: R196U2-L02

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

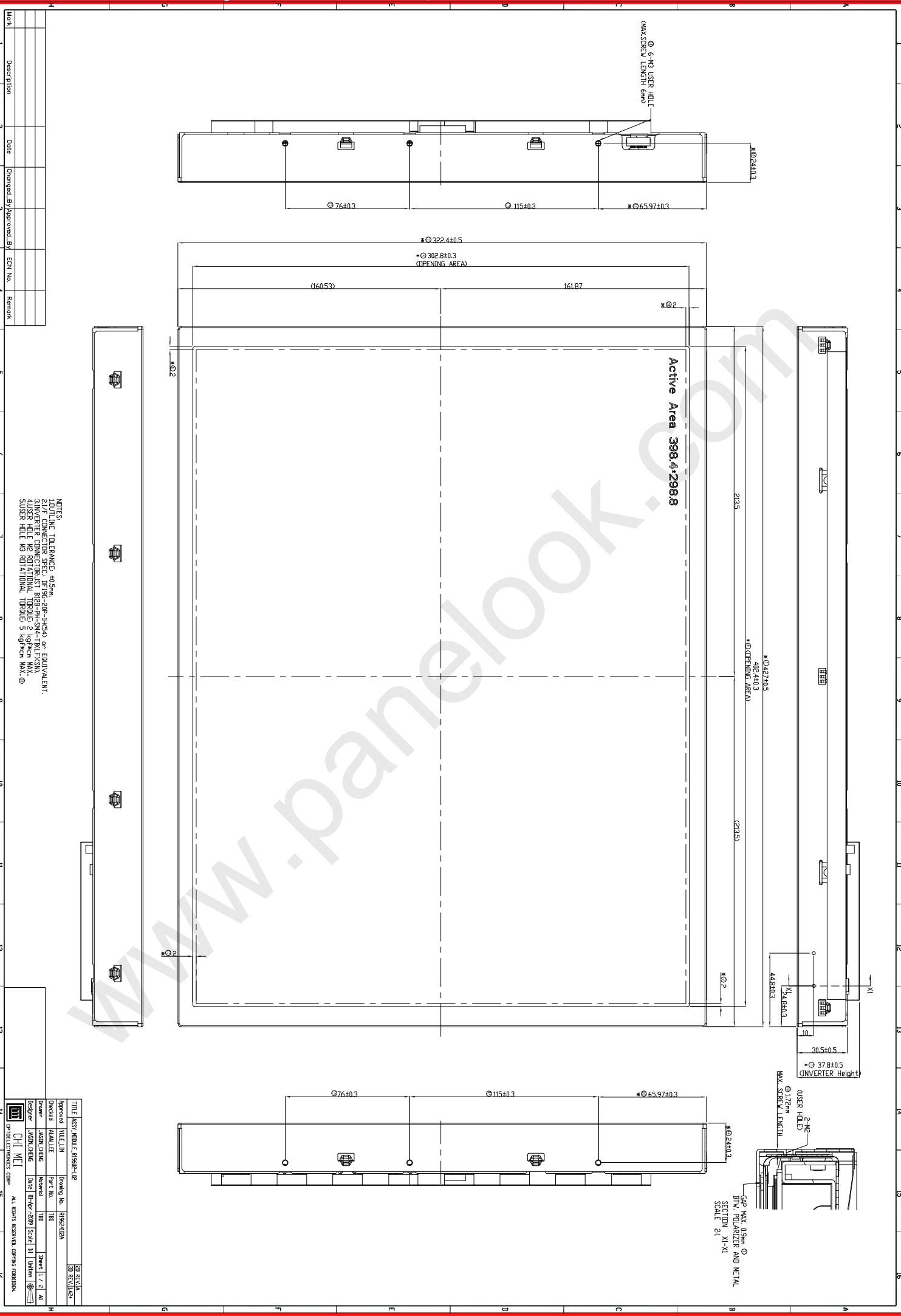
10.2 SAFETY PRECAUTIONS

(1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

**** End of document ****



NOTES:
1.OUTLINE TOLERANCE: ±0.5mm
2.I/F CONNECTOR: HRS DF19G-20P-1H(54) or EQUIVALENT.
3.INVERTER CONNECTOR: JST B2B-PH-SM4-TBLF(LF)(SN).
4.USER HOLE M2 ROTATIONAL TORQUE 2 kgf*cm MAX.
5.USER HOLE M3 ROTATIONAL TORQUE 5 kgf*cm MAX.@

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE	ASSY_MIDDLE_R19GUE-L02		
Approved	YULE_LIN	Drawing No.	R19GC4002A
Checked	ALAN_LEE		
Drawer	JASON_CHENG	Part No.	TBD
Designer	JASON_CHENG	Material	TBD
		Date	01-Apr-2009
		Scale	1/1
		Sheet	1 / 2
		Unit:mm	A1

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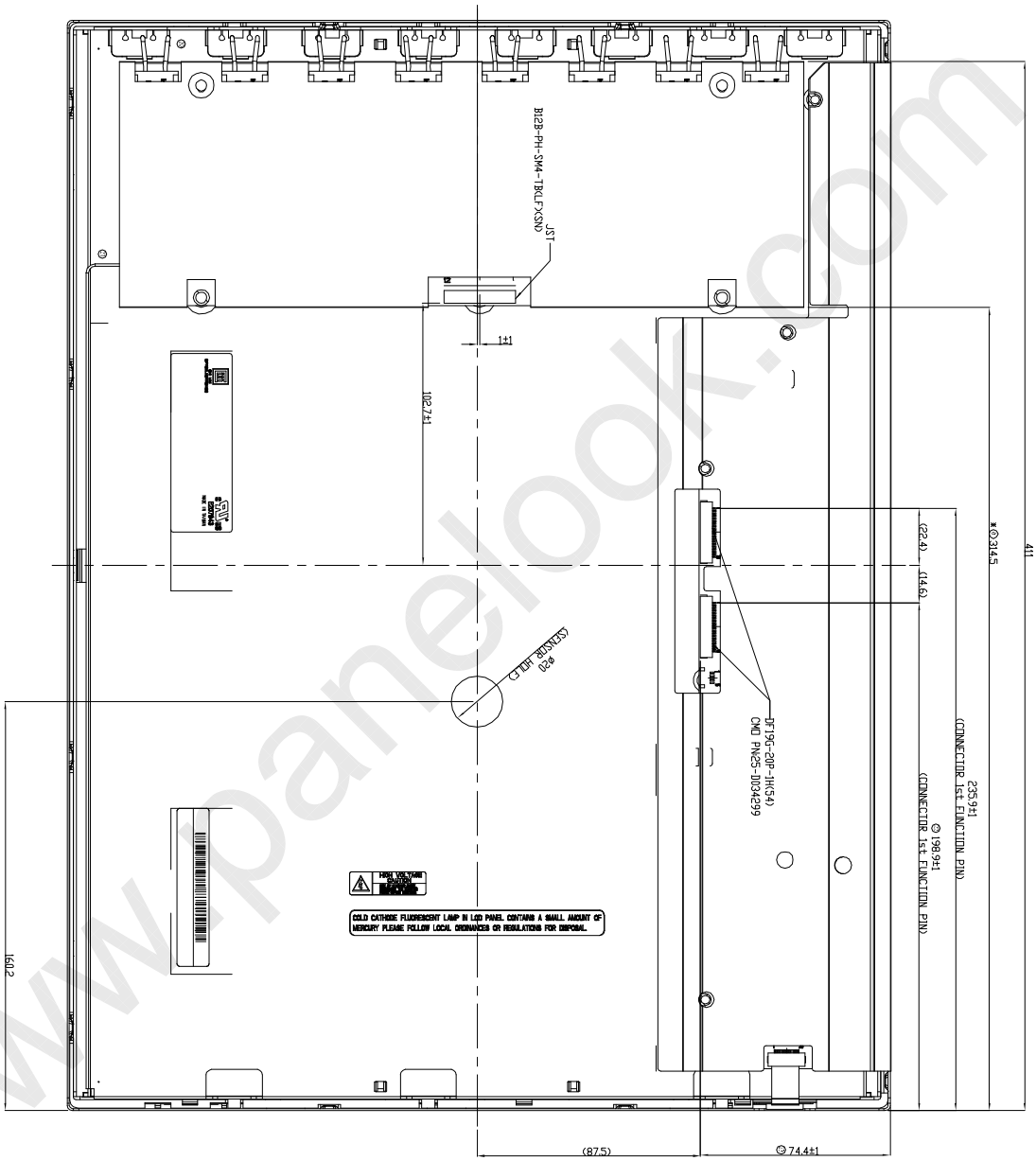
Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark



NOTES:
1.OUTLINE TOLERANCE: ±0.5mm.
2.I/F CONNECTOR SPEC: DF19G-20P-1H(54) or EQUIVALENT.
3.INVERTER CONNECTOR:JST B12B-PH-SM4-TBLF(SN).
4.MASTER HOLE M2 ROTATIONAL TORQUE: 2 Kgf*cm MAX.
5.SLOTER HOLE M3 ROTATIONAL TORQUE: 3 Kgf*cm MAX.

TITLE	ASSY_MIDDLE_R19GU2-L01		
Approved	YULE_LIN	Drawing No.	R19GC4082A
Checked	ALAN_LEE	Part No.	
Drawer	JASON_CHENG	Material	TBD
Designer	JASON_CHENG	Date	01-Apr-2009
		Scale	1/1
		Unit	mm
		Sheet	2 / 2
			A1

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