Doc. Number:

☐ **Tentative Specification**

☐ **Preliminary Specification**

■ **Approval Specification**

MODEL NO.: R208R3
SUFFIX: L01

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

記錄	工作	審核	角色	投票
2011-09-19 19:40:28	APPL 產品管理處	yuhsiang.chang (張喻翔/514-10922)	Director	Accept

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REVISION HISTORY

Version	Date	Page	Description
0.0	2006/12/12	All	R208R3 -L01 Specifications was first issued
1.0	2007/06/28	26 15	Correction, the select command of gamma table New Added, VDIM vs Dimming Range Chart
2.0	2007/08/20	9	New Added, Note(6)
3.0	2011/09/02	5 6 21	Power Supply Specification update Backlight Specification update Optical Specification update

1. GENERAL DESCRIPTION

1.1 OVERVIEW

R208R3-L01 is an 20.8" TFT Liquid Crystal Display module with 14 CCFL Backlight unit and 31 pins and one port 2ch-LVDS interface. This module supports 2048 x 1536 QXGA mode and displays 16.7M colors driven by 8bit drivers. The LCD module includes built-in inverter for Backlight.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	20.8" real diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	2048 (xR,G,B) x 1536	Pixel	-
Pixel Pitch	0.207 (H) x 0.207 (V)	mm	-
Pixel Arrangement	Sub-pixel Vertical stripe	-	-
Display Colors	16.7M	color	-
Transmissive Mode	Dual domain IPS, Normally Black	-	-
Surface Treatment	Anti-glare type	-	-
Luminance, White	600	cd/m2	-
Power Consumption	Total 76.32W (typ.) @ cell 9.12 W (typ.), BL 67.2 W (typ.)		(1)

Note (1) The specified power consumption: Total= cell + BL

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	456.2	457.0	457.8	mm	(1)
	Vertical (V)	349.2	350.0	350.8	mm	
	Thickness (T)	-	45	45.8	mm	
Bezel Area	Horizontal	-	427.9	-	mm	
	Vertical	-	322	-	mm	
Active Area	Horizontal	-	423.93	-	mm	
	Vertical	-	317.95	-	mm	
Weight		-	-	2580	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	ºC	(1)
Operating Ambient Temperature	TOP	0	55	ºC	(1), (2)

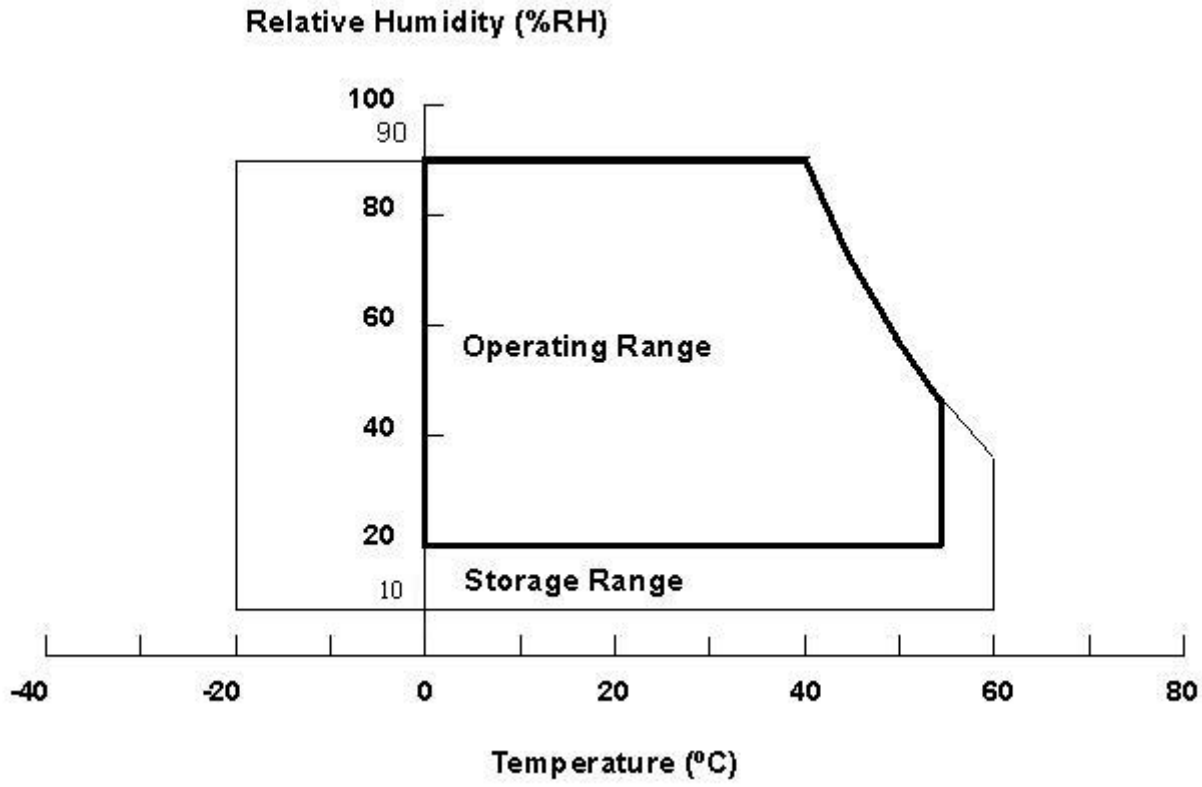
Note (1)

(a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	13.2	V	(1)
Logic Input Voltage	V_{IN}	-0.3	4.3	V	

3.2.2 BACKLIGHT UNIT

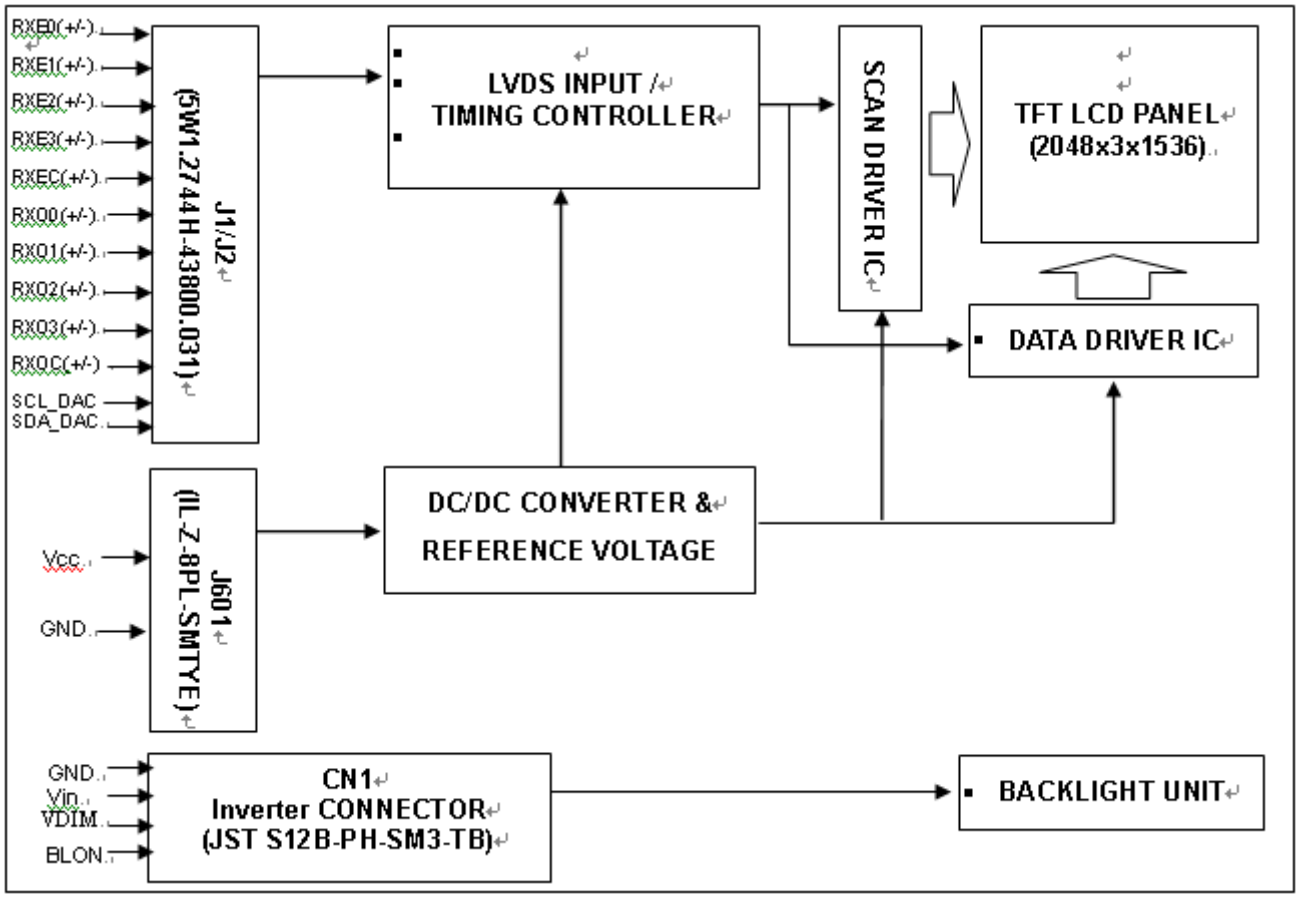
Item	Symbol	Value			Unit	Note
		Min.	Typ	Max.		
Lamp Voltage	V_L	720	800	880	V_{RMS}	(1), (2)
Lamp current	I_L	3	6	8	mA_{RMS}	
Lamp frequency	F_L	40	---	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 4.3.3 and 4.3.4 for further information).

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

4.2.1(Master) : Left side (Front View)

PIN ASSIGNMENT (J1)

Pin	Name	Description
1	NC	Not connection Should keep open.
2	NC	Not connection Should keep open.
3	NC	Not connection Should keep open.
4	GMA_SEL	0: Dicom; 1: Gamma 2.2 (0 : Ground ; 1 : 3.3V) ;default is zero
5	NC	Not connection Should keep open.
6	DGND	Digital Ground
7	SDA_DAC	I2C data for adjustment brightness. [Note (5)]
8	SCL_DAC	I2C clock for adjustment brightness. [Note (5)]
9	DGND	Digital Ground
10	LGND	LVDS Ground
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXO3-	Negative LVDS differential data input. Channel O3 (odd)
13	RXOC+	Positive LVDS differential clock input. (odd)
14	RXOC-	Negative LVDS differential clock input. (odd)
15	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
16	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
17	RXO1+	Positive LVDS differential data input. Channel O1 (odd)

18	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
20	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
21	RXE3+	Positive LVDS differential data input. Channel E3 (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXEC+	Positive LVDS differential clock input. (even)
24	RXEC-	Negative LVDS differential clock input. (even)
25	RXE2+	Positive LVDS differential data input. Channel E2 (even)
26	RXE2-	Negative LVDS differential data input. Channel E2 (even)
27	RXE1+	Positive LVDS differential data input. Channel E1 (even)
28	RXE1-	Negative LVDS differential data input. Channel E1 (even)
29	RXE0+	Positive LVDS differential data input. Channel E0 (even)
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)
31	LGND	LVDS Ground

4.2.2 J2(Slave) : Right side(Front View)

PIN ASSIGNMENT (J2)

Pin	Name	Description
1	BLON	Backlight on/off signal (HI:backlight ON, Low:backlight OFF)
2	VDIM-IN	Brightness Dimming Control Voltage(0~3V, 0V:MaxBrightness)
3	VDIM-OUT	Brightness Dimming Control Voltage Output Generated by I2C command
4	NC	Not connection Should keep open.
5	NC	Not connection Should keep open.
6	DGND	Digital Ground
7	NC	Not connection Should keep open.
8	NC	Not connection Should keep open.
9	DGND	Digital Ground
10	LGND	LVDS Ground
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXO3-	Negative LVDS differential data input. Channel O3 (odd)
13	RXOC+	Positive LVDS differential clock input. (odd)
14	RXOC-	Negative LVDS differential clock input. (odd)
15	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
16	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
17	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
18	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
20	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
21	RXE3+	Positive LVDS differential data input. Channel E3 (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXEC+	Positive LVDS differential clock input. (even)
24	RXEC-	Negative LVDS differential clock input. (even)
25	RXE2+	Positive LVDS differential data input. Channel E2 (even)
26	RXE2-	Negative LVDS differential data input. Channel E2 (even)
27	RXE1+	Positive LVDS differential data input. Channel E1 (even)
28	RXE1-	Negative LVDS differential data input. Channel E1 (even)
29	RXE0+	Positive LVDS differential data input. Channel E0 (even)
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)
31	LGND	LVDS Ground

Note (1) Connector Part No.: ARC 5W1.2744H-43800.031or equivalent.

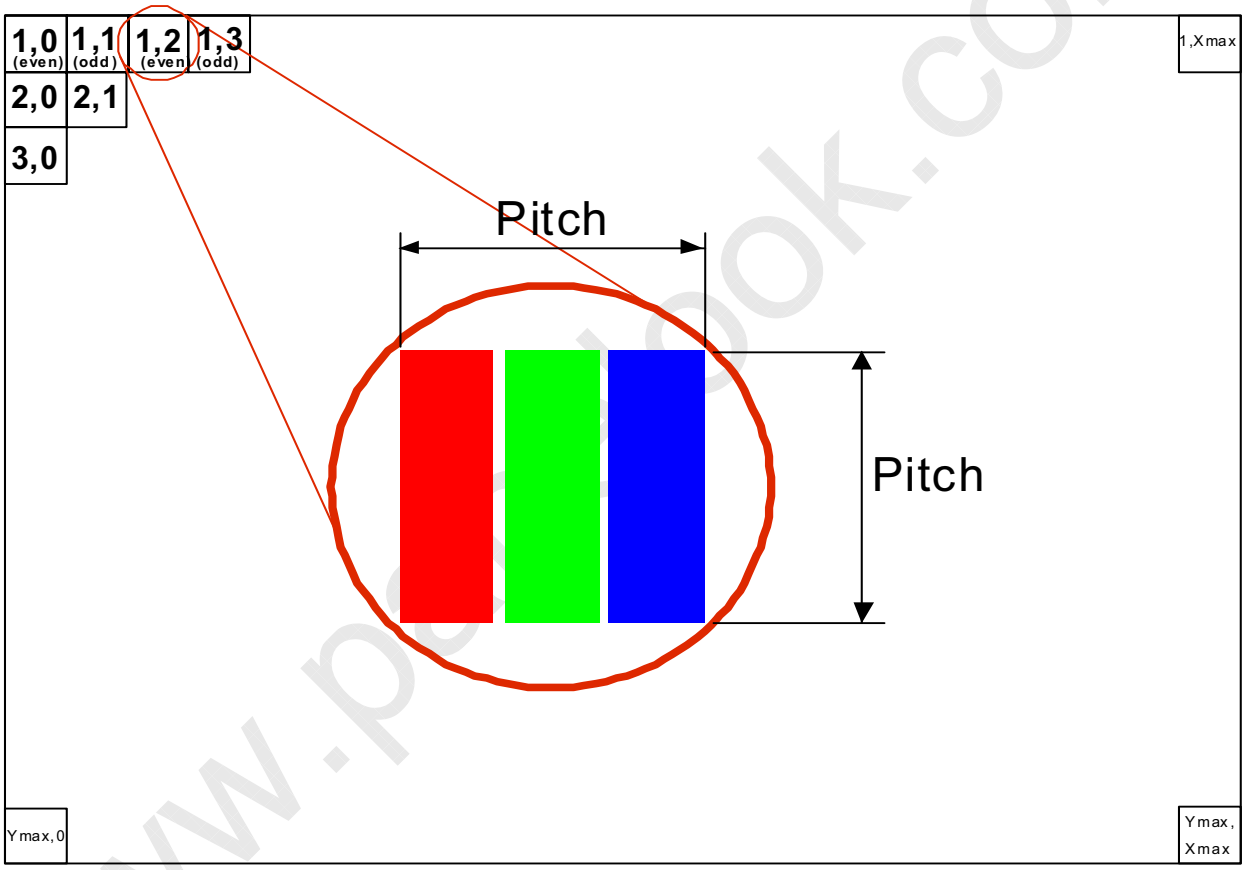
Note (2) The first pixel is even.

Note (3) Input signal of even and odd clock should be the same timing.

Note (4) You can adjust brightness by two methods, one is by I2C function of J1, the other is by pin 11 of Inverter connector(CN1). If you select one method to adjust brightness, another method's input pin(s) should be open.

Note (5) If you don't use I2C to adjust brightness by J1, you should make the pin7, pin8 of J1 open.

Note (6) The module uses a 100-ohm resistor between positive and negative data lines of each receiver input.



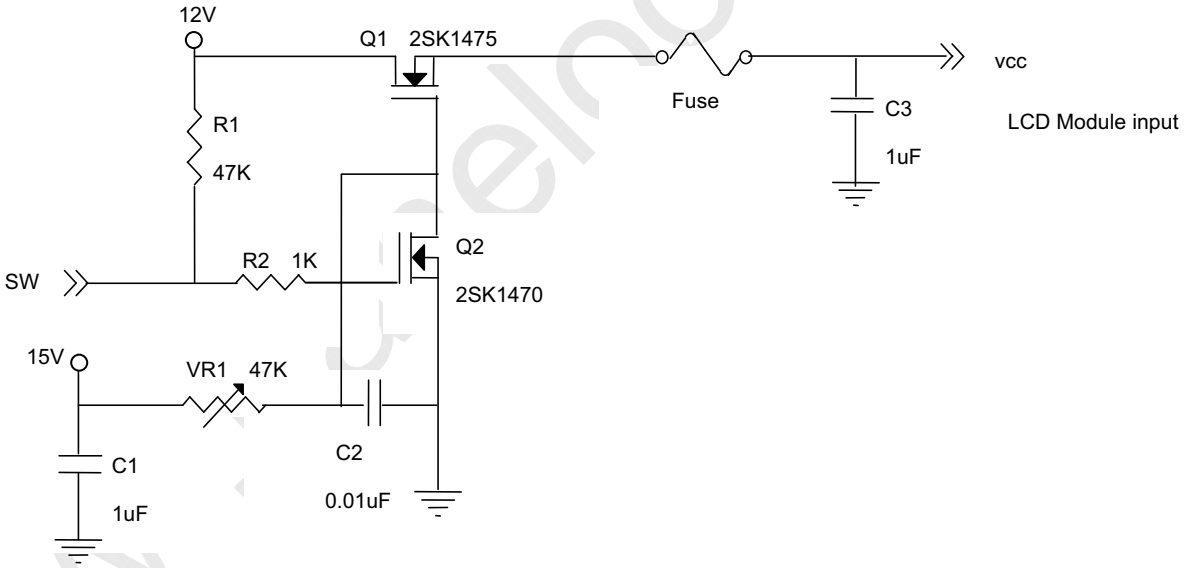
4.3 ELECTRICAL CHARACTERISTICS

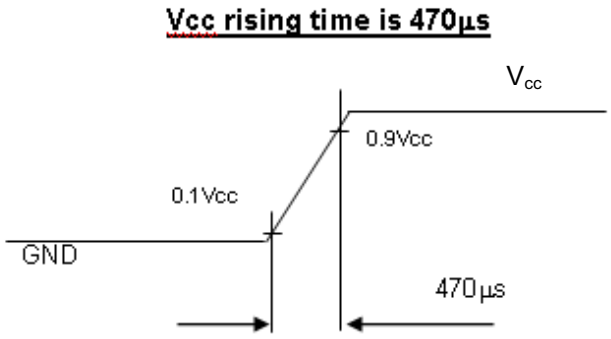
4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	11.4	12	12.6	V	-
Ripple Voltage		V_{RP}	-	-	300	mV	-
Rush Current		I_{RUSH}	-	-	3.8	A	(2)
Power Supply Current	White			760	1064	A	(3)a
	Black			450	630	A	(3)b
	Vertical Stripe			720	1008	A	(3)c
Power Consumption		PLCD	-	9.12	11.85	Watt	(4)
LVDS differential input voltage		Vid	100	-	600	mV	
LVDS common input voltage		Vic	1.0	1.25	1.4	V	
Logic High Input Voltage		VIH	2.64	-	-	V	
Logic Low Input Voltage		VIL	-	-	0.66	V	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) Measurement Conditions:





Note (3) The specified power supply current is under the conditions at Vcc =12.0 V, Ta = 25 ± 2 °C, Fr = 60Hz, whereas a power dissipation check pattern below is displayed.

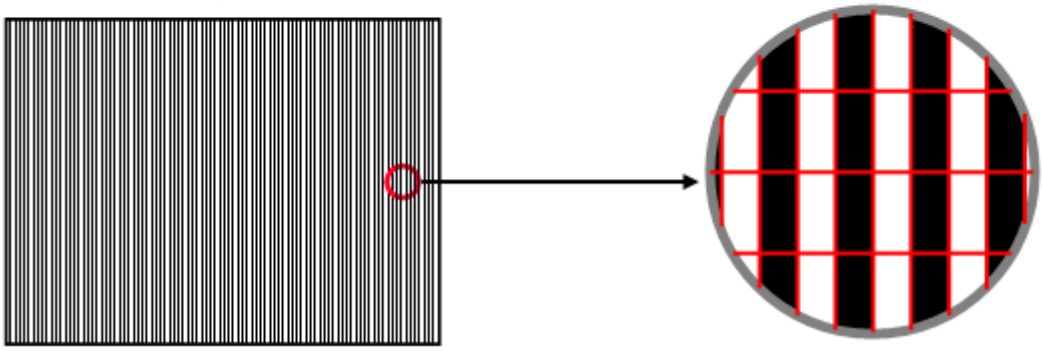
a. White Pattern

Active Area

b. Black Pattern

Active Area

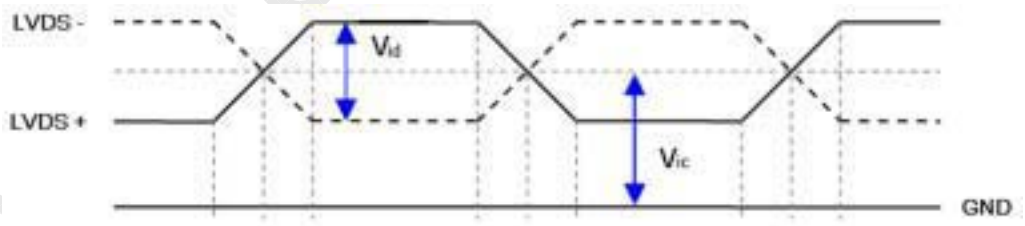
c. Vertical Stripe Pattern



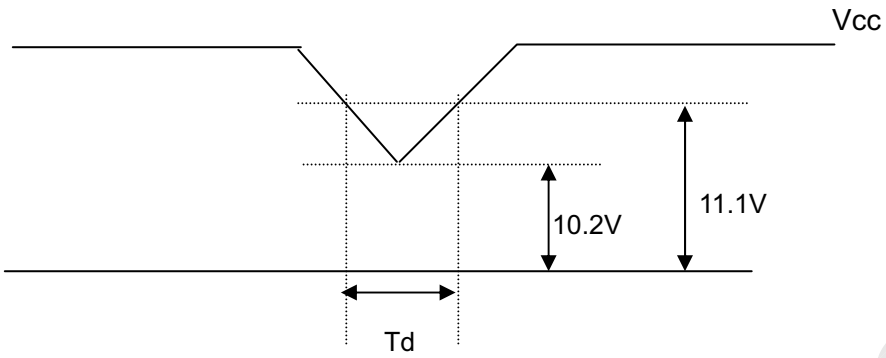
Active Area

Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition



4.3.2 Vcc Power Dip Condition

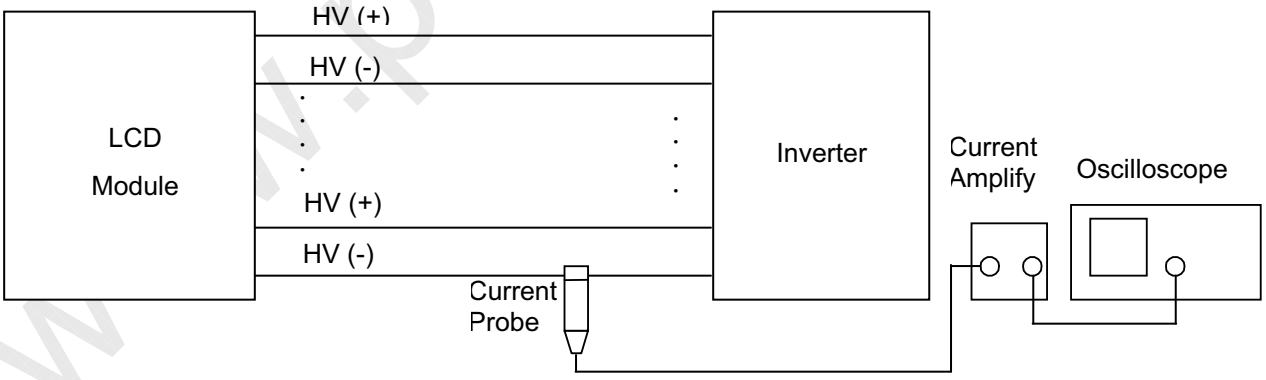


Dip condition: $10.2V \le Vcc \le 11.1V, Td \le 20ms$

4.3.3 BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	720	800	880	V_{RMS}	(I_L = 6 mA)
Lamp Current	I_L	3	6	8	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	---	---	1250 (25 ºC)	V_{RMS}	(2)
		---	---	1380(0 ºC)	V_{RMS}	(2)
Operating Frequency	F_L	40	---	80	KHz	(3)
Lamp Life Time	L_{BL}	50000 hr	---	---	Hrs	(5)

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I I_L = 3~8 mArms until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (5) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

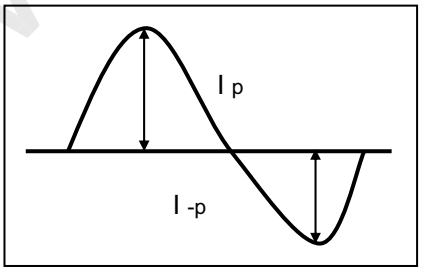
The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within $\sqrt{2}$ ± 10%;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

4.3.4 INVERTER ELECTRICAL CHARATERISTIC

Item	Symbol	Description	Min.	Typ.	Max.	Unit
1	V_{in}	Input voltage	11.4	12	12.6	V
2	I_{in}	Input current (@Vin=12V)	---	6.5	7	A
3	P_{in}	Input power	---	78	84	W
4	BLON	Inverter On/Off control: OFF	-0.1	0	0.8	V
		Inverter On/Off control: ON	2	3.3	6	V
5	VDIM	Output current control VDIM: 0V, maximum brightness VDIM: 3V, minimum brightness	0	---	3	V
6	F_b	Burst Mode Frequency	225	250	275	Hz
7	Freq.	Operating frequency	45	50	55	KHz
8	I_{out}	Output current, VDIM=0V (high side)	5.5	6	6.5	mA

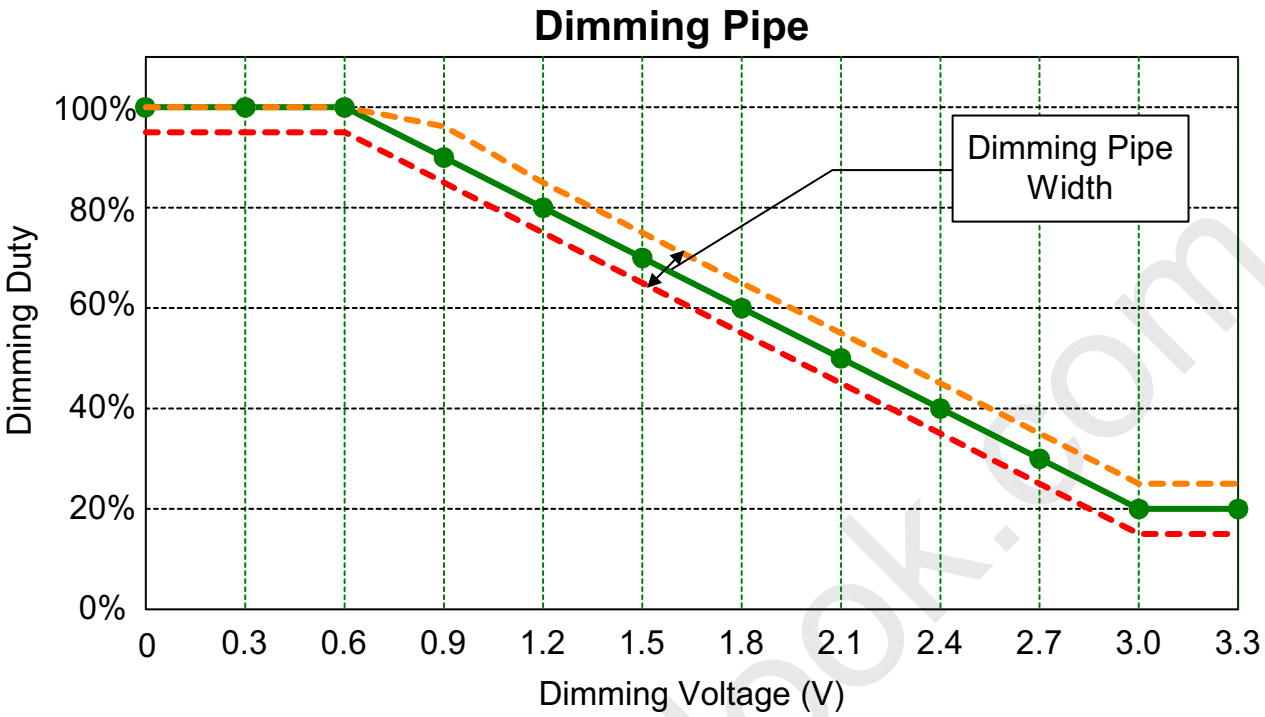
4.3.5 INVERTER INPUT SIGNAL

Pin No.	Symbol	Description
1	Vin	Input voltage
2	Vin	Input voltage
3	Vin	Input voltage
4	Vin	Input voltage
5	Vin	Input voltage
6	Gnd	Ground
7	Gnd	Ground
8	Gnd	Ground
9	Gnd	Ground
10	Gnd	Ground
11	VDIM	Brightness control (0~3V)
12	BLON	Inverter On/Off control (5.0/0V)

Note (1) Connector Part No.: S12B-PH-SM3-TB (JST) or equivalent

Note (2) User's connector Part No.:➔ PHR-12 (JST)

The following chart is the VDIM vs. Dimming Range for your reference.



4.4 LVDS INPUT SIGNAL SPECIFICATIONS

4.4.1 LVDS DATA MAPPING TABLE

VESA MODE

LVDS_SEL = Ground or Open								
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6

JEITA MODE

LVDS_SEL = 3.3V								
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG2	OR7	OR6	OR5	OR4	OR3	OR2
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB3	OB2	OG7	OG6	OG5	OG4	OG3
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB7	OB6	OB5	OB4
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB1	OB0	OG1	OG0	OR1	OR0
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG2	ER7	ER6	ER5	ER4	ER3	ER2
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB3	EB2	EG7	EG6	EG5	EG4	EG3
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB7	EB6	EB5	EB4
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB1	EB0	EG1	EG0	ER1	ER0

4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

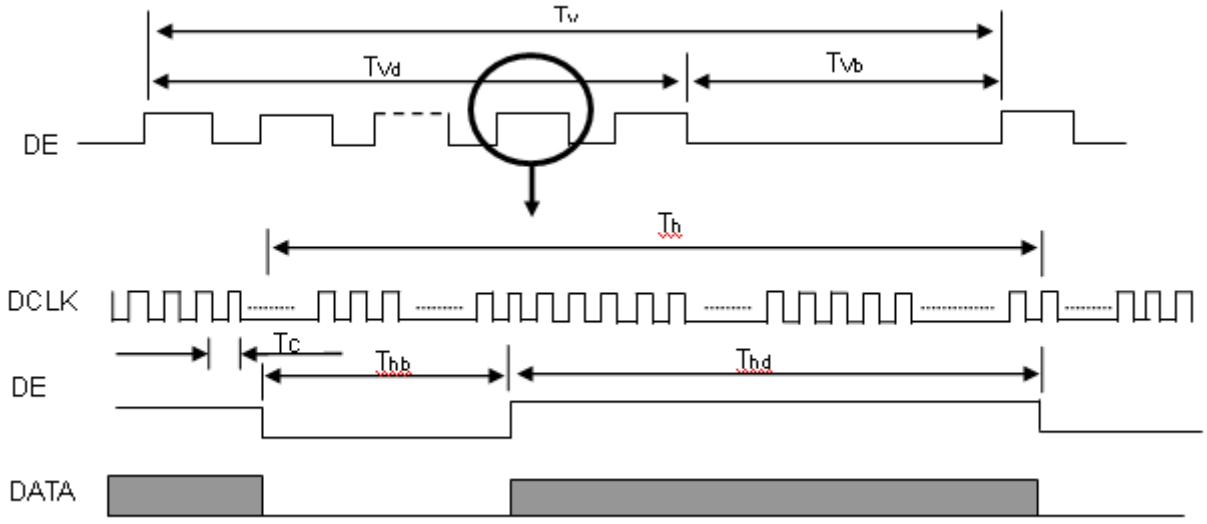
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

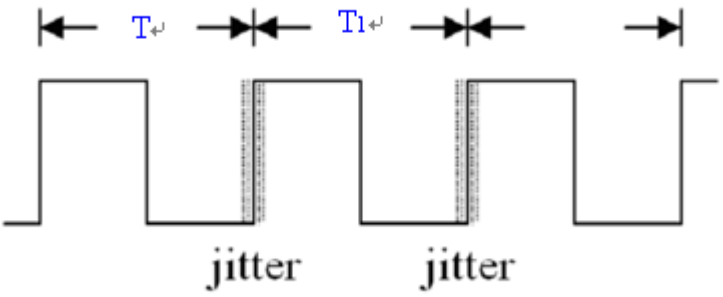
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_c	60	65	66	MHz	-
	Period	T_c	15.15	15.38	16.66	ns	
	Input cycle to cycle jitter	T_{rcl}	-----			ns	(1)
	Input Clock to data skew	TLVCCS				ps	(2)
	Spread spectrum modulation range	Fclkin_mod	0.97*Fc	---	1.03*Fc	MHz	(3)
	Spread spectrum modulation frequency	F_{SSM}	---	---	200	KHz	
Vertical Display Term	Frame Rate	F_r		60		Hz	$T_v=T_{vd}+T_{vb}$
	Total	T_v	1546	1612	1628	Th	-
	Active Display	T_{vd}	1536	1536	1536	Th	-
	Blank	T_{vb}	T_v-T_{vd}	76	T_v-T_{vd}	Th	-
Horizontal Display Term	Total	T_h	640	672	700	Tc	$T_h=T_{hd}+T_{hb}$
	Active Display	T_{hd}	512	512	512	Tc	-
	Blank	T_{hb}	T_h-T_{hd}	160	T_h-T_{hd}	Tc	-

Note: Because this module is operated by DE only mode, H_{sync} and V_{sync} input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

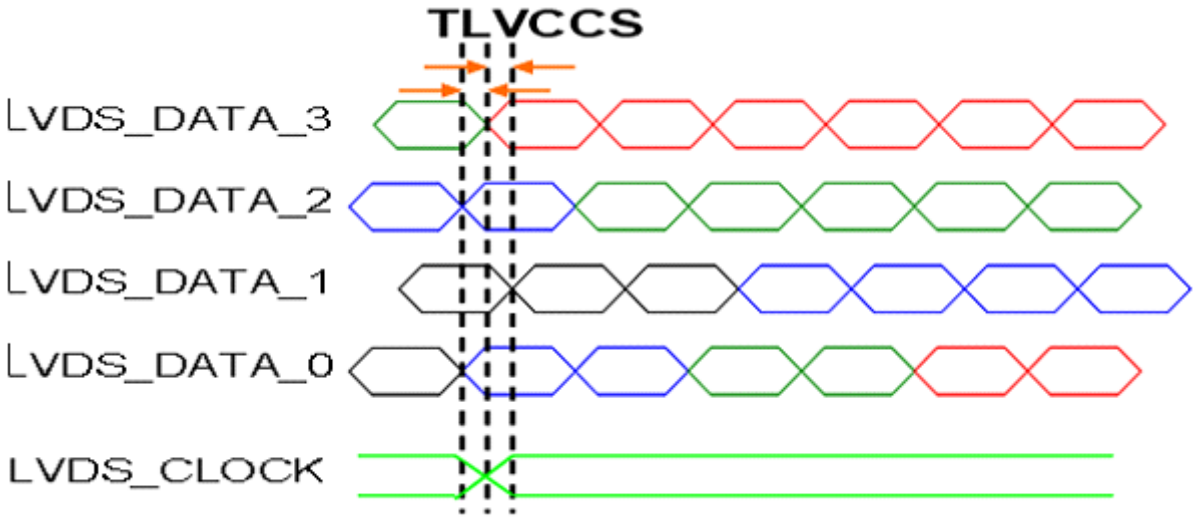
INPUT SIGNAL TIMING DIAGRAM



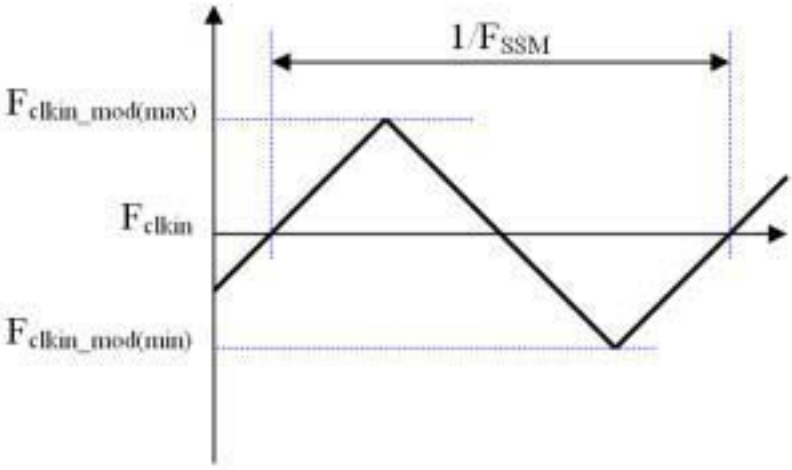
Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



Note (2) Input Clock to data skew is defined as below figures.

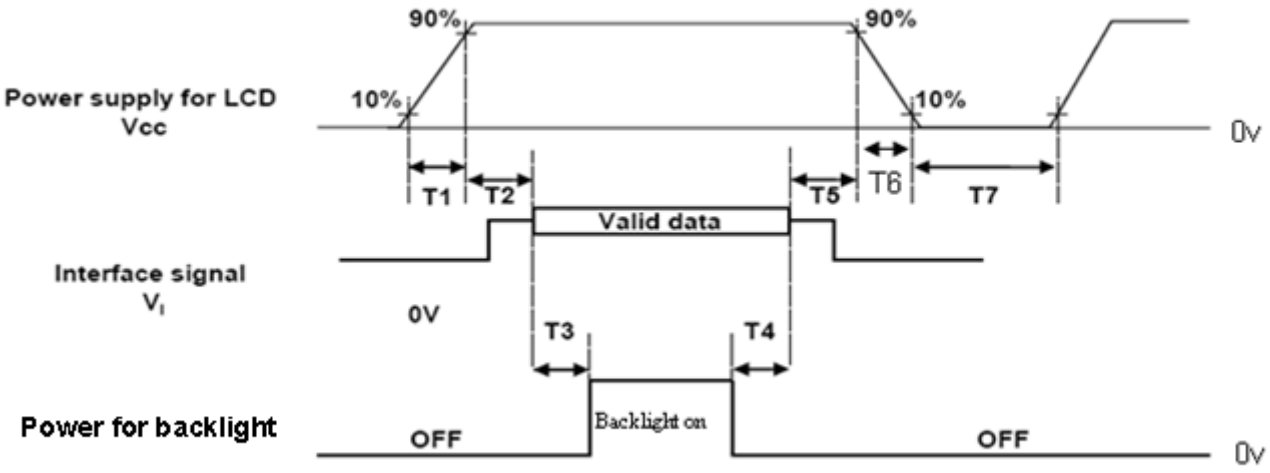


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Timing Specifications:

Parameters	Values			Units
	Min	Typ.	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	450	-	-	ms
T4	90	-	-	ms
T5	0	-	50	ms
T6	5	-	100	ms
T7	500	-	-	ms

Note.

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of V_{CC} = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T7 should be measured after the module has been fully discharged between power of and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

(6) It is not guaranteed that products are damaged which is caused by not following the Power Sequence.

(7) It is suggested that Vcc falling time follows T6 specification; else slight noise is likely to occur when LCD is turned off (even backlight is already off).

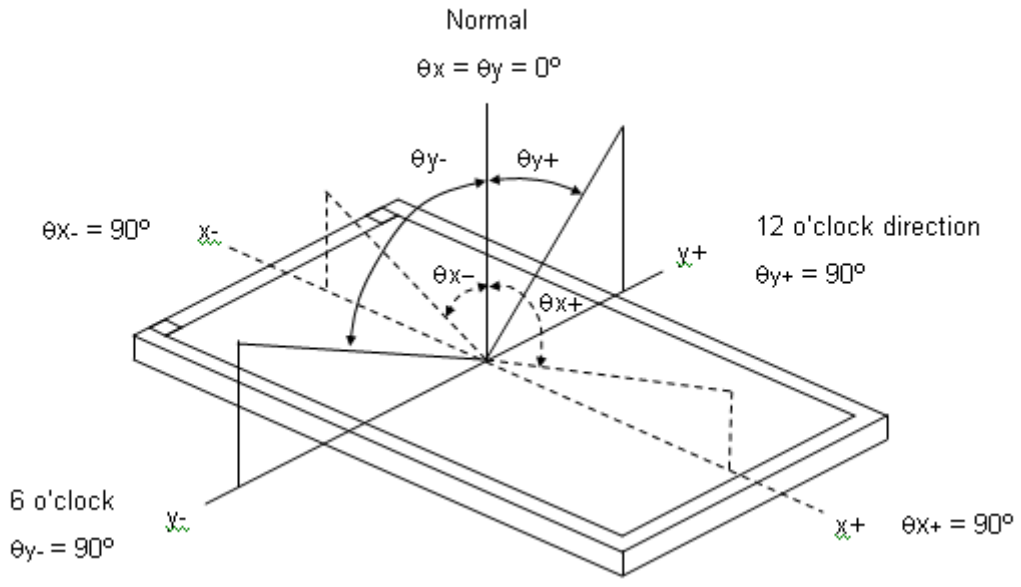
5. OPTICAL CHARACTERISTICS

5.1 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 5.1. The following items should be measured under the test conditions described in 5.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE 1931)	Red	R_x	θ_x=0°, θ_Y =0° CS-1000T	Typ.- 0.03	0.638	Typ.+ 0.03	-	(1), (5)
		R_y			0.325			
	Green	G_x			0.292			
		G_y			0598			
	Blue	B_x			0.147			
		B_y			0.056			
	White	W_x			0.294			
		W_y			0.309			
Center Luminance of White		L_C		500	600	---	cd/m^2	(4), (5)
Contrast Ratio		CR		700	900	---	-	(2), (5)
Response Time		T_R	θ_x=0°, θ_Y =0°	---	10	15	ms	(3)
		T_F		---	10	15	ms	
White Variation(adjacent)		δW_a	θ_x=0°, θ_Y =0° USB2000	90	---	---	-	(5), (6)
White Variation(total)		δW_t	θ_x=0°, θ_Y =0° USB2000	70	80	---	-	(5), (6)
Viewing Angle		Θ_{y+}	CR ≧ 10 USB2000	80	88	---	Deg.	(1), (5)
		Θ_{y-}		80	88			
		Θ_{x+}		80	88			
		Θ_{x-}		80	88			

Note (1)Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

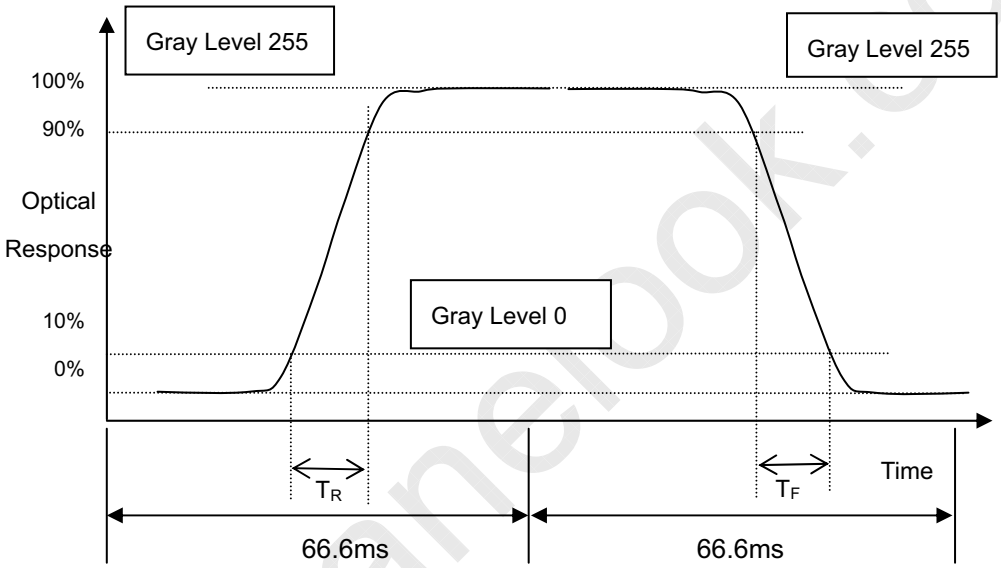
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (4).

Note (3) Definition of Response Time (T_R, T_F):

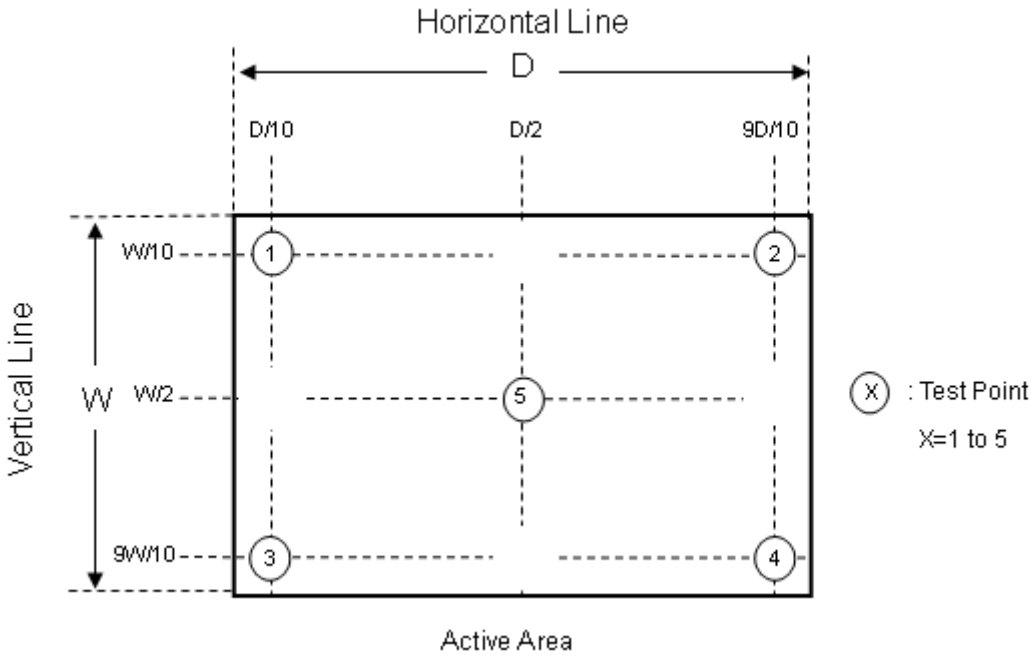


Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point

L_C = L (5)

L (x) is corresponding to the luminance of the point X at the following figure.



Note (5) Measurement Setup:

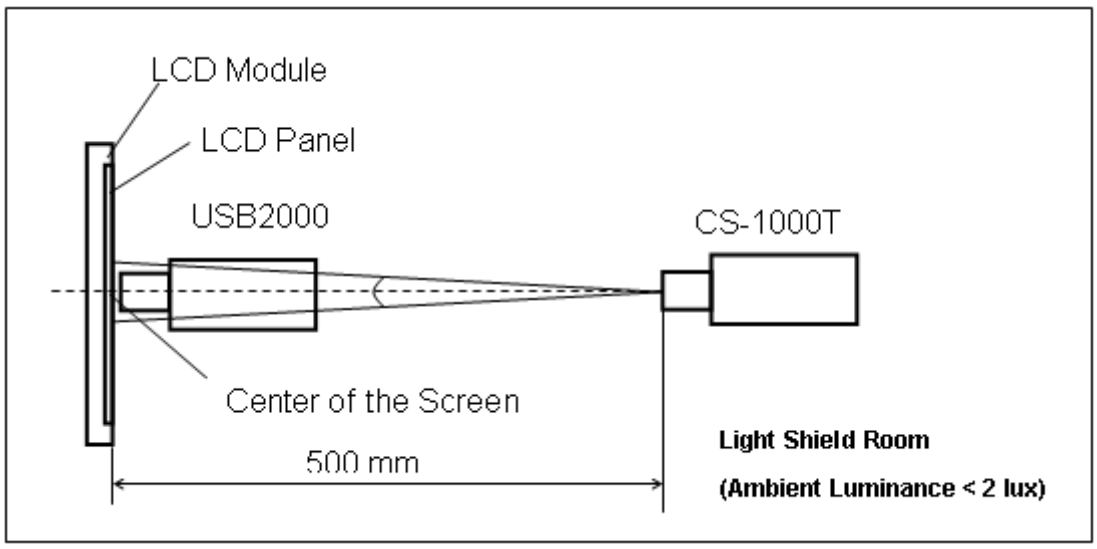
The LCD module should be stabilized at given temperature for 60 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 60 minutes in a windless room.

Unless otherwise specified, the ambient conditions are as following.

Ambient Temperature: 25 ± 2 (degreeC)

Ambient Humidity: 25 ~ 85 (%)

Atmospheric Pressure: 86.0 ~ 104.0 (kP_a)

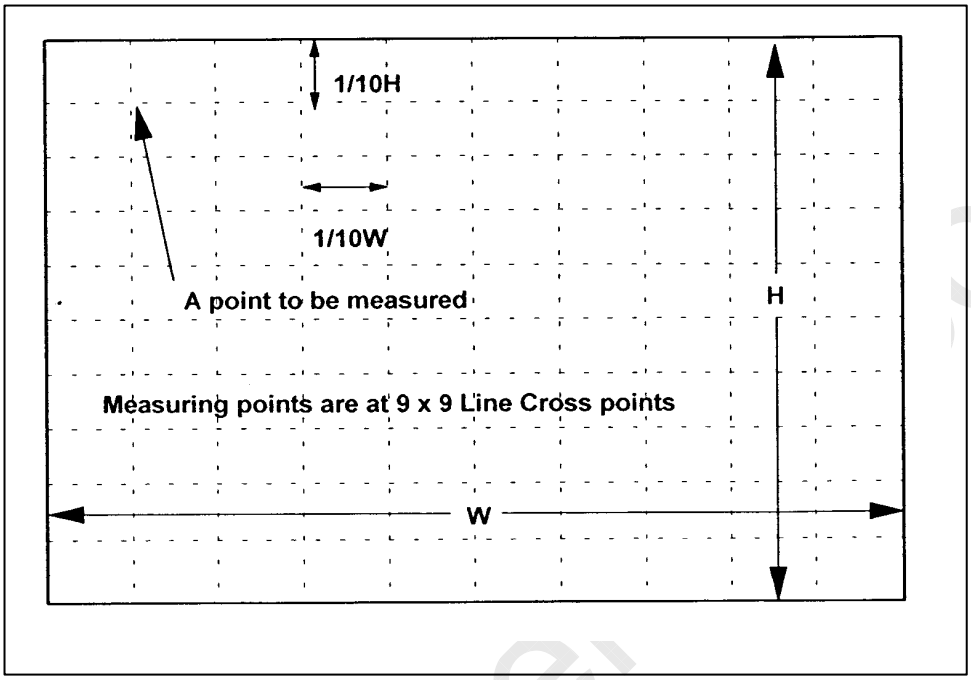


Note (6) There is the Uniformity Measurement below:

'L_{bright} ' represents the Luminance of the point that is brighter than the other point to be compared.

'L_{dark} ' represents the Luminance of the point that is darker than the other point to be compared.

Measuring points are shown in the following Fig.



When the backlight is on with all pixels in the white (maximum gray) level, the luminance uniformity is defined as follows;

Where:

L_{bright}: The luminance of the brightness part of the area

L_{dark}: The luminance of the darkest part of the area

1. Screen Total

$$\text{Luminance Uniformity} = \frac{L_{dark}}{L_{bright}} \geq 0.70$$

over the entire screen.

6. RELIABILITY TEST ITEM

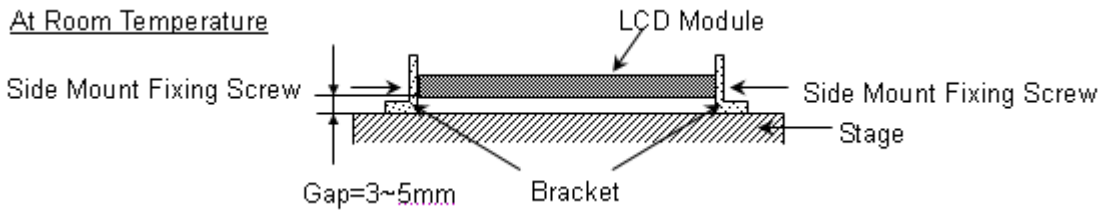
Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃ , 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 55℃, 240hours	
Low Temperature Operation (LTO)	Ta= 0℃ , 240hours	
High Temperature Storage (HTS)	Ta= 60℃ , 240hours	
Low Temperature Storage (LTS)	Ta= -20℃ , 240hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G_{rms} Wave: Half-sine Frequency: 10 - 300 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 11 ms Direction : ± X, ± Y, ± Z.(one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min , 60℃ / 30min , 100 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω)	
	Air Discharge: ± 15KV, 150pF(330Ω)	

Note (1) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



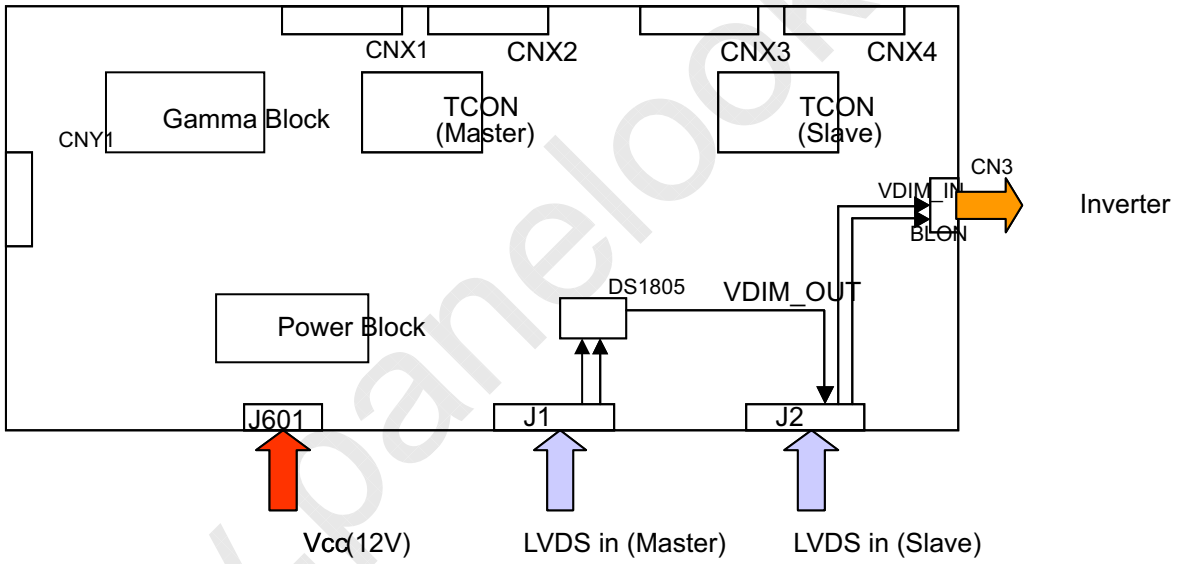
7. Input Parameters Detail

7.1 Backlight on/off (BLON) and brightness adjustment (VDIM_IN / VDIM_OUT)

The backlight unit can be controlled to turn on or turn off by BLON signal that is in the pin 1 of J2. The input voltage specification of BLON signal is described in section 3.3. If the input voltage level is low, the backlight unit will be turned off. If high, it will be turned on.

The backlight unit also can be controlled to adjust brightness by VDIM_IN signal that is in pin 2 of J2. The input voltage range is from 0V to 3V. The maximum brightness is acquirement when the input voltage is 0V. If the input voltage is 3V, the backlight unit will present the minimum brightness.

You can use I2C interface protocol to program DS1805 (DAC, Digital-to-Analog Converter) by pin7, 8 of J1. The port-1 of DS1805 will generate one voltage that you want. Then, the voltage is sent to VDIM_OUT signal that is in pin 3 of J2. The systems can feedback this signal to VDIM_IN signal to control the BLU brightness. Please refer to I2C interface protocol in MAXIM DS1805 datasheet for brightness adjustment.



Panel control board

7.2. I2C Specification

Following describes the I2C specifications equipped in the LCD module. Since the DAC (MAXIM DS1805) is used for Brightness, please refer to its own specifications in detail. 2 signals (SCL_DAC and SDA_DAC) in the LCD module interface are used for the DAC. The address for DAC is '0101101'b. Its port-1 is for Brightness. Reserved addresses are from '0010000'b to '0011111'b and from '0110000'b to '0111111'b.

7.2.1 I2C Feature Summary

- Standard mode (100KHz max) support
- 3.3V interface
- Slave mode operation only

7.2.2 Electrical Specification

2 signals (SCL_DAC and SDA_DAC) are equipped at the LCD module interface. SCL_DAC is the clock input and SDA_DAC is the data input/output. These signals should be driven by Open-Drain or Open-Collector without any pull-up resister. Both signals are pulled up by 4.7K ohm resisters to 3.3V(typ.) respectively in the LCD module.

Electrical Specification of I2C Slave

	Symbol	Min	Max	Unit
Input Low voltage	Vil	-0.5	0.5	V
Input High voltage	Vih	2.3	3.6	V
Input Hysteresis voltage	Vhys	0.4	-	V
Input leakage current @ Vil-Min or Vih-Max (*1)	Ii	-30	30	uA
Output Low voltage	Vol	-	0.5	V
Output High impedance leakage current (*3)	Ioh	-30	30	uA

NOTE:

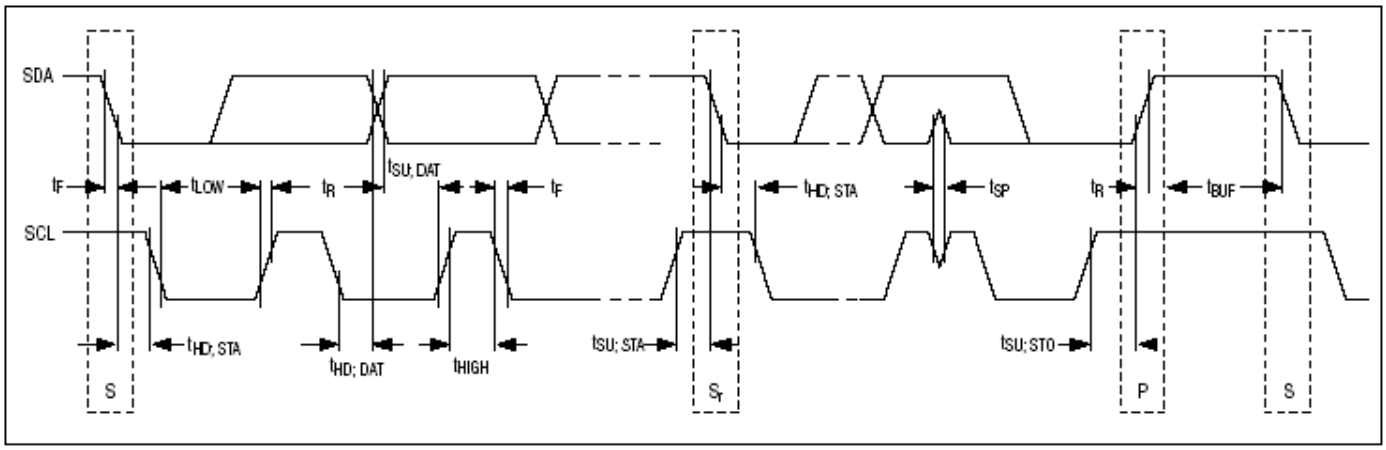
*1: Without pull up resisters (4.7K ohm)

8.2.3 Timing Specification

In the following figure and table, slave is the MCU in the LCD module and master is the scalar to drive the LCD module.

“S” is the START condition and “P” is the STOP condition.

I2C Bus timing



I2C Timing Specification of I2C Slave

	Symbol	Min	Max	Unit	Notes
Frequency of SCL	fSCL	0	100	KHz	
Bus Free Time from STOP to START	tBUF	4.7	-	us	
Setup time of START(Repeated START)	tSU:STA	4.7	-	us	
Hold time of START(Repeated START)	tHD:STA	4.0	-	us	
Low time of SCL	tLOW	4.7	-	us	
High time of SCL	tHIGH	4.0	-	us	
Data hold time	tHD:DAT	0	-	us	
Data setup time	tSU:DAT	250	-	ns	
Data change from SCL falling edge (to master)	tCH:DAT	300	900	ns	
Rise time	tR	-	1000	ns	
Fall time	tF	-	300	ns	
Setup time of STOP	tSU:STO	4.0	-	us	
Spike suppression	tSP	-	50	ns	

8. PACKING

8.1 PACKING SPECIFICATIONS

(1) 5 LCD modules / 1 Box

(2) Box dimensions: 468(L) X 402(W) X 591(H) mm

(3) Weight: approximately: 15kg (5 modules per box)

8.2 PACKING METHOD

(1) Carton Packing should have no failure in the following reliability test items.

Test Item	Test Conditions	Note
Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Dropping Test	1 Corner , 3 Edge, 6 Face, 61cm	Non Operation

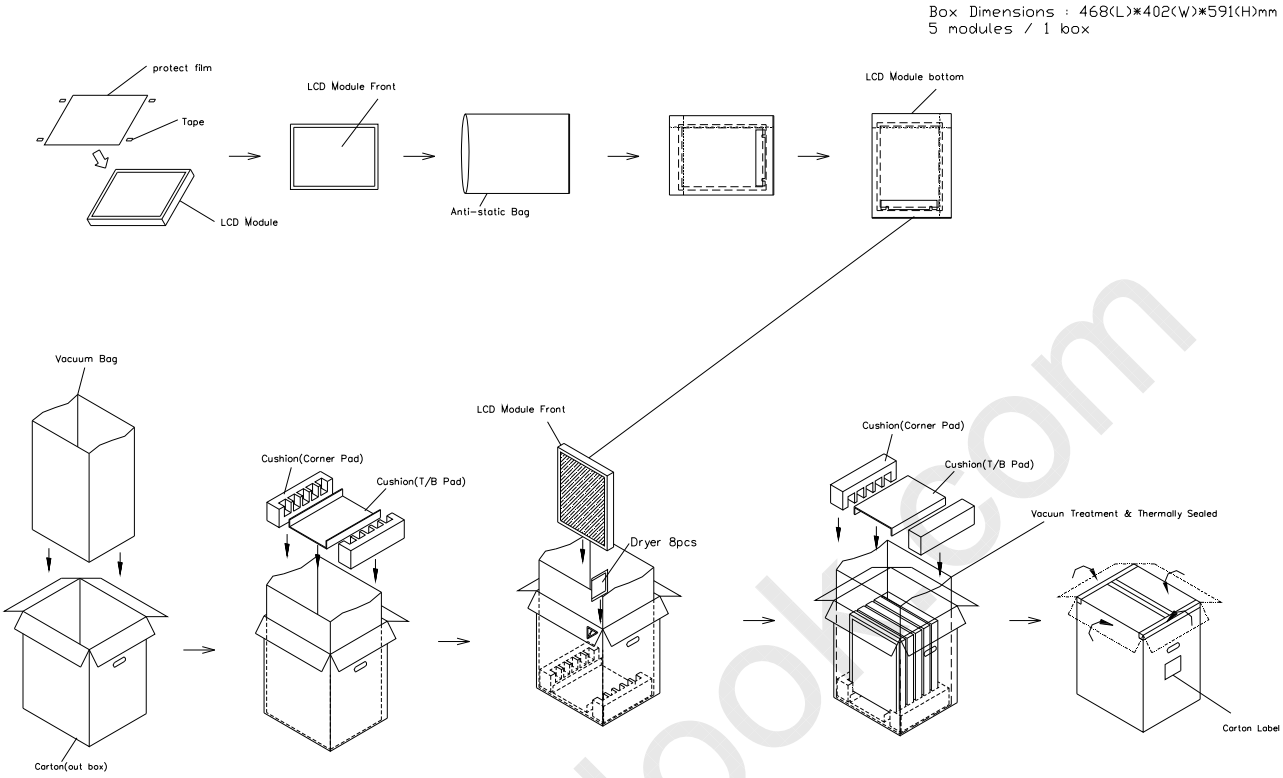
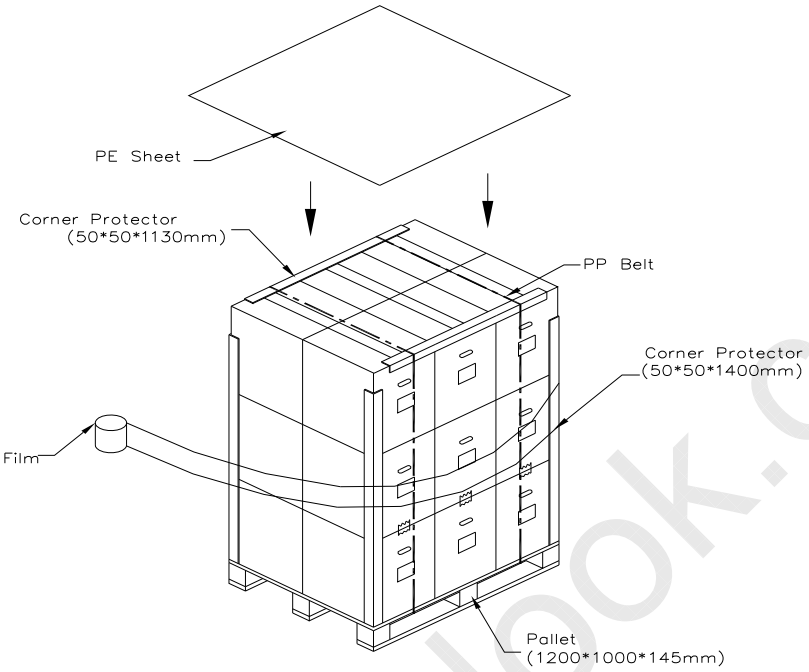


Figure. 8-1 Packing method

8.3 PALLET

Sea and land transportation



Air transportation

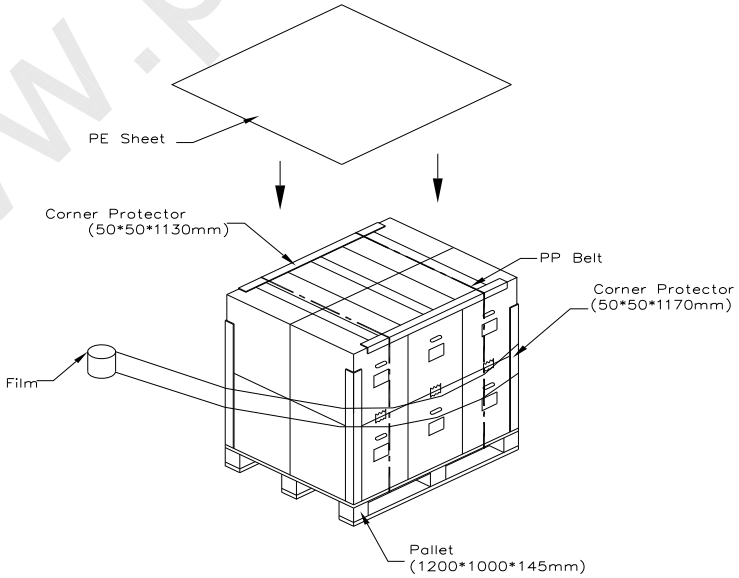
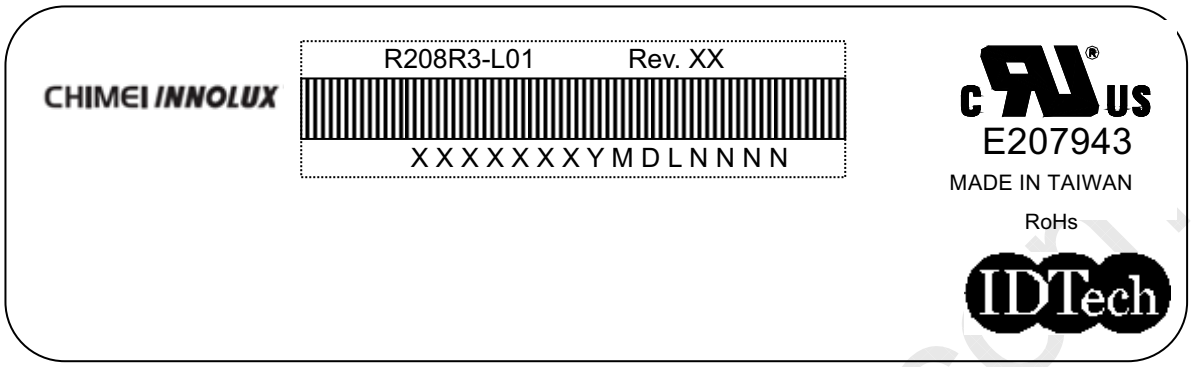


Figure. 8-2 Packing method

9. CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: R208R3-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) CMI barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMI internal use	-
XX	Revision	Cover all the change
X	CMI internal use	-
XX	CMI internal use	-
YMD	Year, month, day	Year: 0~9, 2001=1, 2002=2, 2003=3…2010=0, 2011=1, 2012=2… Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U.
L	Product line #	Line 1=1, Line 2=2, Line 3=3, …
NNNN	Serial number	Manufacturing sequence of product

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10)When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

10.2 STORAGE PRECAUTIONS

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0℃ to 35℃ and relative humidity of less than 70%

(2) Do not store the TFT – LCD module in direct sunlight

(3) The module should be stored in dark place. It is prohibited to apply sunlight or fluorescent light in storing

10.3 OPERATION PRECAUTIONS

(1) The LCD product should be operated under normal condition.

Normal condition is defined as below :

Temperature : 20±15℃

Humidity: 65±20%

Display pattern: continually changing pattern (Not stationary)

(2) If the product will be used in extreme conditions such as high temperature, high humidity, high altitude ,display pattern or operation time etc…It is strongly recommended to contact CMO for application engineering advice . Otherwise, Its reliability and function may not be guaranteed.

10.4 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the module's end of life, it is not harmful in case of normal operation and storage.

10.5 SAFETY STANDARDS

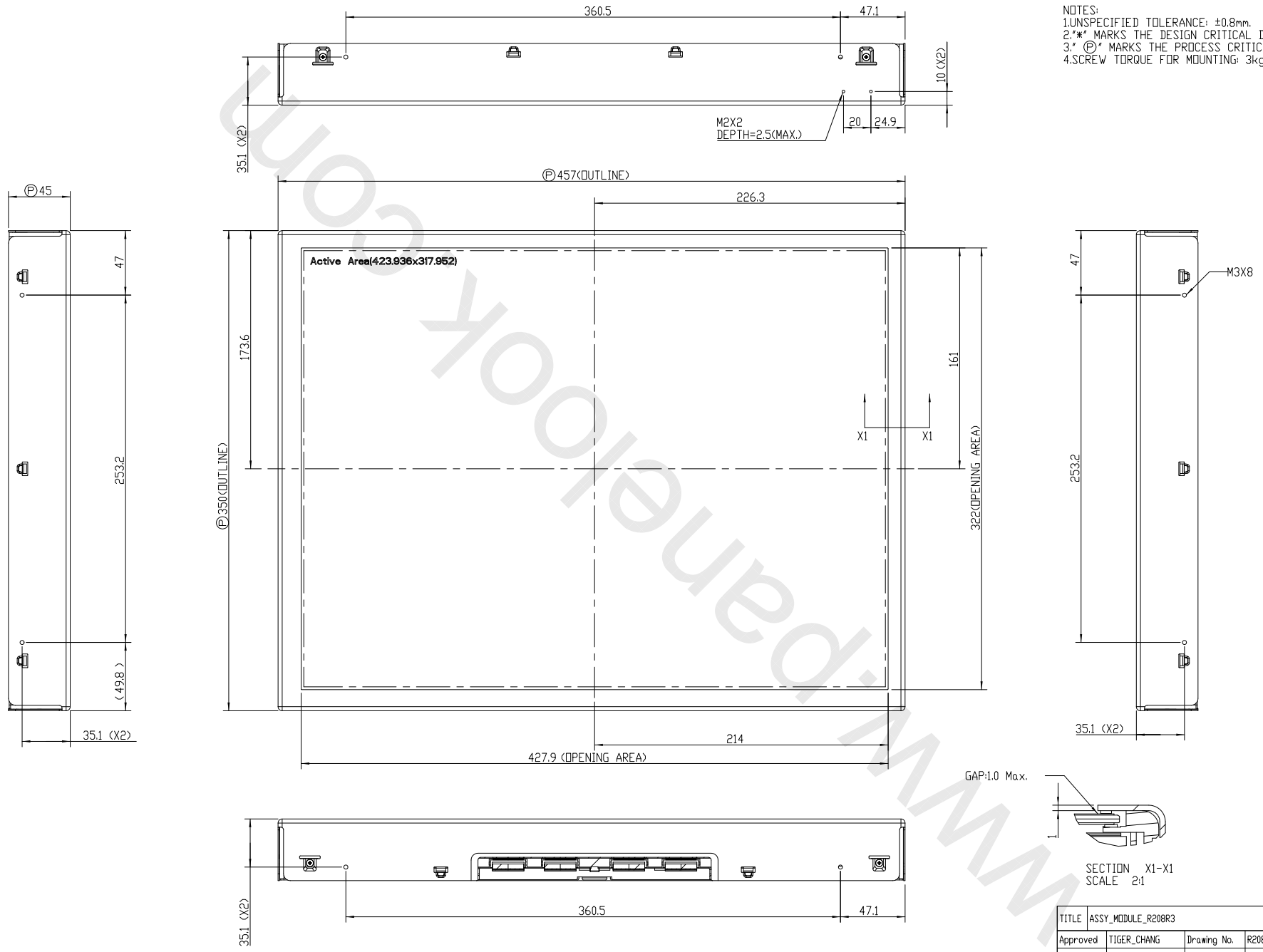
The LCD module should be certified with safety regulations as follows:

(1) UL60950-1 or updated standard.

(2) IEC60950-1 or updated standard.

10.6 OTHER

When fixed patterns are displayed for a long time, remnant image is likely to occur.



NOTES:
1.UNSPECIFIED TOLERANCE: ±0.8mm.
2."*" MARKS THE DESIGN CRITICAL DIMENSION.
3." Ⓟ" MARKS THE PROCESS CRITICAL DIMENSION.
4.SCREW TORQUE FOR MOUNTING: 3kgf-cm(MAX.)

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
A	Add Al Tape	2007.08.29	Honglong	Tiger_Chang	EA0022801	

TITLE	ASSY_MODULE_R208R3			2D REV.	B
				3D REV.	1.13
Approved	TIGER_CHANG	Drawing No.	R20814101B		
Checked	ALAN_LEE	Part No.	RK8R301902		
Drawer	HONGLONG_HSU	Material	TBD	Sheet	1 / 2 A2
Designer	TIGER_CHANG	Date	29-Aug-2007	Scale	1:2 Unit:mm

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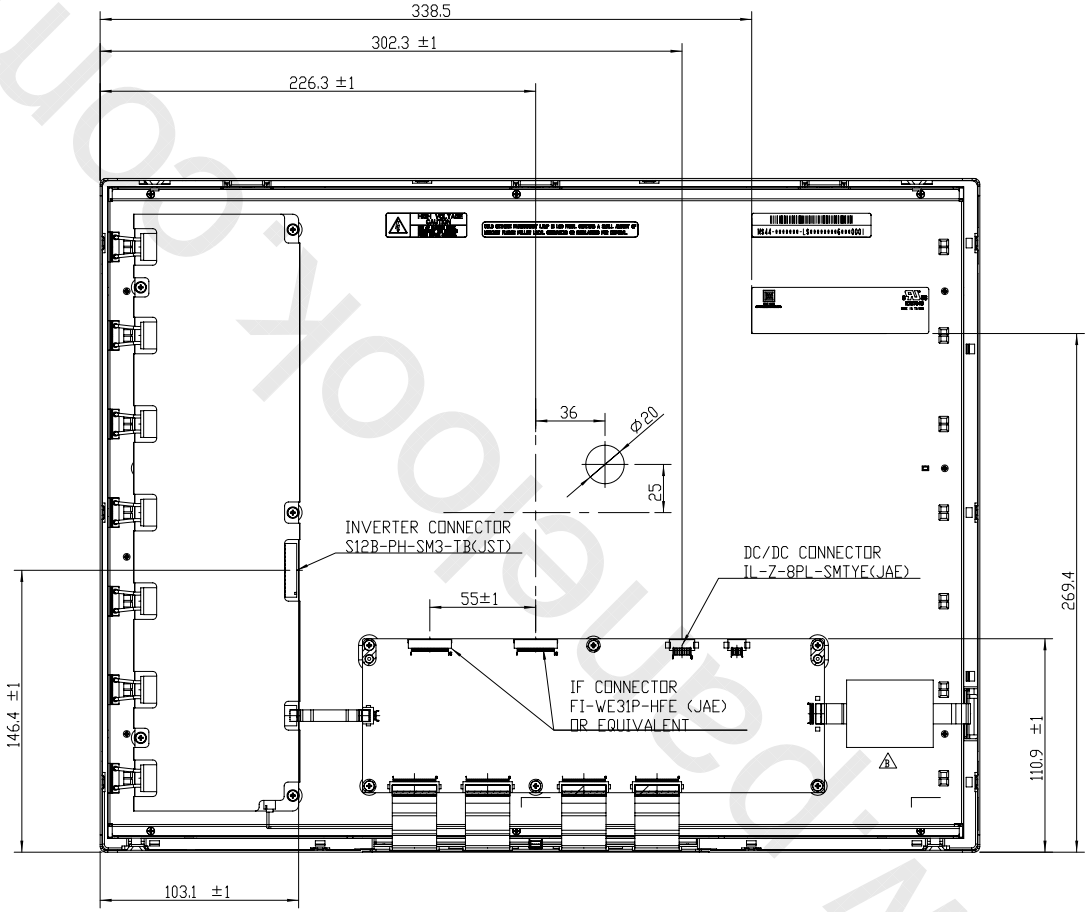

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A	Add Al Tape	2007.08.29	Honglong	Tiger_Chang	EA0022801	

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