RX13T Group
Renesas MCUs

R01DS0341EJ0110
Rev.1.10
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32-MHz 32-bit RX MCUs, built-in FPU, 50 DMIPS, power supply 5 V
12-bit ADC (equipped with 3-channel synchronous S/H circuits, programmable gain amplifier × 3 ch, and comparator)
32-MHz PWM (three-phase complementary output × 1 ch), On-chip data flash memory

Features

■ 32-bit RX CPU core
- Max. operating frequency: 32 MHz
  Capable of 50 DMIPS in operation at 32 MHz
- Accumulator handles 64-bit results (for a single instruction) from 32-bit × 32-bit operations
- Multiplication and division unit handles 32-bit × 32-bit operations (multiplication instructions take one CPU clock cycle)
- Built-in FPU: 32-bit single-precision floating point (compliant to IEEE754)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit

■ Low power design and architecture
- Operation from a single 2.7-V to 5.5-V supply
- Three low power consumption modes

■ On-chip code flash memory, no wait states
- 128-/64-Kbyte capacities
- On-board or off-board user programming
- For instructions and operands

■ On-chip data flash memory
- 4 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states
- 12 Kbytes of SRAM

■ DMA
- DTC: Five transfer modes

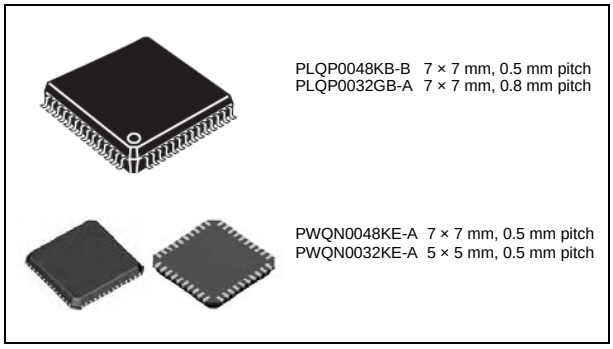
■ Reset and supply management
- Seven types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- Main clock oscillator frequency: 1 to 20 MHz
- External clock input frequency: Up to 20 MHz
- PLL circuit input: 4 MHz to 8 MHz
- Low-speed on-chip oscillator: 4 MHz
- High-speed on-chip oscillator: 32 MHz ±1%
- IWDT-dedicated on-chip oscillator: 15 kHz
- On-chip clock frequency accuracy measurement circuit (CAC)

■ Independent watchdog timer
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ MPC
- Multiple locations are selectable for I/O pins of peripheral functions



■ Up to 4 communications channels
- SCI with many useful functions (3 channels)
  Asynchronous mode, clock synchronous mode, smart card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- I^2C bus interface: Transfer at up to 400 kbps (one channel)

■ Up to 8 extended-function timers
- 16-bit MTU3 (six channels): 32 MHz operation, input capture, output compare, three-phase complementary PWM × 1 channel-output, CPU-efficient complementary PWM, phase counting mode (2 channels)
- 16-bit compare-match timers (2 channels)

■ 12-bit A/D converter: 8 ch
- On-chip sample-and-hold circuit: 12-bit × up to 3 channels
- Sampling time can be set for each channel
- Group scan priority control mode (3 levels)
- Self-diagnostic function and analog input disconnection detection assistance function (compliant to IEC60730)
- Input signal amplitude by the programmable gain amplifier (3 channels)
- ADC: 3-channel simultaneous sample-and-hold circuit (3 shunt method), double data register (1 shunt method), amplifier (3 channels), comparator (3 channels)

■ Register write protection function can protect values in important registers against overwriting.

■ Up to 39 pins for general I/O ports
- 5-V tolerant, open drain, input pull-up

■ Operating temperature range
- –40 to +85°C
- –40 to +105°C

■ Applications
- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/3)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit registers • Basic instructions: 73 Variable-length instruction format • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 64 K/128 Kbytes • 32 MHz, no-wait memory access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 12 Kbytes • 32 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 4 Kbytes • Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, low-speed and high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC): Available • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 32 MHz (at max.) Peripheral modules run in synchronization with the PCLKB: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) The ICLK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1, 2, 4, 8, 16, 32, 64)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 9 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode and middle-speed operating mode

Table 1.1 Outline of Specifications (2/3)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 256 • External interrupts: 7 (NMI, IRQ0 to IRQ5 pins) • Non-maskable interrupts: 5 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	Data transfer controller (DTCb)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: External interrupts and interrupt requests from peripheral functions • Sequence transfer
I/O ports	General I/O ports	48-/32-pin • I/O: 38/22 • Input: 1/1 • Pull-up resistors: 38/22 • Open-drain outputs: 30/18 • 5-V tolerance: 2/2
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 3 (MTU3c)	• 6 units (16 bis × 6 channels) • Provides up to 16 pulse-input/output lines and three pulse-input lines • Select from among fourteen counter-input clock signals for each channel (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, PCLK/32, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) other than channel 1/3/4, for which only eleven signals are available, channel 2 for 12, channel 5 for 10 • 26 output compare/input capture registers • Counter clear operation (with compare match- or input capture-sourced simultaneous counter clear capability) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffer operation • Cascaded operation • 28 interrupt sources • Automatic transfer of register data • Pulse output modes: Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode 3-phase non-overlapping waveform output for inverter control Automatic dead time setting Adjustable PWM duty cycle: from 0 to 100% A/D conversion request delaying function Interrupt at crest/trough can be skipped Double buffer function • Reset-synchronized PWM mode Outputs three phases each for positive and negative PWM waveforms in user-specified duty cycle • Phase counting modes: 16-bit mode (channel 1 and 2)/32-bit mode (channel 1 and 2) • Dead time compensation counter function • A/D converter start trigger can be generated • A/D converter start triggers can be skipped • Signals from the input capture and external counter clock pins are input via a digital filter
	Port output enable 3 (POE3C)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 3 channels (channel 1 and 5: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from MTU timers Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
12-bit A/D converter (S12ADF)		• 12 bits (8 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Assist on analog input disconnection detection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), or an external trigger signal • Sample-and-hold function Sample-and-hold circuit included (3 channels) • Amplification of input signals by a programmable gain amplifier (3 channels) Amplification rate: 2.000 times, 2.500 times, 3.077 times, 5.000 times, 8.000 times, 10.000 times (total of 6 steps)
Comparator C (CMPC)		• 3 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage: Select from among two voltages • Analog input voltage: Select from among four voltages
D/A converter (DA) for generating comparator C reference voltage		• 1 channel • 8-bit resolution • Output voltage: 0 to AVCC0 • Reference voltage generation circuit for comparator C
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 2.7 to 5.5V: 32 MHz
Supply current		11 mA at 32 MHz (typ.)
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 32-pin LQFP (PLQP0032GB-A) 7 × 7 mm, 0.8 mm pitch 48-pin HWQFN (PWQN0048KE-A) 7 × 7 mm, 0.5 mm pitch 32-pin HWQFN (PWQN0032KE-A) 5 × 5 mm, 0.5 mm pitch
Debugging interface		FINE interface

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX13T Group	
		48 Pins	32 Pins
Interrupts	External interrupts	NMI, IRQ0 to IRQ5	NMI, IRQ0 to IRQ2, IRQ5
DTC	Data transfer controller	Available	
Timers	Multi-function timer pulse unit 3	6 channels	
	Port output enable 3	POE0#, POE8#, POE10#	POE8#, POE10#
	Compare match timer	2 channels × 1 units	
	Independent watchdog timer	Available	
Communication functions	Serial communications interfaces (SCIg)	2 channels (SCI1, SCI5)	
	Serial communications interfaces (SCIh)	1 channel (SCI12)	
	I^2C bus interface	1 channel	
12-bit A/D converter		8 channels	5 channels
Comparator C		3 channels	
CRC calculator		Available	
Data operation circuit		Available	
Clock frequency accuracy measurement circuit		Available	
Packages		48-pin LFQFP (0.5 mm) 48-pin HWQFN (0.5 mm)	32-pin LQFP (0.8 mm) 32-pin HWQFN (0.5 mm)

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX13T (D version)	R5F513T5ADFL	R5F513T5ADFL#30	PLQP0048KB-B	128 Kbytes	12 Kbytes	4 Kbytes	32 MHz	–40 to +85°C
	R5F513T5ADNE	R5F513T5ADNE#20	PWQN0048KE-A					
	R5F513T5ADFJ	R5F513T5ADFJ#30	PLQP0032GB-A					
	R5F513T5ADNH	R5F513T5ADNH#20	PWQN0032KE-A					
	R5F513T3ADFL	R5F513T3ADFL#30	PLQP0048KB-B	64 Kbytes				
	R5F513T3ADNE	R5F513T3ADNE#20	PWQN0048KE-A					
	R5F513T3ADFJ	R5F513T3ADFJ#30	PLQP0032GB-A					
	R5F513T3ADNH	R5F513T3ADNH#20	PWQN0032KE-A					
RX13T (G version)	R5F513T5AGFL	R5F513T5AGFL#30	PLQP0048KB-B	128 Kbytes				–40 to +105°C
	R5F513T5AGNE	R5F513T5AGNE#20	PWQN0048KE-A					
	R5F513T5AGFJ	R5F513T5AGFJ#30	PLQP0032GB-A					
	R5F513T5AGNH	R5F513T5AGNH#20	PWQN0032KE-A					
	R5F513T3AGFL	R5F513T3AGFL#30	PLQP0048KB-B	64 Kbytes				
	R5F513T3AGNE	R5F513T3AGNE#20	PWQN0048KE-A					
	R5F513T3AGFJ	R5F513T3AGFJ#30	PLQP0032GB-A					
	R5F513T3AGNH	R5F513T3AGNH#20	PWQN0032KE-A					

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.

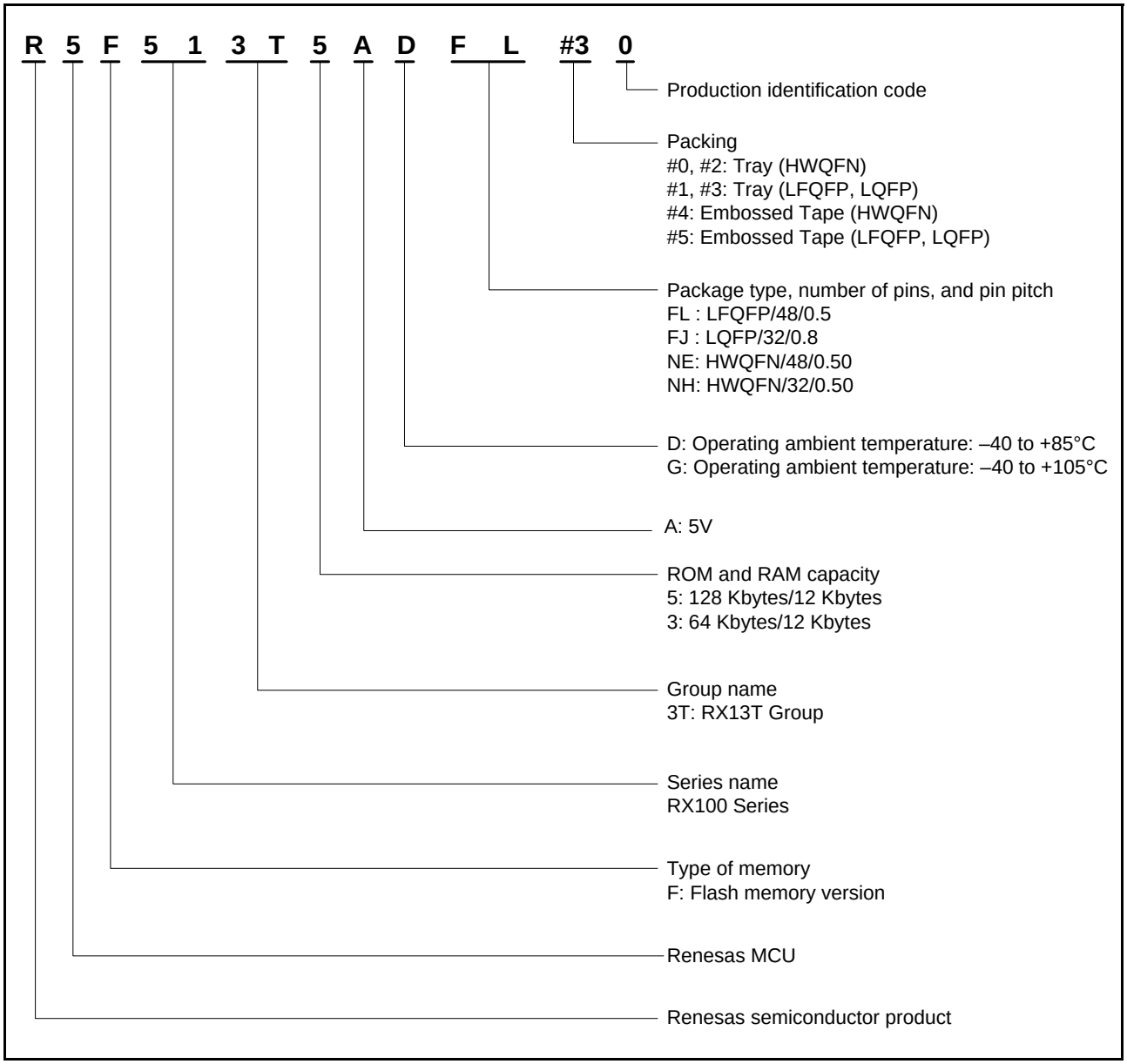


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

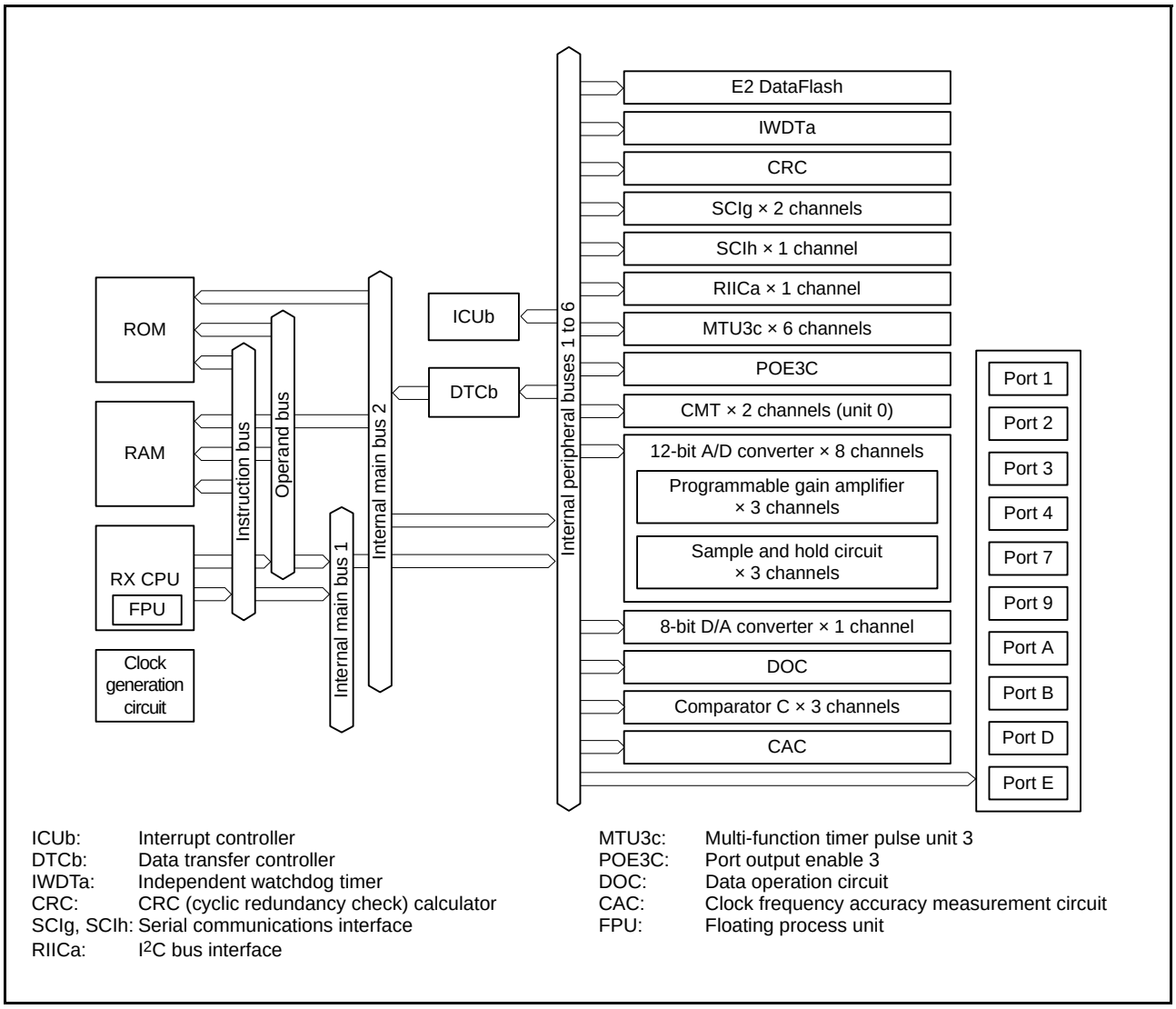


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/2)

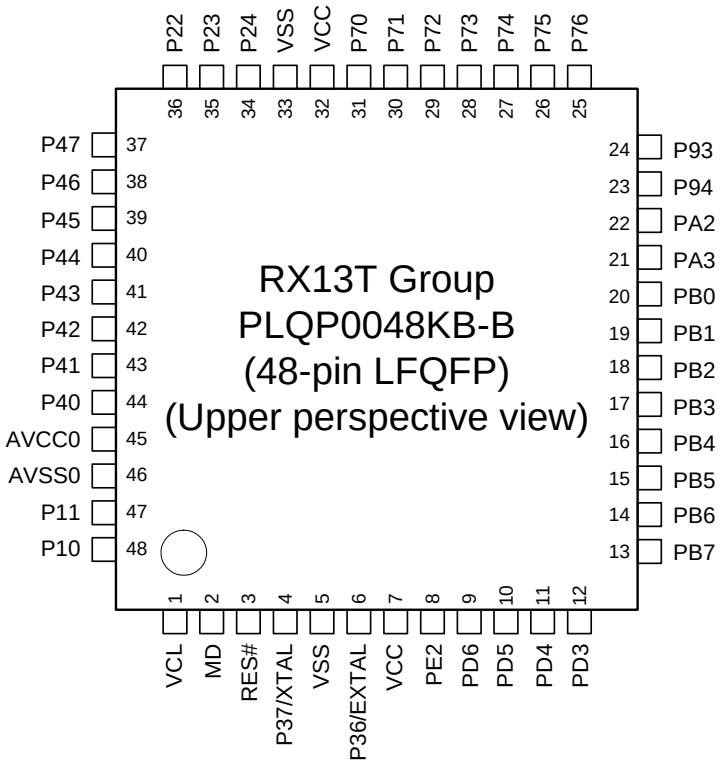
Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ5	Input	Interrupt request pins.
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	ADSM0	Output	A/D trigger output pin.
Port output enable 3	POE0#, POE8#, POE10#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	RXD1, RXD5	Input	Input pins for received data.
	TXD1, TXD5	Output	Output pins for transmitted data.
	CTS1#, CTS5#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5	I/O	Input/output pins for the clock.
	SMISO1, SMISO5	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5	I/O	Input/output pins for master transmit data.
	SS1#, SS5#	Input	Chip-select input pins.

Table 1.4 Pin Functions (2/2)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for SCIf received data
	TXDX12	Output	Output pin for SCIf transmitted data
	SIOX12	I/O	Input/output pin for SCIf received or transmitted data
I^2C bus interface	SCL0	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.
12-bit A/D converter	AN000 to AN007	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
	ADST0	Output	Output pin for A/D conversion status.
Comparator C	CMPC00, CMPC02, CMPC03	Input	Analog input pin for CMPC0
	CMPC10, CMPC12, CMPC13	Input	Analog input pin for CMPC1
	CMPC20, CMPC22	Input	Analog input pin for CMPC2
	COMP0 to COMP2	Output	Comparator detection result output pins.
	CVREFC0	Input	Analog reference voltage supply pins for comparator C.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter, comparator C, and the 8-bit D/A converter for generating comparator C reference voltage. Connect this pin to VCC when these modules are not used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter, comparator C, and the 8-bit D/A converter for generating comparator C reference voltage. Connect this pin to VSS when these modules are not used.
I/O ports	P10, P11	I/O	2-bit input/output pins.
	P22 to P24	I/O	3-bit input/output pins.
	P36, P37	I/O	2-bit input/output pins.
	P40 to P47	I/O	8-bit input/output pins.
	P70 to P76	I/O	7-bit input/output pins.
	P93, P94	I/O	2-bit input/output pins.
	PA2, PA3	I/O	2-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD3 to PD6	I/O	4-bit input/output pins.
	PE2	Input	1-bit input pin.

1.5 Pin Assignments

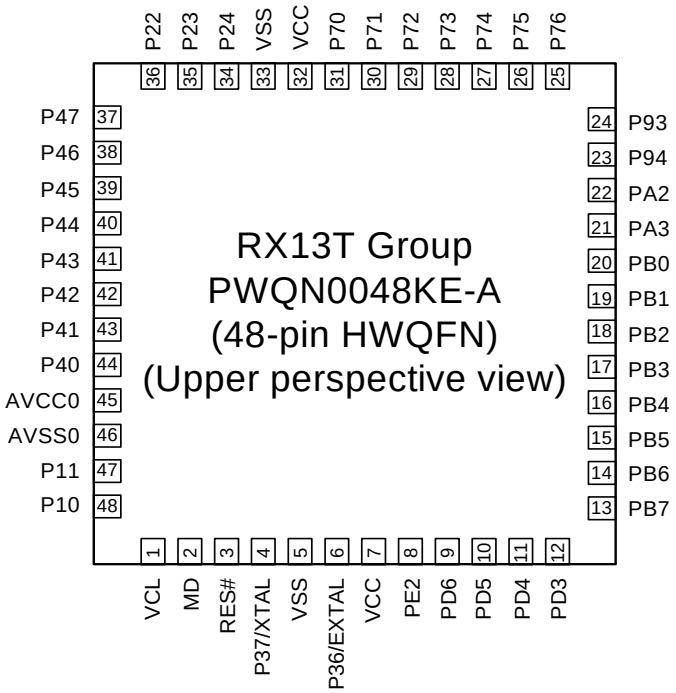
1.5.1 48-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)”.

Figure 1.3 Pin Assignments of the 48-Pin LFQFP

1.5.2 48-Pin HWQFN

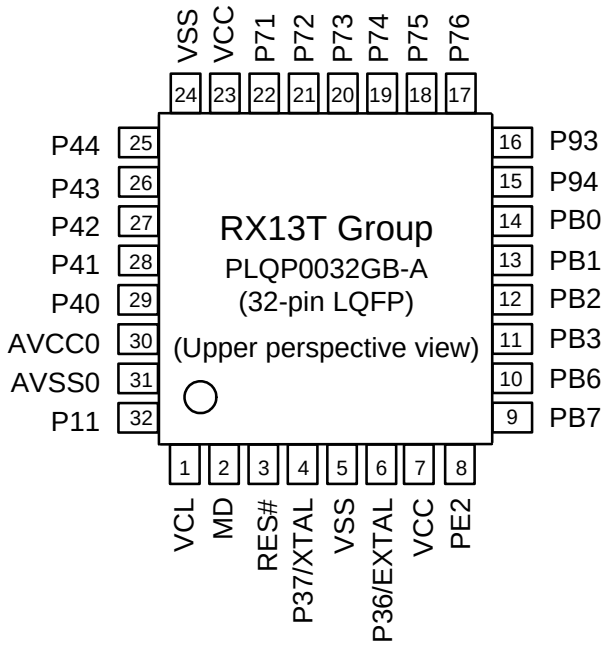


Note: It is recommended to connect an exposed die pad to VSS.

Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)”.

Figure 1.4 Pin Assignments of the 48-Pin HWQFN

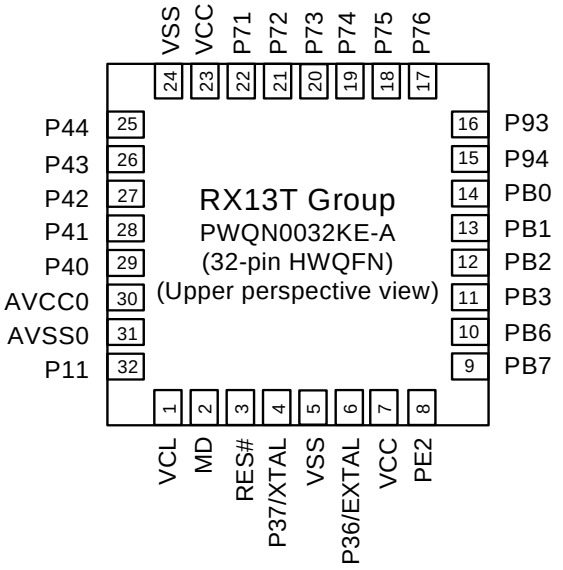
1.5.3 32-Pin LQFP



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (32-Pin LQFP/HWQFN)”.

Figure 1.5 Pin Assignments of the 32-Pin LQFP

1.5.4 32-Pin HWQFN



Note: It is recommended to connect an exposed die pad to VSS.

Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (32-Pin LQFP/HWQFN)”.

Figure 1.6 Pin Assignments of the 32-Pin HWQFN

1.6 List of Pins and Pin Functions

1.6.1 48-Pin LFQFP/HWQFN

Table 1.5 List of Pins and Pin Functions (48-Pin LFQFPLQFP/HWQFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, CAC)	Communications (SCI, RIIC)	Others
1	VCL				
2	MD				FINED
3	RES#				
4	XTAL	P37			
5	VSS				
6	EXTAL	P36			
7	VCC				
8		PE2	POE10#		NMI/IRQ0
9		PD6	MTIOC0D	CTS1#/RTS1#/SS1#	IRQ5/ADST0
10		PD5	MTIOC0C	RXD1/SMISO1/SSCL1	IRQ3
11		PD4	MTIOC0B	SCK1	IRQ2
12		PD3	MTIOC0A	TXD1/SMOSI1/SSDA1	
13		PB7	MTIOC3C/MTCLKD	RXD1/SMISO1/SSCL1/RXD5/SMISO5/ SSCL5	IRQ5
14		PB6	MTIOC1B/MTIOC3A	TXD1/SMOSI1/SSDA1/TXD5/SMOSI5/ SSDA5	
15		PB5			ADTRG0#
16		PB4	POE8#		IRQ3
17		PB3	MTIOC0A/CACREF	SCK5/SCK12	
18		PB2	MTIOC0B/MTCLKC/ADSM0	TXD5/SMOSI5/SSDA5/SDA0	
19		PB1	MTIOC0C/MTIC5W/MTCLKA	RXD5/SMISO5/SSCL5/SCL0	IRQ2
20		PB0	MTIOC0D/MTIOC2A/MTCLKB	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12	
21		PA3	MTIOC1B/MTIOC2A	CTS12#/RTS12#/SS12#	
22		PA2	MTIOC1A/MTIOC2B	CTS5#/RTS5#/SS5#	IRQ4
23		P94	MTIOC2B/MTIC5U/MTCLKA	RXD12/RXDX12/SMISO12/SSCL12	IRQ1
24		P93	MTIOC1A/MTIC5V	SCK5/SCK12	IRQ0/ADTRG0#
25		P76	MTIOC4D		
26		P75	MTIOC4C		
27		P74	MTIOC3D		
28		P73	MTIOC4B		
29		P72	MTIOC4A		
30		P71	MTIOC3B		
31		P70	POE0#		IRQ5
32	VCC				
33	VSS				
34		P24	MTIC5U	RXD5/SMISO5/SSCL5	IRQ3/COMP0
35		P23	MTIC5V/CACREF	TXD5/SMOSI5/SSDA5	IRQ4/COMP1
36		P22	MTIC5W		IRQ2/COMP2
37		P47*1			AN007/CMPC13
38		P46*1			AN006/CMPC03
39		P45*1			AN005/CMPC22
40		P44*1			AN004/CMPC12
41		P43*1			AN003/CMPC02
42		P42*1			AN002/CMPC20
43		P41*1			AN001/CMPC10
44		P40*1			AN000/CMPC00
45	AVCC0				
46	AVSS0				
47		P11	MTIOC3A/MTCLKA/POE8#		IRQ1/CVREFC0

Table 1.5 List of Pins and Pin Functions (48-Pin LFQFPLQFP/HWQFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, CAC)	Communications (SCI, RIIC)	Others
48		P10	MTCLKB		IRQ0

Note 1. The power source of the I/O buffer for these pins is AVCC0.

1.6.2 32-Pin LQFP/HWQFN

Table 1.6 List of Pins and Pin Functions (32-Pin LQFP/HWQFN)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, CAC)	Communications (SCI, RIIC)	Others
1	VCL				
2	MD				FINED
3	RES#				
4	XTAL	P37			
5	VSS				
6	EXTAL	P36			
7	VCC				
8		PE2	POE10#		NMI/IRQ0
9		PB7	MTIOC3C/MTCLKD	RXD1/SMISO1/SSCL1/RXD5/SMISO5/ SSCL5	IRQ5
10		PB6	MTIOC1B/MTIOC3A	TXD1/SMOSI1/SSDA1/TXD5/SMOSI5/ SSDA5	
11		PB3	MTIOC0A/CACREF	SCK5/SCK12	
12		PB2	MTIOC0B/MTCLKC/ADSM0	TXD5/SMOSI5/SSDA5/SDA0	
13		PB1	MTIOC0C/MTIC5W/MTCLKA	RXD5/SMISO5/SSCL5/SCL0	IRQ2
14		PB0	MTIOC0D/MTIOC2A/MTCLKB	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12	
15		P94	MTIOC2B/MTIC5U/MTCLKA	RXD12/RXDX12/SMISO12/SSCL12	IRQ1
16		P93	MTIOC1A/MTIC5V	SCK5/SCK12	IRQ0/ADTRG0#
17		P76	MTIOC4D		
18		P75	MTIOC4C		
19		P74	MTIOC3D		
20		P73	MTIOC4B		
21		P72	MTIOC4A		
22		P71	MTIOC3B		
23	VCC				
24	VSS				
25		P44*1			AN004/CMPC12
26		P43*1			AN003/CMPC02
27		P42*1			AN002/CMPC20
28		P41*1			AN001/CMPC10
29		P40*1			AN000/CMPC00
30	AVCC0				
31	AVSS0				
32		P11	MTIOC3A/MTCLKA/POE8#		IRQ1/CVREFC0

Note 1. The power source of the I/O buffer for these pins is AVCC0.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	P40 to P47	V_{in}	–0.3 to AVCC0+0.3	V
	PB1, PB2 (5-V tolerant)		–0.3 to +6.5	
	Other than above		–0.3 to VCC+0.3	
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN007 used	V_{AN}	–0.3 to AVCC0+0.3	V
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, and between the AVCC0 and AVSS0 pins. Place capacitors with values of about 0.1 µF as close as possible to every power supply pin and use the shortest and widest possible traces for the wiring.
Connect the VCL pin to a VSS pin via a 4.7-µF capacitor. The capacitor must be placed close to the pin.
Do not input signals to ports other than 5-V tolerant ports while the device is not powered.
The current injection that results from input of such a signal may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

2.2 Recommended operating conditions

Table 2.2 Recommended Operating Conditions (1)

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltages		VCC*1, *2	2.7	—	5.5	V
		VSS	—	0	—	
Analog power supply voltages		AVCC0*1, *2	VCC	—	5.5	V
		AVSS0	—	0	—	
Operating temperature	D version	T_{opr}	–40	—	85	°C
	G version		–40	—	105	

Note 1. AVCC0 and VCC can be set individually within the operating range.
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	4.7 µF ±3.0%*1

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 4.7 µF and a capacitance tolerance is ±30% or better.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5-V tolerant)	V_{IH}	0.7 × VCC	—	5.8	V	
	PB1, PB2 (5-V tolerant)		0.8 × VCC	—	5.8		
	P10, P11, P22 to P24, P36, P37, P70 to P76, P93, P94, PA2, PA3, PB0, PB3 to PB7, PD3 to PD6, PE2, RES#		0.8 × VCC	—	VCC + 0.3		
	P40 to P47		0.8 × AVCC0	—	AVCC0 + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	0.3 × VCC		
	P40 to P47		–0.3	—	0.2 × AVCC0		
	Other than RIIC input pin or P40 to P47		–0.3	—	0.2 × VCC		
Schmitt trigger input hysteresis	RIIC input pin (except for SMBus)	ΔV_T	0.05 × VCC	—	—		
	P40 to P47		0.1 × AVCC0	—	—		
	Other than RIIC input pin or P40 to P47		0.1 × VCC	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	0.9 × VCC	—	VCC + 0.3	V	
	EXTAL (external clock input)		0.8 × VCC	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	0.1 × VCC		
	EXTAL (external clock input)		–0.3	—	0.2 × VCC		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Table 2.5 DC Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, PE2	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	P40 to P47	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V, AVCC0
	PB1, PB2 (5-V tolerant)		—	—	1.0		V_{in} = 0 V, 5.8 V
	Other than above		—	—	0.2		V_{in} = 0 V, VCC
Input capacitance	All input pins	C_{in}	—	4	15	pF	V_{in} = 0 mV, f = 1 MHz, T_a = 25°C
Input pull-up resistor	All ports (except for PE2)	R_U	10	20	50	kΩ	V_{in} = 0 V

Table 2.6 DC Characteristics (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.*4	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.1	—	mA	
				ICLK = 16 MHz		2.1	—		
				ICLK = 8 MHz		1.6	—		
			All peripheral operation: Normal *3	ICLK = 32 MHz		10.6	—		
				ICLK = 16 MHz		6.0	—		
				ICLK = 8 MHz		3.6	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	18.1		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.5	—		
				ICLK = 16 MHz		1.2	—		
				ICLK = 8 MHz		1.0	—		
			All peripheral operation: Normal *3	ICLK = 32 MHz		5.6	—		
				ICLK = 16 MHz		3.3	—		
				ICLK = 8 MHz		2.1	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.0	—		
				ICLK = 16 MHz		0.9	—		
				ICLK = 8 MHz		0.8	—		
			All peripheral operation: Normal *3	ICLK = 32 MHz		3.8	—		
				ICLK = 16 MHz		2.3	—		
				ICLK = 8 MHz		1.6	—		
		Increase during BGO operation*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz		1.9	—		
				ICLK = 8 MHz		1.3	—		
				ICLK = 1 MHz		0.3	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		4.8	—		
				ICLK = 8 MHz		3.3	—		
				ICLK = 1 MHz		0.9	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	8.2		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.2	—		
				ICLK = 8 MHz		0.7	—		
				ICLK = 1 MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.8	—		
				ICLK = 8 MHz		1.9	—		
				ICLK = 1 MHz		0.7	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.0	—		
				ICLK = 8 MHz		0.6	—		
				ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		2.1	—		
				ICLK = 8 MHz		1.5	—		
				ICLK = 1 MHz		0.6	—		
		Increase during BGO operation*5				2.5	—		

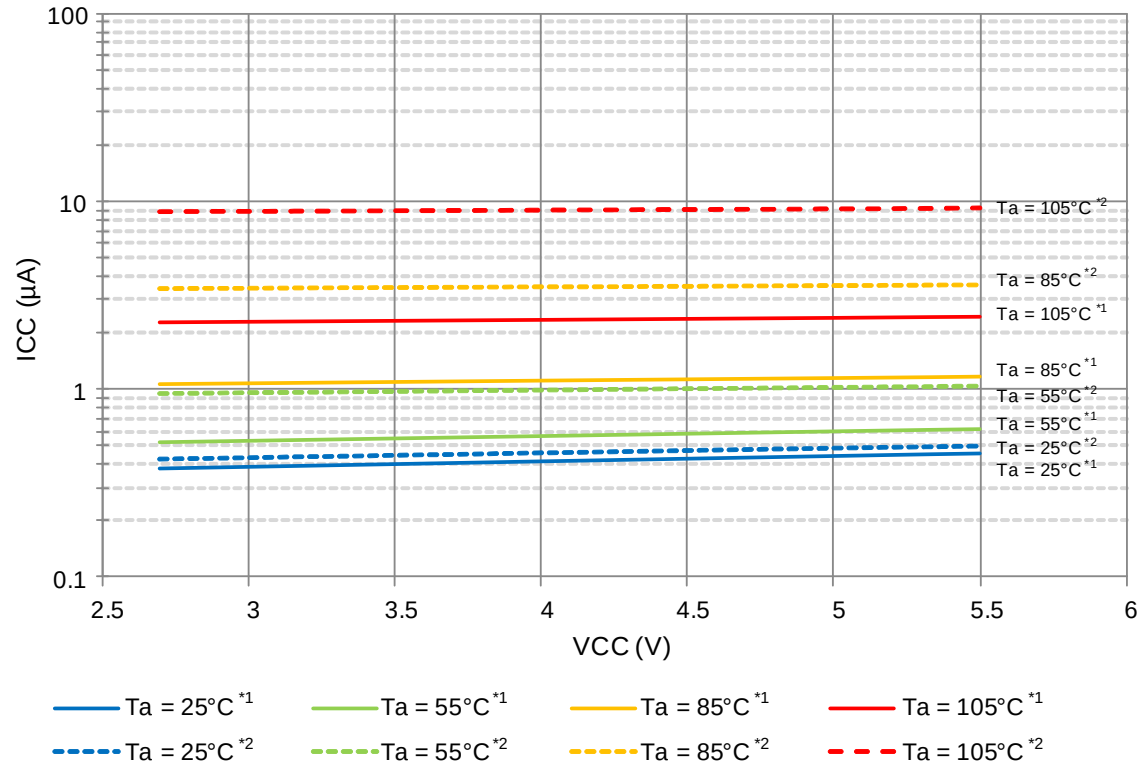
Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up resistors are disabled.
Note 2. Peripheral module clocks are stopped. This does not include BGO operation. The clock source is the PLL. FCLK and PCLK are set for division by 64.
Note 3. Peripheral module clocks are supplied. This does not include BGO operation. The clock source is the PLL. The FCLK and PCLK operating clocks run at the same frequency as ICLK.
Note 4. Values when VCC = 5 V.
Note 5. This is an increase caused by program/erase operation to the ROM or E2 DataFlash during executing the user program.
Note 6. Peripheral module clocks are stopped. The clock source is the PLL when ICLK is 12 MHz, is the HOCO when the ICLK is at 8 MHz, or is the LOCO when the ICLK is at another frequency. FCLK and PCLK are set for division by 64.
Note 7. Peripheral module clocks are supplied. The clock source is the PLL when ICLK is 12 MHz, is the HOCO when the ICLK is at 8 MHz, or is the LOCO when the ICLK is at another frequency. The FCLK and PCLK operating clocks run at the same frequency as ICLK.

Table 2.7 DC Characteristics (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

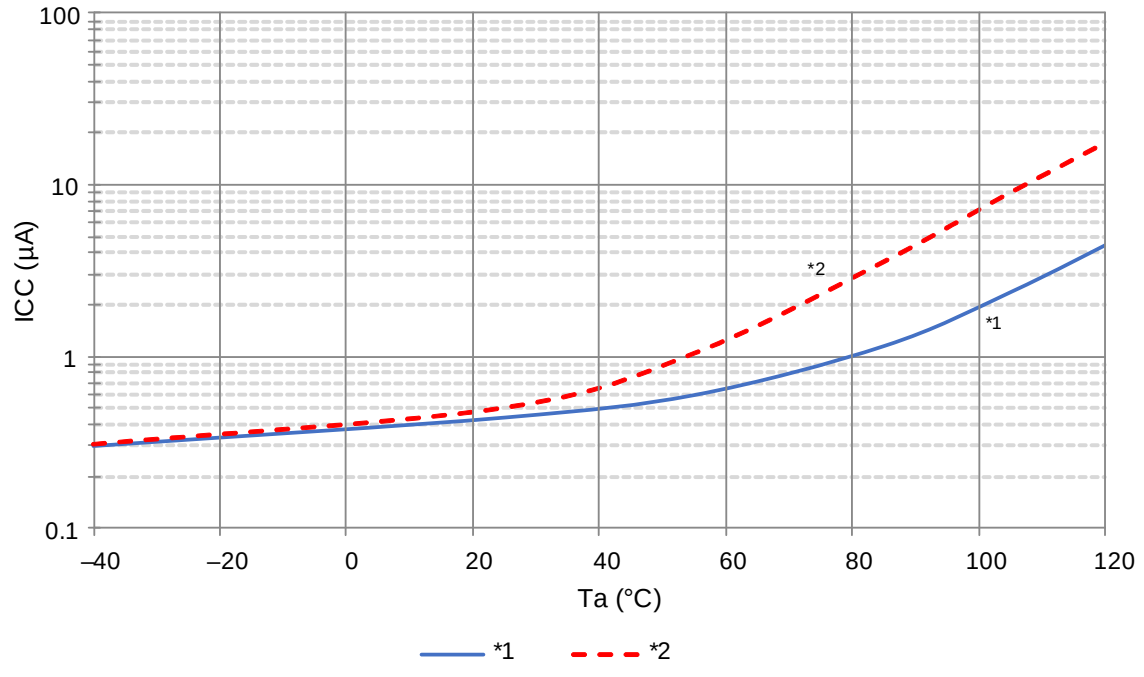
Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.44	0.74	µA	
		T_a = 55°C		0.60	1.78		
		T_a = 85°C		1.16	8.36		
		T_a = 105°C		2.38	20.49		

Note 1. Supply current values are with all output pins unloaded and all input pull-up resistors are disabled.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 5 V.



Note 1. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 2.1 Voltage Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 2.2 Temperature Dependency in Software Standby Mode (Reference Data)

Table 2.8 DC Characteristics (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	300	mW	D-version product
Permissible total consumption power*1	Pd	—	105	mW	G-version product

Note: Please contact a Renesas Electronics sales office for information on the derating of the G-version product. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

Table 2.9 DC Characteristics (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*2	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (when the sample-and-hold circuit and programmable gain amplifier are in use)	I_{AVCC}	—	4.6	6.9	mA	
	During A/D conversion (when the sample-and-hold circuit is in use but the programmable gain amplifier is not)		—	3.1	4.8		
	During A/D conversion (when the sample-and-hold circuit is not in use but the programmable gain amplifier is)		—	2.5	3.9		
	During A/D conversion (when neither the sample-and-hold circuit nor the programmable gain amplifier is in use)		—	1.0	1.8		
	During D/A conversion*1		—	0.7	1.0		
	Waiting for A/D and D/A conversion (all units)		—	—	1.4	µA	
Comparator C operating current*3	Comparator enabled (per channel)	I_{CMP}	—	40	60	µA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.

Note 2. When VCC = AVCC0 = 5 V.

Note 3. Current consumed only by the comparator C module.

Table 2.10 DC Characteristics (7)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup	SrVCC	0.02	—	20	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	—		

Note 1. When OFS1.LVDAS = 0.

Note 2. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 2.11 DC Characteristics (8)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 2.3 $V_{r\,(VCC)} \leq 0.2 \times VCC$
		—	—	1	MHz	Figure 2.3 $V_{r\,(VCC)} \leq 0.08 \times VCC$
		—	—	10		Figure 2.3 $V_{r\,(VCC)} \leq 0.06 \times VCC$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

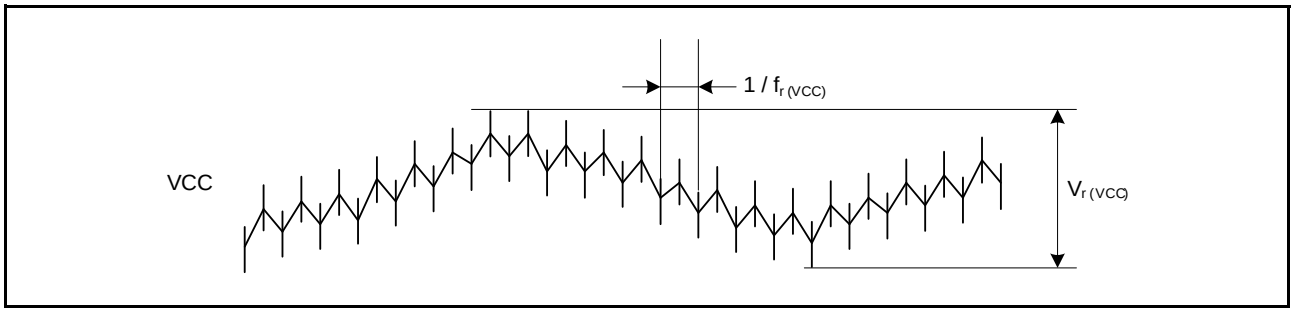


Figure 2.3 Ripple Waveform

Table 2.12 Permissible Output Currents

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible low-level output current	Large current ports (P71 to P76, PB6)		I_{OL}	10.0	mA
	RIIC pins			6.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible low-level output current	Total of large current ports		ΣI_{OL}	50	mA
	Total of all output pins			110	
Permissible high-level output current	Large current ports (P71 to P76, PB6)		I_{OH}	–5.0	mA
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible high-level output current	Total of large current ports		ΣI_{OH}	–25	mA
	Total of all output pins			–35	

Note: Do not exceed the permissible total supply current.

Table 2.13 Output Values of Voltage (1)

Conditions: VCC = 2.7 V to 4.0 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	Large current ports (P71 to P76, PB6)		V_{OL}	—	0.5	V	I_{OL} = 10.0 mA
	RIIC pins	Standard mode		—	0.4		I_{OL} = 3.0 mA
		Fast mode		—	0.6		I_{OL} = 6.0 mA
	Ports other than above	Normal output mode		—	0.5		I_{OL} = 1.0 mA
		High-drive output mode		—	0.5		I_{OL} = 2.0 mA
High-level output voltage	Large current ports (P71 to P76, PB6)		V_{OH}	VCC – 0.5	—	V	I_{OH} = –5.0 mA
	P40 to P47			AVCC0 – 0.5	—		I_{OH} = –1.0 mA
	Ports other than above	Normal output mode		VCC – 0.5	—		I_{OH} = –1.0 mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = –2.0 mA

Table 2.14 Output Values of Voltage (2)

Conditions: VCC = 4.0 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Low-level output voltage	Large current ports (P71 to P76, PB6)		V_{OL}	—	0.8	V	I_{OL} = 10.0 mA
	RIIC pins	Standard mode		—	0.4		I_{OL} = 3.0 mA
		Fast mode		—	0.6		I_{OL} = 6.0 mA
	Ports other than above	Normal output mode		—	0.8		I_{OL} = 2.0 mA
		High-drive output mode		—	0.8		I_{OL} = 4.0 mA
High-level output voltage	Large current ports (P71 to P76, PB6)		V_{OH}	VCC – 0.8	—	V	I_{OH} = –5.0 mA
	P40 to P47			AVCC0 – 0.8	—		I_{OH} = –2.0 mA
	Ports other than above	Normal output mode		VCC – 0.8	—		I_{OH} = –2.0 mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = –4.0 mA

2.3.1 Normal I/O Pin Output Voltage Characteristics

Table 2.15 Normal I/O Pin V_{OH} Voltage Characteristics (Reference Data)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, Ta = 25°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	All output pins (except for P71 to P76, PB6)	Normal output mode	V_{OH}	—	3.27	—	V	I_{OH} = –0.5 mA
				—	3.24	—		I_{OH} = –1.0 mA
				—	3.19	—		I_{OH} = –2.0 mA
				—	3.06	—		I_{OH} = –4.0 mA
				—	2.79	—		I_{OH} = –8.0 mA
		High-drive output mode	V_{OH}	—	3.29	—	V	I_{OH} = –0.5 mA
				—	3.28	—		I_{OH} = –1.0 mA
				—	3.25	—		I_{OH} = –2.0 mA
				—	3.21	—		I_{OH} = –4.0 mA
				—	3.11	—		I_{OH} = –8.0 mA
	P71 to P76, PB6	Large current Ports	V_{OH}	—	3.29	—	V	I_{OH} = –1.0 mA
				—	3.27	—		I_{OH} = –2.0 mA
				—	3.24	—		I_{OH} = –4.0 mA
				—	3.23	—		I_{OH} = –5.0 mA
				—	3.15	—		I_{OH} = –10.0 mA

Table 2.16 Normal I/O Pin V_{OH} Voltage Characteristics (Reference Data)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, Ta = 25°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	All output pins (except for P71 to P76, PB6)	Normal output mode	V_{OH}	—	4.98	—	V	I_{OH} = –0.5 mA
				—	4.96	—		I_{OH} = –1.0 mA
				—	4.92	—		I_{OH} = –2.0 mA
				—	4.83	—		I_{OH} = –4.0 mA
				—	4.65	—		I_{OH} = –8.0 mA
		High-drive output mode	V_{OH}	—	4.99	—	V	I_{OH} = –0.5 mA
				—	4.98	—		I_{OH} = –1.0 mA
				—	4.97	—		I_{OH} = –2.0 mA
				—	4.93	—		I_{OH} = –4.0 mA
				—	4.86	—		I_{OH} = –8.0 mA
	P71 to P76, PB6	Large current Ports	V_{OH}	—	4.99	—	V	I_{OH} = –1.0 mA
				—	4.98	—		I_{OH} = –2.0 mA
				—	4.96	—		I_{OH} = –4.0 mA
				—	4.95	—		I_{OH} = –5.0 mA
				—	4.89	—		I_{OH} = –10.0 mA

Table 2.17 Normal I/O Pin V_{OL} Voltage Characteristics (Reference Data)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, Ta = 25°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Low-level output voltage	All output pins (except for P71 to P76, PB6)	Normal output mode	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
				—	0.05	—		I_{OL} = 1.0 mA
				—	0.09	—		I_{OL} = 2.0 mA
				—	0.20	—		I_{OL} = 4.0 mA
				—	0.43	—		I_{OL} = 8.0 mA
		High-drive output mode	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
				—	0.02	—		I_{OL} = 1.0 mA
				—	0.04	—		I_{OL} = 2.0 mA
				—	0.08	—		I_{OL} = 4.0 mA
				—	0.16	—		I_{OL} = 8.0 mA
	P71 to P76, PB6	Large current Ports	V_{OL}	—	0.01	—	V	I_{OL} = 1.0 mA
				—	0.02	—		I_{OL} = 2.0 mA
				—	0.05	—		I_{OL} = 4.0 mA
				—	0.06	—		I_{OL} = 5.0 mA
				—	0.12	—		I_{OL} = 10.0 mA

Table 2.18 Normal I/O Pin V_{OL} Voltage Characteristics (Reference Data)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, Ta = 25°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Low-level output voltage	All output pins (except for P71 to P76, PB6)	Normal output mode	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
				—	0.03	—		I_{OL} = 1.0 mA
				—	0.07	—		I_{OL} = 2.0 mA
				—	0.14	—		I_{OL} = 4.0 mA
				—	0.29	—		I_{OL} = 8.0 mA
		High-drive output mode	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
				—	0.01	—		I_{OL} = 1.0 mA
				—	0.03	—		I_{OL} = 2.0 mA
				—	0.05	—		I_{OL} = 4.0 mA
				—	0.11	—		I_{OL} = 8.0 mA
				—	0.23	—		I_{OL} = 16.0 mA
	P71 to P76, PB6	Large current Ports	V_{OL}	—	0.01	—	V	I_{OL} = 1.0 mA
				—	0.02	—		I_{OL} = 2.0 mA
				—	0.03	—		I_{OL} = 4.0 mA
				—	0.04	—		I_{OL} = 5.0 mA
				—	0.09	—		I_{OL} = 10.0 mA

2.4 AC Characteristics

2.4.1 Clock Timing

Table 2.19 Operating Frequency Value (High-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency*4	System clock (ICLK)	f_{max}	—	—	32	MHz
	FlashIF clock (FCLK)*1, *2		—	—	32	
	Peripheral module clock (PCLKB)		—	—	32	
	Peripheral module clock (PCLKD)*3		—	—	32	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The minimum frequency of PCLKD is 1 MHz when the A/D converter is to be used.
Note 4. The maximum operating frequencies do not take errors in the HOCO frequency and jitters in the PLL signal. Refer to Table 2.21, Clock Timing.

Table 2.20 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit
Maximum operating frequency*4	System clock (ICLK)	f_{max}	—	—	12	MHz
	FlashIF clock (FCLK)*1, *2		—	—	12	
	Peripheral module clock (PCLKB)		—	—	12	
	Peripheral module clock (PCLKD)*3		—	—	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The minimum frequency of PCLKD is 1 MHz when the A/D converter is to be used.
Note 4. The maximum operating frequencies do not take errors in the HOCO frequency and jitters in the PLL signal. Refer to Table 2.21, Clock Timing.

Table 2.21 Clock Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.4
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 2.5
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 2.6
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 2.7
HOCO clock oscillation frequency	f_{HOCO}	31.52	32	32.48	MHz	T_a = –40 to +85°C
		31.68	32	32.32		T_a = –20 to +85°C
		31.36	32	32.64		T_a = –40 to +105°C
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	41.3	μs	Figure 2.9
PLL circuit oscillation frequency	f_{PLL}	24	—	32	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	74.4	μs	Figure 2.10
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

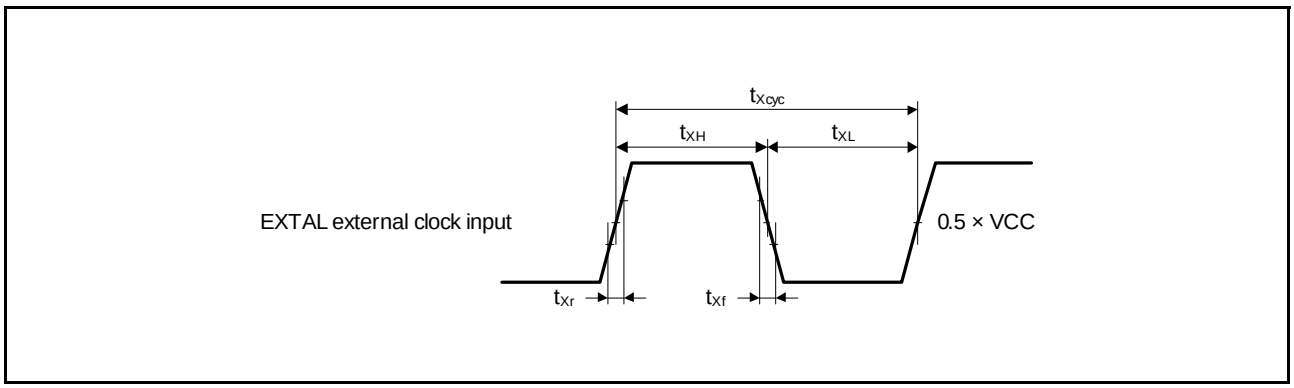


Figure 2.4 EXTAL External Clock Input Timing

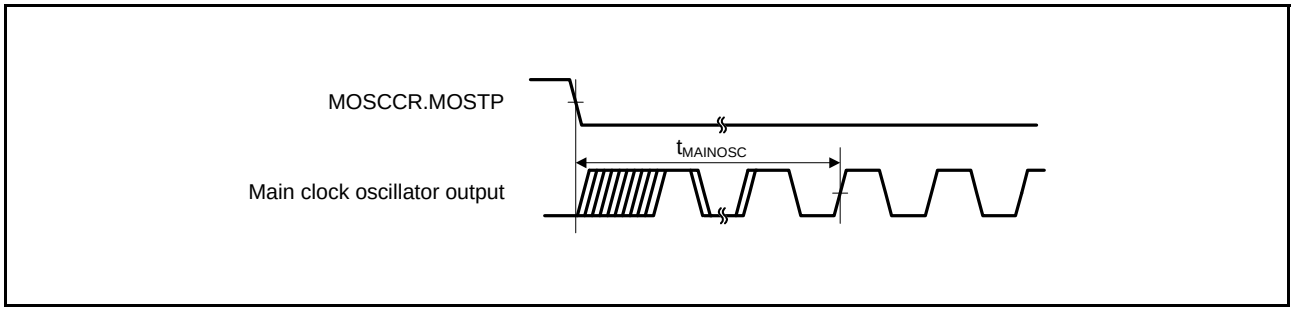


Figure 2.5 Main Clock Oscillation Start Timing

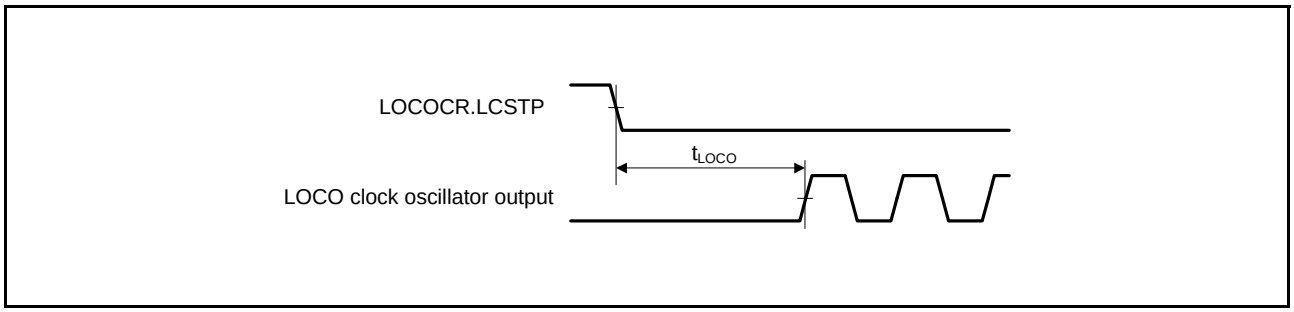


Figure 2.6 LOCO Clock Oscillation Start Timing

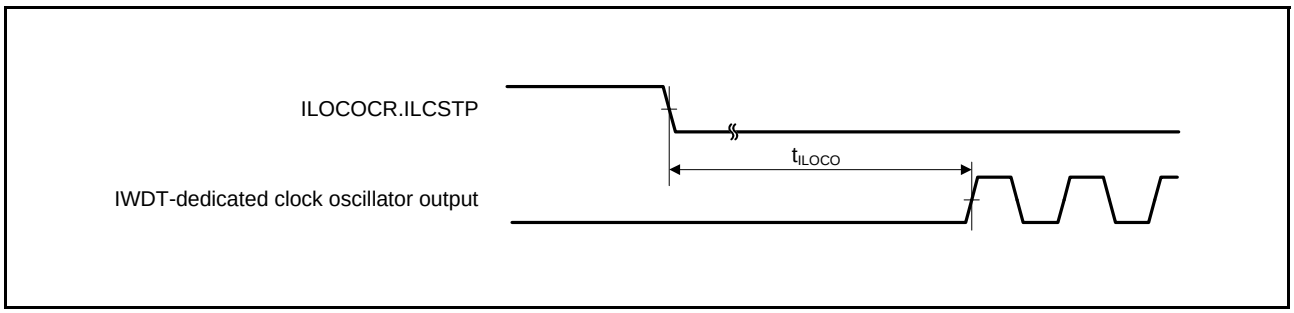


Figure 2.7 IWDT-Dedicated Clock Oscillation Start Timing

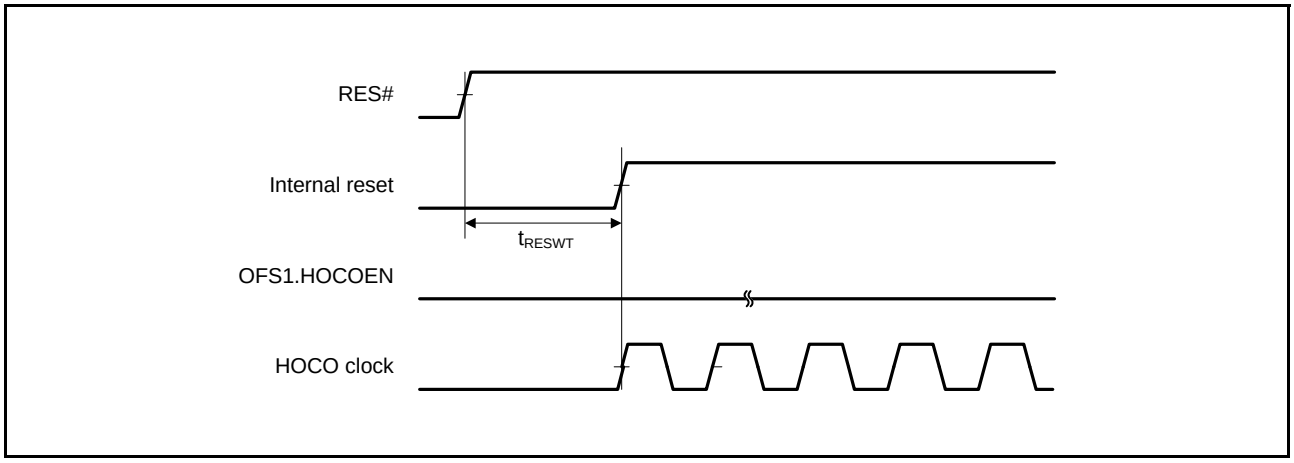


Figure 2.8 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

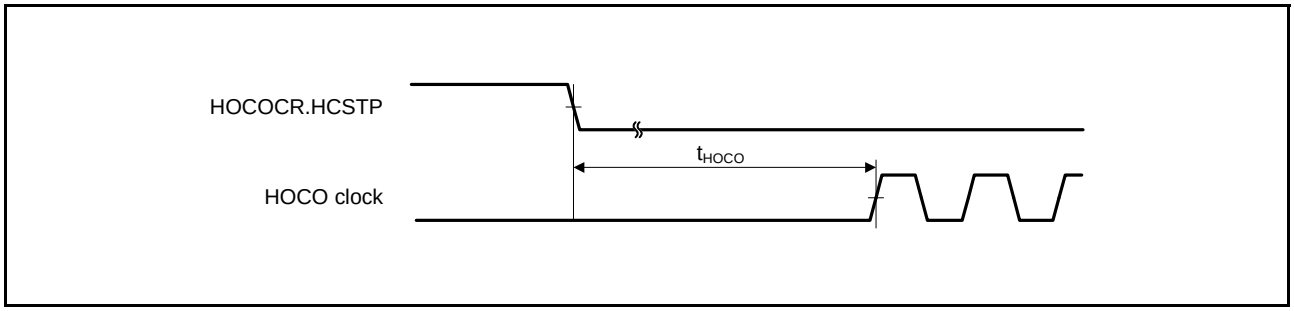


Figure 2.9 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

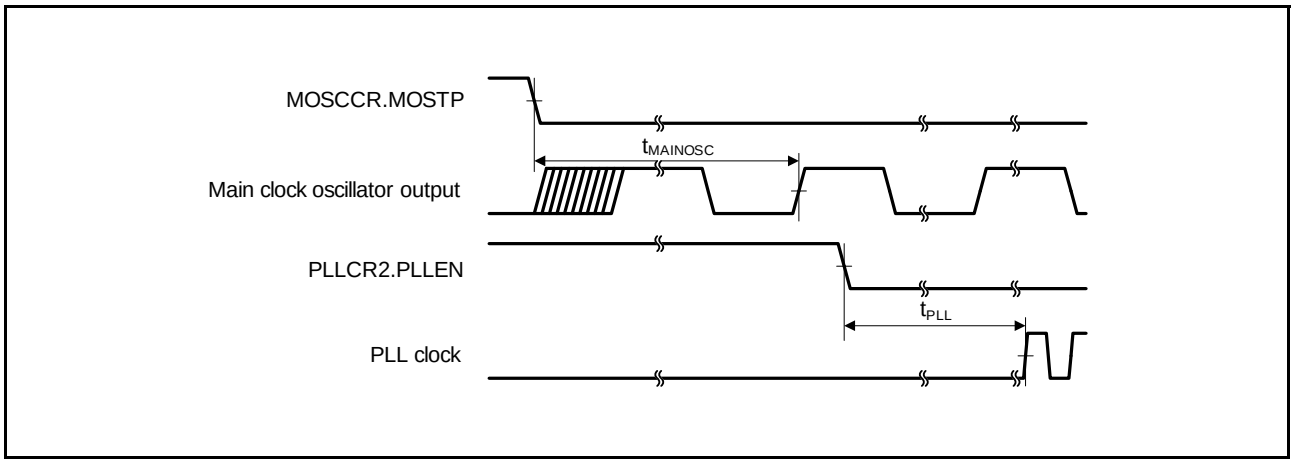


Figure 2.10 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

2.4.2 Reset Timing

Table 2.22 Reset Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 2.11
	Other than above	t_{RESW}	30	—	—	µs	Figure 2.12
Wait time after RES# cancellation (at power-on)		t_{RESWT}	—	27.5	—	ms	Figure 2.11
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	120	—	µs	Figure 2.12
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 2.13
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*1		t_{RESW2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESW2}	—	170	—	µs	

Note 1. When IWDTCR.CKS[3:0] = 0000b.

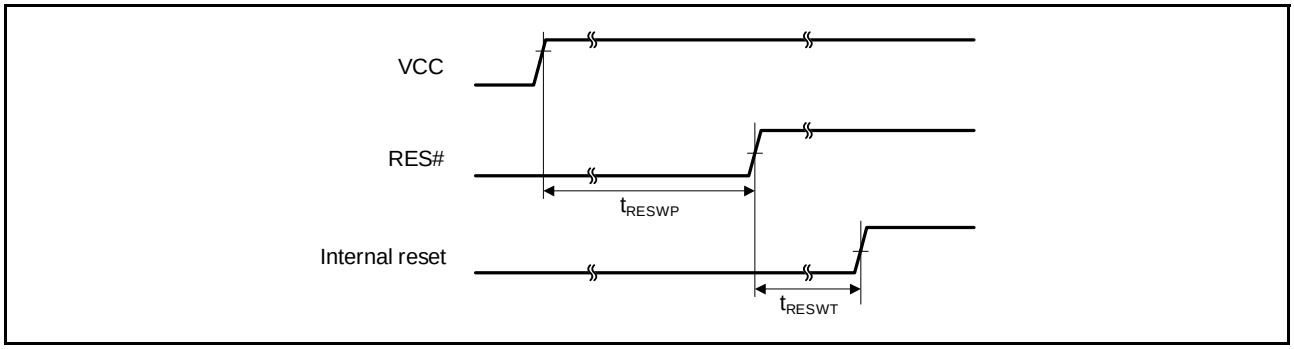


Figure 2.11 Reset Input Timing at Power-On

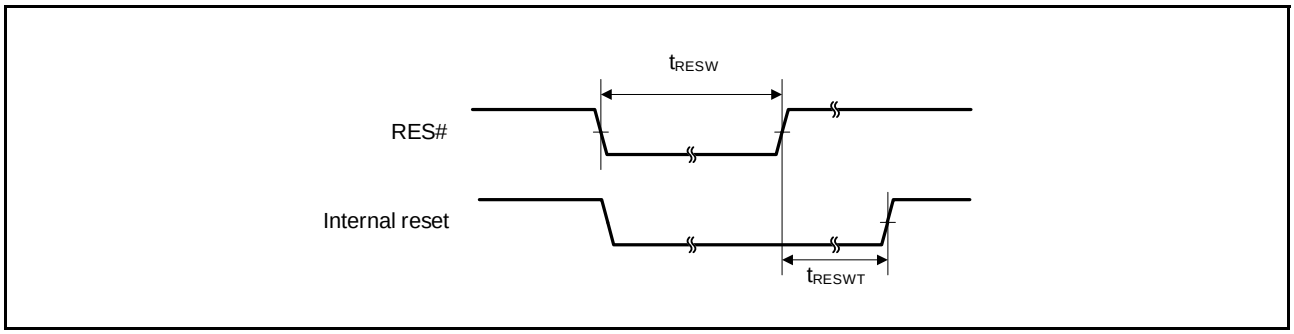


Figure 2.12 Reset Input Timing (1)

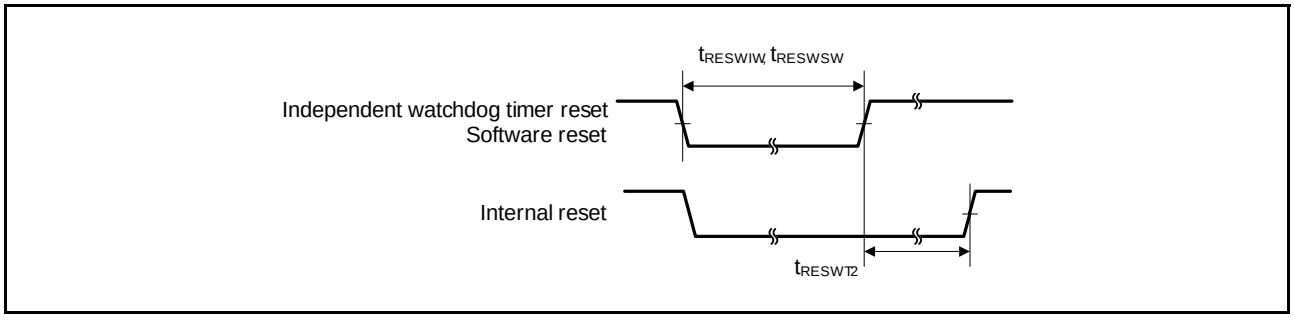


Figure 2.13 Reset Input Timing (2)

2.4.3 Timing of Recovery from Low Power Consumption Modes

Table 2.23 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 2.14
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3		
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	35	50	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	70	95		
		HOCO clock oscillator operating		t_{SBYHO}	—	40	55		
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55		

Note: Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of PLL is 32 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 4. When the frequency of the external clock is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 5. When the frequency of PLL is 32 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 2.24 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 2.14
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3		
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85		
		HOCO clock oscillator operating		t_{SBYHO}	—	40	50		
		LOCO clock oscillator operating		t_{SBYLO}	—	5	7		

Note: Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of the PLL is 24 MHz and that of the ILCK is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 4. When the frequency of the external clock is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 5. When the frequency of the PLL is 24 MHz and that of the ILCK is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

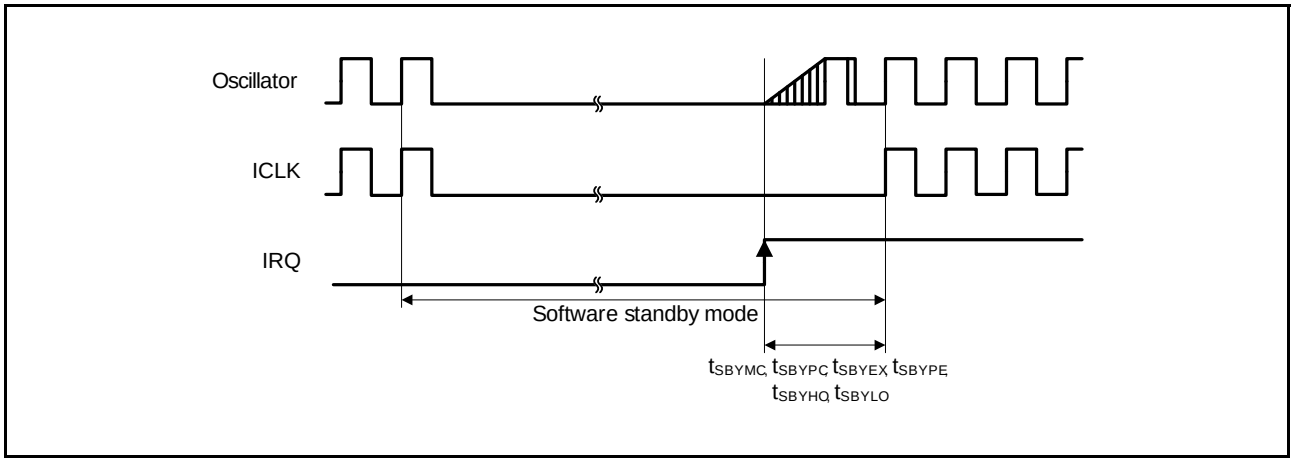


Figure 2.14 Software Standby Mode Recovery Timing

Table 2.25 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 2.15
	Middle-speed mode*3	t_{DSLP}	—	3	4		

Note: Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.
Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.

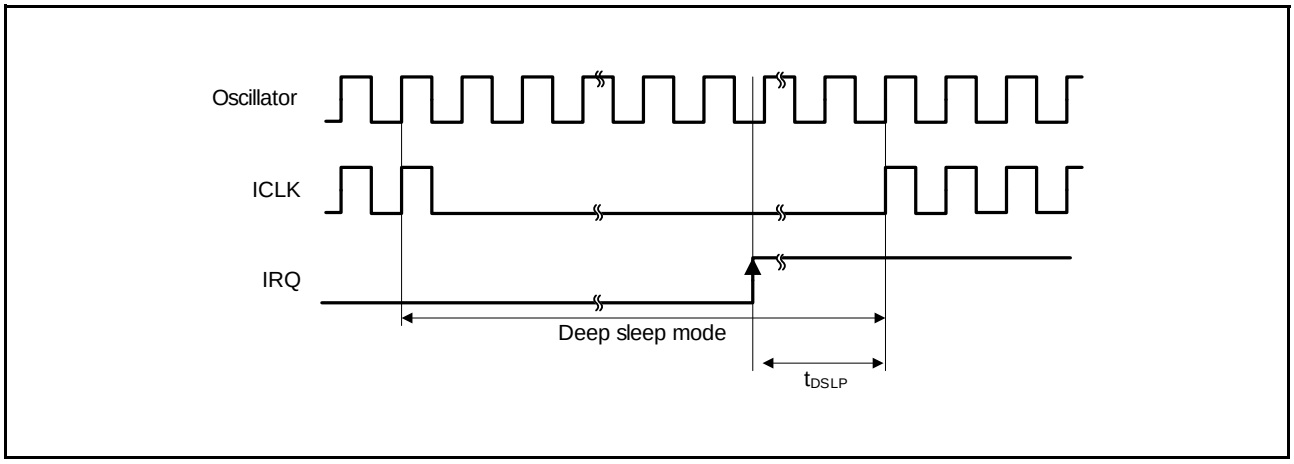


Figure 2.15 Deep Sleep Mode Recovery Timing

Table 2.26 Operating Mode Transition Time

Conditions: VCC = 2.7 V to AVCC0, AVCC0 = 2.7 V to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs

Note: Values when the frequencies of PCLKB, PCLKD, and FCLK are not divided.

2.4.4 Control Signal Timing

Table 2.27 Control Signal Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} ×3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} ×3.5 *3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 5).

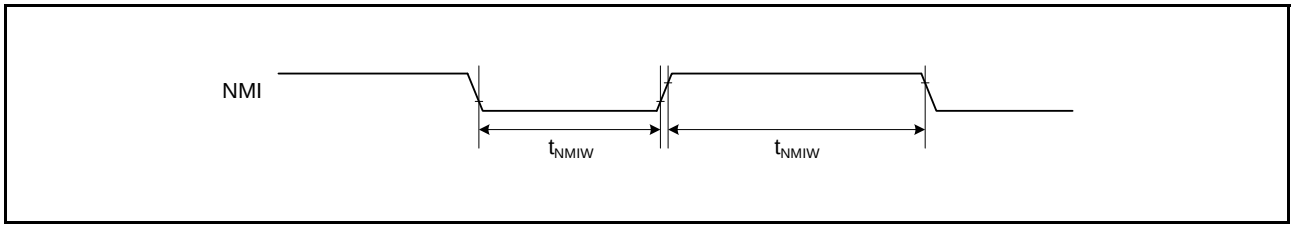


Figure 2.16 NMI Interrupt Input Timing

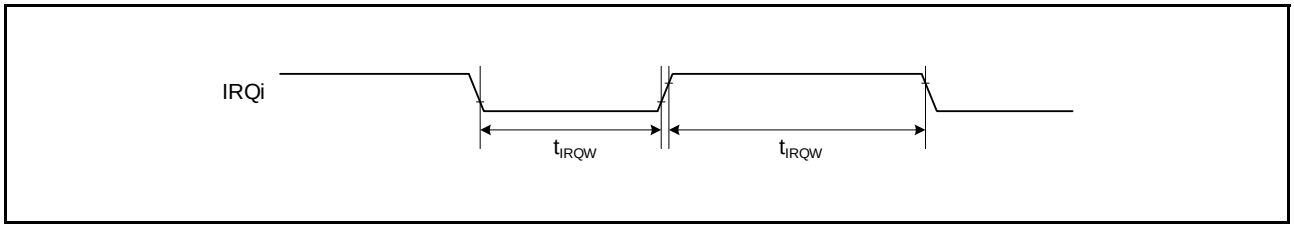


Figure 2.17 IRQ Interrupt Input Timing

2.4.5 Timing of On-Chip Peripheral Modules

2.4.5.1 I/O ports

Table 2.28 Timing of I/O ports

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{Pcyc}	Figure 2.18

Note 1. t_{Pcyc}: PCLK cycle

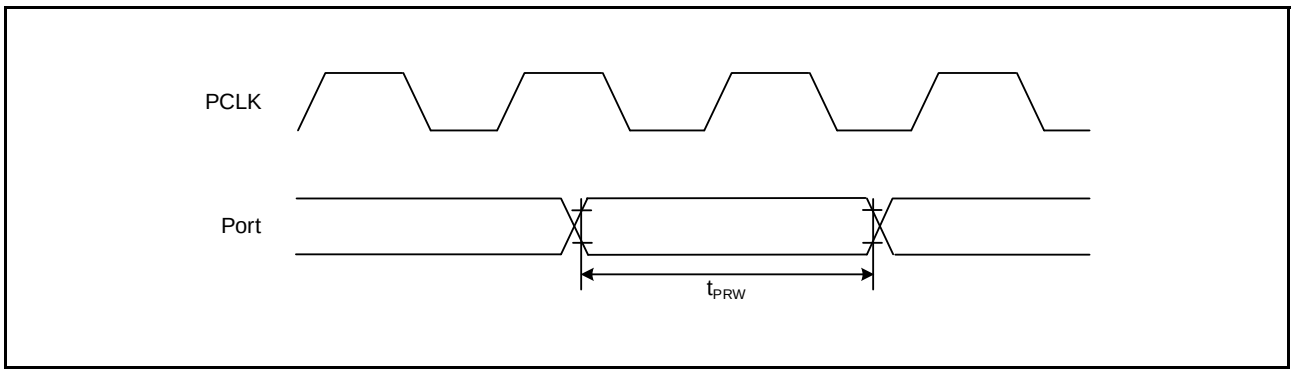


Figure 2.18 I/O Port Input Timing

2.4.5.2 MTU

Table 2.29 Timing of MTU

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 2.19
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—		Figure 2.20
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{Pcyc}: PCLK cycle

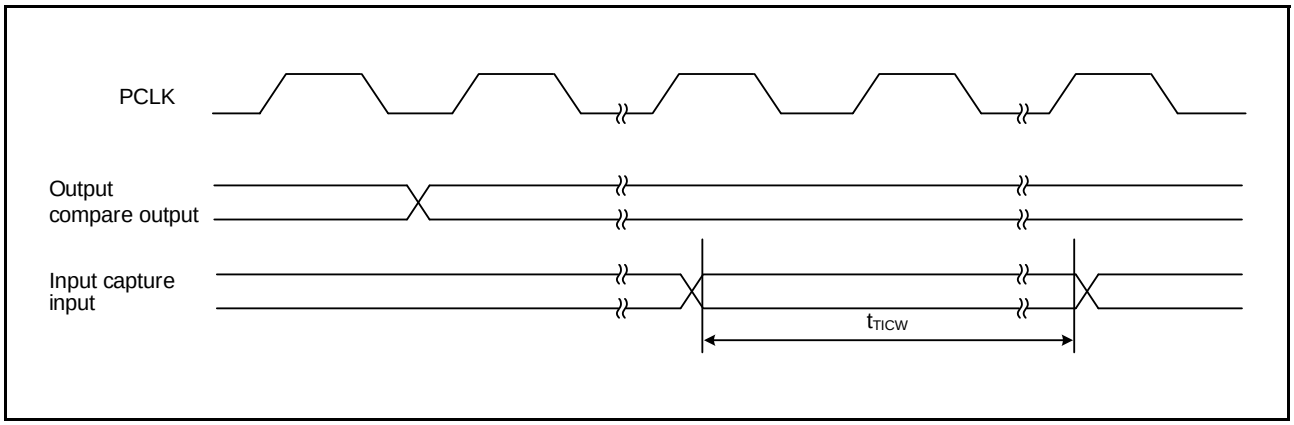


Figure 2.19 MTU Input/Output Timing

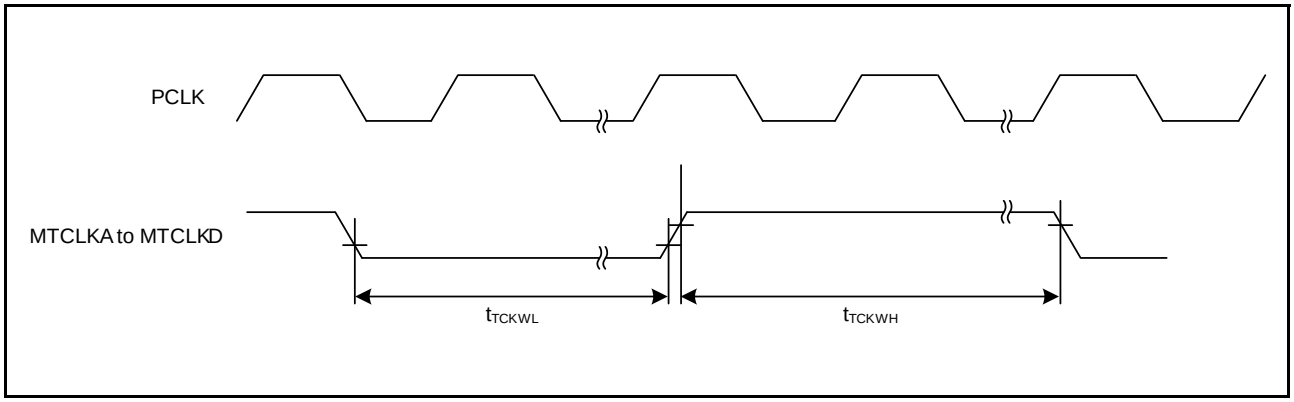


Figure 2.20 MTU Clock Input Timing

2.4.5.3 POE

Table 2.30 Timing of POE

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
POE	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 2.21
	Output disable time	Transition of the POE# signal level	t_{POEDI}	—	5 t_{Pcyc} + 0.24	µs	Figure 2.22 In the case of falling-edge detection (ICSRm.POEnM[3:0] = 0000 (m =1, 3, 4; n = 0, 8,10))
		Simultaneous conduction of output pins	t_{POEDO}	—	3 t_{Pcyc} + 0.2		Figure 2.23
		Detection of comparator outputs	t_{POEDC}	—	5 t_{Pcyc} + 0.2		Figure 2.24 When the noise filter for a comparator C is not in use (CMPCTL.CDFS[1:0] = 00), and the values exclude the time until the level of the detection signal changes after a comparator C detects the required change in voltage.
		Register setting	t_{POEDS}	—	1 t_{Pcyc} + 0.2		Figure 2.25 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	21		Figure 2.26

Note 1. t_{Pcyc}: PCLK cycle

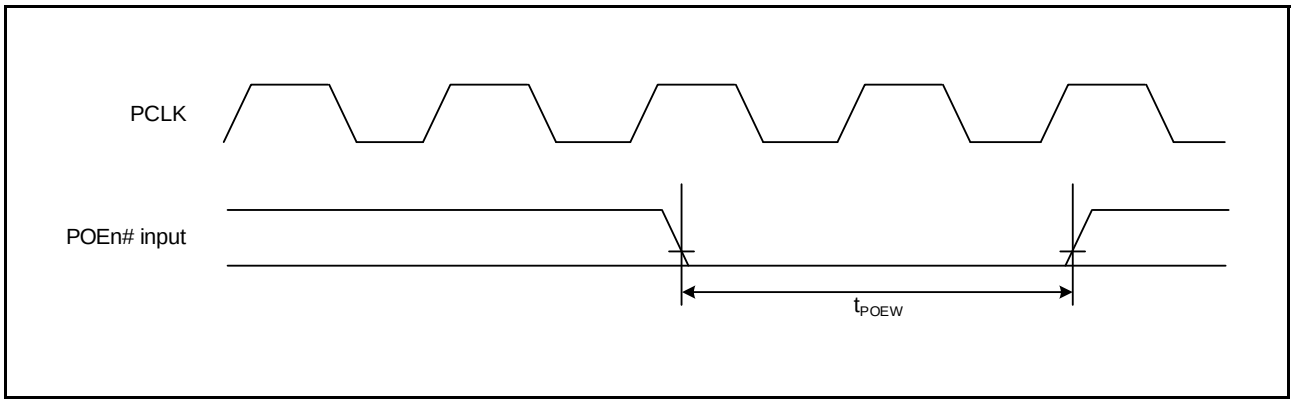


Figure 2.21 POE# Input Timing (n = 0, 8, 10)

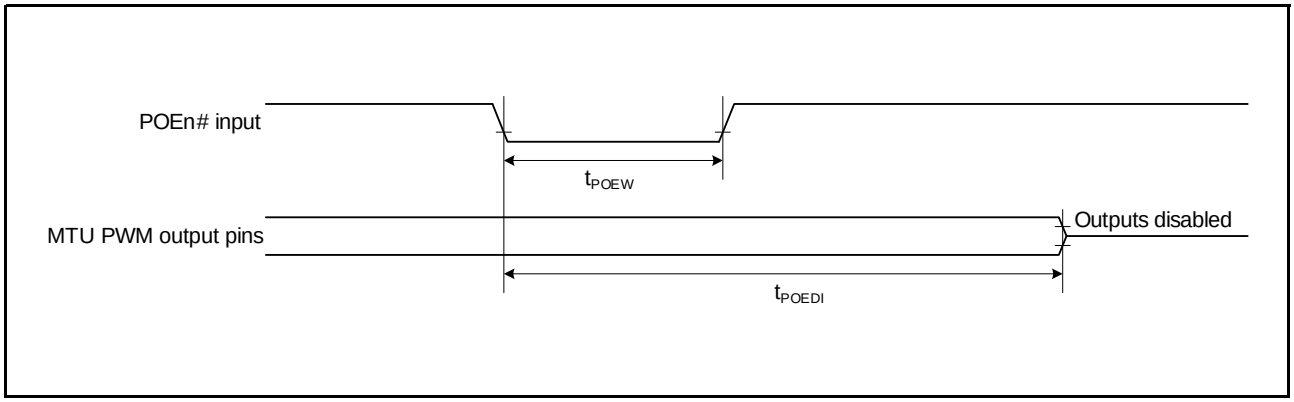
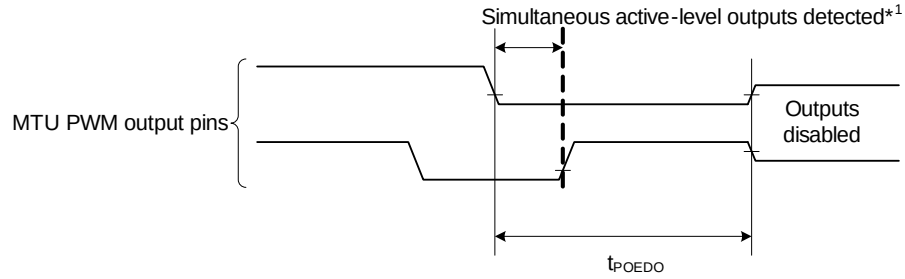


Figure 2.22 Output Disable Time for POE in Response to Transition of the POEn# Signal Level (n = 0, 8, 10)



Note 1. When the active level is set to low .

Figure 2.23 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

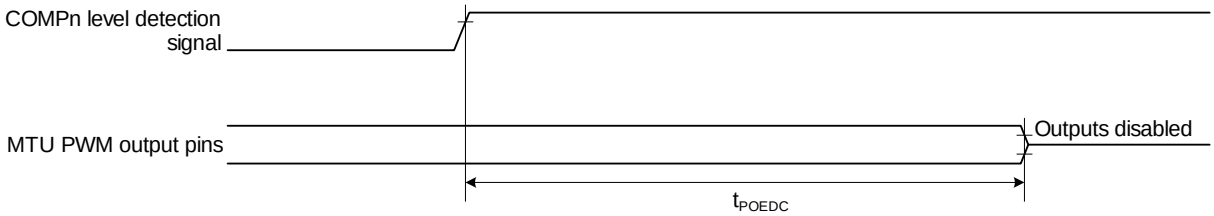


Figure 2.24 Output Disable Time for POE in Response to Detection of the Comparator Outputs (n = 0 to 2)

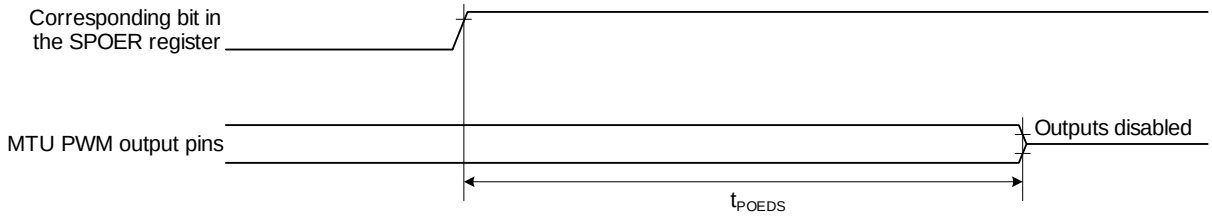


Figure 2.25 Output Disable Time for POE in Response to the Register Setting

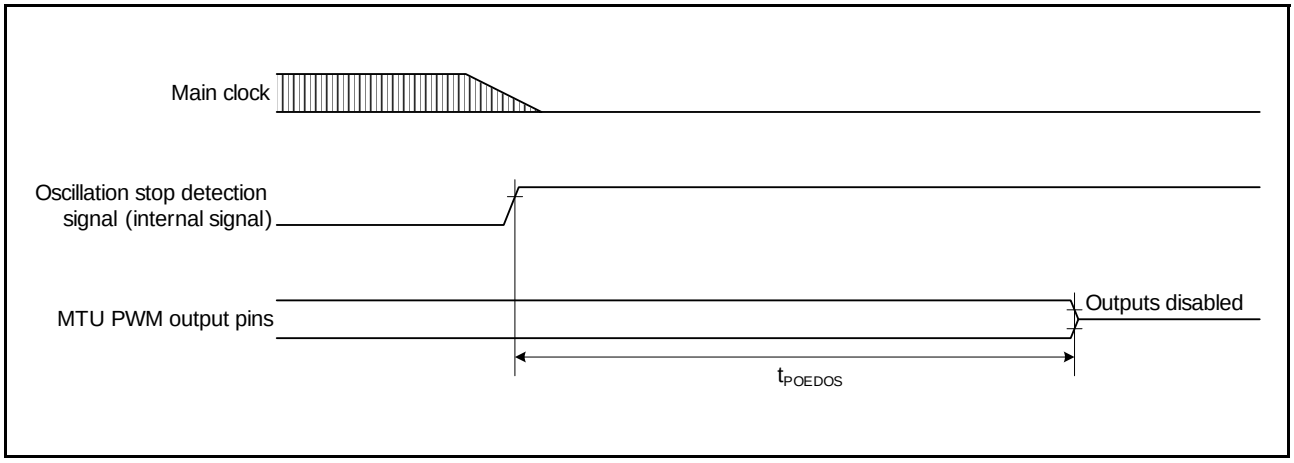


Figure 2.26 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.4.5.4 SCI

Table 2.31 Timing of SCI

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
SCI	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.27
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20		
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 2.28 C = 30 pF
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20		
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40		
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40		
			VCC = 2.7 V or above		—	65		
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—		
			VCC = 2.7 V or above		65	—		
	Receive data setup time (slave)	Clock synchronous			40	—		
	Receive data hold time	Clock synchronous		t_{RXH}	40	—		

Note 1. t_{Pcyc}: PCLK cycle

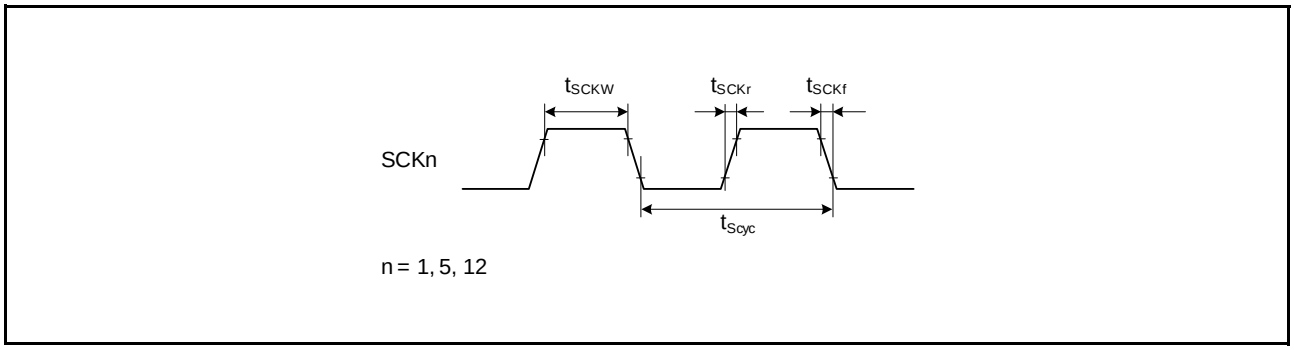


Figure 2.27 SCK Clock Input Timing

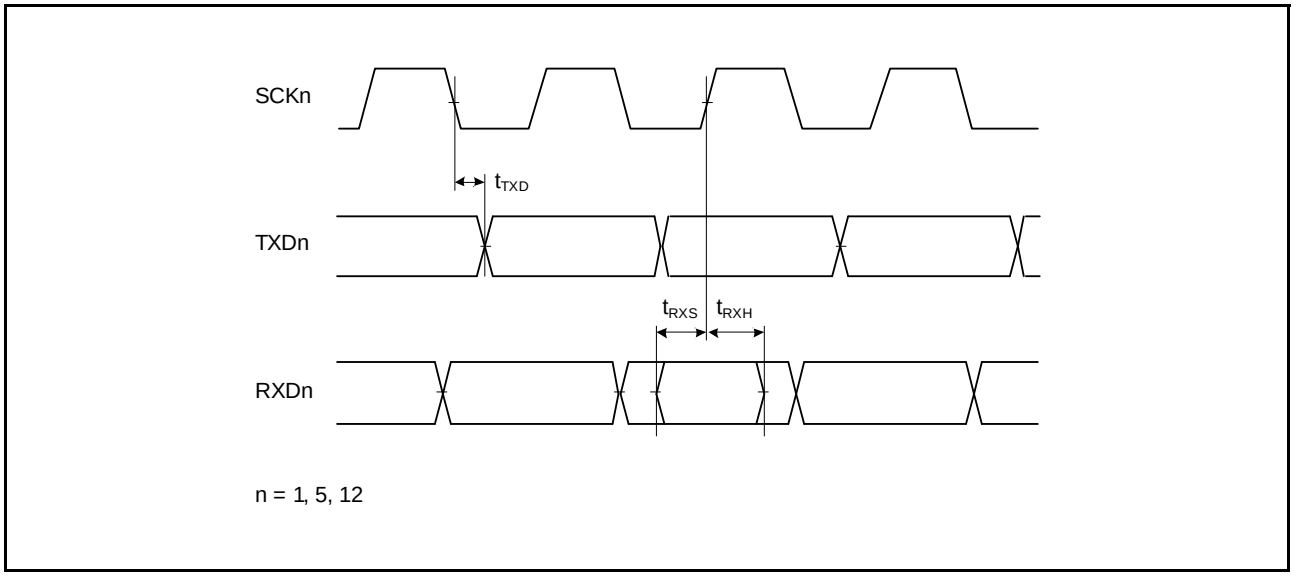


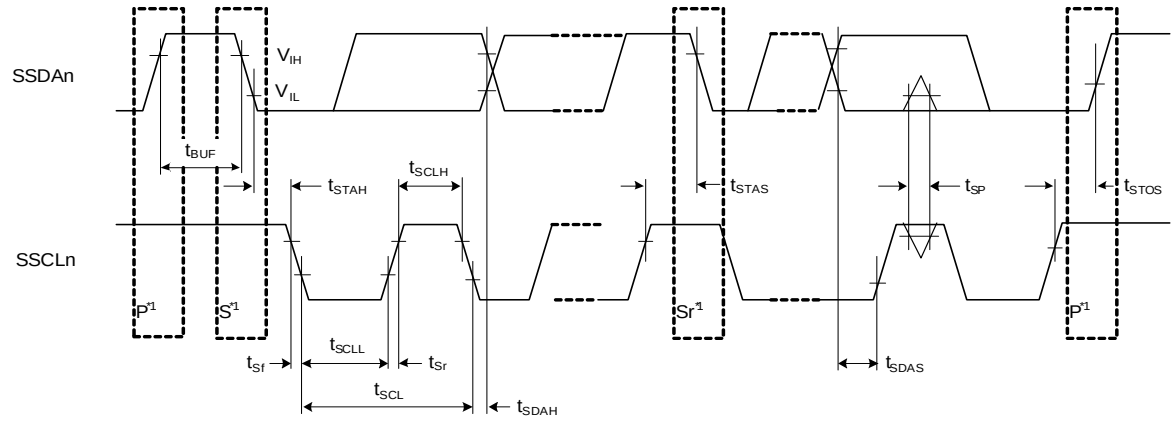
Figure 2.28 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.32 Timing of Simple I²C

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I²C (Standard mode)	SSCL, SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.29
	SSCL, SSDA input fall time	t_{Sf}	—	300		
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}*1		
	Data input setup time	t_{SDAS}	250	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL, SSDA capacitive load	C_b*2	—	400	pF	
Simple I²C (Fast mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	Figure 2.29
	SSCL, SSDA input fall time	t_{Sf}	—	300		
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}*1		
	Data input setup time	t_{SDAS}	100	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL, SSDA capacitive load	C_b*2	—	400	pF	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. C_b is the total capacitance of the bus lines



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

n = 1, 5, 12

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.29 Simple I²C Bus Interface Input/Output Timing

Table 2.33 Timing of Simple SPI

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.30
	SCK clock cycle input (slave)			6	—		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6		
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 2.31, Figure 2.32
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—		
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—		
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time	Master	t_{OH}	–10	—		
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20		
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20		
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 2.33, Figure 2.34
	Slave output release time		t_{REL}	—	6		

Note 1. t_{Pcyc}: PCLK cycle

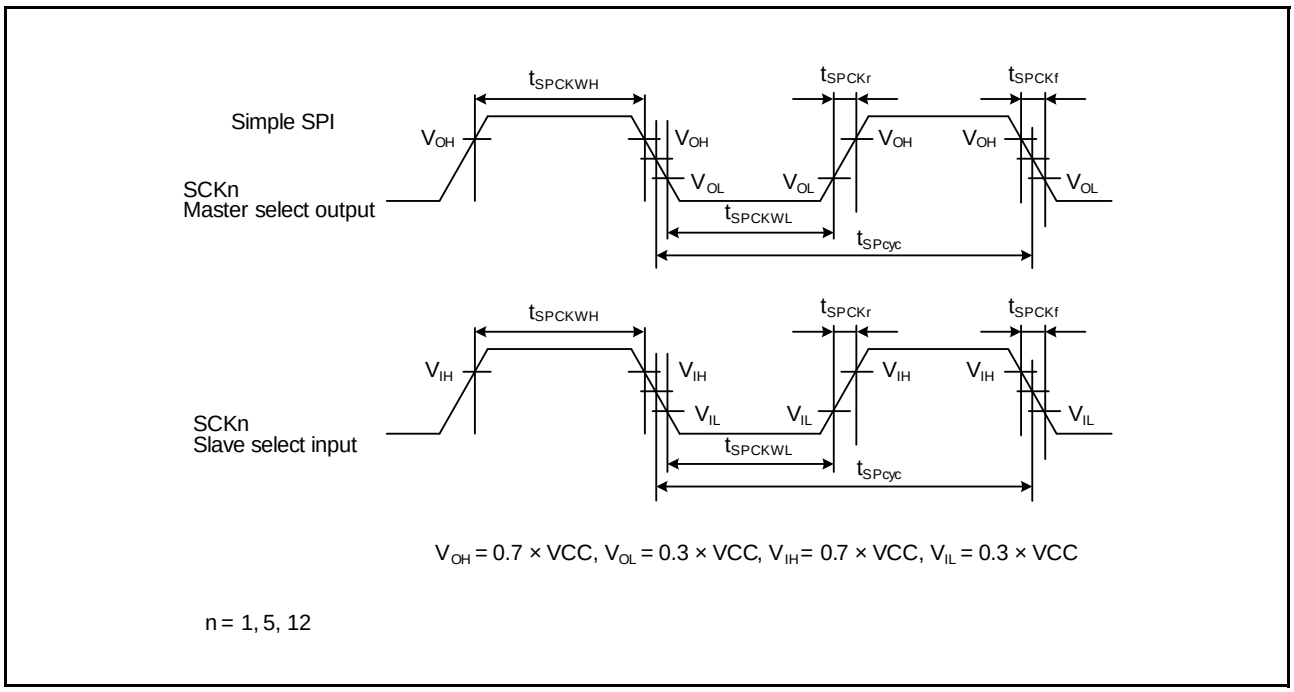


Figure 2.30 Simple SPI Clock Timing

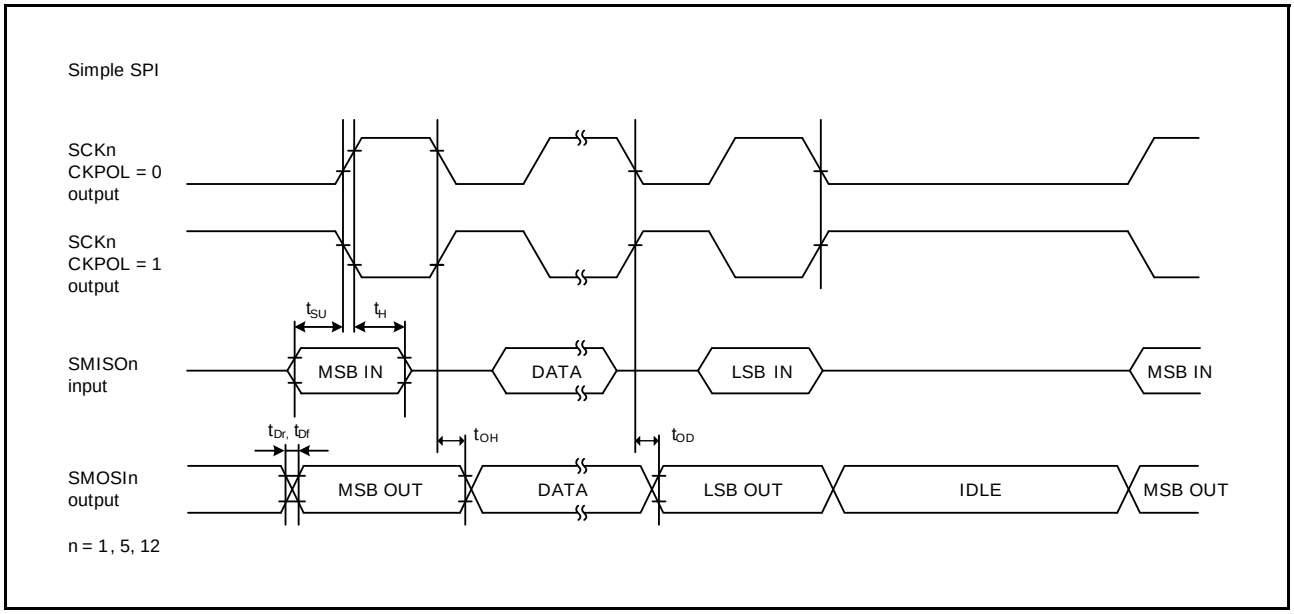


Figure 2.31 Simple SPI Clock Timing (Master, CKPH = 1)

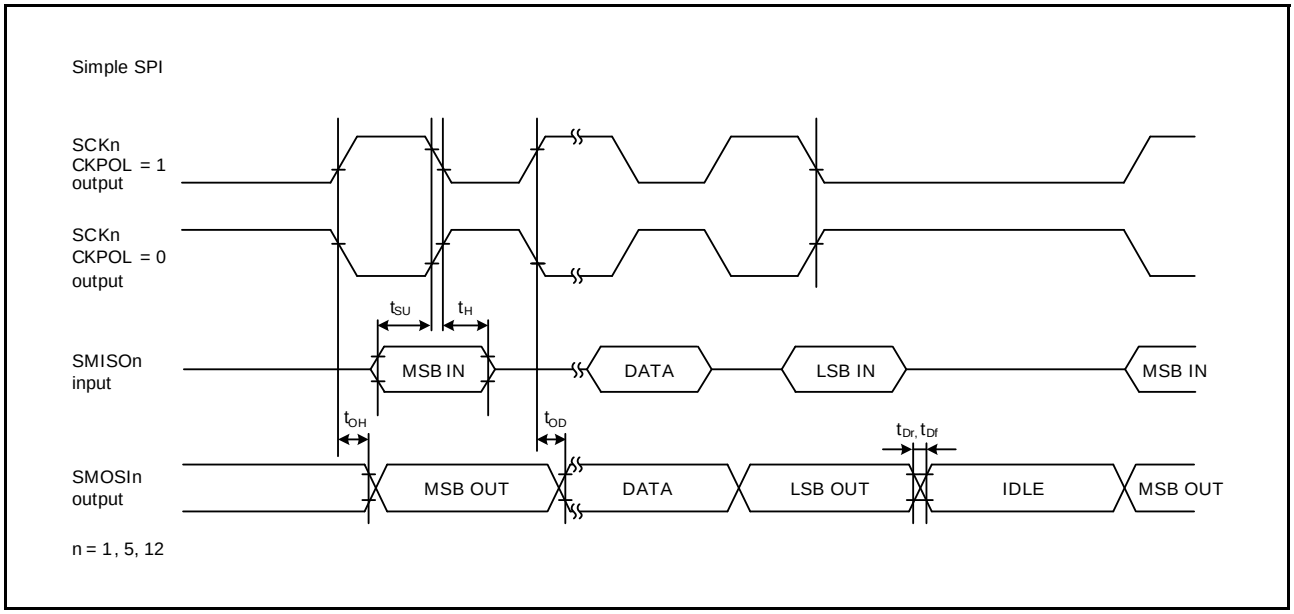


Figure 2.32 Simple SPI Clock Timing (Master, CKPH = 0)

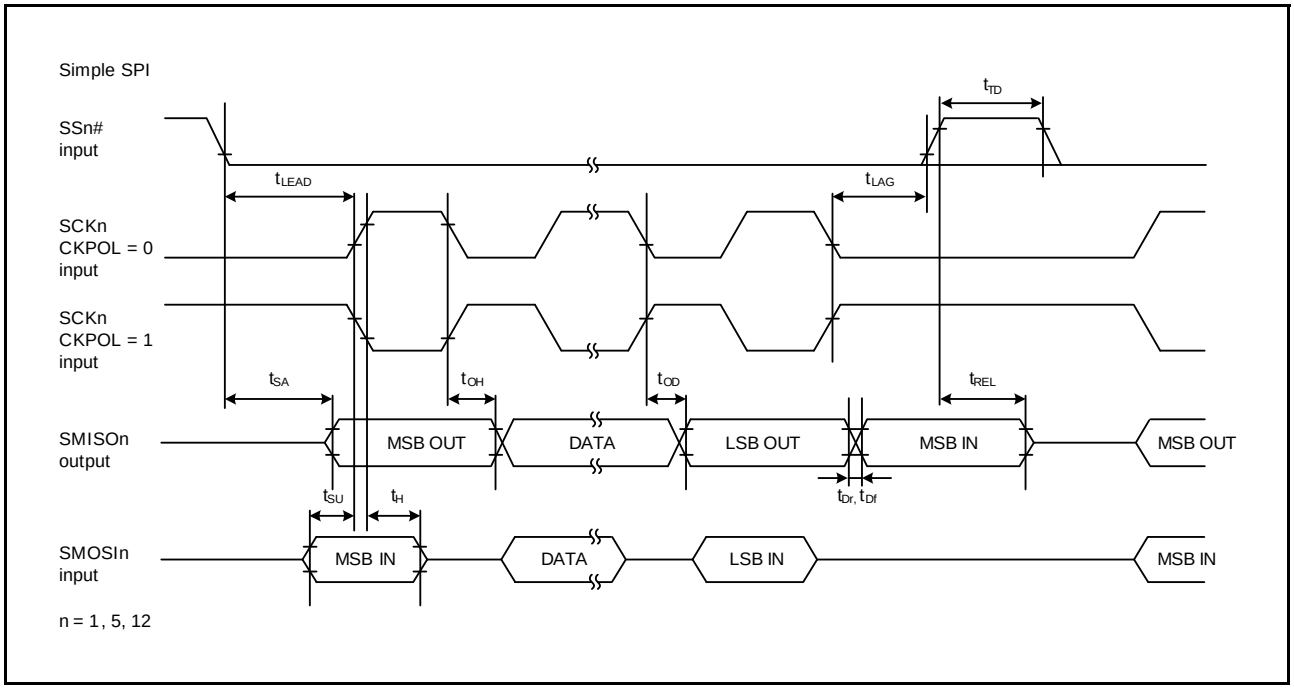


Figure 2.33 Simple SPI Clock Timing (Slave, CKPH = 1)

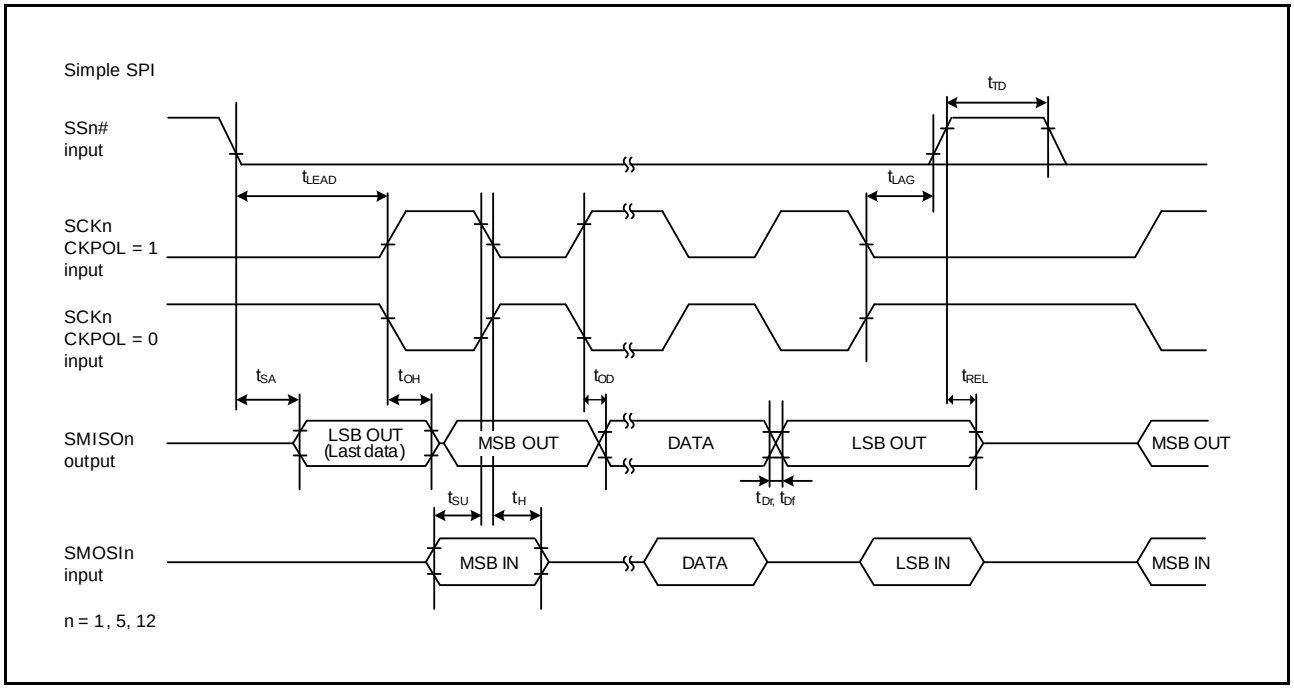


Figure 2.34 Simple SPI Clock Timing (Slave, CKPH = 0)

2.4.5.5 A/D converter

Table 2.34 Timing of A/D converter

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	Trigger input pulse width	t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.35

Note 1. t_{Pcyc}: PCLK cycle

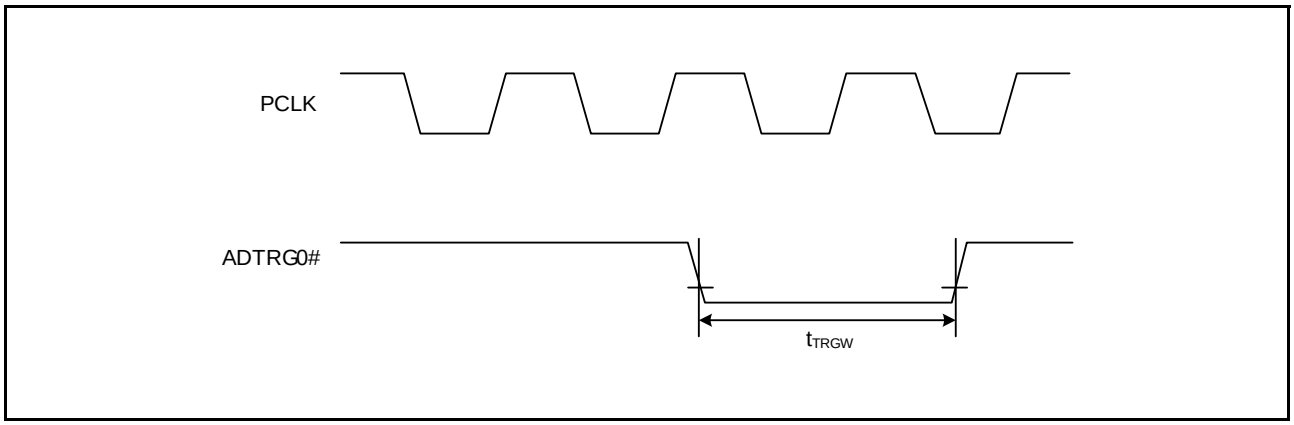


Figure 2.35 A/D Converter External Trigger Input Timing

2.4.5.6 CAC

Table 2.35 Timing of CAC

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$	t_{CACREF}	$4.5\ t_{cac} + 3\ t_{Pcyc}$	—	ns	
		$t_{Pcyc} > t_{cac}$		$5\ t_{cac} + 6.5\ t_{Pcyc}$			

Note: t_{Pcyc}: PCLK cycle
Note: C_b is the total capacitance of the bus lines.

2.4.5.7 RIIC

Table 2.36 Timing of RIIC

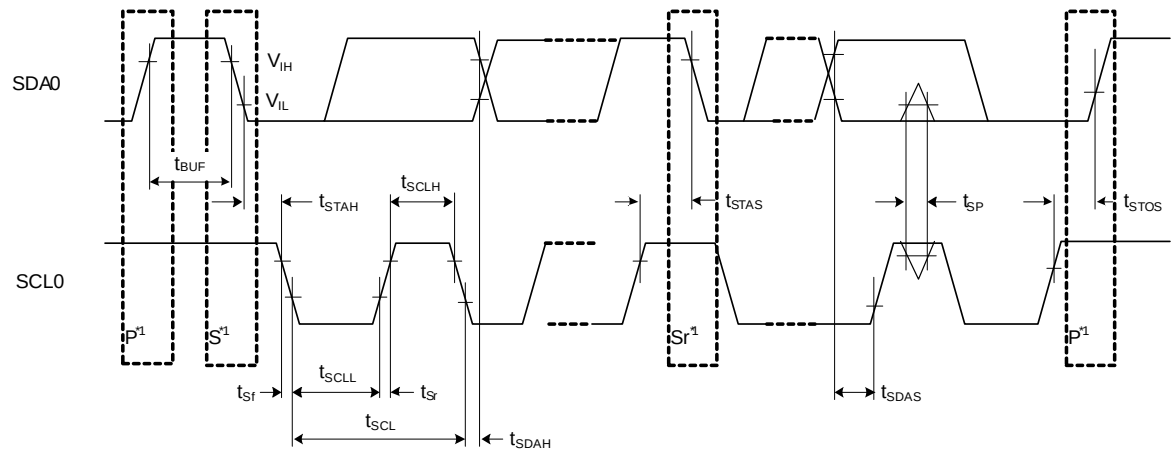
Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.36
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—		
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—		
	SCL, SDA rise time	t_{Sr}	—	1000		
	SCL, SDA fall time	t_{Sf}	—	300		
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}		
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—		
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—		
	Repeated START condition setup time	t_{STAS}	1000	—		
	STOP condition setup time	t_{STOS}	1000	—		
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—		
	Data hold time	t_{SDAH}	0	—		
	SCL, SDA capacitive load	C_b*3	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.36
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—		
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—		
	SCL, SDA rise time	t_{Sr}	—	300		
	SCL, SDA fall time	t_{Sf}	—	300		
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}		
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—		
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—		
	Repeated START condition setup time	t_{STAS}	300	—		
	STOP condition setup time	t_{STOS}	300	—		
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—		
	Data hold time	t_{SDAH}	0	—		
	SCL, SDA capacitive load	C_b*3	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 2. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 3. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.36 RIIC Bus Interface Input/Output Timing

2.5 A/D Conversion Characteristics

Table 2.37 A/D Conversion Characteristics (1)

Conditions: VCC = 4.5 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, Source impedance = 1.0 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Sample-and-hold circuit not in use	1.41	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 0Dh
	Sample-and-hold circuit in use	2.16	—	—		High-precision channel ADSSTRn.SST[7:0] bits = 0Dh ADSHCR.SSTSH[7:0] bits = 0Bh AN000 to 002 = 0.25 V to AVCC0 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error	Sample-and-hold circuit not in use	—	±0.5	±4.5	LSB	
	Sample-and-hold circuit in use	—	±1.5	±6.5		
Full-scale error	Sample-and-hold circuit not in use	—	±0.75	±4.5	LSB	
	Sample-and-hold circuit in use	—	±1.5	±6.5		
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample-and-hold circuit not in use	—	±1.25	±5.0	LSB	
	Sample-and-hold circuit in use	—	±3.0	±8.0		AN000 to 002 = 0.25V to AVCC0 – 0.25
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±1.5	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.38 A/D Conversion Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, Source impedance = 1.0 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Sample-and-hold circuit not in use	1.41	—	—	μs	High-precision channel ADSSTRn.SST[7:0] bits = 0Dh
	Sample-and-hold circuit in use	2.25	—	—		High-precision channel ADSSTRn.SST[7:0] bits = 0Dh ADSHCR.SSTSH[7:0] bits = 0Eh AN000 to 002 = 0.25 V to AVCC0 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error	Sample-and-hold circuit not in use	—	±0.5	±4.5	LSB	
	Sample-and-hold circuit in use	—	±1.5	±6.5		
Full-scale error	Sample-and-hold circuit not in use	—	±0.75	±4.5	LSB	
	Sample-and-hold circuit in use	—	±1.5	±6.5		
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample-and-hold circuit not in use	—	±1.25	±5.0	LSB	
	Sample-and-hold circuit in use	—	±3.0	±8.0		AN000 to 002 = 0.25V to AVCC0 – 0.25
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±1.5	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.39 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 2.7 to 5.5V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.7 to 5.5V	

Table 2.40 A/D Internal Reference Voltage Characteristics

Conditions: VCC = 2.7 V to 5.5V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*1	1.36	1.43	1.50	V	

Note 1. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

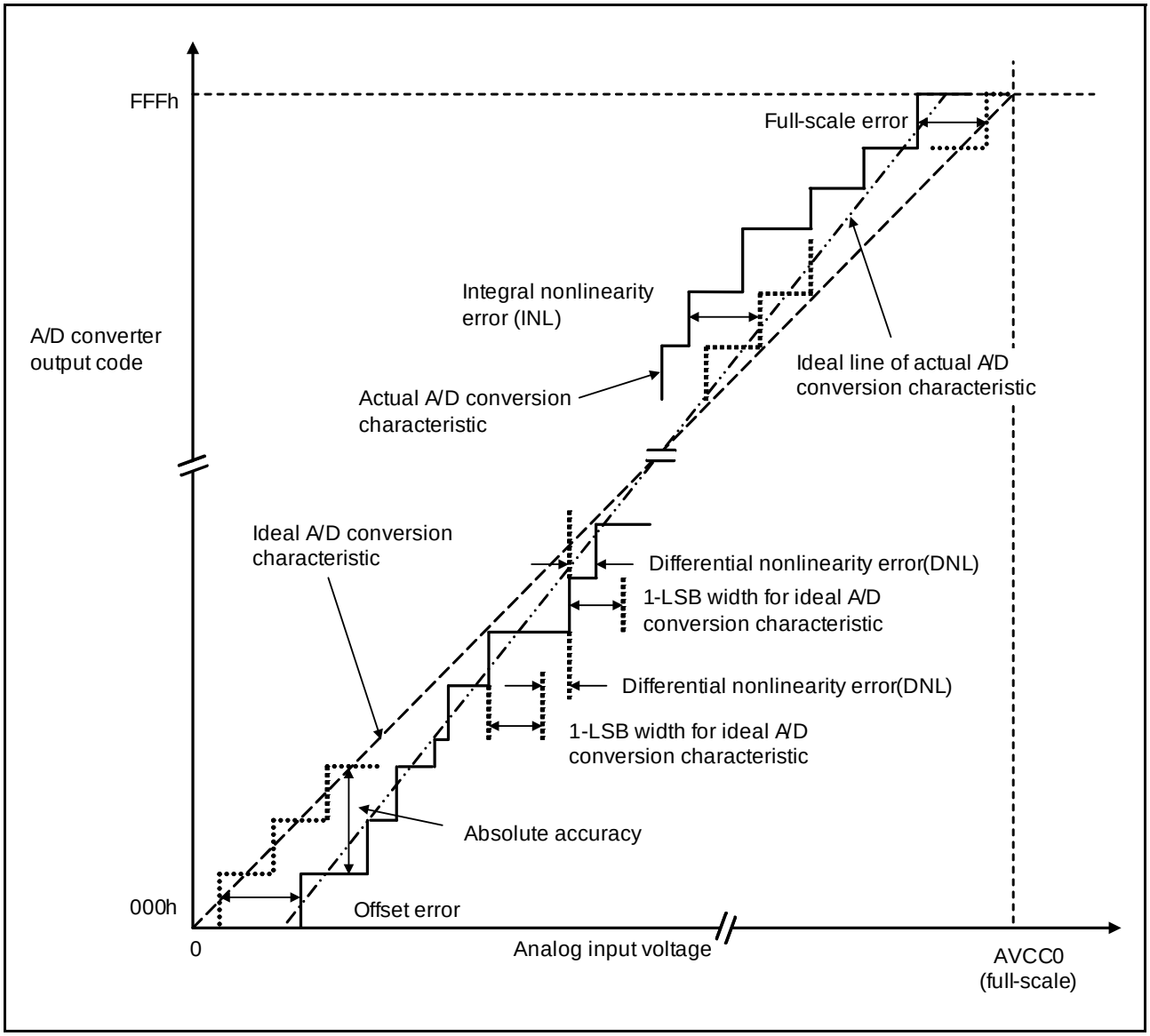


Figure 2.37 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (AVCC0) is 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

2.6 Programmable Gain Amplifier Characteristics

Table 2.41 Programmable Gain Amplifier Characteristics

Conditions: VCC = 2.7 V to AVCC0, AVCC0 = 4.5 V to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage		V_{poff}	—	—	8	mV	
Input voltage range		V_{pin}	V_{pout} (min)/G	—	V_{pout} (max)/G	V	
Output voltage range	G = 2.000, 2.500, 3.077	V_{pout}	0.1 × AVCC0	—	0.9 × AVCC0	V	
	G = 5.000, 8.000, 10.000		0.15 × AVCC0	—	0.85 × AVCC0		
Gain		G	2.000	—	10.000		
Gain error	G = 2.000, 2.500, 3.077	G_{err}	—	±1.0	±1.5	%	
	G = 5.000, 8.000, 10.000		—	±1.5	±2.5		
Slew rate		SR	10	—	—	V/µs	
Operation stabilization wait time		t_{start}	—	—	5.0	µs	

2.7 Comparator Characteristics

Table 2.42 Comparator Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{cioff}	—	—	20	mV	
Reference input voltage range	V_{cref}	0	—	AVCC0	V	
Response time	t_{cr}	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	t_{cf}	—	—	200		
Stabilization wait time for input selection	t_{cwait}	300	—	—	ns	
Operation stabilization wait time	t_{cmp}	—	—	1	µs	

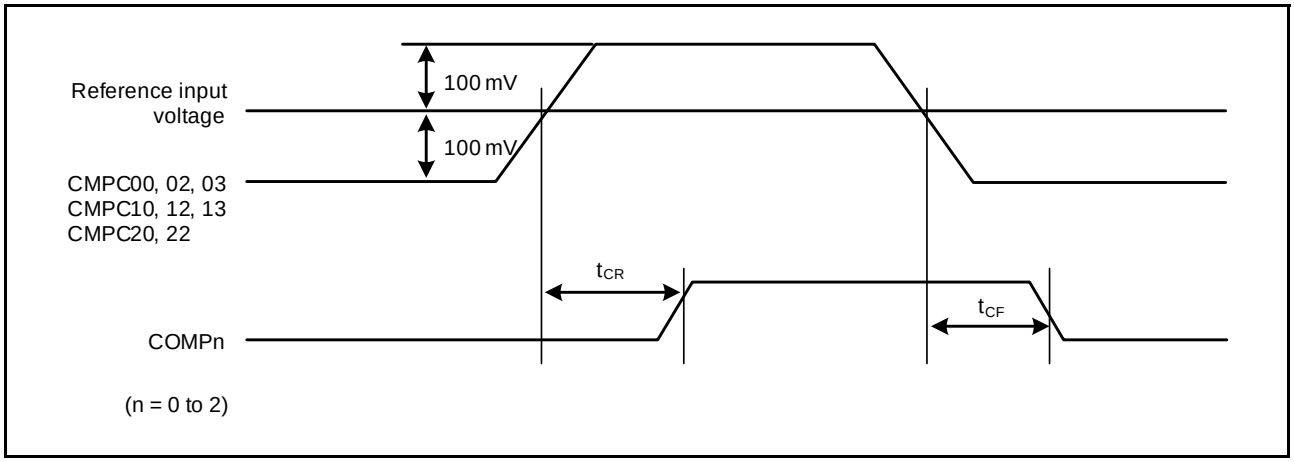


Figure 2.38 Comparator Response Time

2.8 D/A Conversion Characteristics

Table 2.43 D/A Conversion Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	
Absolute accuracy	—	—	±1.0	±3.0	LSB	

2.9 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.44 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 2.39, Figure 2.40
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97		Figure 2.41 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42		Figure 2.42 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48		Figure 2.43 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet0_n denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

Table 2.45 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	t_{POR}	—	28.4	—	ms	Figure 2.40
Wait time after voltage monitoring 0 reset cancellation	t_{LVD0}	—	568	—	µs	Figure 2.41
Wait time after voltage monitoring 1 reset cancellation	t_{LVD1}	—	100	—	µs	Figure 2.42
Wait time after voltage monitoring 2 reset cancellation	t_{LVD2}	—	100	—	µs	Figure 2.43
Response delay time	t_{det}	—	—	350	µs	Figure 2.39
Minimum VCC down time*1	t_{VOFF}	350	—	—	µs	Figure 2.39, VCC = 1.0 V or above
Power-on reset enable time	$t_{W(POR)}$	1	—	—	ms	Figure 2.40, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$Td_{(E-A)}$	—	—	300	µs	Figure 2.42, Figure 2.43
Hysteresis width (power-on reset (POR))	V_{PORH}	—	110	—	mV	
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	—	70	—	mV	Vdet0_0 to 2 selected Vdet1_0 to 4 selected
		—	60	—		Vdet1_5 to 8, LVD2 selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

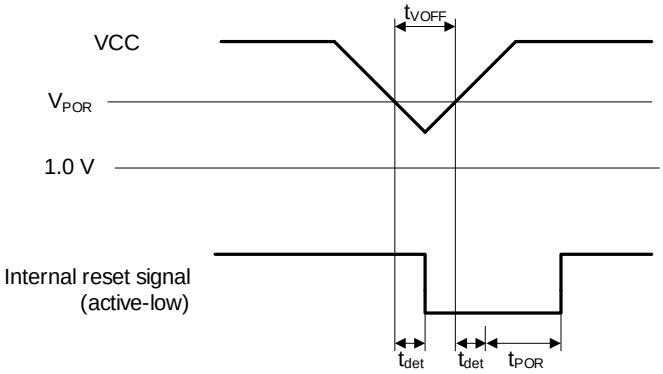
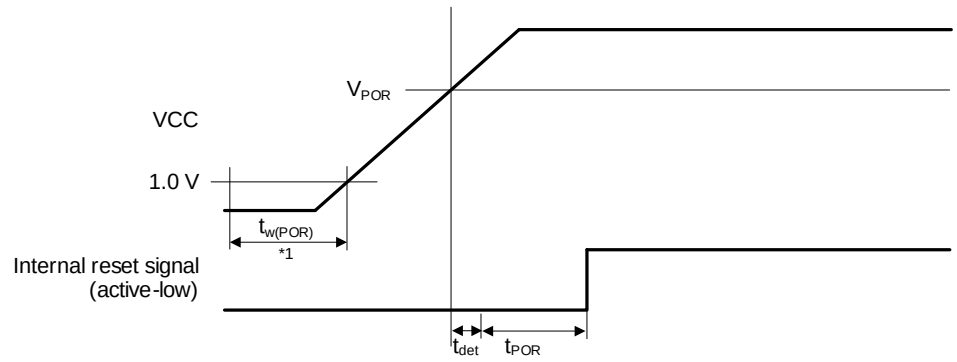


Figure 2.39 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.40 Power-On Reset Timing

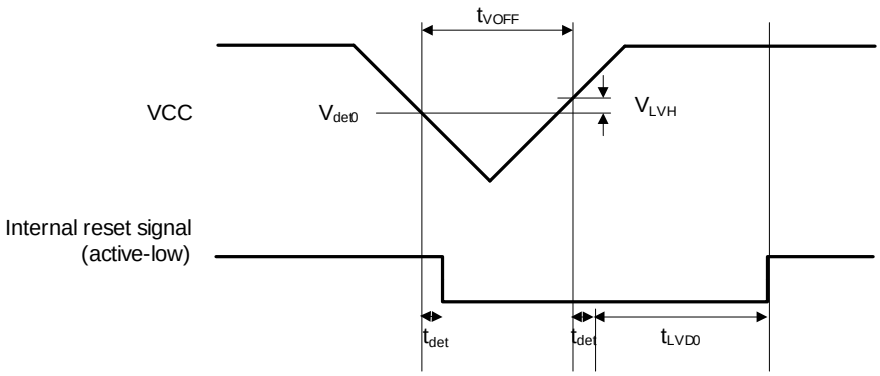


Figure 2.41 Voltage Detection Circuit Timing (V_{det0})

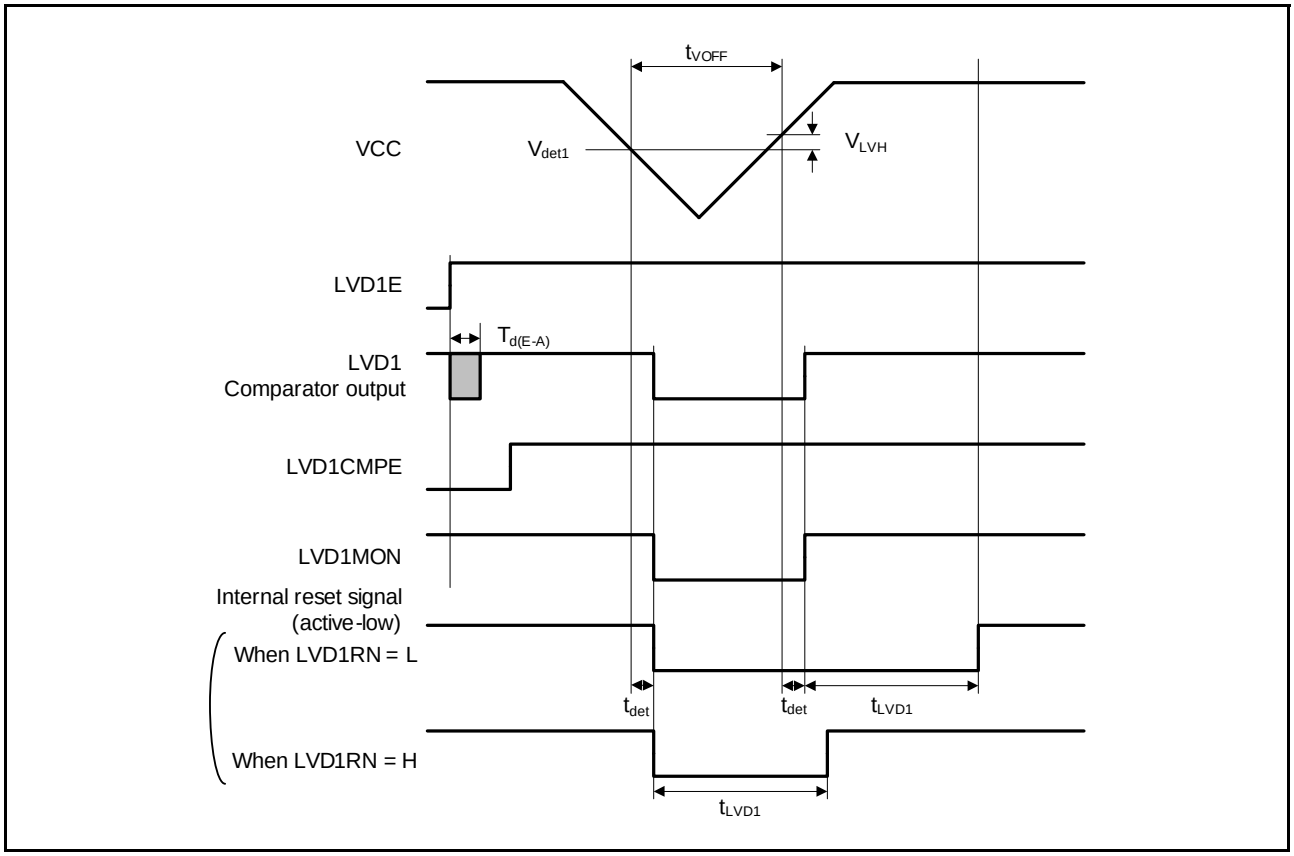


Figure 2.42 Voltage Detection Circuit Timing (V_{det1})

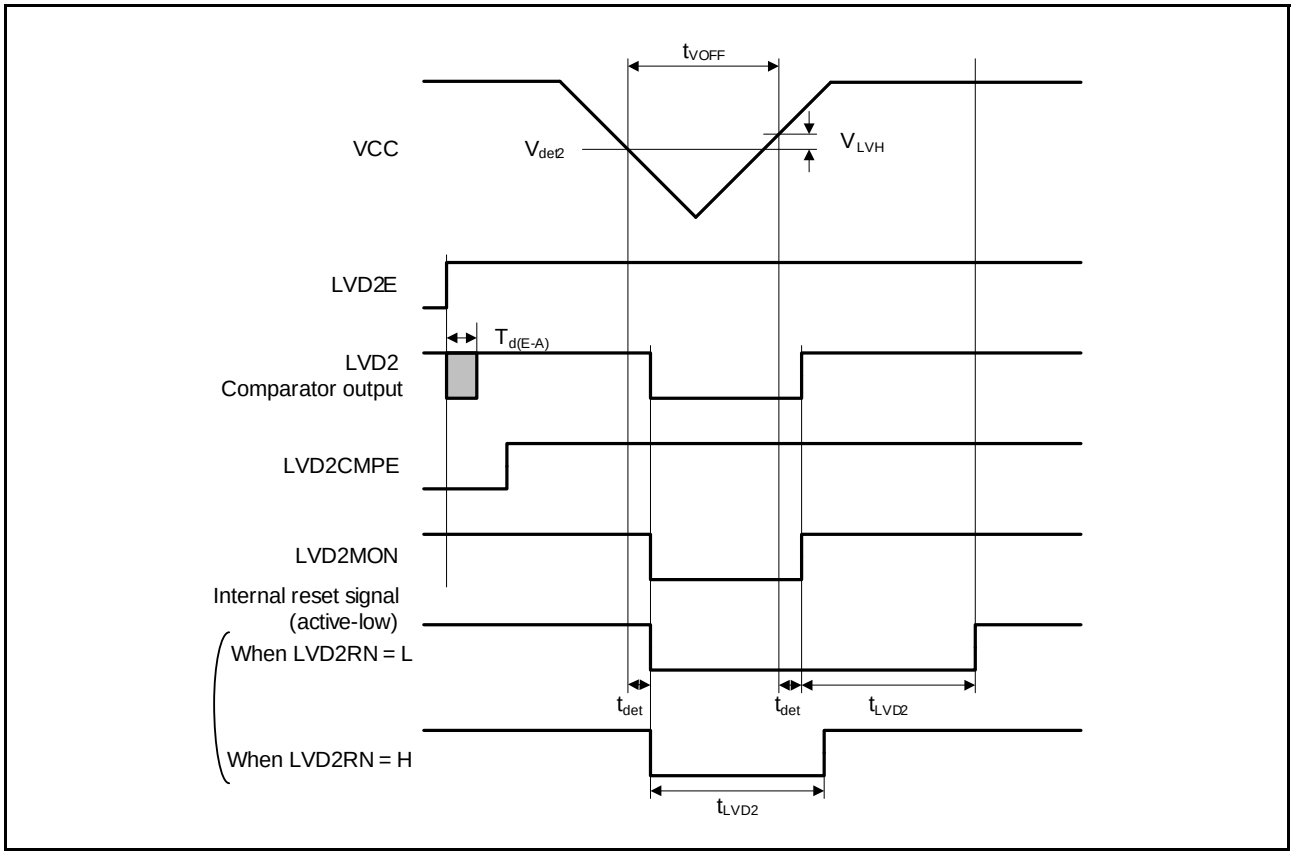


Figure 2.43 Voltage Detection Circuit Timing (V_{det2})

2.10 Oscillation Stop Detection Timing

Table 2.46 Oscillation Stop Detection Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V, Ta = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.44

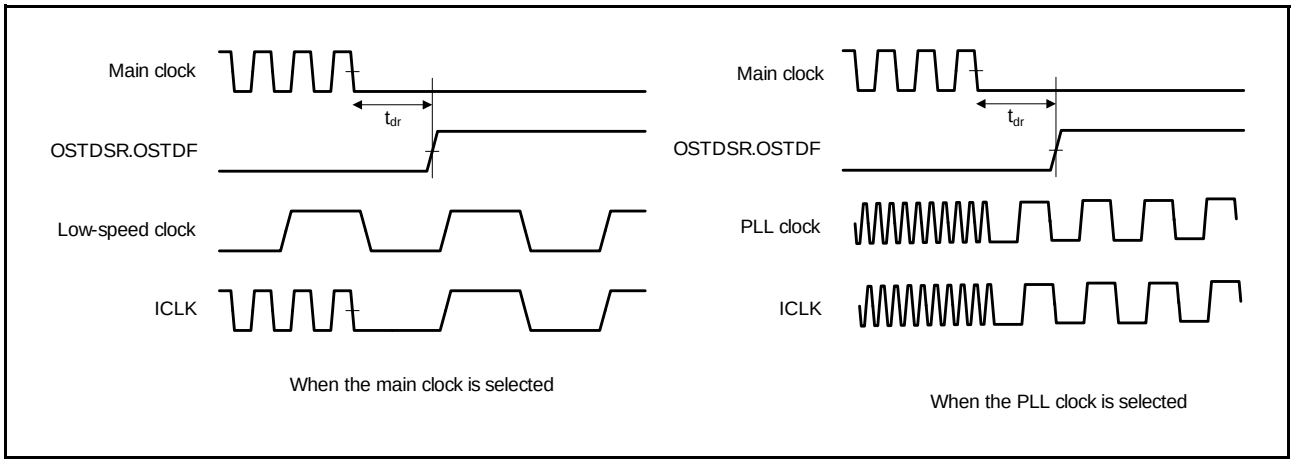


Figure 2.44 Oscillation Stop Detection Timing

2.11 ROM (Code Flash Memory) Characteristics

Table 2.47 ROM (Code Flash Memory) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycle*1		N_{PEC}	1000	—	—	Times	
Data retention	After 1000 times of erase	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of program/erase cycle: The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 256 times for different addresses in a 1-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.48 ROM (Code Flash Memory) Characteristics (2) High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V

Temperature range for program/erase: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	4-byte	t_{P4}	—	103	931	—	52	489	µs
Erase time	1-Kbyte	t_{E1K}	—	8.23	267	—	5.48	214	ms
	128-Kbyte	t_{E128K}	—	203	463	—	20	228	
Blank check time	4-byte	t_{BC4}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{BC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t_{SED}	—	—	21.6	—	—	12.8	µs
Start-up area switching setting time		t_{SAS}	—	12.6	543	—	6.16	432	ms
Access window setting time		t_{AWS}	—	12.6	543	—	6.16	432	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	5	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%. Check the accuracy of the frequency from the clock source.

Table 2.49 ROM (Code Flash Memory) Characteristics (3) Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V

Temperature range for program/erase: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	4-byte	t_{P4}	—	143	1330	—	96.8	932	µs
Erase time	1-Kbyte	t_{E1K}	—	8.3	269	—	5.85	219	ms
	128-Kbyte	t_{E128K}	—	203	464	—	46	260	
Blank check time	4-byte	t_{BC4}	—	—	78	—	—	50	µs
	1-Kbyte	t_{BC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{SED}	—	—	33.6	—	—	25.6	µs
Start-up area switching setting time		t_{SAS}	—	13.2	549	—	7.6	445	ms
Access window setting time		t_{AWS}	—	13.2	549	—	7.6	445	ms
ROM mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
ROM mode transition wait time 2		t_{MS}	3	—	—	3	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%. Check the accuracy of the frequency from the clock source.

2.12 E2 DataFlash (Data Flash Memory) Characteristics

Table 2.50 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Program/erase cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data retention	After 10000 times of erase	t_{DDRP}	20*2, *3	—	—	Year	T_a = +85°C
	After 100000 times of erase		5*2, *3	—	—		
	After 1000000 times of erase		—	1*2, *3	—		T_a = +25°C

Note 1. Definition of program/erase cycle: The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 1-byte program is performed 1000 times for different addresses in a 1-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).
Note 2. Characteristic when using the flash programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 2.51 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V
Temperature range for program/erase: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	1-byte	t_{DP1}	—	86	761	—	40.5	374	µs
Erase time	1-Kbyte	t_{DE1K}	—	17.4	456	—	6.15	228	ms
	4-Kbyte	t_{DE4K}	—	35.8	474	—	7.5	229	
Blank check time	1-byte	t_{DBC1}	—	—	48	—	—	15.9	µs
	1-Kbyte	t_{DBC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t_{DSED}	—	—	21.5	—	—	12.8	µs
DataFlash STOP recovery time		t_{DSTOP}	5.0	—	—	5	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 2.52 E2 DataFlash Characteristics (3): middle-speed operating mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = VCC to 5.5 V, VSS = AVSS0 = 0 V
Temperature range for program/erase: T_a = –40 to +85°C

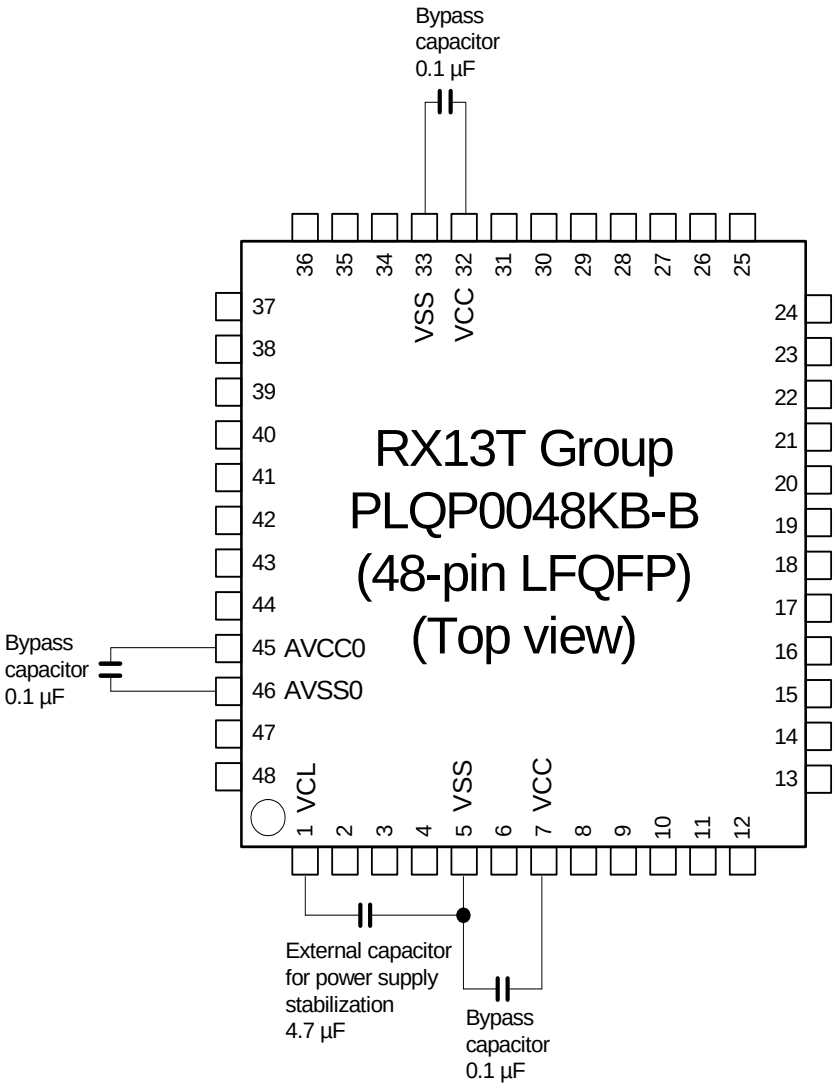
Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Program time	1-byte	t_{DP1}	—	126	1160	—	85.4	818	µs
Erase time	1-Kbyte	t_{DE1K}	—	17.5	457	—	7.76	259	ms
	4-Kbyte	t_{DE4K}	—	35.9	476	—	9.0	260	
Blank check time	1-byte	t_{DBC1}	—	—	78	—	—	50	µs
	1-Kbyte	t_{DBC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t_{DSED}	—	—	33.5	—	—	25.5	µs
DataFlash STOP recovery time		t_{DSTOP}	720	—	—	720	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

2.13 Usage Notes

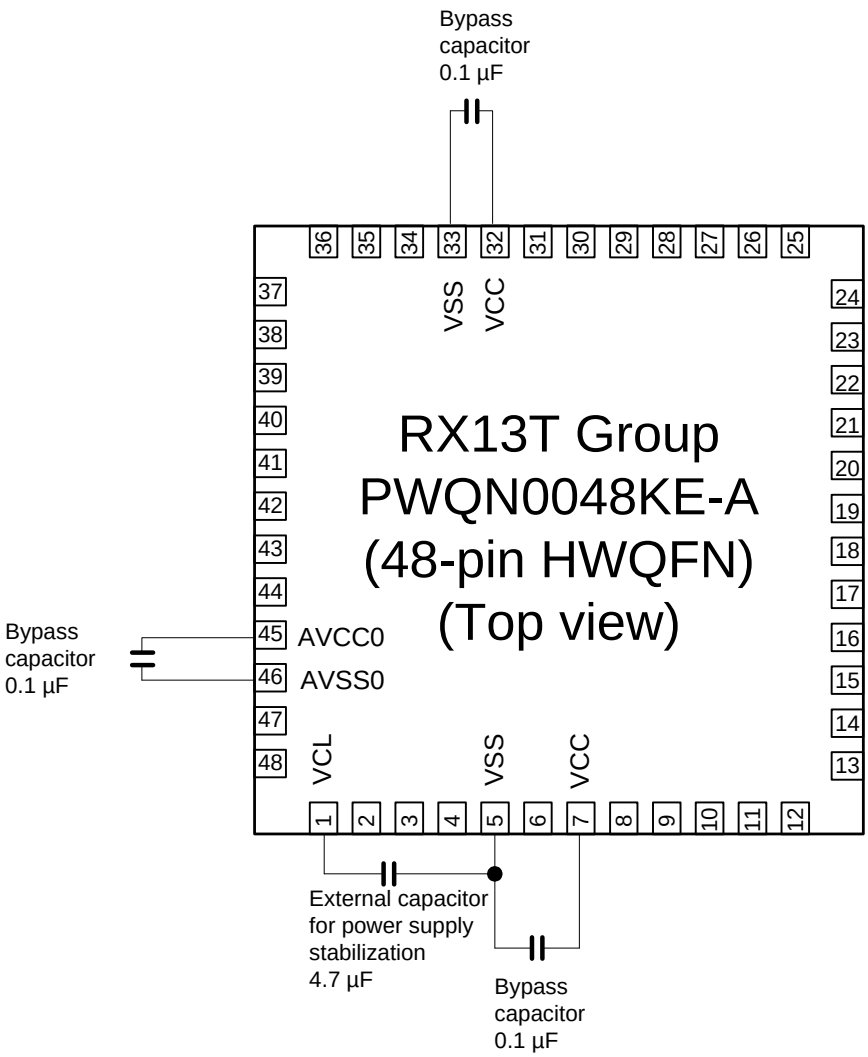
2.13.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 2.45 to Figure 2.48 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 26, 12-Bit A/D Converter (S12ADF) in the User's Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.



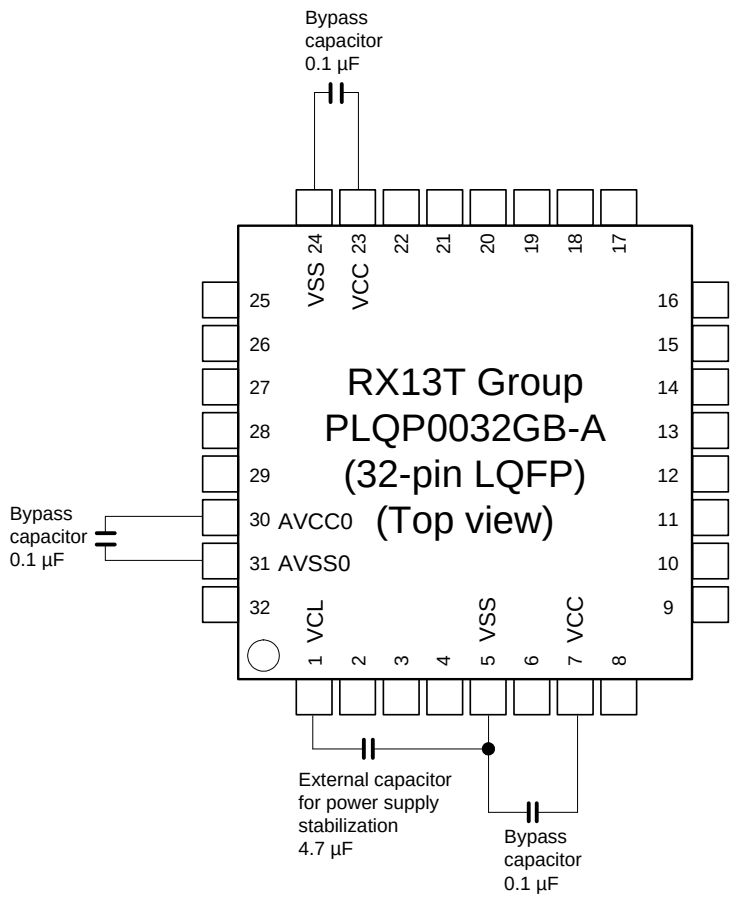
Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.45 Connecting Capacitors (48-Pin LFQFP)



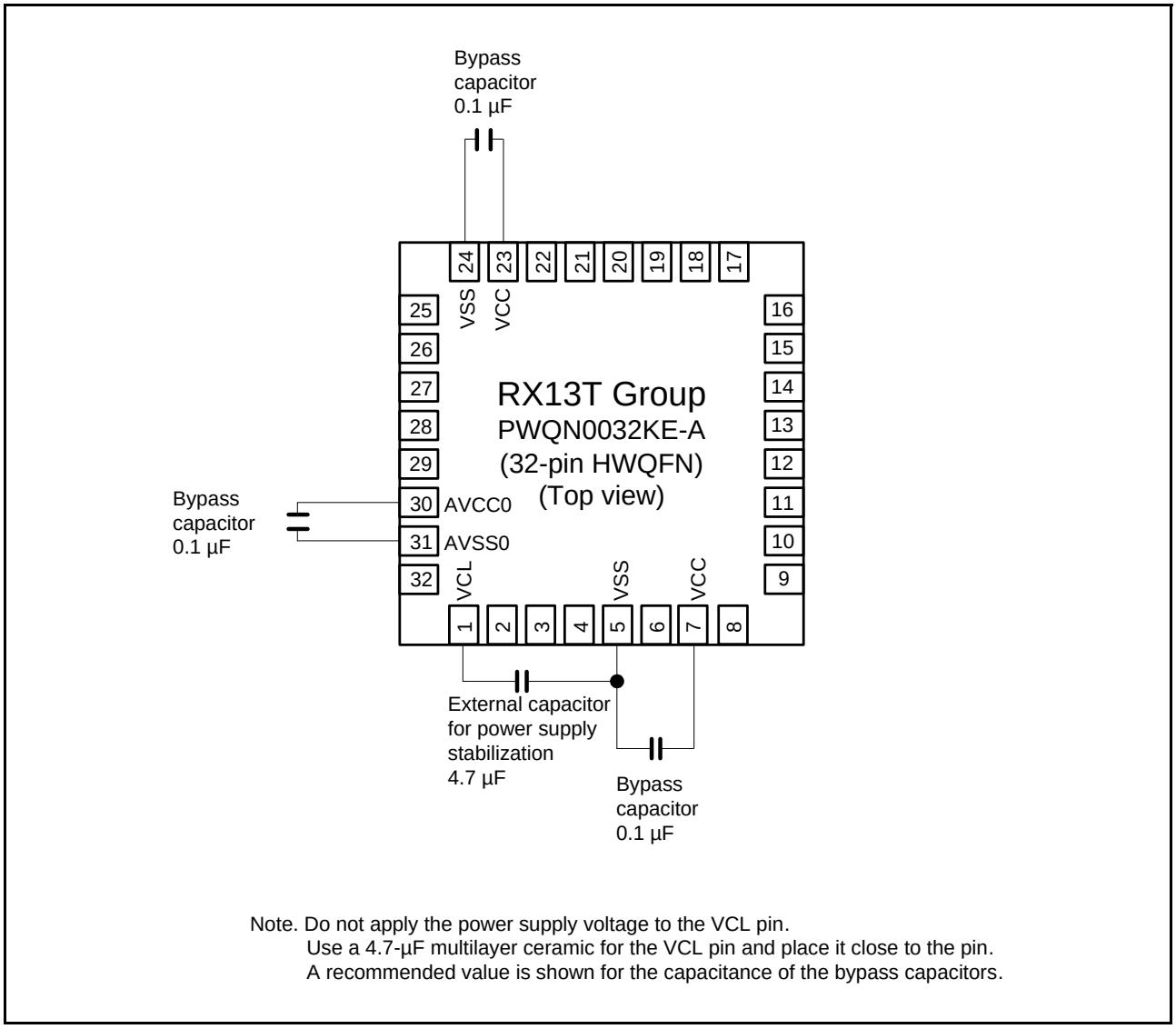
Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.46 Connecting Capacitors (48-Pin HWQFN)



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.47 Connecting Capacitors (32-Pin LQFP)



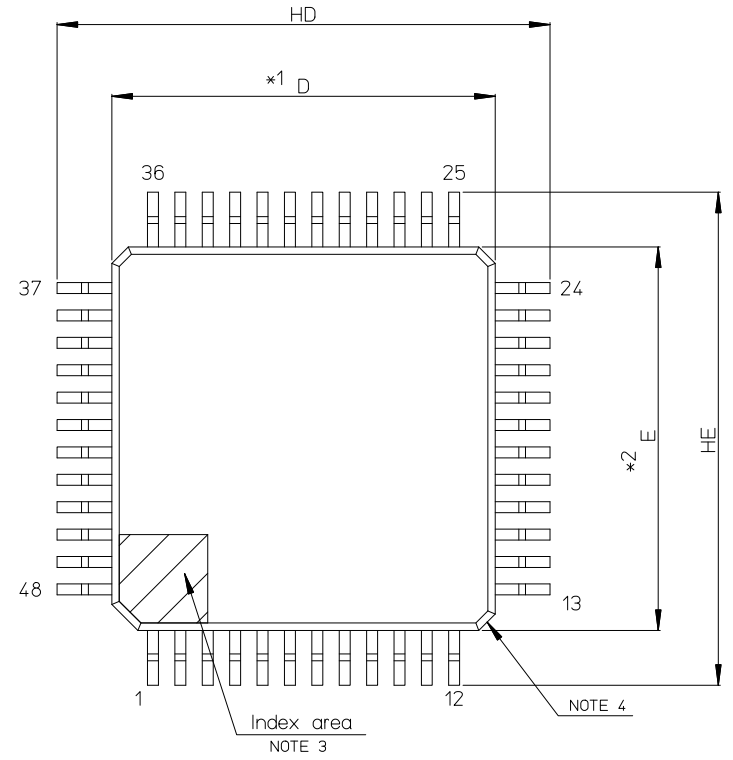
Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

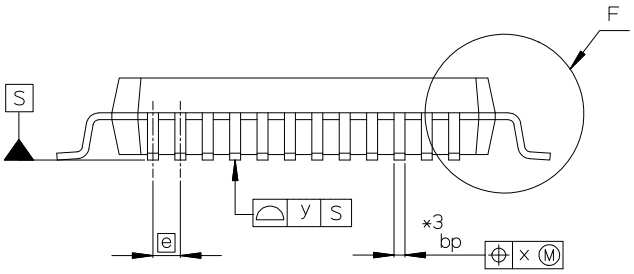
Figure 2.48 Connecting Capacitors (32-Pin HWQFN)

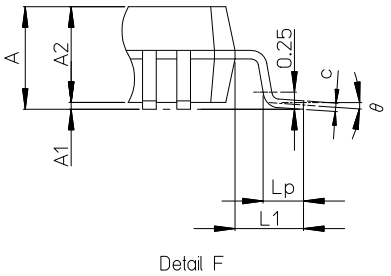
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	——	0.2g







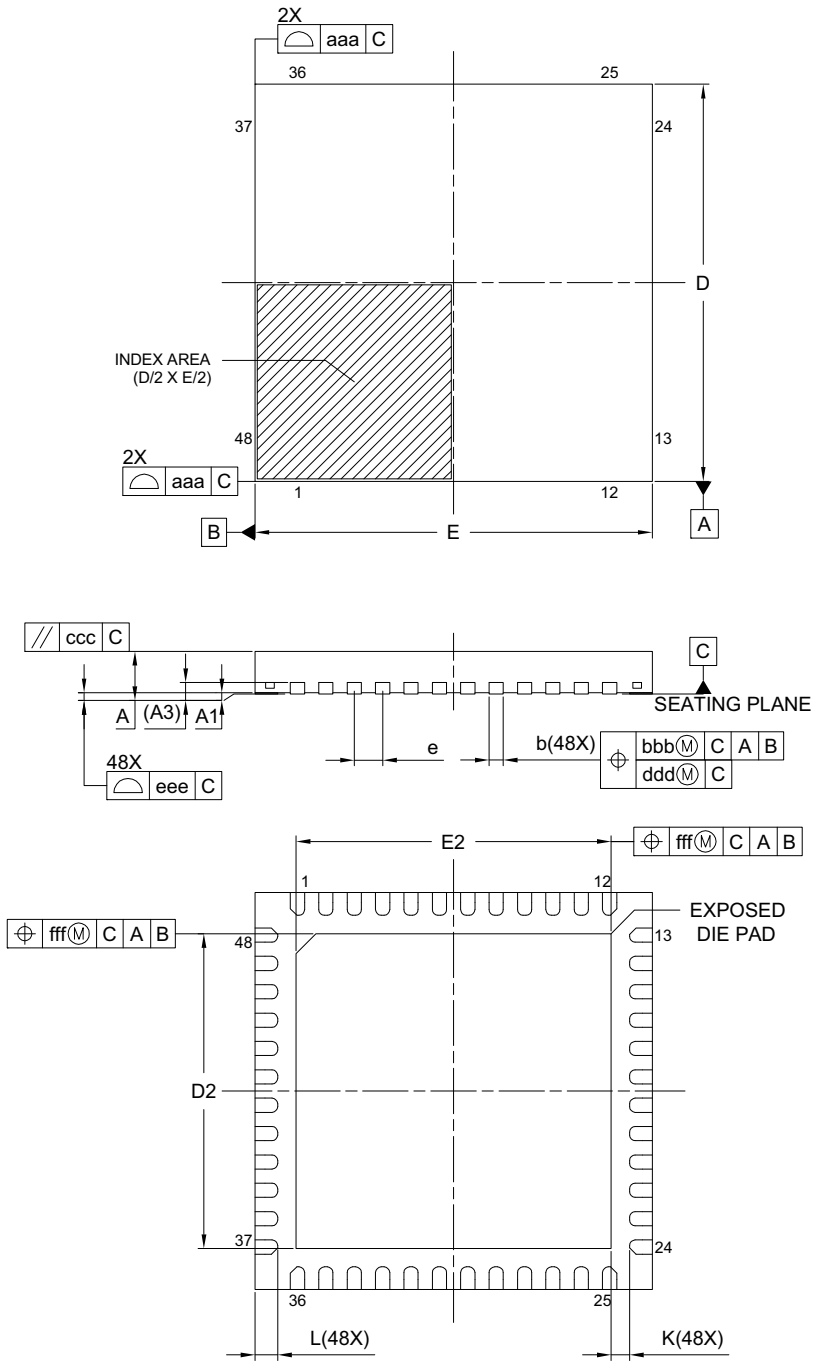
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	——	1.4	——
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.17	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure A 48-Pin LFQFP (PLQP0048KB-B)

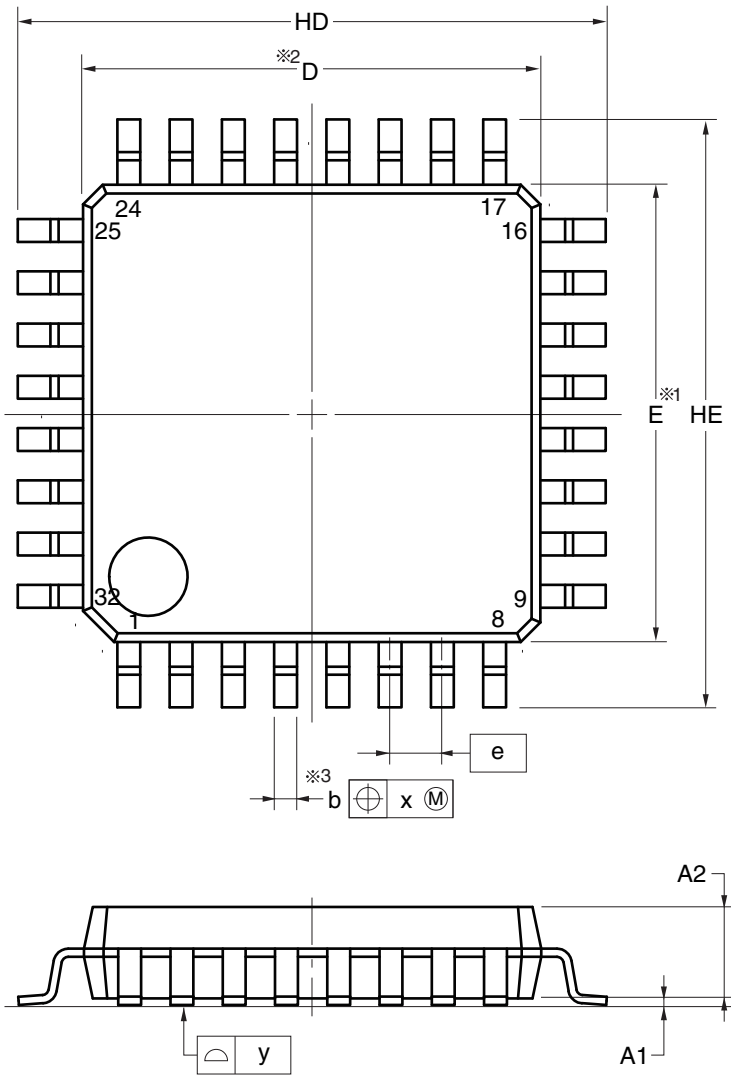
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KE-A	0.13

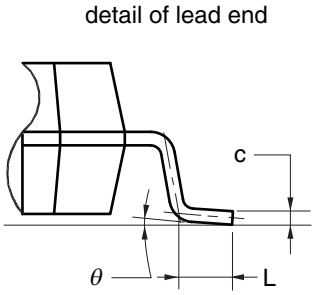


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.50	5.55	5.60
E_2	5.50	5.55	5.60
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure B 48-Pin HWQFN (PWQN0048KE-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2





(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

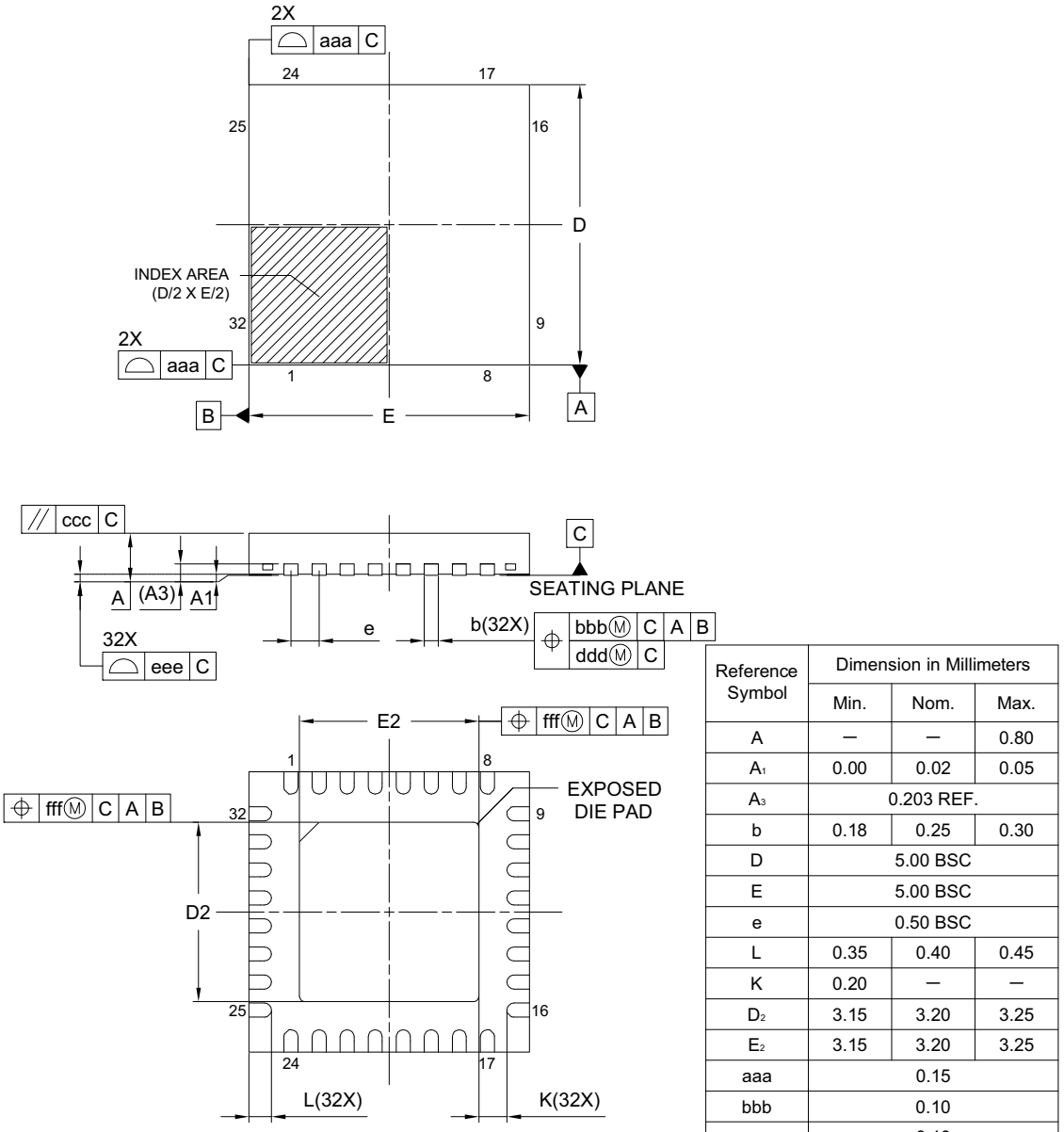
NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

Figure C 32-Pin LQFP (PLQP0032GB-A)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure D 32-Pin HWQFN (PWQN0032KE-A)

REVISION HISTORY	RX13T Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Aug 20, 2019	—	First edition, issued	
1.10	Mar 16, 2021	Features		
		1	48-pin HWQFN and 32-pin HWQFN Package Images, added	
		1. Overview		
		All	48-pin HWQFN and 32-pin HWQFN specifications, added	
		2. Electrical Characteristics		
		36 to 49	2.4.5 Timing of On-Chip Peripheral Modules, order of tables changed	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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