R61523

16,777,216–Color, 360x640-Dot Graphics LCD Controller Driver for α-Si TFT Panel

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Rev.1.01
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Description

The R61523 is liquid crystal controller driver LSI with internal frame memory for α-Si TFT panel sized 360RGB x 640-dot at maximum. The R61523 supports MIPI DBI Type B (16/8 bits) as system interface to microcomputer as well as high-speed frame memory write function, enabling efficient data transfer. It also supports MIPI DSI as high-speed interface.

The R61523 incorporates step-up and voltage follower circuits to generate drive voltage required for a-Si TFT panel and dynamic backlight control function to control backlight brightness depending on image data reducing power consumption at the backlight with slightest influence on the display quality.

Other features include 8-color display and power management functions, making the driver best suitable for small or mid sized portable devices such as digital mobile phones, small PDAs and mobile TV devices.

*MIPI: Mobile Industrial Processor Interface, DBI: Display Bus Interface, DSI: Display Serial Interface

Features

- Single chip driver for 16, 777, 216-color TFT 360RGB x 640-dot graphics (with internal gate and power supply circuits)
- Command set (Compliant with MIPI DCS Version 1.01.00) *DCS: Display Command Set
- System interface
  - MIPI-DBI (Compliant with MIPI DBI Version 2.00)
    Type B 16/8 bits
  - MIPI DSI 2 lanes (300Mbps/lane): 2 data lanes and 1 clock lane
    MIPI DSI: Version 1.01.00r11 21-Feb-2008
    MIPI D-PHY: Version 0.90.00 8-Oct-2007
- Video image display interface (see Note 1)
  - TE-I/F (MIPI DBI + TE synchronization signal output)
  - MIPI DSI TE-reporting
- Abundant color display and drawing functions
  - 16,777,216-color display
  - Partial display function
  - RGB-separate γ correction function
- Low-power consumption architecture (allowing direct input of interface I/O power supply)
  - Deep standby mode
  - 8-color mode (Idle Mode)
  - Input power supply voltage:
    Logic power supply: IOVCC
    MIPI D-PHY power supply: DPHYVCC
    Liquid crystal analog circuit power supply: VCI
- Dynamic backlight control function
- Internal liquid crystal drive power supply circuit
  - Liquid crystal drive (source driver/VCOM): DDVDHA/DDVDHB, VREG1, VCL
  - Gate driver power supply: VGH, VGL

  – VCOM drive (common VCOM method): VCOMH, VCOML
- RGB-separate γ correction function
- TFT display storage capacitance: Cst (common VCOM method)
- Internal frame memory: 691,200 bytes
- Liquid crystal display drive circuits: 1080 source signal lines and 640 gate signal lines
- One-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal NVM (32 bits for user identification code, 12 bits for VCOM adjustment): Rewriting data is guaranteed up to 5 times.
- Dummy pins used to fix pin to VCC or GND (see Note 2)

Notes: 1. Japanese Patent No. 3,826,159
Korean Patent No. 747,636
United States Patent No. 7,176,870
2. Japanese Patent No. 3,980,066
Korean Patent No. 401,270
Taiwan Patent No. 175,413
United States Patent No. 6,323,930
Japanese Patent No. 4,226,627
United States Patent No. 6,924,868

Power Supply Specification

Table 1 R61523 Power Supply Specification

No.	Item		R61523
1	TFT data line drive circuit		1080 outputs
2	TFT gate line drive circuit		640 outputs
3	TFT display storage capacitance		Cst (common VCOM method)
4	Liquid crystal drive output	S1-1080	V0 ~ V255 grayscales
		G1-640	VGH-VGL
		VCOM	VCOMH = 3.0V ~ (DDVDH*-0.5V) (* = A, B) VCOML = (VCL+0.5V) ~ 0V
5	Input voltages	IOVCC (interface voltage and logic regulator power supply)	1.65V ~ 3.60V (See note 1)
		DPHYVCC (MIPI DSI-PHY power supply)	1.65V ~ 1.95V (See note 1) 1.65V ~ 3.60V (When DSI is not used)
		VCI (LCD drive power supply)	2.60V ~ 3.00V
6	System interface (MIPI DBI)	CSX, DCX, WRX, RDX, DB[15:0], TE, IM[2:0], RESX	IOVCC-GND (See note 1)
7	LED I/F	LEDPWM	IOVCC-GND
8	LCD drive supply voltages	DDVDHA, DDVDHB	5.6V (Typ.), VCI x 2
		VGH	16.0V (Typ.), VCI2 x 4 (See note 2)
		VGL	-10.5V (Typ.), -(VCI2 x 2 + VCI3) (See note 2)
		VGH-VGL	Max. 28V
		VCL	-2.8V (Typ.), VCI x -1
		VCI-VCL	Max. 6V
9	Internal step-up circuit	DDVDH	VCI x 2
		VGH	VCI2 x 4
		VGL	-1*(VCI2 x 2 + VCI3)
		VCL	VCI x –1

Notes:
1. Connect to IOVCC and DPHYVCC, or CSX, DCX, WRX, RDX, DB[15:0], TE, IM[2:0], and RESX on the FPC when the electrical potentials are the same.
2. VCI2 and VCI3 are the power supply of the voltages generated from the internal power supply circuit.
3. For voltage, see DC Characteristics in Electrical Characteristics.

Block Diagram

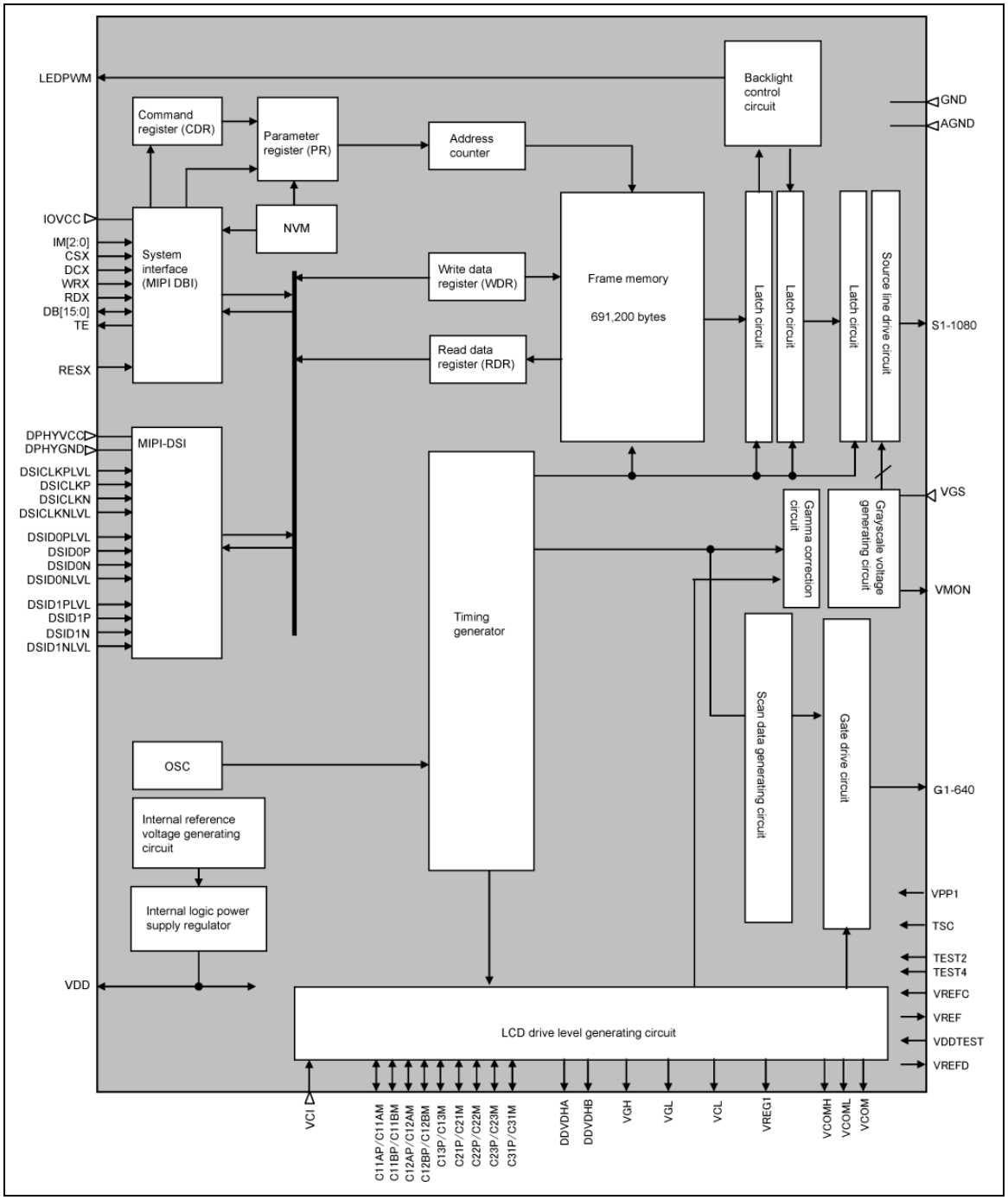


Figure 1

Block Function

(1) System Interface

The R61523 supports MIPI DSI and MIPI DBI Type B (16/8 bits). The interface is selected by setting IM[0:2] pin.

Table 2

IM2	IM1	IM0	Interface	Used pin	Available color number
0	0	0	Setting inhibited	–	–
0	0	1	Setting inhibited	–	–
0	1	0	DBI Type B 16 bits	DB[15:0]	65,536 / 262,144 / 16,777,216
0	1	1	DBI Type B 8 bits	DB[7:0]	65,536 / 262,144 / 16,777,216
1	0	0	DSI	D0, D1	65,536 / 262,144 / 16,777,216
1	0	1	Setting inhibited	–	–
1	1	0	Setting inhibited	–	–
1	1	1	Setting inhibited	–	–

Set the number of colors using set_pixel_format (3Ah).

(a) MIPI DBI Type B (16/8 Bits)

The R61523 supports MIPI DBI Type B (16/8 bits) that uses a command method which has 8-bit command registers and 8-bit parameter registers. Also, the R61523 has a 24-bit write register (WDR) and read register (RDR). The WDR is used to store data temporarily that is automatically written to the internal frame memory through internal operation of the chip. The RDR is used to temporarily store the data read out from the frame memory.

The WDR is used to temporarily store the data read out from the host processor to the frame memory. For this reason, invalid data is sent to the data bus at first and valid data is sent as the R61523 reads second and subsequent data from the frame memory via RDR.

Table 3 Register Selection

			Function
DCX	RDX	WRX	
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(2) Video Image Interface (TE-signal, TE-reporting)

The R61523 supports TE as external display interface for video image.

When DBI is selected, display data is written in sync with TE signal which is generated from internal clock to prevent flicker on the panel.

When DSI is selected, display data is written in sync with the start of the frame period by TE-reporting function. This enables updating image data without flicker on the panel.

(3) Address Counter (AC)

The address counter (AC) gives an address to the frame memory. Address information defined by CDR and PR is transferred to the AC. The AC is automatically updated plus or minus 1 as the R61523 writes/reads data to/from the frame memory. Display data can be written only to the rectangular area defined in the frame memory.

(4) Frame Memory

The R61523 incorporates the frame memory that has a capacity of 691,200 bytes, which can store bit-pattern data of 360RGB x 640 graphics display at maximum using 24 bits to represent one pixel.

(5) Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale setting value in the γ correction register. RGB-separate γ correction setting enables the maximum of 16,777,216-color display.

(6) LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates VREG1, VGH, VGL, VCL, and VCOM levels to drive the liquid crystal panel.

(7) Timing Generator

The timing generator is used to generate timing signals for the operation of internal circuits such as frame memory. The timing signals for display operation such as frame memory read and frame memory access by host processor are generated separately so that the two do not interfere with each other.

(8) Oscillator (OSC)

The R61523 incorporates an oscillator. The frame frequency can be adjusted by commands.

(9) LCD Driver Circuit

The LCD driver circuit consists of a 1080-channel source driver (S[1:1080]). The display pattern data is latched when 360RGB pixels of data are input. The voltage is output from the source driver according to the latched data. The shift direction of source output can be changed by setting SS bit (C0h). The gate driver circuit consists of a 640-channel gate driver (G[1:640]). The voltage at VGH level or VGL level is output from the gate driver. The shift direction of gate output can be changed by GS bit (C0h). The scan mode of the gate driver can be changed by SM bit (C0h) according to the mounting condition.

(10) Internal Logic Power Supply Regulator

The internal logic power supply regulator generates power supply for internal logic circuit.

(11) Backlight Control Circuit

Backlight control circuit adjusts backlight brightness according to histogram of the image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

Pin Function

Table 4 External Power Supply Pins

Signal	I/O	Connect to	Function	Unused pin
IOVCC	I	Power supply	Power supply to interface pins and internal VDD regulator.	-
GND	I	Power supply	GND for Internal logic and interface pins. GND=0V.	-
VCI	I	Power supply	Power supply to liquid crystal power supply analog circuit.	-
AGND	I	Power supply	Analog GND (logic regulator and liquid crystal power supply circuit). Connect to GND on the FPC to prevent noise in case of COG.	-
DPHYVCC	I	Power supply	Power supply to MIPI DSI D-PHY. Connect to power supply when DSI is not used.	-
DPHYGND	I	Power supply	GND for MIPI DSI D-PHY. Connect to GND on the FPC to prevent noise in case of COG.	-

Table 5 System Interface Pins (Amplitude: IOVCC - GND)

Signal	I/O	Connect to	Function	Unused pin
CSX	I	Host Processor	Chip select signal. Low: Select (Accessible) High: Not select (Inaccessible) Make sure to connect to host processor. Follow AC timing to control the signal.	IOVCC
DCX	I	Host Processor	Command/data select signal Low: Select command High: Select data	IOVCC
WRX	I	Host Processor	Write strobe signal in DBI Type B operation. Write data when WRX is Low.	IOVCC
RDX	I	Host Processor	Read strobe signal. Read out data when RDX is Low.	IOVCC
DB[15:0]	I/O	Host Processor	16-bit bi-directional data bus in DBI Type B operation. 8-bit interface: Use DB [7:0] 16-bit interface: Use DB [15:0] Abnormal current (through current) does not occur when CSX is High and the data bus is Hi-z.	IOVCC or GND
TE	O	Host Processor	Tearing Effect output signal	Open
IM[2:0]	I	Host Processor	Interface select signal. Select interface from DBI Type B and DSI.	-
RESX	I	Host Processor or external RC oscillator	Reset pin. The R61523 is initialized when RESX is Low. Make sure to execute power-on reset when turning power on.	-

Table 6 MIPI DSI Pins

Signal	I/O	Connect to	Function	Unused pin
DSICLKPLVL	I	DSICLKP	DSI CLK+ signal. Connect to DSICLKP on the FPC in case of COG.	DPHYGND
DSICLKP	I	Host Processor	DSI CLK+ signal. Connect to DSICLKPLVL on the FPC in case of COG.	DPHYGND
DSICLKN	I	Host Processor	DSI CLK- signal. Connect to DSICLKNLVL on the FPC in case of COG.	DPHYGND
DSICLKNLVL	I	DSICLKN	DSI CLK- signal. Connect to DSICLKN on the FPC in case of COG.	DPHYGND
DSID0PLVL	I	DSID0P	DSI D0+ signal. Connect to DSID0P on the FPC in case of COG.	DPHYGND
DSID0P	I/O	Host Processor	DSI D0+ signal. Connect to DSID0PLVL on the FPC in case of COG.	DPHYGND
DSID0N	I/O	Host Processor	DSI D0- signal. Connect to DSID0NLVL on the FPC in case of COG.	DPHYGND
DSID0NLVL	I	DSID0N	DSI D0- signal. Connect to DSID0N on the FPC in case of COG.	DPHYGND
DSID1PLVL	I	DSID1P	DSI D1+ signal. Connect to DSID1P on the FPC in case of COG.	DPHYGND
DSID1P	I	Host Processor	DSI D1+ signal. Connect to DSID1PLVL on the FPC in case of COG.	DPHYGND
DSID1N	I	Host Processor	DSI D1- signal. Connect to DSID1NLVL on the FPC in case of COG.	DPHYGND
DSID1NLVL	I	DSID1N	DSI D1- signal. Connect to DSID1N on the FPC in case of COG.	DPHYGND

Table 7 LED Driver Control Pins (Amplitude: IOVCC-GND)

Signal	I/O	Connect to	Function	Unused pin
LEDPWM	O	LED driver	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High).	Open

Table 8 Power Supply Circuit Pins

Signal	I/O	Connect to	Function	Unused pin
VDD	O	Stabilizing capacitor	Output from internal logic regulator. Used for the internal logic power supply. Connect to stabilizing capacitor.	-
DDVDHA, DDVDHB	O	Stabilizing capacitor	Source driver liquid crystal and VCOM drive power supply. The output level from a step-up circuit, generated from VCI. The step-up factor is 2. Connect to stabilizing capacitor.	-
VGH	O	Stabilizing capacitor, liquid crystal panel	Liquid crystal drive power supply. The output level form a step-up circuit, generated from VCI2. The step-up factor is 4.	-
VGL	O	Stabilizing capacitor, liquid crystal panel	Liquid crystal drive power supply. The output level form a step-up circuit, generated from VCI2 and VCI3. The step-up factor is -(VCI2 x 2 + VCI3).	-
VCL	O	Stabilizing capacitor	VCOML drive power supply. Connect to stabilizing capacitor.	-
C11AP, C11AM, C11BP, C11BM, C12AP, C12AM, C12BP, C12BM, C13P, C13M, C21P, C21M, C22P, C22M, C23P, C23M, C31P, C31M	I/O	Step-up capacitor	Capacitor connection pins for a step-up circuit.	-

Table 9 LCD Drive Power Supply Pins

Signal	I/O	Connect to	Function	Unused pin
VREG1	O	Stabilizing capacitor	The output level generated from VCIR. The output level from the internal reference power supply is determined by the factor, which is set by instruction (VRH*). VREG serves as reference of (1) source driver grayscale, (2) VCOMH level, and (3) VCOM width. Connect a stabilizing capacitor to use this pin.	-
VCOM	O	TFT common electrode	Power supply to TFT panel's common electrode. VCOM output level alternates between VCOMH and VCOML. The alternating cycle is set by a register. Also, the VCOM output can be started and halted by register setting.	-
VCOMH	O	Stabilizing capacitor	VCOM High level, which is set by internal electronic volume (VCM).	-
VCOML	O	Stabilizing capacitor	VCOM Low level, which is set by instruction (VDV).	-
VGS	O	GND	Reference level of the grayscale voltage generating circuit.	-
S[1:1080]	O	Liquid crystal panel	Liquid crystal application voltages. The shift direction of segment signal output can be changed by setting the SS bit. SS = 0: The data in the frame memory address "00000h" is outputted from S1. SS = 1: The data in the frame memory address "00000h" is outputted from S1080.	Open
G[1:640]	O	Liquid crystal panel	Gate line output signals. VGH: Gate line is selected. VGL: Gate line is not selected.	Open

Table 10 Other Pins (Test and Dummy)

Signal	I/O	Connect to	Function	Unused pin
VREFC	I	GND	Test pin. Fix to GND.	-
VREFD	O	Open	Test pin. Leave it open.	-
VREF	O	Open	Test pin. Leave it open.	-
VDDTEST	I	GND	Test pin. Fix to GND.	-
GNDDUM, AGNDDUM	O	-	Pins to fix electrical potential. Do not use them for other purposes. The electrical potential can be fixed by connecting unused interface pins and test pins to these dummy pins on the glass. Leave them open when they are not used.	Open
DPHYGNDDUM [1:2]	I	GND	Fix to GND on FPC. The electrical potential can be fixed by connecting unused interface pins and test pins to these dummy pins on the glass.	-
VMON	O	Open	Test pin. Leave it open.	-
TSC	I	GND	Test pin. Fix to GND.	-
TEST2	I	GND	Test pin. Fix to GND.	-
TEST4	I	GND	Test pin. Fix to GND.	-
VPP1	I	GND	Test pin. Leave it open or fix to GND. Do not make an ITO wiring when leaving it open.	Open/ GND
DUMMYR[1:4]	-	-	Short-circuited in the LSI to measure COG contact resistance. DUMMYR1 and DUMMYR2, DUMMYR3 and DUMMYR4 are short-circuited.	Open
DUMMY[1:2]	O	Open	Dummy pads. Leave them open.	-
TESTO[1:10]	O	Open	Dummy pads. Leave them open.	-

Patents of dummy pins used to fix pin to VCC or GND are granted as below.

PATENTS ISSUED: Japanese Patent No. 3,980,066
Korean Patent No. 401,270
Taiwan Patent No. 175,413
United States Patent No. 6,323,930
Japanese Patent No. 4,226,627
United States Patent No. 6,924,868

R61523 Pad Coordinates(No.1)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1	DUMMY1	-13320.0	-449.0
2	DUMMYR1	-13240.0	-449.0
3	DUMMYR2	-13160.0	-449.0
4	VCOM	-13080.0	-449.0
5	VCOM	-13000.0	-449.0
6	VCOM	-12920.0	-449.0
7	VCOM	-12840.0	-449.0
8	AGND	-12760.0	-449.0
9	AGND	-12680.0	-449.0
10	AGND	-12600.0	-449.0
11	AGND	-12520.0	-449.0
12	AGND	-12440.0	-449.0
13	AGND	-12360.0	-449.0
14	GND	-12280.0	-449.0
15	GND	-12200.0	-449.0
16	GND	-12120.0	-449.0
17	GND	-12040.0	-449.0
18	GND	-11960.0	-449.0
19	GND	-11880.0	-449.0
20	DDVDHB	-11800.0	-449.0
21	DDVDHB	-11720.0	-449.0
22	DDVDHB	-11640.0	-449.0
23	DDVDHB	-11560.0	-449.0
24	DDVDHB	-11480.0	-449.0
25	DDVDHB	-11400.0	-449.0
26	C11BP	-11320.0	-449.0
27	C11BP	-11240.0	-449.0
28	C11BP	-11160.0	-449.0
29	C11BP	-11080.0	-449.0
30	C11BP	-11000.0	-449.0
31	C11BP	-10920.0	-449.0
32	C11BM	-10840.0	-449.0
33	C11BM	-10760.0	-449.0
34	C11BM	-10680.0	-449.0
35	C11BM	-10600.0	-449.0
36	C11BM	-10520.0	-449.0
37	C11BM	-10440.0	-449.0
38	AGND	-10360.0	-449.0
39	AGND	-10280.0	-449.0
40	AGND	-10200.0	-449.0
41	AGND	-10120.0	-449.0
42	AGND	-10040.0	-449.0
43	AGND	-9960.0	-449.0
44	C12BP	-9880.0	-449.0
45	C12BP	-9800.0	-449.0
46	C12BP	-9720.0	-449.0
47	C12BP	-9640.0	-449.0
48	C12BP	-9560.0	-449.0
49	C12BP	-9480.0	-449.0
50	C12BM	-9400.0	-449.0

(Unit: um)

Pad No.	Pad Name	X	Y
51	C12BM	-9320.0	-449.0
52	C12BM	-9240.0	-449.0
53	C12BM	-9160.0	-449.0
54	C12BM	-9080.0	-449.0
55	C12BM	-9000.0	-449.0
56	VCI	-8920.0	-449.0
57	VCI	-8840.0	-449.0
58	VCI	-8760.0	-449.0
59	VCI	-8680.0	-449.0
60	VCI	-8600.0	-449.0
61	VCI	-8520.0	-449.0
62	VCI	-8440.0	-449.0
63	VCI	-8360.0	-449.0
64	C12AM	-8280.0	-449.0
65	C12AM	-8200.0	-449.0
66	C12AM	-8120.0	-449.0
67	C12AM	-8040.0	-449.0
68	C12AM	-7960.0	-449.0
69	C12AM	-7880.0	-449.0
70	C12AP	-7800.0	-449.0
71	C12AP	-7720.0	-449.0
72	C12AP	-7640.0	-449.0
73	C12AP	-7560.0	-449.0
74	C12AP	-7480.0	-449.0
75	C12AP	-7400.0	-449.0
76	AGND	-7320.0	-449.0
77	AGND	-7240.0	-449.0
78	AGND	-7160.0	-449.0
79	AGND	-7080.0	-449.0
80	AGND	-7000.0	-449.0
81	AGND	-6920.0	-449.0
82	C11AM	-6840.0	-449.0
83	C11AM	-6760.0	-449.0
84	C11AM	-6680.0	-449.0
85	C11AM	-6600.0	-449.0
86	C11AM	-6520.0	-449.0
87	C11AM	-6440.0	-449.0
88	C11AP	-6360.0	-449.0
89	C11AP	-6280.0	-449.0
90	C11AP	-6200.0	-449.0
91	C11AP	-6120.0	-449.0
92	C11AP	-6040.0	-449.0
93	C11AP	-5960.0	-449.0
94	DDVDHA	-5880.0	-449.0
95	DDVDHA	-5800.0	-449.0
96	DDVDHA	-5720.0	-449.0
97	DDVDHA	-5640.0	-449.0
98	DDVDHA	-5560.0	-449.0
99	DDVDHA	-5480.0	-449.0
100	GNDDUM	-5400.0	-449.0

R61523 Pad Coordinates(No.2)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
101	GNDDUM	-5320.0	-449.0
102	VDDTEST	-5240.0	-449.0
103	VREFC	-5160.0	-449.0
104	VREFD	-5080.0	-449.0
105	VREF	-5000.0	-449.0
106	TSC	-4920.0	-449.0
107	TEST2	-4840.0	-449.0
108	TEST4	-4760.0	-449.0
109	GND	-4680.0	-449.0
110	GND	-4600.0	-449.0
111	GND	-4520.0	-449.0
112	GND	-4440.0	-449.0
113	GND	-4360.0	-449.0
114	GND	-4280.0	-449.0
115	GND	-4200.0	-449.0
116	GND	-4120.0	-449.0
117	IOVCC	-4040.0	-449.0
118	IOVCC	-3960.0	-449.0
119	IOVCC	-3880.0	-449.0
120	IOVCC	-3800.0	-449.0
121	IOVCC	-3720.0	-449.0
122	IOVCC	-3640.0	-449.0
123	IOVCC	-3560.0	-449.0
124	VDD	-3480.0	-449.0
125	VDD	-3400.0	-449.0
126	VDD	-3320.0	-449.0
127	VDD	-3240.0	-449.0
128	VDD	-3160.0	-449.0
129	VDD	-3080.0	-449.0
130	VDD	-3000.0	-449.0
131	VDD	-2920.0	-449.0
132	VDD	-2840.0	-449.0
133	VDD	-2760.0	-449.0
134	DPHYVCC	-2680.0	-449.0
135	DPHYVCC	-2600.0	-449.0
136	DPHYVCC	-2520.0	-449.0
137	DPHYVCC	-2440.0	-449.0
138	DSID0N	-2360.0	-449.0
139	DSID0N	-2280.0	-449.0
140	DSID0N	-2200.0	-449.0
141	DSID0NLVL	-2120.0	-449.0
142	DSID0PLVL	-2040.0	-449.0
143	DSID0P	-1960.0	-449.0
144	DSID0P	-1880.0	-449.0
145	DSID0P	-1800.0	-449.0
146	DPHYGNDDUM1	-1720.0	-449.0
147	DSICLKN	-1640.0	-449.0
148	DSICLKN	-1560.0	-449.0
149	DSICLKN	-1480.0	-449.0
150	DSICLKNLVL	-1400.0	-449.0

(Unit: um)

Pad No.	Pad Name	X	Y
151	DSICLKPLVL	-1320.0	-449.0
152	DSICLKP	-1240.0	-449.0
153	DSICLKP	-1160.0	-449.0
154	DSICLKP	-1080.0	-449.0
155	DPHYGNDDUM2	-1000.0	-449.0
156	DSID1N	-920.0	-449.0
157	DSID1N	-840.0	-449.0
158	DSID1N	-760.0	-449.0
159	DSID1NLVL	-680.0	-449.0
160	DSID1PLVL	-600.0	-449.0
161	DSID1P	-520.0	-449.0
162	DSID1P	-440.0	-449.0
163	DSID1P	-360.0	-449.0
164	DPHYGND	-280.0	-449.0
165	DPHYGND	-200.0	-449.0
166	DPHYGND	-120.0	-449.0
167	DPHYGND	-40.0	-449.0
168	GND	40.0	-449.0
169	GND	120.0	-449.0
170	GND	200.0	-449.0
171	GND	280.0	-449.0
172	GND	360.0	-449.0
173	GND	440.0	-449.0
174	VGS	520.0	-449.0
175	AGND	600.0	-449.0
176	AGND	680.0	-449.0
177	AGND	760.0	-449.0
178	AGND	840.0	-449.0
179	AGND	920.0	-449.0
180	AGND	1000.0	-449.0
181	AGND	1080.0	-449.0
182	AGND	1160.0	-449.0
183	VPP1	1240.0	-449.0
184	AGNDDUM	1320.0	-449.0
185	LEDPWM	1400.0	-449.0
186	TE	1480.0	-449.0
187	DB15	1560.0	-449.0
188	DB14	1640.0	-449.0
189	DB13	1720.0	-449.0
190	DB12	1800.0	-449.0
191	DB11	1880.0	-449.0
192	DB10	1960.0	-449.0
193	DB9	2040.0	-449.0
194	DB8	2120.0	-449.0
195	IOVCC	2200.0	-449.0
196	IOVCC	2280.0	-449.0
197	IOVCC	2360.0	-449.0
198	IOVCC	2440.0	-449.0
199	IOVCC	2520.0	-449.0
200	IOVCC	2600.0	-449.0

R61523 Pad Coordinates(No.3)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
201	DB7	2680.0	-449.0
202	DB6	2760.0	-449.0
203	DB5	2840.0	-449.0
204	DB4	2920.0	-449.0
205	DB3	3000.0	-449.0
206	DB2	3080.0	-449.0
207	DB1	3160.0	-449.0
208	DB0	3240.0	-449.0
209	CSX	3320.0	-449.0
210	DCX	3400.0	-449.0
211	WRX	3480.0	-449.0
212	RDX	3560.0	-449.0
213	RESX	3640.0	-449.0
214	GND	3720.0	-449.0
215	GND	3800.0	-449.0
216	GND	3880.0	-449.0
217	GND	3960.0	-449.0
218	GND	4040.0	-449.0
219	GND	4120.0	-449.0
220	IM0	4200.0	-449.0
221	IM1	4280.0	-449.0
222	IM2	4360.0	-449.0
223	VMON	4440.0	-449.0
224	VMON	4520.0	-449.0
225	VREG1	4600.0	-449.0
226	VREG1	4680.0	-449.0
227	VCOMH	4760.0	-449.0
228	VCOMH	4840.0	-449.0
229	VCOML	4920.0	-449.0
230	VCOML	5000.0	-449.0
231	VCL	5080.0	-449.0
232	VCL	5160.0	-449.0
233	VCL	5240.0	-449.0
234	VCL	5320.0	-449.0
235	C13M	5400.0	-449.0
236	C13M	5480.0	-449.0
237	C13M	5560.0	-449.0
238	C13M	5640.0	-449.0
239	C13P	5720.0	-449.0
240	C13P	5800.0	-449.0
241	C13P	5880.0	-449.0
242	C13P	5960.0	-449.0
243	AGND	6040.0	-449.0
244	AGND	6120.0	-449.0
245	AGND	6200.0	-449.0
246	AGND	6280.0	-449.0
247	AGND	6360.0	-449.0
248	VGH	6440.0	-449.0
249	VGH	6520.0	-449.0
250	VGH	6600.0	-449.0

(Unit: um)

Pad No.	Pad Name	X	Y
251	VGH	6680.0	-449.0
252	VGH	6760.0	-449.0
253	VGH	6840.0	-449.0
254	C21P	6920.0	-449.0
255	C21P	7000.0	-449.0
256	C21P	7080.0	-449.0
257	C21P	7160.0	-449.0
258	C21P	7240.0	-449.0
259	C21P	7320.0	-449.0
260	C21P	7400.0	-449.0
261	C21M	7480.0	-449.0
262	C21M	7560.0	-449.0
263	C21M	7640.0	-449.0
264	C21M	7720.0	-449.0
265	C21M	7800.0	-449.0
266	C21M	7880.0	-449.0
267	C21M	7960.0	-449.0
268	C22P	8040.0	-449.0
269	C22P	8120.0	-449.0
270	C22P	8200.0	-449.0
271	C22P	8280.0	-449.0
272	C22P	8360.0	-449.0
273	C22P	8440.0	-449.0
274	C22P	8520.0	-449.0
275	C22M	8600.0	-449.0
276	C22M	8680.0	-449.0
277	C22M	8760.0	-449.0
278	C22M	8840.0	-449.0
279	C22M	8920.0	-449.0
280	C22M	9000.0	-449.0
281	C22M	9080.0	-449.0
282	C23P	9160.0	-449.0
283	C23P	9240.0	-449.0
284	C23P	9320.0	-449.0
285	C23P	9400.0	-449.0
286	C23P	9480.0	-449.0
287	C23P	9560.0	-449.0
288	C23P	9640.0	-449.0
289	C23M	9720.0	-449.0
290	C23M	9800.0	-449.0
291	C23M	9880.0	-449.0
292	C23M	9960.0	-449.0
293	C23M	10040.0	-449.0
294	C23M	10120.0	-449.0
295	C23M	10200.0	-449.0
296	C31P	10280.0	-449.0
297	C31P	10360.0	-449.0
298	C31P	10440.0	-449.0
299	C31P	10520.0	-449.0
300	C31P	10600.0	-449.0

R61523 Pad Coordinates(No.4)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
301	C31P	10680.0	-449.0
302	C31P	10760.0	-449.0
303	C31M	10840.0	-449.0
304	C31M	10920.0	-449.0
305	C31M	11000.0	-449.0
306	C31M	11080.0	-449.0
307	C31M	11160.0	-449.0
308	C31M	11240.0	-449.0
309	C31M	11320.0	-449.0
310	VGL	11400.0	-449.0
311	VGL	11480.0	-449.0
312	VGL	11560.0	-449.0
313	VGL	11640.0	-449.0
314	VGL	11720.0	-449.0
315	VGL	11800.0	-449.0
316	GND	11880.0	-449.0
317	GND	11960.0	-449.0
318	GND	12040.0	-449.0
319	GND	12120.0	-449.0
320	GND	12200.0	-449.0
321	GND	12280.0	-449.0
322	AGND	12360.0	-449.0
323	AGND	12440.0	-449.0
324	AGND	12520.0	-449.0
325	AGND	12600.0	-449.0
326	AGND	12680.0	-449.0
327	AGND	12760.0	-449.0
328	VCOM	12840.0	-449.0
329	VCOM	12920.0	-449.0
330	VCOM	13000.0	-449.0
331	VCOM	13080.0	-449.0
332	DUMMYR3	13160.0	-449.0
333	DUMMYR4	13240.0	-449.0
334	DUMMY2	13320.0	-449.0
335	TESTO1	13515.0	436.0
336	TESTO2	13500.0	326.0
337	G2	13485.0	436.0
338	G4	13470.0	326.0
339	G6	13455.0	436.0
340	G8	13440.0	326.0
341	G10	13425.0	436.0
342	G12	13410.0	326.0
343	G14	13395.0	436.0
344	G16	13380.0	326.0
345	G18	13365.0	436.0
346	G20	13350.0	326.0
347	G22	13335.0	436.0
348	G24	13320.0	326.0
349	G26	13305.0	436.0
350	G28	13290.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
351	G30	13275.0	436.0
352	G32	13260.0	326.0
353	G34	13245.0	436.0
354	G36	13230.0	326.0
355	G38	13215.0	436.0
356	G40	13200.0	326.0
357	G42	13185.0	436.0
358	G44	13170.0	326.0
359	G46	13155.0	436.0
360	G48	13140.0	326.0
361	G50	13125.0	436.0
362	G52	13110.0	326.0
363	G54	13095.0	436.0
364	G56	13080.0	326.0
365	G58	13065.0	436.0
366	G60	13050.0	326.0
367	G62	13035.0	436.0
368	G64	13020.0	326.0
369	G66	13005.0	436.0
370	G68	12990.0	326.0
371	G70	12975.0	436.0
372	G72	12960.0	326.0
373	G74	12945.0	436.0
374	G76	12930.0	326.0
375	G78	12915.0	436.0
376	G80	12900.0	326.0
377	G82	12885.0	436.0
378	G84	12870.0	326.0
379	G86	12855.0	436.0
380	G88	12840.0	326.0
381	G90	12825.0	436.0
382	G92	12810.0	326.0
383	G94	12795.0	436.0
384	G96	12780.0	326.0
385	G98	12765.0	436.0
386	G100	12750.0	326.0
387	G102	12735.0	436.0
388	G104	12720.0	326.0
389	G106	12705.0	436.0
390	G108	12690.0	326.0
391	G110	12675.0	436.0
392	G112	12660.0	326.0
393	G114	12645.0	436.0
394	G116	12630.0	326.0
395	G118	12615.0	436.0
396	G120	12600.0	326.0
397	G122	12585.0	436.0
398	G124	12570.0	326.0
399	G126	12555.0	436.0
400	G128	12540.0	326.0

R61523 Pad Coordinates(No.5)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
401	G130	12525.0	436.0
402	G132	12510.0	326.0
403	G134	12495.0	436.0
404	G136	12480.0	326.0
405	G138	12465.0	436.0
406	G140	12450.0	326.0
407	G142	12435.0	436.0
408	G144	12420.0	326.0
409	G146	12405.0	436.0
410	G148	12390.0	326.0
411	G150	12375.0	436.0
412	G152	12360.0	326.0
413	G154	12345.0	436.0
414	G156	12330.0	326.0
415	G158	12315.0	436.0
416	G160	12300.0	326.0
417	G162	12285.0	436.0
418	G164	12270.0	326.0
419	G166	12255.0	436.0
420	G168	12240.0	326.0
421	G170	12225.0	436.0
422	G172	12210.0	326.0
423	G174	12195.0	436.0
424	G176	12180.0	326.0
425	G178	12165.0	436.0
426	G180	12150.0	326.0
427	G182	12135.0	436.0
428	G184	12120.0	326.0
429	G186	12105.0	436.0
430	G188	12090.0	326.0
431	G190	12075.0	436.0
432	G192	12060.0	326.0
433	G194	12045.0	436.0
434	G196	12030.0	326.0
435	G198	12015.0	436.0
436	G200	12000.0	326.0
437	G202	11985.0	436.0
438	G204	11970.0	326.0
439	G206	11955.0	436.0
440	G208	11940.0	326.0
441	G210	11925.0	436.0
442	G212	11910.0	326.0
443	G214	11895.0	436.0
444	G216	11880.0	326.0
445	G218	11865.0	436.0
446	G220	11850.0	326.0
447	G222	11835.0	436.0
448	G224	11820.0	326.0
449	G226	11805.0	436.0
450	G228	11790.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
451	G230	11775.0	436.0
452	G232	11760.0	326.0
453	G234	11745.0	436.0
454	G236	11730.0	326.0
455	G238	11715.0	436.0
456	G240	11700.0	326.0
457	G242	11685.0	436.0
458	G244	11670.0	326.0
459	G246	11655.0	436.0
460	G248	11640.0	326.0
461	G250	11625.0	436.0
462	G252	11610.0	326.0
463	G254	11595.0	436.0
464	G256	11580.0	326.0
465	G258	11565.0	436.0
466	G260	11550.0	326.0
467	G262	11535.0	436.0
468	G264	11520.0	326.0
469	G266	11505.0	436.0
470	G268	11490.0	326.0
471	G270	11475.0	436.0
472	G272	11460.0	326.0
473	G274	11445.0	436.0
474	G276	11430.0	326.0
475	G278	11415.0	436.0
476	G280	11400.0	326.0
477	G282	11385.0	436.0
478	G284	11370.0	326.0
479	G286	11355.0	436.0
480	G288	11340.0	326.0
481	G290	11325.0	436.0
482	G292	11310.0	326.0
483	G294	11295.0	436.0
484	G296	11280.0	326.0
485	G298	11265.0	436.0
486	G300	11250.0	326.0
487	G302	11235.0	436.0
488	G304	11220.0	326.0
489	G306	11205.0	436.0
490	G308	11190.0	326.0
491	G310	11175.0	436.0
492	G312	11160.0	326.0
493	G314	11145.0	436.0
494	G316	11130.0	326.0
495	G318	11115.0	436.0
496	G320	11100.0	326.0
497	G322	11085.0	436.0
498	G324	11070.0	326.0
499	G326	11055.0	436.0
500	G328	11040.0	326.0

R61523 Pad Coordinates(No.6)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
501	G330	11025.0	436.0
502	G332	11010.0	326.0
503	G334	10995.0	436.0
504	G336	10980.0	326.0
505	G338	10965.0	436.0
506	G340	10950.0	326.0
507	G342	10935.0	436.0
508	G344	10920.0	326.0
509	G346	10905.0	436.0
510	G348	10890.0	326.0
511	G350	10875.0	436.0
512	G352	10860.0	326.0
513	G354	10845.0	436.0
514	G356	10830.0	326.0
515	G358	10815.0	436.0
516	G360	10800.0	326.0
517	G362	10785.0	436.0
518	G364	10770.0	326.0
519	G366	10755.0	436.0
520	G368	10740.0	326.0
521	G370	10725.0	436.0
522	G372	10710.0	326.0
523	G374	10695.0	436.0
524	G376	10680.0	326.0
525	G378	10665.0	436.0
526	G380	10650.0	326.0
527	G382	10635.0	436.0
528	G384	10620.0	326.0
529	G386	10605.0	436.0
530	G388	10590.0	326.0
531	G390	10575.0	436.0
532	G392	10560.0	326.0
533	G394	10545.0	436.0
534	G396	10530.0	326.0
535	G398	10515.0	436.0
536	G400	10500.0	326.0
537	G402	10485.0	436.0
538	G404	10470.0	326.0
539	G406	10455.0	436.0
540	G408	10440.0	326.0
541	G410	10425.0	436.0
542	G412	10410.0	326.0
543	G414	10395.0	436.0
544	G416	10380.0	326.0
545	G418	10365.0	436.0
546	G420	10350.0	326.0
547	G422	10335.0	436.0
548	G424	10320.0	326.0
549	G426	10305.0	436.0
550	G428	10290.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
551	G430	10275.0	436.0
552	G432	10260.0	326.0
553	G434	10245.0	436.0
554	G436	10230.0	326.0
555	G438	10215.0	436.0
556	G440	10200.0	326.0
557	G442	10185.0	436.0
558	G444	10170.0	326.0
559	G446	10155.0	436.0
560	G448	10140.0	326.0
561	G450	10125.0	436.0
562	G452	10110.0	326.0
563	G454	10095.0	436.0
564	G456	10080.0	326.0
565	G458	10065.0	436.0
566	G460	10050.0	326.0
567	G462	10035.0	436.0
568	G464	10020.0	326.0
569	G466	10005.0	436.0
570	G468	9990.0	326.0
571	G470	9975.0	436.0
572	G472	9960.0	326.0
573	G474	9945.0	436.0
574	G476	9930.0	326.0
575	G478	9915.0	436.0
576	G480	9900.0	326.0
577	G482	9885.0	436.0
578	G484	9870.0	326.0
579	G486	9855.0	436.0
580	G488	9840.0	326.0
581	G490	9825.0	436.0
582	G492	9810.0	326.0
583	G494	9795.0	436.0
584	G496	9780.0	326.0
585	G498	9765.0	436.0
586	G500	9750.0	326.0
587	G502	9735.0	436.0
588	G504	9720.0	326.0
589	G506	9705.0	436.0
590	G508	9690.0	326.0
591	G510	9675.0	436.0
592	G512	9660.0	326.0
593	G514	9645.0	436.0
594	G516	9630.0	326.0
595	G518	9615.0	436.0
596	G520	9600.0	326.0
597	G522	9585.0	436.0
598	G524	9570.0	326.0
599	G526	9555.0	436.0
600	G528	9540.0	326.0

R61523 Pad Coordinates(No.7)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
601	G530	9525.0	436.0
602	G532	9510.0	326.0
603	G534	9495.0	436.0
604	G536	9480.0	326.0
605	G538	9465.0	436.0
606	G540	9450.0	326.0
607	G542	9435.0	436.0
608	G544	9420.0	326.0
609	G546	9405.0	436.0
610	G548	9390.0	326.0
611	G550	9375.0	436.0
612	G552	9360.0	326.0
613	G554	9345.0	436.0
614	G556	9330.0	326.0
615	G558	9315.0	436.0
616	G560	9300.0	326.0
617	G562	9285.0	436.0
618	G564	9270.0	326.0
619	G566	9255.0	436.0
620	G568	9240.0	326.0
621	G570	9225.0	436.0
622	G572	9210.0	326.0
623	G574	9195.0	436.0
624	G576	9180.0	326.0
625	G578	9165.0	436.0
626	G580	9150.0	326.0
627	G582	9135.0	436.0
628	G584	9120.0	326.0
629	G586	9105.0	436.0
630	G588	9090.0	326.0
631	G590	9075.0	436.0
632	G592	9060.0	326.0
633	G594	9045.0	436.0
634	G596	9030.0	326.0
635	G598	9015.0	436.0
636	G600	9000.0	326.0
637	G602	8985.0	436.0
638	G604	8970.0	326.0
639	G606	8955.0	436.0
640	G608	8940.0	326.0
641	G610	8925.0	436.0
642	G612	8910.0	326.0
643	G614	8895.0	436.0
644	G616	8880.0	326.0
645	G618	8865.0	436.0
646	G620	8850.0	326.0
647	G622	8835.0	436.0
648	G624	8820.0	326.0
649	G626	8805.0	436.0
650	G628	8790.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
651	G630	8775.0	436.0
652	G632	8760.0	326.0
653	G634	8745.0	436.0
654	G636	8730.0	326.0
655	G638	8715.0	436.0
656	G640	8700.0	326.0
657	TESTO3	8685.0	436.0
658	TESTO4	8445.0	436.0
659	S1080	8430.0	326.0
660	S1079	8415.0	436.0
661	S1078	8400.0	326.0
662	S1077	8385.0	436.0
663	S1076	8370.0	326.0
664	S1075	8355.0	436.0
665	S1074	8340.0	326.0
666	S1073	8325.0	436.0
667	S1072	8310.0	326.0
668	S1071	8295.0	436.0
669	S1070	8280.0	326.0
670	S1069	8265.0	436.0
671	S1068	8250.0	326.0
672	S1067	8235.0	436.0
673	S1066	8220.0	326.0
674	S1065	8205.0	436.0
675	S1064	8190.0	326.0
676	S1063	8175.0	436.0
677	S1062	8160.0	326.0
678	S1061	8145.0	436.0
679	S1060	8130.0	326.0
680	S1059	8115.0	436.0
681	S1058	8100.0	326.0
682	S1057	8085.0	436.0
683	S1056	8070.0	326.0
684	S1055	8055.0	436.0
685	S1054	8040.0	326.0
686	S1053	8025.0	436.0
687	S1052	8010.0	326.0
688	S1051	7995.0	436.0
689	S1050	7980.0	326.0
690	S1049	7965.0	436.0
691	S1048	7950.0	326.0
692	S1047	7935.0	436.0
693	S1046	7920.0	326.0
694	S1045	7905.0	436.0
695	S1044	7890.0	326.0
696	S1043	7875.0	436.0
697	S1042	7860.0	326.0
698	S1041	7845.0	436.0
699	S1040	7830.0	326.0
700	S1039	7815.0	436.0

R61523 Pad Coordinates(No.8)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
701	S1038	7800.0	326.0
702	S1037	7785.0	436.0
703	S1036	7770.0	326.0
704	S1035	7755.0	436.0
705	S1034	7740.0	326.0
706	S1033	7725.0	436.0
707	S1032	7710.0	326.0
708	S1031	7695.0	436.0
709	S1030	7680.0	326.0
710	S1029	7665.0	436.0
711	S1028	7650.0	326.0
712	S1027	7635.0	436.0
713	S1026	7620.0	326.0
714	S1025	7605.0	436.0
715	S1024	7590.0	326.0
716	S1023	7575.0	436.0
717	S1022	7560.0	326.0
718	S1021	7545.0	436.0
719	S1020	7530.0	326.0
720	S1019	7515.0	436.0
721	S1018	7500.0	326.0
722	S1017	7485.0	436.0
723	S1016	7470.0	326.0
724	S1015	7455.0	436.0
725	S1014	7440.0	326.0
726	S1013	7425.0	436.0
727	S1012	7410.0	326.0
728	S1011	7395.0	436.0
729	S1010	7380.0	326.0
730	S1009	7365.0	436.0
731	S1008	7350.0	326.0
732	S1007	7335.0	436.0
733	S1006	7320.0	326.0
734	S1005	7305.0	436.0
735	S1004	7290.0	326.0
736	S1003	7275.0	436.0
737	S1002	7260.0	326.0
738	S1001	7245.0	436.0
739	S1000	7230.0	326.0
740	S999	7215.0	436.0
741	S998	7200.0	326.0
742	S997	7185.0	436.0
743	S996	7170.0	326.0
744	S995	7155.0	436.0
745	S994	7140.0	326.0
746	S993	7125.0	436.0
747	S992	7110.0	326.0
748	S991	7095.0	436.0
749	S990	7080.0	326.0
750	S989	7065.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
751	S988	7050.0	326.0
752	S987	7035.0	436.0
753	S986	7020.0	326.0
754	S985	7005.0	436.0
755	S984	6990.0	326.0
756	S983	6975.0	436.0
757	S982	6960.0	326.0
758	S981	6945.0	436.0
759	S980	6930.0	326.0
760	S979	6915.0	436.0
761	S978	6900.0	326.0
762	S977	6885.0	436.0
763	S976	6870.0	326.0
764	S975	6855.0	436.0
765	S974	6840.0	326.0
766	S973	6825.0	436.0
767	S972	6810.0	326.0
768	S971	6795.0	436.0
769	S970	6780.0	326.0
770	S969	6765.0	436.0
771	S968	6750.0	326.0
772	S967	6735.0	436.0
773	S966	6720.0	326.0
774	S965	6705.0	436.0
775	S964	6690.0	326.0
776	S963	6675.0	436.0
777	S962	6660.0	326.0
778	S961	6645.0	436.0
779	S960	6630.0	326.0
780	S959	6615.0	436.0
781	S958	6600.0	326.0
782	S957	6585.0	436.0
783	S956	6570.0	326.0
784	S955	6555.0	436.0
785	S954	6540.0	326.0
786	S953	6525.0	436.0
787	S952	6510.0	326.0
788	S951	6495.0	436.0
789	S950	6480.0	326.0
790	S949	6465.0	436.0
791	S948	6450.0	326.0
792	S947	6435.0	436.0
793	S946	6420.0	326.0
794	S945	6405.0	436.0
795	S944	6390.0	326.0
796	S943	6375.0	436.0
797	S942	6360.0	326.0
798	S941	6345.0	436.0
799	S940	6330.0	326.0
800	S939	6315.0	436.0

R61523 Pad Coordinates(No.9)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
801	S938	6300.0	326.0
802	S937	6285.0	436.0
803	S936	6270.0	326.0
804	S935	6255.0	436.0
805	S934	6240.0	326.0
806	S933	6225.0	436.0
807	S932	6210.0	326.0
808	S931	6195.0	436.0
809	S930	6180.0	326.0
810	S929	6165.0	436.0
811	S928	6150.0	326.0
812	S927	6135.0	436.0
813	S926	6120.0	326.0
814	S925	6105.0	436.0
815	S924	6090.0	326.0
816	S923	6075.0	436.0
817	S922	6060.0	326.0
818	S921	6045.0	436.0
819	S920	6030.0	326.0
820	S919	6015.0	436.0
821	S918	6000.0	326.0
822	S917	5985.0	436.0
823	S916	5970.0	326.0
824	S915	5955.0	436.0
825	S914	5940.0	326.0
826	S913	5925.0	436.0
827	S912	5910.0	326.0
828	S911	5895.0	436.0
829	S910	5880.0	326.0
830	S909	5865.0	436.0
831	S908	5850.0	326.0
832	S907	5835.0	436.0
833	S906	5820.0	326.0
834	S905	5805.0	436.0
835	S904	5790.0	326.0
836	S903	5775.0	436.0
837	S902	5760.0	326.0
838	S901	5745.0	436.0
839	S900	5730.0	326.0
840	S899	5715.0	436.0
841	S898	5700.0	326.0
842	S897	5685.0	436.0
843	S896	5670.0	326.0
844	S895	5655.0	436.0
845	S894	5640.0	326.0
846	S893	5625.0	436.0
847	S892	5610.0	326.0
848	S891	5595.0	436.0
849	S890	5580.0	326.0
850	S889	5565.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
851	S888	5550.0	326.0
852	S887	5535.0	436.0
853	S886	5520.0	326.0
854	S885	5505.0	436.0
855	S884	5490.0	326.0
856	S883	5475.0	436.0
857	S882	5460.0	326.0
858	S881	5445.0	436.0
859	S880	5430.0	326.0
860	S879	5415.0	436.0
861	S878	5400.0	326.0
862	S877	5385.0	436.0
863	S876	5370.0	326.0
864	S875	5355.0	436.0
865	S874	5340.0	326.0
866	S873	5325.0	436.0
867	S872	5310.0	326.0
868	S871	5295.0	436.0
869	S870	5280.0	326.0
870	S869	5265.0	436.0
871	S868	5250.0	326.0
872	S867	5235.0	436.0
873	S866	5220.0	326.0
874	S865	5205.0	436.0
875	S864	5190.0	326.0
876	S863	5175.0	436.0
877	S862	5160.0	326.0
878	S861	5145.0	436.0
879	S860	5130.0	326.0
880	S859	5115.0	436.0
881	S858	5100.0	326.0
882	S857	5085.0	436.0
883	S856	5070.0	326.0
884	S855	5055.0	436.0
885	S854	5040.0	326.0
886	S853	5025.0	436.0
887	S852	5010.0	326.0
888	S851	4995.0	436.0
889	S850	4980.0	326.0
890	S849	4965.0	436.0
891	S848	4950.0	326.0
892	S847	4935.0	436.0
893	S846	4920.0	326.0
894	S845	4905.0	436.0
895	S844	4890.0	326.0
896	S843	4875.0	436.0
897	S842	4860.0	326.0
898	S841	4845.0	436.0
899	S840	4830.0	326.0
900	S839	4815.0	436.0

R61523 Pad Coordinates(No.10)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
901	S838	4800.0	326.0
902	S837	4785.0	436.0
903	S836	4770.0	326.0
904	S835	4755.0	436.0
905	S834	4740.0	326.0
906	S833	4725.0	436.0
907	S832	4710.0	326.0
908	S831	4695.0	436.0
909	S830	4680.0	326.0
910	S829	4665.0	436.0
911	S828	4650.0	326.0
912	S827	4635.0	436.0
913	S826	4620.0	326.0
914	S825	4605.0	436.0
915	S824	4590.0	326.0
916	S823	4575.0	436.0
917	S822	4560.0	326.0
918	S821	4545.0	436.0
919	S820	4530.0	326.0
920	S819	4515.0	436.0
921	S818	4500.0	326.0
922	S817	4485.0	436.0
923	S816	4470.0	326.0
924	S815	4455.0	436.0
925	S814	4440.0	326.0
926	S813	4425.0	436.0
927	S812	4410.0	326.0
928	S811	4395.0	436.0
929	S810	4380.0	326.0
930	S809	4365.0	436.0
931	S808	4350.0	326.0
932	S807	4335.0	436.0
933	S806	4320.0	326.0
934	S805	4305.0	436.0
935	S804	4290.0	326.0
936	S803	4275.0	436.0
937	S802	4260.0	326.0
938	S801	4245.0	436.0
939	S800	4230.0	326.0
940	S799	4215.0	436.0
941	S798	4200.0	326.0
942	S797	4185.0	436.0
943	S796	4170.0	326.0
944	S795	4155.0	436.0
945	S794	4140.0	326.0
946	S793	4125.0	436.0
947	S792	4110.0	326.0
948	S791	4095.0	436.0
949	S790	4080.0	326.0
950	S789	4065.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
951	S788	4050.0	326.0
952	S787	4035.0	436.0
953	S786	4020.0	326.0
954	S785	4005.0	436.0
955	S784	3990.0	326.0
956	S783	3975.0	436.0
957	S782	3960.0	326.0
958	S781	3945.0	436.0
959	S780	3930.0	326.0
960	S779	3915.0	436.0
961	S778	3900.0	326.0
962	S777	3885.0	436.0
963	S776	3870.0	326.0
964	S775	3855.0	436.0
965	S774	3840.0	326.0
966	S773	3825.0	436.0
967	S772	3810.0	326.0
968	S771	3795.0	436.0
969	S770	3780.0	326.0
970	S769	3765.0	436.0
971	S768	3750.0	326.0
972	S767	3735.0	436.0
973	S766	3720.0	326.0
974	S765	3705.0	436.0
975	S764	3690.0	326.0
976	S763	3675.0	436.0
977	S762	3660.0	326.0
978	S761	3645.0	436.0
979	S760	3630.0	326.0
980	S759	3615.0	436.0
981	S758	3600.0	326.0
982	S757	3585.0	436.0
983	S756	3570.0	326.0
984	S755	3555.0	436.0
985	S754	3540.0	326.0
986	S753	3525.0	436.0
987	S752	3510.0	326.0
988	S751	3495.0	436.0
989	S750	3480.0	326.0
990	S749	3465.0	436.0
991	S748	3450.0	326.0
992	S747	3435.0	436.0
993	S746	3420.0	326.0
994	S745	3405.0	436.0
995	S744	3390.0	326.0
996	S743	3375.0	436.0
997	S742	3360.0	326.0
998	S741	3345.0	436.0
999	S740	3330.0	326.0
1000	S739	3315.0	436.0

R61523 Pad Coordinates(No.11)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1001	S738	3300.0	326.0
1002	S737	3285.0	436.0
1003	S736	3270.0	326.0
1004	S735	3255.0	436.0
1005	S734	3240.0	326.0
1006	S733	3225.0	436.0
1007	S732	3210.0	326.0
1008	S731	3195.0	436.0
1009	S730	3180.0	326.0
1010	S729	3165.0	436.0
1011	S728	3150.0	326.0
1012	S727	3135.0	436.0
1013	S726	3120.0	326.0
1014	S725	3105.0	436.0
1015	S724	3090.0	326.0
1016	S723	3075.0	436.0
1017	S722	3060.0	326.0
1018	S721	3045.0	436.0
1019	S720	3030.0	326.0
1020	S719	3015.0	436.0
1021	S718	3000.0	326.0
1022	S717	2985.0	436.0
1023	S716	2970.0	326.0
1024	S715	2955.0	436.0
1025	S714	2940.0	326.0
1026	S713	2925.0	436.0
1027	S712	2910.0	326.0
1028	S711	2895.0	436.0
1029	S710	2880.0	326.0
1030	S709	2865.0	436.0
1031	S708	2850.0	326.0
1032	S707	2835.0	436.0
1033	S706	2820.0	326.0
1034	S705	2805.0	436.0
1035	S704	2790.0	326.0
1036	S703	2775.0	436.0
1037	S702	2760.0	326.0
1038	S701	2745.0	436.0
1039	S700	2730.0	326.0
1040	S699	2715.0	436.0
1041	S698	2700.0	326.0
1042	S697	2685.0	436.0
1043	S696	2670.0	326.0
1044	S695	2655.0	436.0
1045	S694	2640.0	326.0
1046	S693	2625.0	436.0
1047	S692	2610.0	326.0
1048	S691	2595.0	436.0
1049	S690	2580.0	326.0
1050	S689	2565.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
1051	S688	2550.0	326.0
1052	S687	2535.0	436.0
1053	S686	2520.0	326.0
1054	S685	2505.0	436.0
1055	S684	2490.0	326.0
1056	S683	2475.0	436.0
1057	S682	2460.0	326.0
1058	S681	2445.0	436.0
1059	S680	2430.0	326.0
1060	S679	2415.0	436.0
1061	S678	2400.0	326.0
1062	S677	2385.0	436.0
1063	S676	2370.0	326.0
1064	S675	2355.0	436.0
1065	S674	2340.0	326.0
1066	S673	2325.0	436.0
1067	S672	2310.0	326.0
1068	S671	2295.0	436.0
1069	S670	2280.0	326.0
1070	S669	2265.0	436.0
1071	S668	2250.0	326.0
1072	S667	2235.0	436.0
1073	S666	2220.0	326.0
1074	S665	2205.0	436.0
1075	S664	2190.0	326.0
1076	S663	2175.0	436.0
1077	S662	2160.0	326.0
1078	S661	2145.0	436.0
1079	S660	2130.0	326.0
1080	S659	2115.0	436.0
1081	S658	2100.0	326.0
1082	S657	2085.0	436.0
1083	S656	2070.0	326.0
1084	S655	2055.0	436.0
1085	S654	2040.0	326.0
1086	S653	2025.0	436.0
1087	S652	2010.0	326.0
1088	S651	1995.0	436.0
1089	S650	1980.0	326.0
1090	S649	1965.0	436.0
1091	S648	1950.0	326.0
1092	S647	1935.0	436.0
1093	S646	1920.0	326.0
1094	S645	1905.0	436.0
1095	S644	1890.0	326.0
1096	S643	1875.0	436.0
1097	S642	1860.0	326.0
1098	S641	1845.0	436.0
1099	S640	1830.0	326.0
1100	S639	1815.0	436.0

R61523 Pad Coordinates(No.12)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1101	S638	1800.0	326.0
1102	S637	1785.0	436.0
1103	S636	1770.0	326.0
1104	S635	1755.0	436.0
1105	S634	1740.0	326.0
1106	S633	1725.0	436.0
1107	S632	1710.0	326.0
1108	S631	1695.0	436.0
1109	S630	1680.0	326.0
1110	S629	1665.0	436.0
1111	S628	1650.0	326.0
1112	S627	1635.0	436.0
1113	S626	1620.0	326.0
1114	S625	1605.0	436.0
1115	S624	1590.0	326.0
1116	S623	1575.0	436.0
1117	S622	1560.0	326.0
1118	S621	1545.0	436.0
1119	S620	1530.0	326.0
1120	S619	1515.0	436.0
1121	S618	1500.0	326.0
1122	S617	1485.0	436.0
1123	S616	1470.0	326.0
1124	S615	1455.0	436.0
1125	S614	1440.0	326.0
1126	S613	1425.0	436.0
1127	S612	1410.0	326.0
1128	S611	1395.0	436.0
1129	S610	1380.0	326.0
1130	S609	1365.0	436.0
1131	S608	1350.0	326.0
1132	S607	1335.0	436.0
1133	S606	1320.0	326.0
1134	S605	1305.0	436.0
1135	S604	1290.0	326.0
1136	S603	1275.0	436.0
1137	S602	1260.0	326.0
1138	S601	1245.0	436.0
1139	S600	1230.0	326.0
1140	S599	1215.0	436.0
1141	S598	1200.0	326.0
1142	S597	1185.0	436.0
1143	S596	1170.0	326.0
1144	S595	1155.0	436.0
1145	S594	1140.0	326.0
1146	S593	1125.0	436.0
1147	S592	1110.0	326.0
1148	S591	1095.0	436.0
1149	S590	1080.0	326.0
1150	S589	1065.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
1151	S588	1050.0	326.0
1152	S587	1035.0	436.0
1153	S586	1020.0	326.0
1154	S585	1005.0	436.0
1155	S584	990.0	326.0
1156	S583	975.0	436.0
1157	S582	960.0	326.0
1158	S581	945.0	436.0
1159	S580	930.0	326.0
1160	S579	915.0	436.0
1161	S578	900.0	326.0
1162	S577	885.0	436.0
1163	S576	870.0	326.0
1164	S575	855.0	436.0
1165	S574	840.0	326.0
1166	S573	825.0	436.0
1167	S572	810.0	326.0
1168	S571	795.0	436.0
1169	S570	780.0	326.0
1170	S569	765.0	436.0
1171	S568	750.0	326.0
1172	S567	735.0	436.0
1173	S566	720.0	326.0
1174	S565	705.0	436.0
1175	S564	690.0	326.0
1176	S563	675.0	436.0
1177	S562	660.0	326.0
1178	S561	645.0	436.0
1179	S560	630.0	326.0
1180	S559	615.0	436.0
1181	S558	600.0	326.0
1182	S557	585.0	436.0
1183	S556	570.0	326.0
1184	S555	555.0	436.0
1185	S554	540.0	326.0
1186	S553	525.0	436.0
1187	S552	510.0	326.0
1188	S551	495.0	436.0
1189	S550	480.0	326.0
1190	S549	465.0	436.0
1191	S548	450.0	326.0
1192	S547	435.0	436.0
1193	S546	420.0	326.0
1194	S545	405.0	436.0
1195	S544	390.0	326.0
1196	S543	375.0	436.0
1197	S542	360.0	326.0
1198	S541	345.0	436.0
1199	TESTO5	330.0	326.0
1200	TESTO6	-330.0	326.0

R61523 Pad Coordinates(No.13)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1201	S540	-345.0	436.0
1202	S539	-360.0	326.0
1203	S538	-375.0	436.0
1204	S537	-390.0	326.0
1205	S536	-405.0	436.0
1206	S535	-420.0	326.0
1207	S534	-435.0	436.0
1208	S533	-450.0	326.0
1209	S532	-465.0	436.0
1210	S531	-480.0	326.0
1211	S530	-495.0	436.0
1212	S529	-510.0	326.0
1213	S528	-525.0	436.0
1214	S527	-540.0	326.0
1215	S526	-555.0	436.0
1216	S525	-570.0	326.0
1217	S524	-585.0	436.0
1218	S523	-600.0	326.0
1219	S522	-615.0	436.0
1220	S521	-630.0	326.0
1221	S520	-645.0	436.0
1222	S519	-660.0	326.0
1223	S518	-675.0	436.0
1224	S517	-690.0	326.0
1225	S516	-705.0	436.0
1226	S515	-720.0	326.0
1227	S514	-735.0	436.0
1228	S513	-750.0	326.0
1229	S512	-765.0	436.0
1230	S511	-780.0	326.0
1231	S510	-795.0	436.0
1232	S509	-810.0	326.0
1233	S508	-825.0	436.0
1234	S507	-840.0	326.0
1235	S506	-855.0	436.0
1236	S505	-870.0	326.0
1237	S504	-885.0	436.0
1238	S503	-900.0	326.0
1239	S502	-915.0	436.0
1240	S501	-930.0	326.0
1241	S500	-945.0	436.0
1242	S499	-960.0	326.0
1243	S498	-975.0	436.0
1244	S497	-990.0	326.0
1245	S496	-1005.0	436.0
1246	S495	-1020.0	326.0
1247	S494	-1035.0	436.0
1248	S493	-1050.0	326.0
1249	S492	-1065.0	436.0
1250	S491	-1080.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
1251	S490	-1095.0	436.0
1252	S489	-1110.0	326.0
1253	S488	-1125.0	436.0
1254	S487	-1140.0	326.0
1255	S486	-1155.0	436.0
1256	S485	-1170.0	326.0
1257	S484	-1185.0	436.0
1258	S483	-1200.0	326.0
1259	S482	-1215.0	436.0
1260	S481	-1230.0	326.0
1261	S480	-1245.0	436.0
1262	S479	-1260.0	326.0
1263	S478	-1275.0	436.0
1264	S477	-1290.0	326.0
1265	S476	-1305.0	436.0
1266	S475	-1320.0	326.0
1267	S474	-1335.0	436.0
1268	S473	-1350.0	326.0
1269	S472	-1365.0	436.0
1270	S471	-1380.0	326.0
1271	S470	-1395.0	436.0
1272	S469	-1410.0	326.0
1273	S468	-1425.0	436.0
1274	S467	-1440.0	326.0
1275	S466	-1455.0	436.0
1276	S465	-1470.0	326.0
1277	S464	-1485.0	436.0
1278	S463	-1500.0	326.0
1279	S462	-1515.0	436.0
1280	S461	-1530.0	326.0
1281	S460	-1545.0	436.0
1282	S459	-1560.0	326.0
1283	S458	-1575.0	436.0
1284	S457	-1590.0	326.0
1285	S456	-1605.0	436.0
1286	S455	-1620.0	326.0
1287	S454	-1635.0	436.0
1288	S453	-1650.0	326.0
1289	S452	-1665.0	436.0
1290	S451	-1680.0	326.0
1291	S450	-1695.0	436.0
1292	S449	-1710.0	326.0
1293	S448	-1725.0	436.0
1294	S447	-1740.0	326.0
1295	S446	-1755.0	436.0
1296	S445	-1770.0	326.0
1297	S444	-1785.0	436.0
1298	S443	-1800.0	326.0
1299	S442	-1815.0	436.0
1300	S441	-1830.0	326.0

R61523 Pad Coordinates(No.14)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1301	S440	-1845.0	436.0
1302	S439	-1860.0	326.0
1303	S438	-1875.0	436.0
1304	S437	-1890.0	326.0
1305	S436	-1905.0	436.0
1306	S435	-1920.0	326.0
1307	S434	-1935.0	436.0
1308	S433	-1950.0	326.0
1309	S432	-1965.0	436.0
1310	S431	-1980.0	326.0
1311	S430	-1995.0	436.0
1312	S429	-2010.0	326.0
1313	S428	-2025.0	436.0
1314	S427	-2040.0	326.0
1315	S426	-2055.0	436.0
1316	S425	-2070.0	326.0
1317	S424	-2085.0	436.0
1318	S423	-2100.0	326.0
1319	S422	-2115.0	436.0
1320	S421	-2130.0	326.0
1321	S420	-2145.0	436.0
1322	S419	-2160.0	326.0
1323	S418	-2175.0	436.0
1324	S417	-2190.0	326.0
1325	S416	-2205.0	436.0
1326	S415	-2220.0	326.0
1327	S414	-2235.0	436.0
1328	S413	-2250.0	326.0
1329	S412	-2265.0	436.0
1330	S411	-2280.0	326.0
1331	S410	-2295.0	436.0
1332	S409	-2310.0	326.0
1333	S408	-2325.0	436.0
1334	S407	-2340.0	326.0
1335	S406	-2355.0	436.0
1336	S405	-2370.0	326.0
1337	S404	-2385.0	436.0
1338	S403	-2400.0	326.0
1339	S402	-2415.0	436.0
1340	S401	-2430.0	326.0
1341	S400	-2445.0	436.0
1342	S399	-2460.0	326.0
1343	S398	-2475.0	436.0
1344	S397	-2490.0	326.0
1345	S396	-2505.0	436.0
1346	S395	-2520.0	326.0
1347	S394	-2535.0	436.0
1348	S393	-2550.0	326.0
1349	S392	-2565.0	436.0
1350	S391	-2580.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
1351	S390	-2595.0	436.0
1352	S389	-2610.0	326.0
1353	S388	-2625.0	436.0
1354	S387	-2640.0	326.0
1355	S386	-2655.0	436.0
1356	S385	-2670.0	326.0
1357	S384	-2685.0	436.0
1358	S383	-2700.0	326.0
1359	S382	-2715.0	436.0
1360	S381	-2730.0	326.0
1361	S380	-2745.0	436.0
1362	S379	-2760.0	326.0
1363	S378	-2775.0	436.0
1364	S377	-2790.0	326.0
1365	S376	-2805.0	436.0
1366	S375	-2820.0	326.0
1367	S374	-2835.0	436.0
1368	S373	-2850.0	326.0
1369	S372	-2865.0	436.0
1370	S371	-2880.0	326.0
1371	S370	-2895.0	436.0
1372	S369	-2910.0	326.0
1373	S368	-2925.0	436.0
1374	S367	-2940.0	326.0
1375	S366	-2955.0	436.0
1376	S365	-2970.0	326.0
1377	S364	-2985.0	436.0
1378	S363	-3000.0	326.0
1379	S362	-3015.0	436.0
1380	S361	-3030.0	326.0
1381	S360	-3045.0	436.0
1382	S359	-3060.0	326.0
1383	S358	-3075.0	436.0
1384	S357	-3090.0	326.0
1385	S356	-3105.0	436.0
1386	S355	-3120.0	326.0
1387	S354	-3135.0	436.0
1388	S353	-3150.0	326.0
1389	S352	-3165.0	436.0
1390	S351	-3180.0	326.0
1391	S350	-3195.0	436.0
1392	S349	-3210.0	326.0
1393	S348	-3225.0	436.0
1394	S347	-3240.0	326.0
1395	S346	-3255.0	436.0
1396	S345	-3270.0	326.0
1397	S344	-3285.0	436.0
1398	S343	-3300.0	326.0
1399	S342	-3315.0	436.0
1400	S341	-3330.0	326.0

R61523 Pad Coordinates(No.15)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1401	S340	-3345.0	436.0
1402	S339	-3360.0	326.0
1403	S338	-3375.0	436.0
1404	S337	-3390.0	326.0
1405	S336	-3405.0	436.0
1406	S335	-3420.0	326.0
1407	S334	-3435.0	436.0
1408	S333	-3450.0	326.0
1409	S332	-3465.0	436.0
1410	S331	-3480.0	326.0
1411	S330	-3495.0	436.0
1412	S329	-3510.0	326.0
1413	S328	-3525.0	436.0
1414	S327	-3540.0	326.0
1415	S326	-3555.0	436.0
1416	S325	-3570.0	326.0
1417	S324	-3585.0	436.0
1418	S323	-3600.0	326.0
1419	S322	-3615.0	436.0
1420	S321	-3630.0	326.0
1421	S320	-3645.0	436.0
1422	S319	-3660.0	326.0
1423	S318	-3675.0	436.0
1424	S317	-3690.0	326.0
1425	S316	-3705.0	436.0
1426	S315	-3720.0	326.0
1427	S314	-3735.0	436.0
1428	S313	-3750.0	326.0
1429	S312	-3765.0	436.0
1430	S311	-3780.0	326.0
1431	S310	-3795.0	436.0
1432	S309	-3810.0	326.0
1433	S308	-3825.0	436.0
1434	S307	-3840.0	326.0
1435	S306	-3855.0	436.0
1436	S305	-3870.0	326.0
1437	S304	-3885.0	436.0
1438	S303	-3900.0	326.0
1439	S302	-3915.0	436.0
1440	S301	-3930.0	326.0
1441	S300	-3945.0	436.0
1442	S299	-3960.0	326.0
1443	S298	-3975.0	436.0
1444	S297	-3990.0	326.0
1445	S296	-4005.0	436.0
1446	S295	-4020.0	326.0
1447	S294	-4035.0	436.0
1448	S293	-4050.0	326.0
1449	S292	-4065.0	436.0
1450	S291	-4080.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
1451	S290	-4095.0	436.0
1452	S289	-4110.0	326.0
1453	S288	-4125.0	436.0
1454	S287	-4140.0	326.0
1455	S286	-4155.0	436.0
1456	S285	-4170.0	326.0
1457	S284	-4185.0	436.0
1458	S283	-4200.0	326.0
1459	S282	-4215.0	436.0
1460	S281	-4230.0	326.0
1461	S280	-4245.0	436.0
1462	S279	-4260.0	326.0
1463	S278	-4275.0	436.0
1464	S277	-4290.0	326.0
1465	S276	-4305.0	436.0
1466	S275	-4320.0	326.0
1467	S274	-4335.0	436.0
1468	S273	-4350.0	326.0
1469	S272	-4365.0	436.0
1470	S271	-4380.0	326.0
1471	S270	-4395.0	436.0
1472	S269	-4410.0	326.0
1473	S268	-4425.0	436.0
1474	S267	-4440.0	326.0
1475	S266	-4455.0	436.0
1476	S265	-4470.0	326.0
1477	S264	-4485.0	436.0
1478	S263	-4500.0	326.0
1479	S262	-4515.0	436.0
1480	S261	-4530.0	326.0
1481	S260	-4545.0	436.0
1482	S259	-4560.0	326.0
1483	S258	-4575.0	436.0
1484	S257	-4590.0	326.0
1485	S256	-4605.0	436.0
1486	S255	-4620.0	326.0
1487	S254	-4635.0	436.0
1488	S253	-4650.0	326.0
1489	S252	-4665.0	436.0
1490	S251	-4680.0	326.0
1491	S250	-4695.0	436.0
1492	S249	-4710.0	326.0
1493	S248	-4725.0	436.0
1494	S247	-4740.0	326.0
1495	S246	-4755.0	436.0
1496	S245	-4770.0	326.0
1497	S244	-4785.0	436.0
1498	S243	-4800.0	326.0
1499	S242	-4815.0	436.0
1500	S241	-4830.0	326.0

R61523 Pad Coordinates(No.16)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1501	S240	-4845.0	436.0
1502	S239	-4860.0	326.0
1503	S238	-4875.0	436.0
1504	S237	-4890.0	326.0
1505	S236	-4905.0	436.0
1506	S235	-4920.0	326.0
1507	S234	-4935.0	436.0
1508	S233	-4950.0	326.0
1509	S232	-4965.0	436.0
1510	S231	-4980.0	326.0
1511	S230	-4995.0	436.0
1512	S229	-5010.0	326.0
1513	S228	-5025.0	436.0
1514	S227	-5040.0	326.0
1515	S226	-5055.0	436.0
1516	S225	-5070.0	326.0
1517	S224	-5085.0	436.0
1518	S223	-5100.0	326.0
1519	S222	-5115.0	436.0
1520	S221	-5130.0	326.0
1521	S220	-5145.0	436.0
1522	S219	-5160.0	326.0
1523	S218	-5175.0	436.0
1524	S217	-5190.0	326.0
1525	S216	-5205.0	436.0
1526	S215	-5220.0	326.0
1527	S214	-5235.0	436.0
1528	S213	-5250.0	326.0
1529	S212	-5265.0	436.0
1530	S211	-5280.0	326.0
1531	S210	-5295.0	436.0
1532	S209	-5310.0	326.0
1533	S208	-5325.0	436.0
1534	S207	-5340.0	326.0
1535	S206	-5355.0	436.0
1536	S205	-5370.0	326.0
1537	S204	-5385.0	436.0
1538	S203	-5400.0	326.0
1539	S202	-5415.0	436.0
1540	S201	-5430.0	326.0
1541	S200	-5445.0	436.0
1542	S199	-5460.0	326.0
1543	S198	-5475.0	436.0
1544	S197	-5490.0	326.0
1545	S196	-5505.0	436.0
1546	S195	-5520.0	326.0
1547	S194	-5535.0	436.0
1548	S193	-5550.0	326.0
1549	S192	-5565.0	436.0
1550	S191	-5580.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
1551	S190	-5595.0	436.0
1552	S189	-5610.0	326.0
1553	S188	-5625.0	436.0
1554	S187	-5640.0	326.0
1555	S186	-5655.0	436.0
1556	S185	-5670.0	326.0
1557	S184	-5685.0	436.0
1558	S183	-5700.0	326.0
1559	S182	-5715.0	436.0
1560	S181	-5730.0	326.0
1561	S180	-5745.0	436.0
1562	S179	-5760.0	326.0
1563	S178	-5775.0	436.0
1564	S177	-5790.0	326.0
1565	S176	-5805.0	436.0
1566	S175	-5820.0	326.0
1567	S174	-5835.0	436.0
1568	S173	-5850.0	326.0
1569	S172	-5865.0	436.0
1570	S171	-5880.0	326.0
1571	S170	-5895.0	436.0
1572	S169	-5910.0	326.0
1573	S168	-5925.0	436.0
1574	S167	-5940.0	326.0
1575	S166	-5955.0	436.0
1576	S165	-5970.0	326.0
1577	S164	-5985.0	436.0
1578	S163	-6000.0	326.0
1579	S162	-6015.0	436.0
1580	S161	-6030.0	326.0
1581	S160	-6045.0	436.0
1582	S159	-6060.0	326.0
1583	S158	-6075.0	436.0
1584	S157	-6090.0	326.0
1585	S156	-6105.0	436.0
1586	S155	-6120.0	326.0
1587	S154	-6135.0	436.0
1588	S153	-6150.0	326.0
1589	S152	-6165.0	436.0
1590	S151	-6180.0	326.0
1591	S150	-6195.0	436.0
1592	S149	-6210.0	326.0
1593	S148	-6225.0	436.0
1594	S147	-6240.0	326.0
1595	S146	-6255.0	436.0
1596	S145	-6270.0	326.0
1597	S144	-6285.0	436.0
1598	S143	-6300.0	326.0
1599	S142	-6315.0	436.0
1600	S141	-6330.0	326.0

R61523 Pad Coordinates(No.17)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1601	S140	-6345.0	436.0
1602	S139	-6360.0	326.0
1603	S138	-6375.0	436.0
1604	S137	-6390.0	326.0
1605	S136	-6405.0	436.0
1606	S135	-6420.0	326.0
1607	S134	-6435.0	436.0
1608	S133	-6450.0	326.0
1609	S132	-6465.0	436.0
1610	S131	-6480.0	326.0
1611	S130	-6495.0	436.0
1612	S129	-6510.0	326.0
1613	S128	-6525.0	436.0
1614	S127	-6540.0	326.0
1615	S126	-6555.0	436.0
1616	S125	-6570.0	326.0
1617	S124	-6585.0	436.0
1618	S123	-6600.0	326.0
1619	S122	-6615.0	436.0
1620	S121	-6630.0	326.0
1621	S120	-6645.0	436.0
1622	S119	-6660.0	326.0
1623	S118	-6675.0	436.0
1624	S117	-6690.0	326.0
1625	S116	-6705.0	436.0
1626	S115	-6720.0	326.0
1627	S114	-6735.0	436.0
1628	S113	-6750.0	326.0
1629	S112	-6765.0	436.0
1630	S111	-6780.0	326.0
1631	S110	-6795.0	436.0
1632	S109	-6810.0	326.0
1633	S108	-6825.0	436.0
1634	S107	-6840.0	326.0
1635	S106	-6855.0	436.0
1636	S105	-6870.0	326.0
1637	S104	-6885.0	436.0
1638	S103	-6900.0	326.0
1639	S102	-6915.0	436.0
1640	S101	-6930.0	326.0
1641	S100	-6945.0	436.0
1642	S99	-6960.0	326.0
1643	S98	-6975.0	436.0
1644	S97	-6990.0	326.0
1645	S96	-7005.0	436.0
1646	S95	-7020.0	326.0
1647	S94	-7035.0	436.0
1648	S93	-7050.0	326.0
1649	S92	-7065.0	436.0
1650	S91	-7080.0	326.0

(Unit: um)

Pad No.	Pad Name	X	Y
1651	S90	-7095.0	436.0
1652	S89	-7110.0	326.0
1653	S88	-7125.0	436.0
1654	S87	-7140.0	326.0
1655	S86	-7155.0	436.0
1656	S85	-7170.0	326.0
1657	S84	-7185.0	436.0
1658	S83	-7200.0	326.0
1659	S82	-7215.0	436.0
1660	S81	-7230.0	326.0
1661	S80	-7245.0	436.0
1662	S79	-7260.0	326.0
1663	S78	-7275.0	436.0
1664	S77	-7290.0	326.0
1665	S76	-7305.0	436.0
1666	S75	-7320.0	326.0
1667	S74	-7335.0	436.0
1668	S73	-7350.0	326.0
1669	S72	-7365.0	436.0
1670	S71	-7380.0	326.0
1671	S70	-7395.0	436.0
1672	S69	-7410.0	326.0
1673	S68	-7425.0	436.0
1674	S67	-7440.0	326.0
1675	S66	-7455.0	436.0
1676	S65	-7470.0	326.0
1677	S64	-7485.0	436.0
1678	S63	-7500.0	326.0
1679	S62	-7515.0	436.0
1680	S61	-7530.0	326.0
1681	S60	-7545.0	436.0
1682	S59	-7560.0	326.0
1683	S58	-7575.0	436.0
1684	S57	-7590.0	326.0
1685	S56	-7605.0	436.0
1686	S55	-7620.0	326.0
1687	S54	-7635.0	436.0
1688	S53	-7650.0	326.0
1689	S52	-7665.0	436.0
1690	S51	-7680.0	326.0
1691	S50	-7695.0	436.0
1692	S49	-7710.0	326.0
1693	S48	-7725.0	436.0
1694	S47	-7740.0	326.0
1695	S46	-7755.0	436.0
1696	S45	-7770.0	326.0
1697	S44	-7785.0	436.0
1698	S43	-7800.0	326.0
1699	S42	-7815.0	436.0
1700	S41	-7830.0	326.0

R61523 Pad Coordinates(No.18)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1701	S40	-7845.0	436.0
1702	S39	-7860.0	326.0
1703	S38	-7875.0	436.0
1704	S37	-7890.0	326.0
1705	S36	-7905.0	436.0
1706	S35	-7920.0	326.0
1707	S34	-7935.0	436.0
1708	S33	-7950.0	326.0
1709	S32	-7965.0	436.0
1710	S31	-7980.0	326.0
1711	S30	-7995.0	436.0
1712	S29	-8010.0	326.0
1713	S28	-8025.0	436.0
1714	S27	-8040.0	326.0
1715	S26	-8055.0	436.0
1716	S25	-8070.0	326.0
1717	S24	-8085.0	436.0
1718	S23	-8100.0	326.0
1719	S22	-8115.0	436.0
1720	S21	-8130.0	326.0
1721	S20	-8145.0	436.0
1722	S19	-8160.0	326.0
1723	S18	-8175.0	436.0
1724	S17	-8190.0	326.0
1725	S16	-8205.0	436.0
1726	S15	-8220.0	326.0
1727	S14	-8235.0	436.0
1728	S13	-8250.0	326.0
1729	S12	-8265.0	436.0
1730	S11	-8280.0	326.0
1731	S10	-8295.0	436.0
1732	S9	-8310.0	326.0
1733	S8	-8325.0	436.0
1734	S7	-8340.0	326.0
1735	S6	-8355.0	436.0
1736	S5	-8370.0	326.0
1737	S4	-8385.0	436.0
1738	S3	-8400.0	326.0
1739	S2	-8415.0	436.0
1740	S1	-8430.0	326.0
1741	TESTO7	-8445.0	436.0
1742	TESTO8	-8685.0	436.0
1743	G639	-8700.0	326.0
1744	G637	-8715.0	436.0
1745	G635	-8730.0	326.0
1746	G633	-8745.0	436.0
1747	G631	-8760.0	326.0
1748	G629	-8775.0	436.0
1749	G627	-8790.0	326.0
1750	G625	-8805.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
1751	G623	-8820.0	326.0
1752	G621	-8835.0	436.0
1753	G619	-8850.0	326.0
1754	G617	-8865.0	436.0
1755	G615	-8880.0	326.0
1756	G613	-8895.0	436.0
1757	G611	-8910.0	326.0
1758	G609	-8925.0	436.0
1759	G607	-8940.0	326.0
1760	G605	-8955.0	436.0
1761	G603	-8970.0	326.0
1762	G601	-8985.0	436.0
1763	G599	-9000.0	326.0
1764	G597	-9015.0	436.0
1765	G595	-9030.0	326.0
1766	G593	-9045.0	436.0
1767	G591	-9060.0	326.0
1768	G589	-9075.0	436.0
1769	G587	-9090.0	326.0
1770	G585	-9105.0	436.0
1771	G583	-9120.0	326.0
1772	G581	-9135.0	436.0
1773	G579	-9150.0	326.0
1774	G577	-9165.0	436.0
1775	G575	-9180.0	326.0
1776	G573	-9195.0	436.0
1777	G571	-9210.0	326.0
1778	G569	-9225.0	436.0
1779	G567	-9240.0	326.0
1780	G565	-9255.0	436.0
1781	G563	-9270.0	326.0
1782	G561	-9285.0	436.0
1783	G559	-9300.0	326.0
1784	G557	-9315.0	436.0
1785	G555	-9330.0	326.0
1786	G553	-9345.0	436.0
1787	G551	-9360.0	326.0
1788	G549	-9375.0	436.0
1789	G547	-9390.0	326.0
1790	G545	-9405.0	436.0
1791	G543	-9420.0	326.0
1792	G541	-9435.0	436.0
1793	G539	-9450.0	326.0
1794	G537	-9465.0	436.0
1795	G535	-9480.0	326.0
1796	G533	-9495.0	436.0
1797	G531	-9510.0	326.0
1798	G529	-9525.0	436.0
1799	G527	-9540.0	326.0
1800	G525	-9555.0	436.0

R61523 Pad Coordinates(No.19)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1801	G523	-9570.0	326.0
1802	G521	-9585.0	436.0
1803	G519	-9600.0	326.0
1804	G517	-9615.0	436.0
1805	G515	-9630.0	326.0
1806	G513	-9645.0	436.0
1807	G511	-9660.0	326.0
1808	G509	-9675.0	436.0
1809	G507	-9690.0	326.0
1810	G505	-9705.0	436.0
1811	G503	-9720.0	326.0
1812	G501	-9735.0	436.0
1813	G499	-9750.0	326.0
1814	G497	-9765.0	436.0
1815	G495	-9780.0	326.0
1816	G493	-9795.0	436.0
1817	G491	-9810.0	326.0
1818	G489	-9825.0	436.0
1819	G487	-9840.0	326.0
1820	G485	-9855.0	436.0
1821	G483	-9870.0	326.0
1822	G481	-9885.0	436.0
1823	G479	-9900.0	326.0
1824	G477	-9915.0	436.0
1825	G475	-9930.0	326.0
1826	G473	-9945.0	436.0
1827	G471	-9960.0	326.0
1828	G469	-9975.0	436.0
1829	G467	-9990.0	326.0
1830	G465	-10005.0	436.0
1831	G463	-10020.0	326.0
1832	G461	-10035.0	436.0
1833	G459	-10050.0	326.0
1834	G457	-10065.0	436.0
1835	G455	-10080.0	326.0
1836	G453	-10095.0	436.0
1837	G451	-10110.0	326.0
1838	G449	-10125.0	436.0
1839	G447	-10140.0	326.0
1840	G445	-10155.0	436.0
1841	G443	-10170.0	326.0
1842	G441	-10185.0	436.0
1843	G439	-10200.0	326.0
1844	G437	-10215.0	436.0
1845	G435	-10230.0	326.0
1846	G433	-10245.0	436.0
1847	G431	-10260.0	326.0
1848	G429	-10275.0	436.0
1849	G427	-10290.0	326.0
1850	G425	-10305.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
1851	G423	-10320.0	326.0
1852	G421	-10335.0	436.0
1853	G419	-10350.0	326.0
1854	G417	-10365.0	436.0
1855	G415	-10380.0	326.0
1856	G413	-10395.0	436.0
1857	G411	-10410.0	326.0
1858	G409	-10425.0	436.0
1859	G407	-10440.0	326.0
1860	G405	-10455.0	436.0
1861	G403	-10470.0	326.0
1862	G401	-10485.0	436.0
1863	G399	-10500.0	326.0
1864	G397	-10515.0	436.0
1865	G395	-10530.0	326.0
1866	G393	-10545.0	436.0
1867	G391	-10560.0	326.0
1868	G389	-10575.0	436.0
1869	G387	-10590.0	326.0
1870	G385	-10605.0	436.0
1871	G383	-10620.0	326.0
1872	G381	-10635.0	436.0
1873	G379	-10650.0	326.0
1874	G377	-10665.0	436.0
1875	G375	-10680.0	326.0
1876	G373	-10695.0	436.0
1877	G371	-10710.0	326.0
1878	G369	-10725.0	436.0
1879	G367	-10740.0	326.0
1880	G365	-10755.0	436.0
1881	G363	-10770.0	326.0
1882	G361	-10785.0	436.0
1883	G359	-10800.0	326.0
1884	G357	-10815.0	436.0
1885	G355	-10830.0	326.0
1886	G353	-10845.0	436.0
1887	G351	-10860.0	326.0
1888	G349	-10875.0	436.0
1889	G347	-10890.0	326.0
1890	G345	-10905.0	436.0
1891	G343	-10920.0	326.0
1892	G341	-10935.0	436.0
1893	G339	-10950.0	326.0
1894	G337	-10965.0	436.0
1895	G335	-10980.0	326.0
1896	G333	-10995.0	436.0
1897	G331	-11010.0	326.0
1898	G329	-11025.0	436.0
1899	G327	-11040.0	326.0
1900	G325	-11055.0	436.0

R61523 Pad Coordinates(No.20)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
1901	G323	-11070.0	326.0
1902	G321	-11085.0	436.0
1903	G319	-11100.0	326.0
1904	G317	-11115.0	436.0
1905	G315	-11130.0	326.0
1906	G313	-11145.0	436.0
1907	G311	-11160.0	326.0
1908	G309	-11175.0	436.0
1909	G307	-11190.0	326.0
1910	G305	-11205.0	436.0
1911	G303	-11220.0	326.0
1912	G301	-11235.0	436.0
1913	G299	-11250.0	326.0
1914	G297	-11265.0	436.0
1915	G295	-11280.0	326.0
1916	G293	-11295.0	436.0
1917	G291	-11310.0	326.0
1918	G289	-11325.0	436.0
1919	G287	-11340.0	326.0
1920	G285	-11355.0	436.0
1921	G283	-11370.0	326.0
1922	G281	-11385.0	436.0
1923	G279	-11400.0	326.0
1924	G277	-11415.0	436.0
1925	G275	-11430.0	326.0
1926	G273	-11445.0	436.0
1927	G271	-11460.0	326.0
1928	G269	-11475.0	436.0
1929	G267	-11490.0	326.0
1930	G265	-11505.0	436.0
1931	G263	-11520.0	326.0
1932	G261	-11535.0	436.0
1933	G259	-11550.0	326.0
1934	G257	-11565.0	436.0
1935	G255	-11580.0	326.0
1936	G253	-11595.0	436.0
1937	G251	-11610.0	326.0
1938	G249	-11625.0	436.0
1939	G247	-11640.0	326.0
1940	G245	-11655.0	436.0
1941	G243	-11670.0	326.0
1942	G241	-11685.0	436.0
1943	G239	-11700.0	326.0
1944	G237	-11715.0	436.0
1945	G235	-11730.0	326.0
1946	G233	-11745.0	436.0
1947	G231	-11760.0	326.0
1948	G229	-11775.0	436.0
1949	G227	-11790.0	326.0
1950	G225	-11805.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
1951	G223	-11820.0	326.0
1952	G221	-11835.0	436.0
1953	G219	-11850.0	326.0
1954	G217	-11865.0	436.0
1955	G215	-11880.0	326.0
1956	G213	-11895.0	436.0
1957	G211	-11910.0	326.0
1958	G209	-11925.0	436.0
1959	G207	-11940.0	326.0
1960	G205	-11955.0	436.0
1961	G203	-11970.0	326.0
1962	G201	-11985.0	436.0
1963	G199	-12000.0	326.0
1964	G197	-12015.0	436.0
1965	G195	-12030.0	326.0
1966	G193	-12045.0	436.0
1967	G191	-12060.0	326.0
1968	G189	-12075.0	436.0
1969	G187	-12090.0	326.0
1970	G185	-12105.0	436.0
1971	G183	-12120.0	326.0
1972	G181	-12135.0	436.0
1973	G179	-12150.0	326.0
1974	G177	-12165.0	436.0
1975	G175	-12180.0	326.0
1976	G173	-12195.0	436.0
1977	G171	-12210.0	326.0
1978	G169	-12225.0	436.0
1979	G167	-12240.0	326.0
1980	G165	-12255.0	436.0
1981	G163	-12270.0	326.0
1982	G161	-12285.0	436.0
1983	G159	-12300.0	326.0
1984	G157	-12315.0	436.0
1985	G155	-12330.0	326.0
1986	G153	-12345.0	436.0
1987	G151	-12360.0	326.0
1988	G149	-12375.0	436.0
1989	G147	-12390.0	326.0
1990	G145	-12405.0	436.0
1991	G143	-12420.0	326.0
1992	G141	-12435.0	436.0
1993	G139	-12450.0	326.0
1994	G137	-12465.0	436.0
1995	G135	-12480.0	326.0
1996	G133	-12495.0	436.0
1997	G131	-12510.0	326.0
1998	G129	-12525.0	436.0
1999	G127	-12540.0	326.0
2000	G125	-12555.0	436.0

R61523 Pad Coordinates(No.21)

2009.03.09 (Rev0.3)

(Unit: um)

Pad No.	Pad Name	X	Y
2001	G123	-12570.0	326.0
2002	G121	-12585.0	436.0
2003	G119	-12600.0	326.0
2004	G117	-12615.0	436.0
2005	G115	-12630.0	326.0
2006	G113	-12645.0	436.0
2007	G111	-12660.0	326.0
2008	G109	-12675.0	436.0
2009	G107	-12690.0	326.0
2010	G105	-12705.0	436.0
2011	G103	-12720.0	326.0
2012	G101	-12735.0	436.0
2013	G99	-12750.0	326.0
2014	G97	-12765.0	436.0
2015	G95	-12780.0	326.0
2016	G93	-12795.0	436.0
2017	G91	-12810.0	326.0
2018	G89	-12825.0	436.0
2019	G87	-12840.0	326.0
2020	G85	-12855.0	436.0
2021	G83	-12870.0	326.0
2022	G81	-12885.0	436.0
2023	G79	-12900.0	326.0
2024	G77	-12915.0	436.0
2025	G75	-12930.0	326.0
2026	G73	-12945.0	436.0
2027	G71	-12960.0	326.0
2028	G69	-12975.0	436.0
2029	G67	-12990.0	326.0
2030	G65	-13005.0	436.0
2031	G63	-13020.0	326.0
2032	G61	-13035.0	436.0
2033	G59	-13050.0	326.0
2034	G57	-13065.0	436.0
2035	G55	-13080.0	326.0
2036	G53	-13095.0	436.0
2037	G51	-13110.0	326.0
2038	G49	-13125.0	436.0
2039	G47	-13140.0	326.0
2040	G45	-13155.0	436.0
2041	G43	-13170.0	326.0
2042	G41	-13185.0	436.0
2043	G39	-13200.0	326.0
2044	G37	-13215.0	436.0
2045	G35	-13230.0	326.0
2046	G33	-13245.0	436.0
2047	G31	-13260.0	326.0
2048	G29	-13275.0	436.0
2049	G27	-13290.0	326.0
2050	G25	-13305.0	436.0

(Unit: um)

Pad No.	Pad Name	X	Y
2051	G23	-13320.0	326.0
2052	G21	-13335.0	436.0
2053	G19	-13350.0	326.0
2054	G17	-13365.0	436.0
2055	G15	-13380.0	326.0
2056	G13	-13395.0	436.0
2057	G11	-13410.0	326.0
2058	G9	-13425.0	436.0
2059	G7	-13440.0	326.0
2060	G5	-13455.0	436.0
2061	G3	-13470.0	326.0
2062	G1	-13485.0	436.0
2063	TESTO9	-13500.0	326.0
2064	TESTO10	-13515.0	436.0

(Unit: um)

Alignment Mark	X	Y
Cross	-13656.0	436.0
	13656.0	436.0

BUMP Arrangement/Alignment Mark

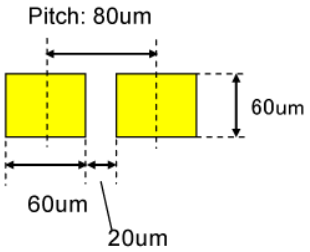
●Chip size: 27.49mm x 1.05mm
●Chip thickness: 230um (Typ.)
●Pad coordinates: Pad center
●Pad origin: Chip center

●Au bump size
(1) 60um x 60um (I/O side: No.1-334)
(2) 15um x 90um (liquid crustal output side: No.335-2064)

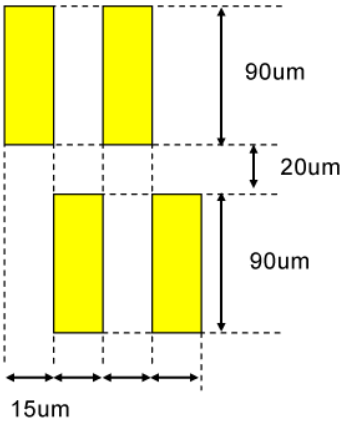
●Au bump pitch: See "Pad Arrangement."
●Au bump height: 12um

●Bump shape

■Bump size (Input side)



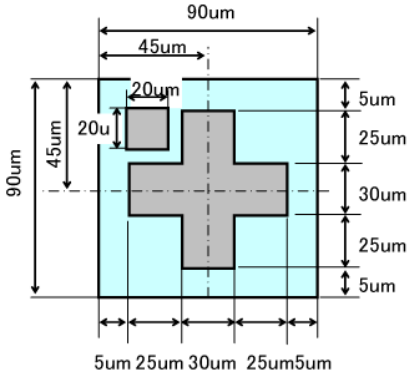
■Bump size (Output side)



●Alignment mark

Alignment mark	X	Y
(1-a)	-13656.0	436.0
(1-b)	13656.0	436.0

1-a: (Left Alignment Mark)



1-b: (Right Alignment Mark)

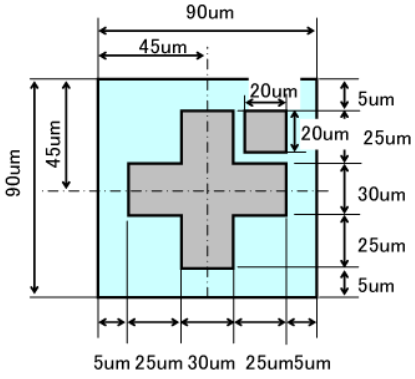


Figure 2

R61523 端子配置図 Rev0.4 09.04.06

Renesas SP Confidential

RENESAS SP

Scribe Center

R61523	COG抵抗(MAX)	端子No
DUMMY1	–	1
DUMMYR1	–	2
DUMMYR2	–	3
VCOM	12 Ω	4
VCOM		5
VCOM		6
VCOM		7
AGND	8 Ω	8
AGND		9
AGND		10
AGND		11
AGND		12
AGND		13
GND	8 Ω	14
GND		15
GND		16
GND		17
GND		18
GND		19
DDVDHB	8 Ω	20
DDVDHB		21
DDVDHB		22
DDVDHB		23
DDVDHB		24
DDVDHB		25
C11BP	8 Ω	26
C11BP		27
C11BP		28
C11BP		29
C11BP		30
C11BP		31
C11BM	8 Ω	32
C11BM		33
C11BM		34
C11BM		35
C11BM		36
C11BM		37
AGND	8 Ω	38
AGND		39
AGND		40
AGND		41
AGND		42
AGND		43
C12BP	8 Ω	44
C12BP		45
C12BP		46
C12BP		47
C12BP		48
C12BP		49
C12BM	8 Ω	50
C12BM		51
C12BM		52
C12BM		53
C12BM		54
C12BM		55
VCI	6 Ω	56
VCI		57
VCI		58
VCI		59
VCI		60
VCI		61
VCI		62
VCI		63
C12AM	8 Ω	64
C12AM		65
C12AM		66
C12AM		67
C12AM		68
C12AM		69
C12AP	8 Ω	70
C12AP		71
C12AP		72
C12AP		73
C12AP		74
C12AP		75
AGND	8 Ω	76
AGND		77
AGND		78
AGND		79
AGND		80
AGND		81
C11AM	8 Ω	82
C11AM		83
C11AM		84
C11AM		85
C11AM		86
C11AM		87
C11AP	8 Ω	88
C11AP		89
C11AP		90
C11AP		91
C11AP		92
C11AP		93
DDVDHA	8 Ω	94
DDVDHA		95
DDVDHA		96
DDVDHA		97
DDVDHA		98
DDVDHA		99
GNDDUM	25 Ω	100
GNDDUM		101
VDDTEST	49 Ω	102
VREFC	49 Ω	103
VREFD	–	104
VREF	–	105
TSC	49 Ω	106
TEST2	49 Ω	107
TEST4	49 Ω	108
GND	6 Ω	109
GND		110
GND		111
GND		112
GND		113
GND		114
GND		115
IOVCC	7 Ω	116
IOVCC		117
IOVCC		118
IOVCC		119
IOVCC		120
IOVCC		121
IOVCC		122
IOVCC		123
VDD	5 Ω	124
VDD		125
VDD		126
VDD		127
VDD		128
VDD		129
VDD		130
VDD		131
VDD		132
VDD		133
DPHYVCC	12 Ω	134
DPHYVCC		135
DPHYVCC		136
DPHYVCC		137
DSID0N	16 Ω	138
DSID0N		139
DSID0N		140
DSID0NLVL	49 Ω	141
DSID0PLVL	49 Ω	142
DSID0P	16 Ω	143
DSID0P		144
DSID0P		145
DPHYGNDDUM1	49 Ω	146
DSICLKN	16 Ω	147
DSICLKN		148
DSICLKN		149
DSICLKNLVL	49 Ω	150
DSICLKPLVL	49 Ω	151
DSICLKP	16 Ω	152
DSICLKP		153
DSICLKP		154
DPHYGNDDUM2	49 Ω	155
DSID1N	16 Ω	156
DSID1N		157
DSID1N		158
DSID1NLVL	49 Ω	159
DSID1PLVL	49 Ω	160
DSID1P	16 Ω	161
DSID1P		162
DSID1P		163
DPHYGND	12 Ω	164
DPHYGND		165
DPHYGND		166
DPHYGND		167
GND	8 Ω	168
GND		169
GND		170
GND		171
GND		172
GND		173
VGS	49 Ω	174
AGND	6 Ω	175
AGND		176
AGND		177
AGND		178
AGND		179
AGND		180
AGND		181
AGND		182
VPP1	49 Ω	183
AGNDDUM	49 Ω	184
LEDPWM	49 Ω	185
TE	49 Ω	186
DB15	49 Ω	187
DB14	49 Ω	188
DB13	49 Ω	189
DB12	49 Ω	190
DB11	49 Ω	191
DB10	49 Ω	192
DB9	49 Ω	193
DB8	49 Ω	194
IOVCC	8 Ω	195
IOVCC		196
IOVCC		197
IOVCC		198
IOVCC		199
IOVCC		200
DB7	49 Ω	201
DB6	49 Ω	202
DB5	49 Ω	203
DB4	49 Ω	204
DB3	49 Ω	205
DB2	49 Ω	206
DB1	49 Ω	207
DB0	49 Ω	208
CSX	49 Ω	209
DCX	49 Ω	210
WRX	49 Ω	211
RDX	49 Ω	212
RESX	49 Ω	213
GND	8 Ω	214
GND		215
GND		216
GND		217
GND		218
GND		219
IM0	49 Ω	220
IM1	49 Ω	221
IM2	49 Ω	222
VMON	–	223
VMON		224
VREGI	25 Ω	225
VREGI		226
VCOMH	25 Ω	227
VCOMH		228
VCOML	25 Ω	229
VCOML		230
VCL	12 Ω	231
VCL		232
VCL		233
VCL		234
C13M	12 Ω	235
C13M		236
C13M		237
C13M		238
C13P	12 Ω	239
C13P		240
C13P		241
C13P		242
AGND	10 Ω	243
AGND		244
AGND		245
AGND		246
AGND		247
VGH	8 Ω	248
VGH		249
VGH		250
VGH		251
VGH		252
VGH		253
C21P	7 Ω	254
C21P		255
C21P		256
C21P		257
C21P		258
C21P		259
C21P		260
C21M	7 Ω	261
C21M		262
C21M		263
C21M		264
C21M		265
C21M		266
C21M		267
C22P	7 Ω	268
C22P		269
C22P		270
C22P		271
C22P		272
C22P		273
C22P		274
C22M	7 Ω	275
C22M		276
C22M		277
C22M		278
C22M		279
C22M		280
C22M		281
C23P	7 Ω	282
C23P		283
C23P		284
C23P		285
C23P		286
C23P		287
C23P		288
C23M	7 Ω	289
C23M		290
C23M		291
C23M		292
C23M		293
C23M		294
C23M		295
C31P	7 Ω	296
C31P		297
C31P		298
C31P		299
C31P		300
C31P		301
C31P		302
C31M	7 Ω	303
C31M		304
C31M		305
C31M		306
C31M		307
C31M		308
C31M		309
VGL	8 Ω	310
VGL		311
VGL		312
VGL		313
VGL		314
VGL		315
GND	8 Ω	316
GND		317
GND		318
GND		319
GND		320
GND		321
AGND	8 Ω	322
AGND		323
AGND		324
AGND		325
AGND		326
AGND		327
VCOM	12 Ω	328
VCOM		329
VCOM		330
VCOM		331
DUMMYR3	–	332
DUMMYR4	–	333
DUMMY2	–	334

端子No	端子名
2064	TESTO10
2063	TESTO9
2062	G1
2061	G3
2060	G5
2059	G7
1746	G633
1745	G635
1744	G637
1743	G639
1742	TESTO8
1741	TESTO7
1740	S1
1739	S2
1738	S3
1737	S4
1204	S537
1203	S538
1202	S539
1201	S540
1200	TESTO6
1199	TESTO5
1198	S541
1197	S542
1196	S543
1195	S544
662	S1077
661	S1078
660	S1079
659	S1080
658	TESTO4
657	TESTO3
656	G640
655	G638
654	G636
653	G634
340	G8
339	G6
338	G4
337	G2
336	TESTO2
335	TESTO1

Top View

BUMP

Chip

VDD(Analog)

VDDI(Digital)

差動信号です。等長・同パターンで配線して下さい。また各ペア間はGNDでシールドしてください。

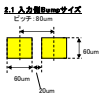
(17) 削除検討

(18) 削除検討

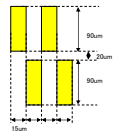
1. チップサイズ

項目	サイズ
短辺(mm)	1.05
長辺(mm)	27.48
面積(mm²)	28.8645
Aspect(長辺/短辺)	26.18

2.1 入力側Bumpサイズ



2.2 出力側Bumpサイズ



2.3 Bump数と出力Bump面積/入力Bump面積

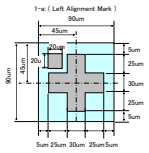
項目	幅(um)	高さ(um)	単位面積 (um²)	n	Sub Total(mm²)
入力側	60	60	3,600	334	1.20
出力側	15	90	1,350	1,730	2.34
比率	–	–	–	–	0.51

2.4 Bump間隔の制約

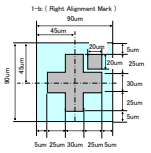
項目	サイズ
a: チップ端~Active Bump(入力)	475 um
b: チップ端~Active Bump(出力)	252.5 um
c: 入力Bump ~ 出力Bump	700 um
d: Gate Bump~ Source Bump	255 um
e: Source Bump~ Source Bump	675 um

3. アライメントマークサイズ

1-a（Left Alignment Mark）



1-b（Right Alignment Mark）



4. 外付け個品点数

1) 外付けショットキーバリアダイオード: 0ヶ

2) 外付け容量、下表参照

#	容量接続(1μF)	備考
①	DDVDHB – GND	DDVDH昇圧(2セット目)
②	C11BP – C11BM	
③	C12BP – C12BM	
④	C12AP – C12AM	DDVDH昇圧(1セット目)
⑤	C11AP – C11AM	
⑥	DDVDHA – GND	
⑦	VDD – GND	論理、RAM用降圧電源
⑧	VREG1 – GND	
⑨	VCL – GND	VCL昇圧
⑩	C13P – C13M	
⑪	VGH – GND	
⑫	C21P – C21M	
⑬	C22P – C22M	VGH/VGL昇圧
⑭	C23P – C23M	
⑮	C31P – C31M	
⑯	VGL – GND	
⑰	VCOMH – GND	削除予定、但しランドを設けて頂きたく
⑱	VCOML – GND	

履歴

Rev.	日付	内容
0.1	09.02.19	新規作成
0.2	09.02.25	誤記訂正(「R61523案」→「R61523」に修正)
0.3	09.03.10	チップサイズ、BUMP間隔a,b,c確定 DSI用端子にFPC上の注意点を追記
0.4	09.04.06	BUMP間隔'a'修正 395um→475um

System Interface Configuration (MIPI-DSI)

The DSI incorporated in the R61523 complies with the following standards.

MIPI DSI: Version 1.01.00r11 21-Feb-2008
MIPI D-PHY: Version 0.90.00 8-Oct-2007
MIPI DCS: Version 1.01.00

(1) Basic DSI Specification

- Number of data lanes: 1/2 data lane(s)
- Maximum data rate: 300Mbps/lane (Total: 600Mbps/2 lanes)
- Only command mode supported
- Only 36h: set_address_mode command (B5 = 0, horizontal direction) supported
- Frame memory window address setting

  2Ah: set_column_address

  SC[9:0] = 2n (n = 0, 1, 2, …179)
  EC[9:0] = 2m – 1 (m = 1, 2, …180)
  EC – SC > 2 pixels

(2) DSI System Configuration

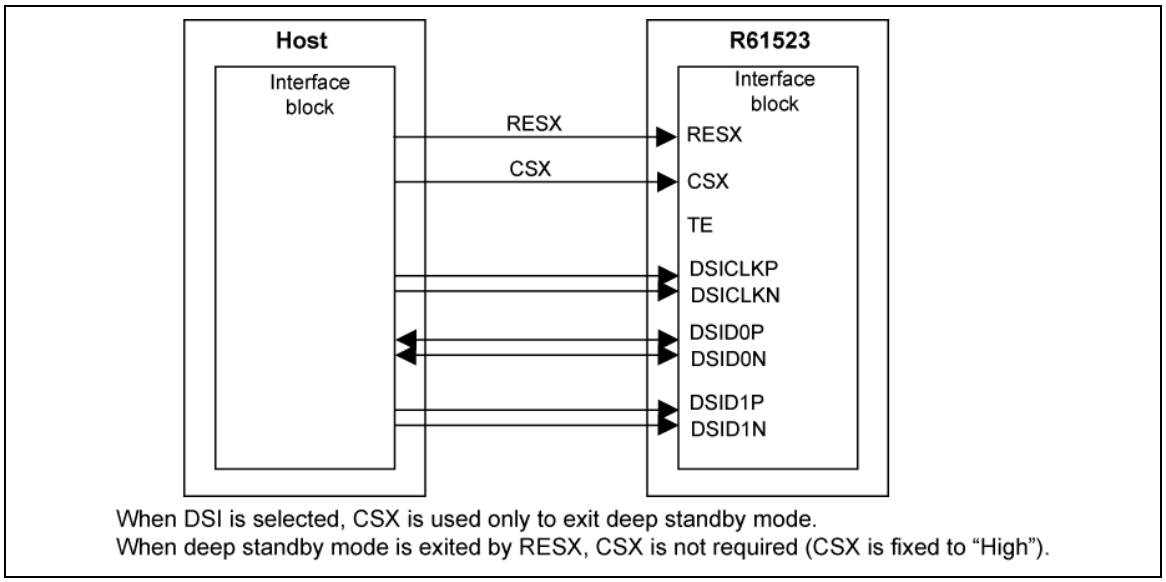


Figure 3

(3) Lane State Definition

Table 11 Lane State Description

State code	Line voltage levels		High speed	Low power	
	Dp-line	Dn-line	Burst mode	Control mode	Escape mode
HS-0	HS Low	HS High	Differential-0	1	1
HS-1	HS High	HS Low	Differential-1	1	1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	2

Notes: 1. During high-speed transmission, the low power receivers observe LP-00 on the lines.
2. If LP-11 occurs during Escape mode, the Lane returns to Stop state (Control mode LP-11).

(4) DSI-CLK Lane

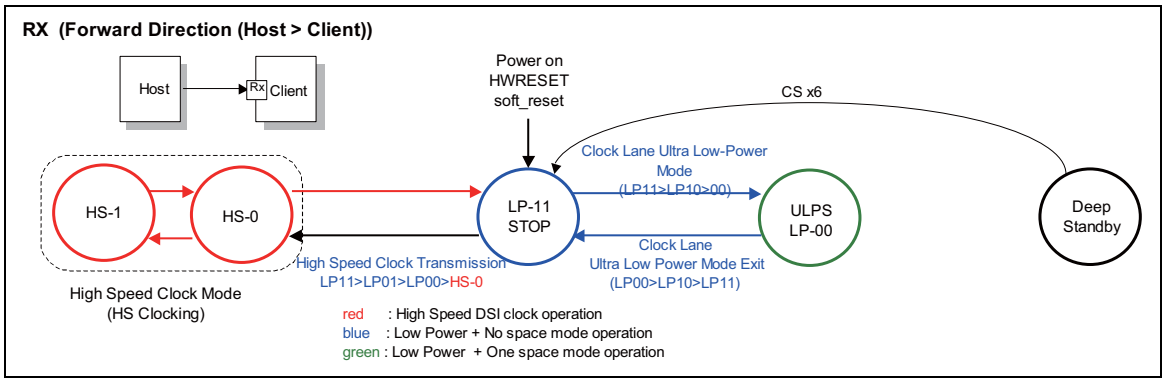


Figure 4 Clock Lane State Diagram

1) Low Power Mode (LP-11: STOP)

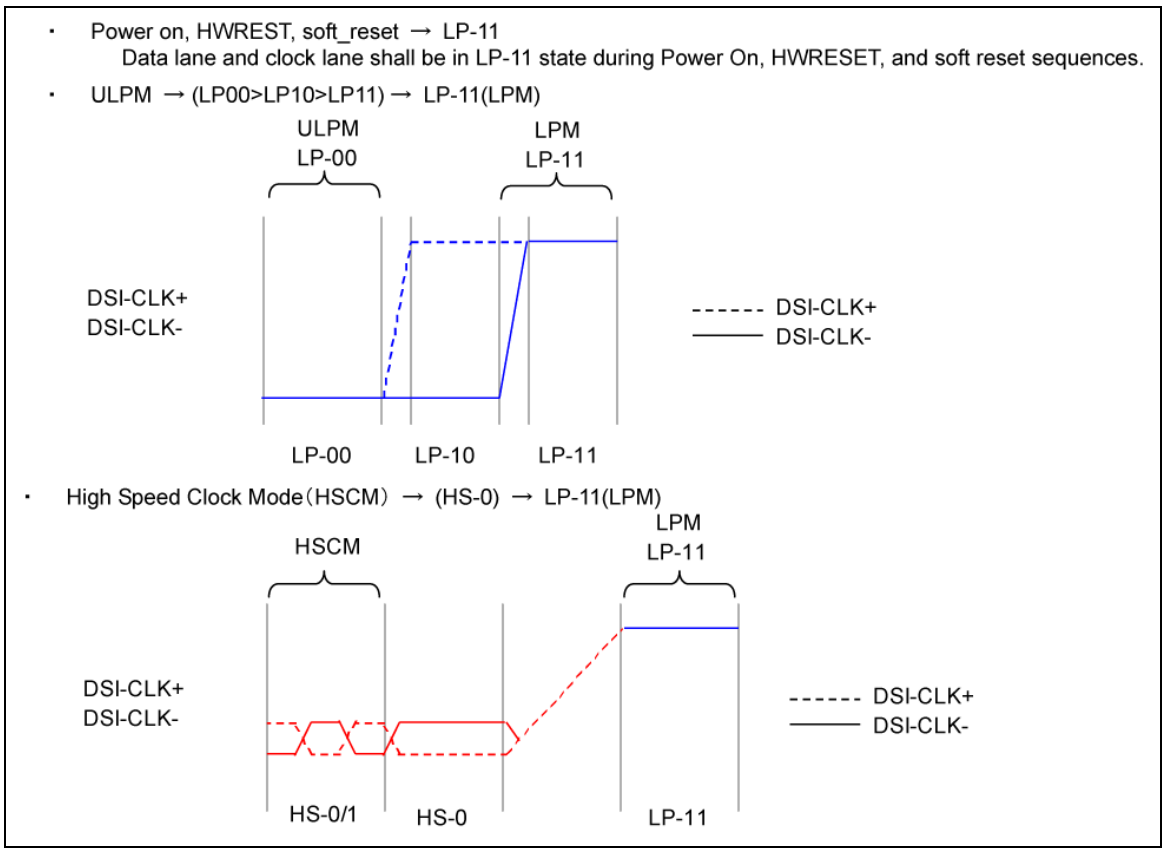


Figure 5 Switching the Clock Lane between Clock Transmission and Low Power Mode 1

2) Ultra Low Power Mode (LP-00: ULPM)

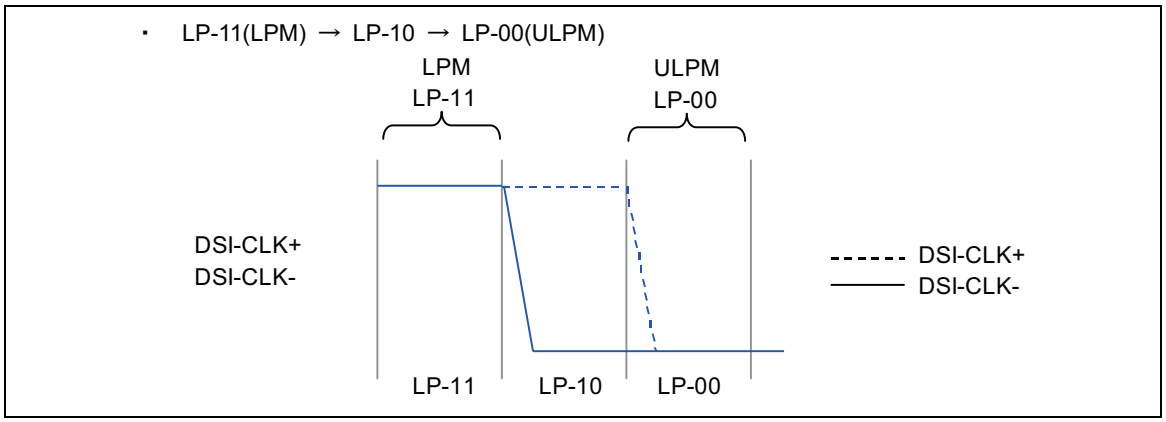


Figure 6 Switching the Clock Lane between Clock Transmission and Low Power Mode 2

3) High-Speed Clock Mode

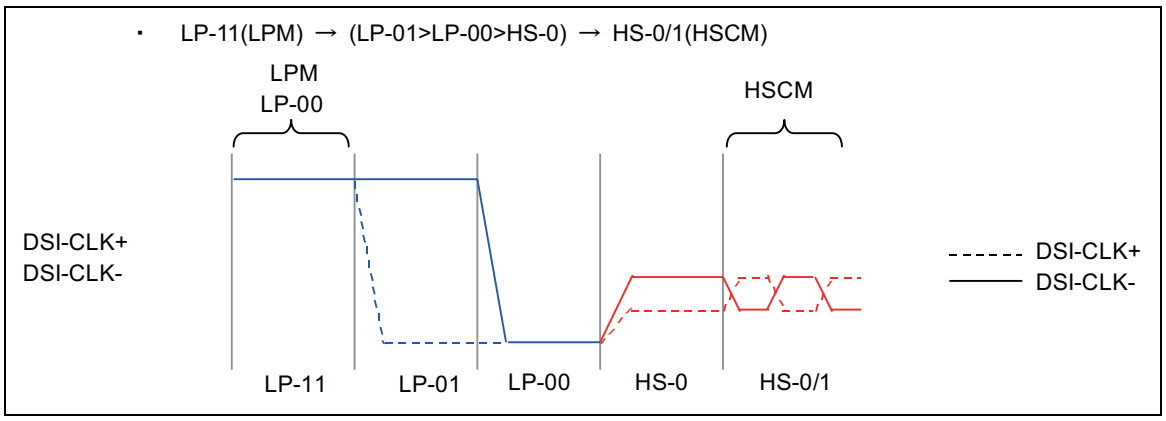


Figure 7 Switching the Clock Lane between Clock Transmission and Low Power Mode 3

4) High-Speed Clock Burst

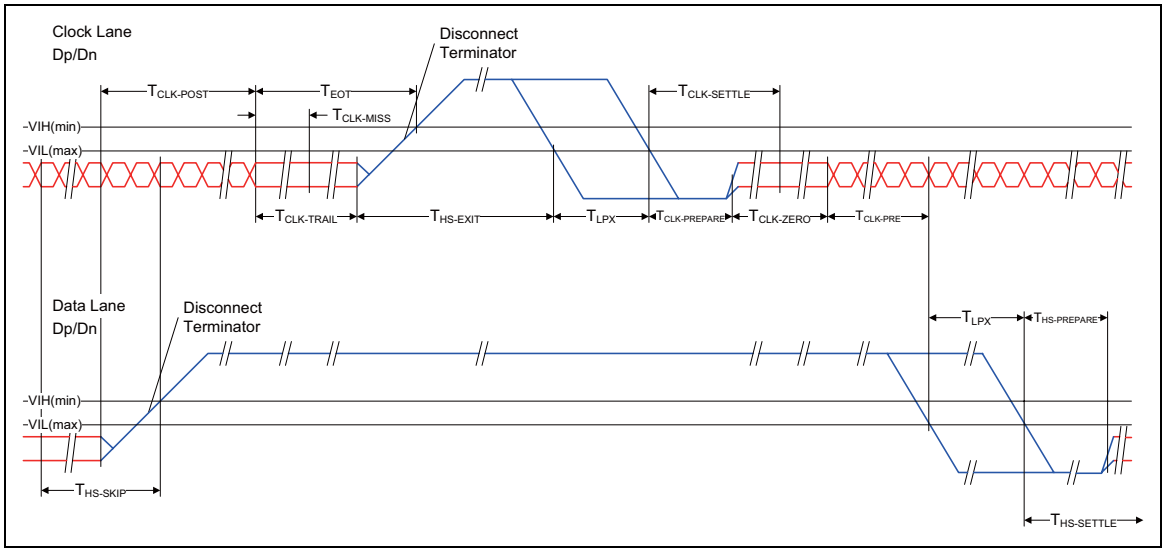


Figure 8 Switching the Clock Lane between Clock Transmission and Low Power Mode 4

(5) DSI-D0 Data Lane

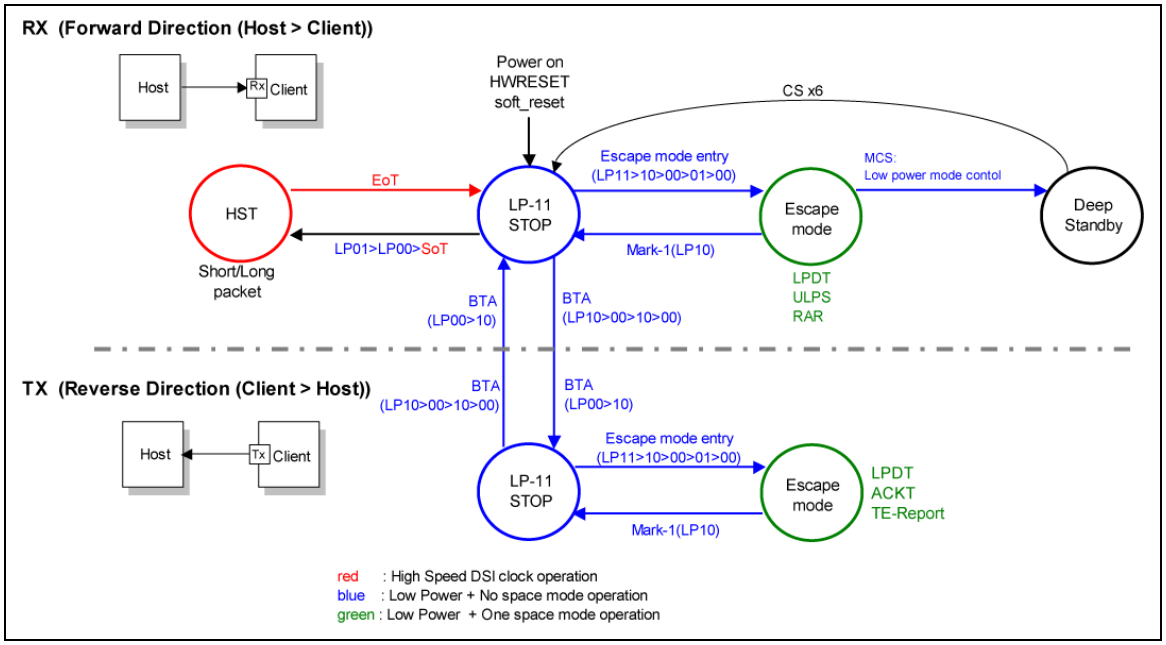


Figure 9 DSI-D0 Data Lane State Diagram

Table 12 Data Lane Operating Modes

No.	Description	Operation code	Note
1	High-Speed Data Transmission Burst	LP-11 > LP-01 > LP-00	
2	Escape mode entry	LP-11 > LP-10 > LP-00 > LP-01 > LP-00	
3	Turnaround	LP-11 > LP-10 > LP-00 > LP-10 > LP-00	1
4	Exit Escape mode(Mark-1)	LP-10	
5	Deep Standby Mode	DSTB=1	2
6	Exit Deep Standby Mode	CSX × 6	3

Notes: 1. Before Turnaround operation, DBI Packet must be sent.
2. DSTB must be sent by Escape mode in Sleep mode.
3. After exiting from the Deep Standby Mode, all of commands are reset.

1) Power On, HWREST, soft_reset → LP-11

Data lane and clock lane should be in LP-11 state during Power On, HWRESET, and soft_reset sequences.

2) Escape mode

- Escape mode entry
- Mark-1 (exit Escape mode)

Table 13 Escape Entry Code

No.	Symbol	Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)	R61523 implementation		Note
					LP-RX	LP-TX	
1	LPDT	Low Power Data Transmission	mode	1110_0001	Yes	Yes	
2	ULPS	Ultra-Low Power State	mode	0001_1110	Yes	No	
3	UDF1	Undefined-1	mode	1001_1111	No	No	
4	UDF2	Undefined-2	mode	1101_1110	No	No	
5	RAR	Remote Application Reset	Trigger	0110_0010	Yes	No	1
6	TER	TE-Report	Trigger	0101_1101	No	Yes	
7	ACKT	Unkown-4 (Acknowledge Trigger)	Trigger	0010_0001	No	Yes	
8	UNK5	Unknown-5	Trigger	1010_0000	No	No	

Note: DSI circuit is reset by Remote Application Reset.

3) Escape mode (Host>Client): Low Power Data Transmission (LPDT)

4) Escape mode (Host>Client): Ultra Low Power State (ULPS)

5) Escape mode (Host>Client): Remote Application Reset (RAR)

6) Escape mode (Client>Host): TE-Reporting (TER)

This supports TE-reporting function. The procedures are as follows:

- Host to Client: Send set_tear_on of DCS.
- Host to Client: Send BTA.
- Client to Host: Send Acknowledge Trigger.
- Client to Host: Send BTA.
- Host: Check Error Report.
- Host to Client: Send BTA.
- Client to Host: Send TE Report when TE occurred at the line of set_scan_line.
- Client to Host: Send BTA.
- Host to Client: Send image data by HST.

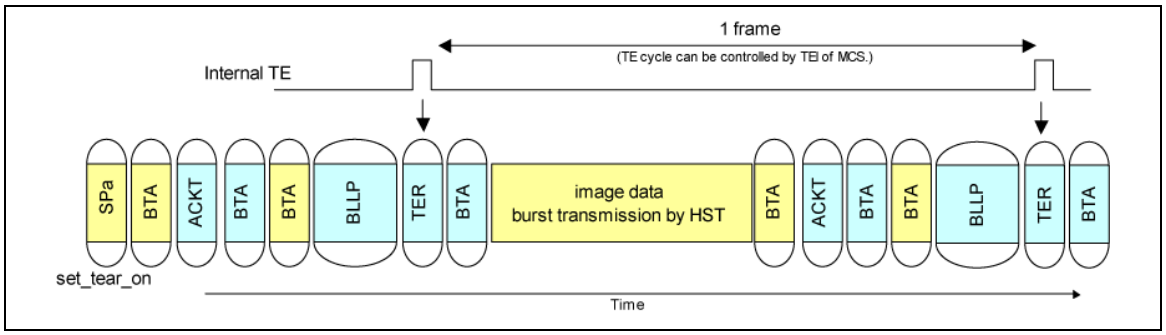


Figure 10

7) Escape mode (Client>Host): Acknowledge Trigger (ACKT)

8) High-Speed Data Transmission (HST)

9) Bus Turnaround (Host>Client) (BTA)

10) Bus Turnaround (Client>Host) (BTA)

(6) Packet Level Communication

1) Short Packet (SPa) Structure

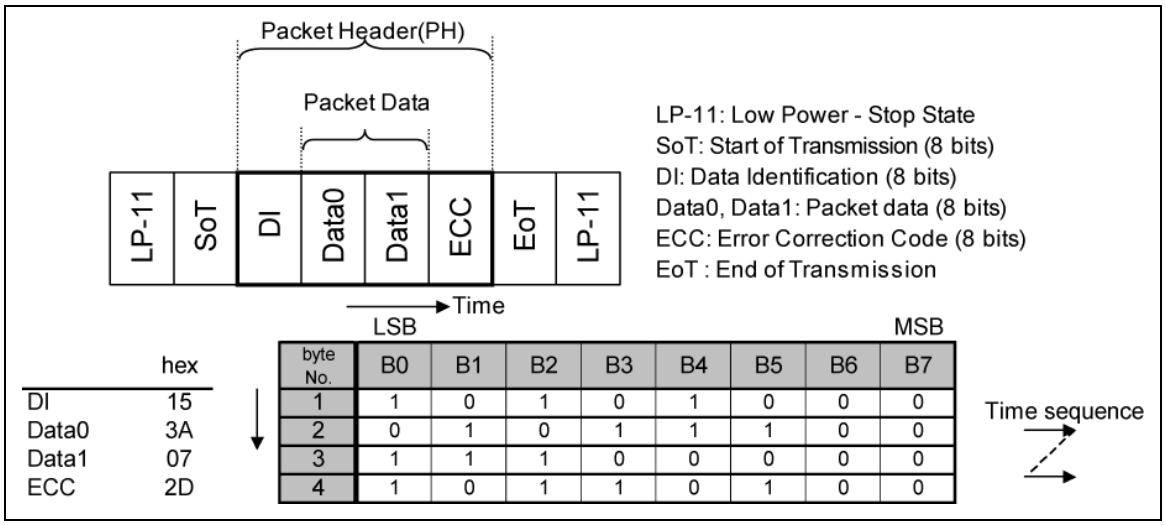


Figure 11 Example of Short Packet (SPa) (DCS WRITE, 1 Parameter)

2) Long Packet (LPa) Structure

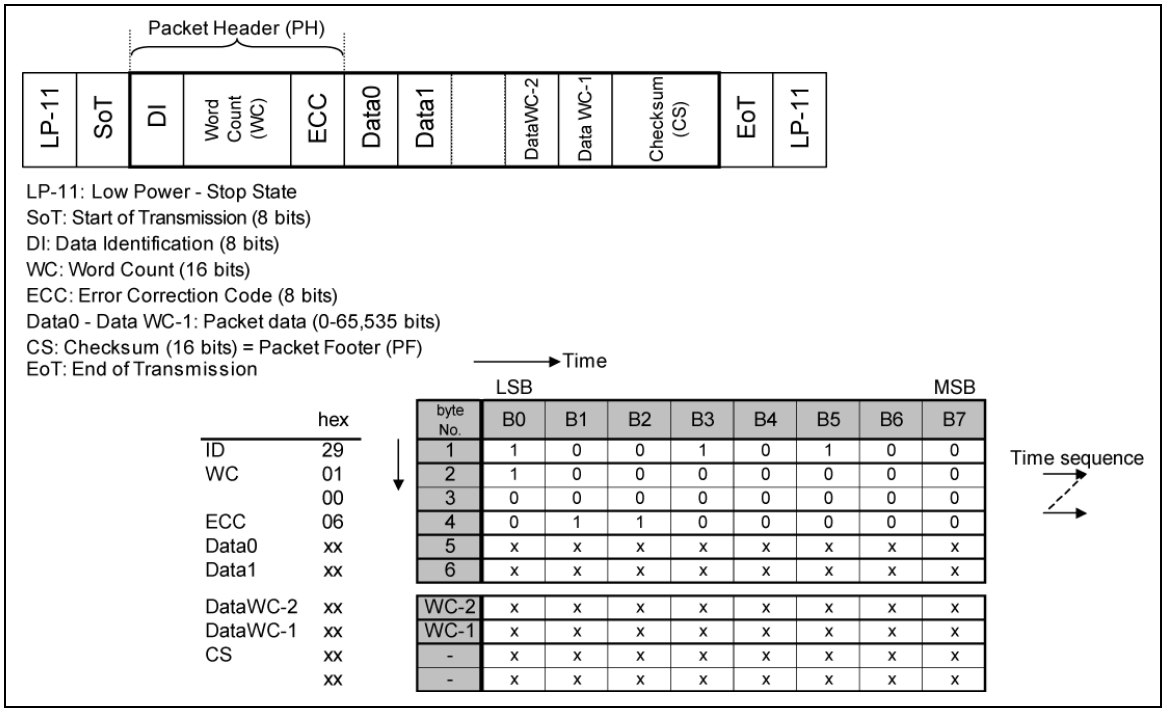


Figure 12

3) Multiple Packet Sending

In the LP-11 state, multiple Short Packets (SPa) and Long Packets (LPa) can be received between SoT and EoT.

LP-11 → SoT → SPa → SPa → EoT

LP-11 → SoT → SPa → LPa → EoT

LP-11 → SoT → LPa → LPa → EoT

LP-11 → SoT → LPa → SPa → EoT

LP-11 → SoT → Combination of the above methods → EoT

(7) Data Identification (DI)

1) Virtual Channel (VC)

The R61523 supports Virtual Channel only when VC = 00. Set VC = 00 during packet transmission. If a packet is received when VC is other than 00, the packet is regarded as invalid. This result is reflected on Error Report.

2) Data Type (DT)

If a Data Type not defined in MIPI DSI specification is received, the subsequent data cannot be received. Transmit data again after checking it is in the LP-11 state using Error Report. If a Data Type not supported in the R61523 is received, it is regarded as NOP, and the result is not reflected on Error Report.

Table 14

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
B7 (0)	B6 (0)	B5	B4	B3	B2	B1	B0

Table 15 R61523 Rx Data Type List

Data Type	Description	Packet size	DBI packet	DPI packet	R61523 (Rx) implementation	Note
01h	Sync Event, V Sync Start	Short		Yes	No	
11h	Sync Event, V Sync End	Short		Yes	No	
21h	Sync Event, H Sync Start	Short		Yes	No	
31h	Sync Event, H Sync End	Short		Yes	No	
08h	End of Transmission packet (EOT)	Short			Yes	
02h	Color Mode (CM) Off Command	Short		Yes	No	
12h	Color Mode (CM) On Command	Short		Yes	No	
22h	Shut Down Peripheral Command	Short		Yes	No	
32h	Turn On Peripheral Command	Short		Yes	No	
03h	Generic Short WRITE, no parameters	Short	Yes		No	
13h	Generic Short WRITE, 1 parameter	Short	Yes		Yes	1, 2
23h	Generic Short WRITE, 2 parameters	Short	Yes		Yes	1, 2
04h	Generic READ, no parameters	Short	Yes		No	
14h	Generic READ, 1 parameter	Short	Yes		Yes	
24h	Generic READ, 2 parameters	Short	Yes		Yes	1, 2
05h	DCS WRITE, no parameters	Short	Yes		Yes	1, 2
15h	DCS WRITE, 1 parameter	Short	Yes		Yes	1, 2
06h	DCS READ, no parameters	Short	Yes		Yes	1, 2
37h	Set Maximum Return Packet Size (default: 0001h)	Short	Yes		Yes	
09h	Null Packet, no data	Long			Yes	
19h	Blanking Packet, no data	Long		Yes	No	
29h	Generic Long Write	Long	Yes		Yes	
39h	DCS Long Write/Write_LUT Command Packet	Long	Yes		Yes	
0Eh	Packet Pixel Stream, 16-bit RGB, 5-6-5 Format	Long		Yes	No	
1Eh	Packet Pixel Stream, 18-bit RGB, 6-6-6 Format	Long		Yes	No	
2Eh	Loosely Packet Pixel Stream, 24-bit RGB, 8-8-8 Format	Long		Yes	No	
3Eh	Packet Pixel Stream, 24-bit RGB, 8-8-8 Format	Long		Yes	No	
Other	All unspecified codes are reserved.				-	

Table 16 R61523 LP-Tx Data Type List

Data Type	Description	Packet size	R61523 (LP-Tx) implementation	Note
00h-01h	Reserved	-	-	
02h	Acknowledge with Error Report	Short	Yes	
03h-07h	Reserved	-	-	
08h	End of Transmission packet (EoT)	Short	No	3
09h-10h	Reserved	-	-	
11h	Generic Short READ Response, 1 byte returned	Short	Yes	
12h	Generic Short READ Response, 2 bytes returned	Short	Yes	
13h-18h	Reserved	-	-	
1Ah	Generic Long READ Response	Long	Yes	
1Bh	Reserved	-	-	
1Ch	DCS Long READ Response	Long	Yes	
1Dh-20h	Reserved	-	-	
21h	DCS Short READ Response, 1 byte returned	Short	Yes	
22h	DCS Short READ Response, 2 bytes returned	Short	Yes	
23h-28h	Reserved	-	-	
29h-3Fh	Reserved	-	-	

Notes: 1. Generic Command is Manufacturer Command. DCS Command is User Command.

2. Generic XXX 1 parameter is Manufacturer Command + 1 byte (all “0”). Generic XXX 2 parameter is Manufacturer Command + 1 parameter. DCS XXX no parameter is User Command + 1 byte (all “0”). DCS XXX 1 parameter is User Command + 1 parameter.

3. Defined in MIPI DSI (p.48) (used for HS transmission).

(8) Word Count (WC) on Long Packet (LPa)

Word Count (WC) = 2 bytes: The number of packet data on Long Packet (0 to 65,535 bytes)

(9) Error Correction Code (ECC)

ECC detects 1-bit errors or multiple-bit errors in each Packet Header. ECC is performed on the following:

- Short Packet: DI, Data0, Data1, and ECC
- Long Packet: DI, WC (2 bytes), and ECC

(10) Packet Data (PD) – Pixel Data Format on Long Packet

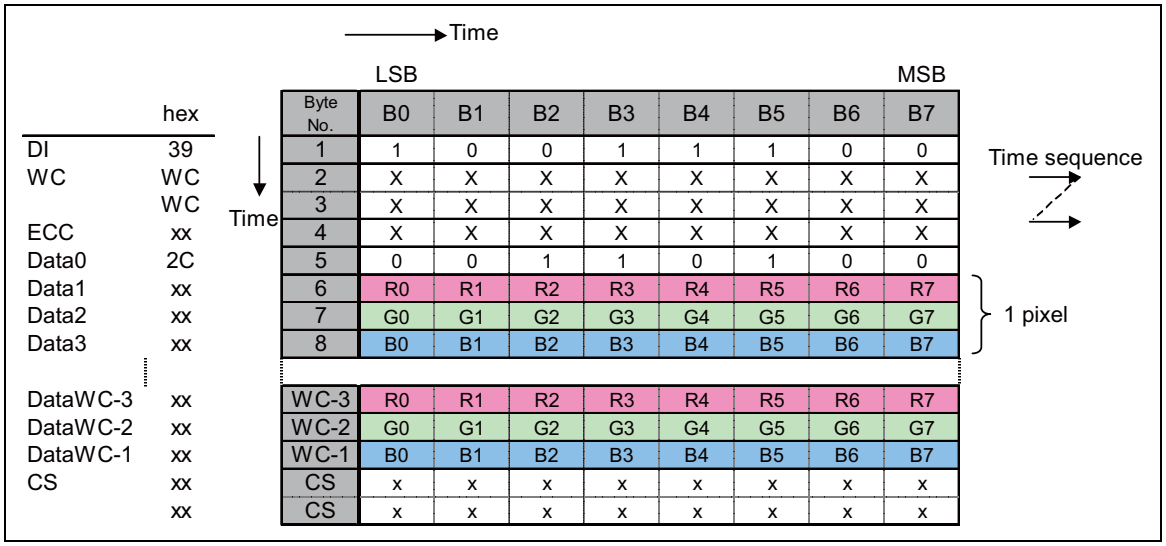


Figure 13 24bpp Pixel Data Format on Long Packet (set_pixel_format (3Ah): D[2:0] = 111)

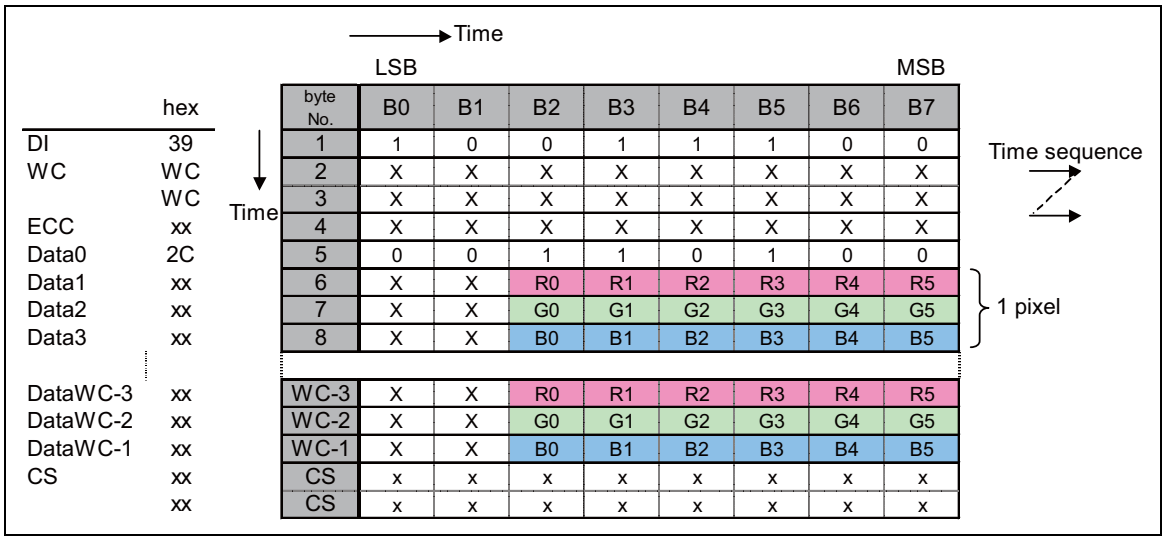


Figure 14 18bpp Pixel Data Format on Long Packet (set_pixel_format (3Ah): D[2:0] = 110)

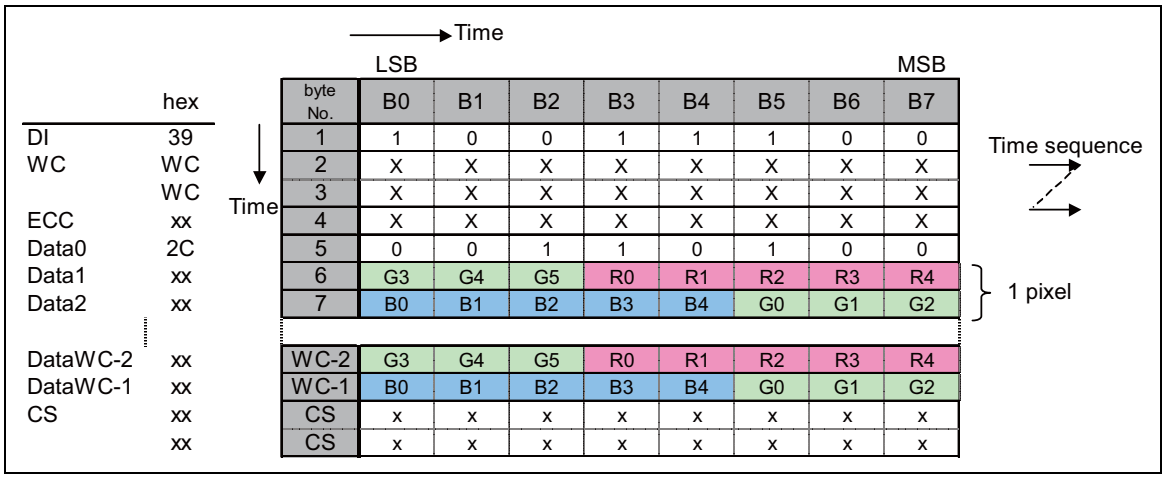


Figure 15 16bpp Pixel Data Format on Long Packet (set_pixel_format (3Ah): D[2:0] = 101)

(11) Packet Footer on Long Packet (LPa)

In Long Packet, Packet Footer is added next to Packet Data. Packet footer includes CRC calculated from Packet Data as checksum.

Checksum (2 bytes) = CRC (Packet Data): CRC = $X^{16} + X^{12} + X^5 + X^0$

(12) Acknowledge with Error Report (AwER)

Table 17

Bit	Description	R61523 implementation	Note
0	SoT Error	Yes	1
1	SoT Sync Error	Yes	1
2	EoT Sync Error	Yes	1
3	Escape Mode Entry Command Error	Yes	1
4	Low Power Transmit Sync Error	Yes	1
5	HS Receive Timeout Error	Yes	1
6	False Control Error	Yes	1
7	Reserved	-	
8	ECC Error, single-bit (detected, and corrected)	Yes	
9	ECC Error, multi-bit (detected, not corrected)	Yes	
10	Checksum Error (Long packet only)	Yes	
11	DSI Data Type Not Recognized	Yes	
12	DSI VC ID Invalid	Yes	
13	Invalid Transmission Length	Yes	1
14	Reserved	-	
15	DSI Protocol Violation	Yes	1

Note 1: Detailed error report condition is defined by R61523 (based on MIPI description).

(13) DCS, MCS, and Data Type List

The following table shows the available data type of each command (DCS and MCS).

Table 18 DCS and Data Type List

			Host to R61523 Data Type (RX)									
DCS Command/Parameter		W/R	Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
			DCS no para	DCS 1 para	DCS -	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set maximum return packet size
00h	nop	C	Yes	No	Yes	No	No	No	No	No	No	-
01h	soft_reset	C	Yes	No	Yes	No	No	No	No	No	No	-
04h	read_DDB_starrt	5	No	No	No	No	No	No	No	No	Yes	16'h5
0Ah	get_power_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Bh	get_address_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Ch	get_pixel_format	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Dh	get_display_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Eh	get_signal_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Fh	get_diagnostic_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
10h	enter_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
11h	exit_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
12h	enter_partial_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
13h	enter_normal_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
28h	set_display_off	C	Yes	No	Yes	No	No	No	No	No	No	-
29h	set_display_on	C	Yes	No	Yes	No	No	No	No	No	No	-
2Ah	set_column_address	4	No	No	Yes	No	No	No	No	No	No	-
2Bh	set_page_address	4	No	No	Yes	No	No	No	No	No	No	-
2Ch	write_memory_start	N	No	No	Yes	No	No	No	No	No	No	-
2Eh	read_memory_start (type 1, 2)	N	No	No	No	No	No	No	No	No	Yes	N byte
30h	set_partial_area	4	No	No	Yes	No	No	No	No	No	No	-
34h	set_tear_off (type 1)	C	Yes	No	Yes	No	No	No	No	No	No	-
35h	set_tear_on (type 1)	1	No	Yes	Yes	No	No	No	No	No	No	-
36h	set_address_mode	1	No	Yes	Yes	No	No	No	No	No	No	-
38h	exit_idle_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
39h	enter_idle_mode	C	Yes	No	Yes	No	No	No	No	No	No	-

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Table 19 DCS and Data Type List (continued)

DCS Command/Parameter		W/R	Host to R61523 Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
			DCS no para	DCS 1 para	DCS -	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set maximum return packet size
3Ah	set_pixel_format	1	No	Yes	Yes	No	No	No	No	No	No	-
3Ch	write_memory_continue	N	No	No	Yes	No	No	No	No	No	No	-
3Eh	read_memory_continue	N	No	No	No	No	No	No	No	No	Yes	N byte
44h	set_tear_scanline	2	No	Yes	Yes	No	No	No	No	No	No	-
45h	get_scanline	2	No	No	No	No	No	No	No	No	Yes	16'h2
A1h	read_DDB_start	5	No	No	No	No	No	No	No	No	Yes	16'h5
A8h	read_DDB_continue	N	No	No	No	No	No	No	No	No	Yes	16'h5

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Table 20 MCS and Data Type List

MCS Command/Parameter		W/R	Host to R61523 Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
			DCS no para	DCS 1 para	DCS -	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set maximum return packet size
B0h	Manufacturer Command Access Packet	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B1h	Low Power Mode Control	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B3h	Frame Memory Access and Interface Setting	2	No	No	No	No	No	Yes	Yes	No	No	16'h2
B5h	Read Checksum and ECC Error Counter	3	No	No	No	No	No	No	Yes	No	No	16'h3
B6h	DSI Control	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B8h	Backlight Control 1	15	No	No	No	No	No	Yes	Yes	No	No	16'hF
B9h	Backlight Control 2	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
BAh	Backlight Control 3	1	No	No	No	No	No	No	Yes	No	No	16'h1
BFh	Device Code Read	5	No	No	No	No	No	No	Yes	No	No	16'h5
C0h	Panel Driving Setting	7	No	No	No	No	No	Yes	Yes	No	No	16'h7
C1h	Display Timing Setting for Normal/Partial Mode	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
C3h	Display Timing Setting for Idle Mode	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
C4h	Source/VCOM/Gate Driving Timing Setting	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
C8h	Gamma Set A	18	No	No	No	No	No	Yes	Yes	No	No	16'h12
C9h	Gamma Set B	18	No	No	No	No	No	Yes	Yes	No	No	16'h12
CAh	Gamma Set C	18	No	No	No	No	No	Yes	Yes	No	No	16'h12
D0h	Power Setting for Common	10	No	No	No	No	No	Yes	Yes	No	No	16'hA
D1h	VCOM Setting	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
D2h	Power Setting for Normal/Partial Mode	3	No	No	No	No	No	Yes	Yes	No	No	16'h3
D4h	Power Setting for Idle Mode	3	No	No	No	No	No	Yes	Yes	No	No	16'h3
D6h	Test Mode	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
D7h	Test Mode	12	No	No	No	No	No	Yes	Yes	No	No	16'hC
D9h	Test Mode	2	No	No	No	No	No	Yes	Yes	No	No	16'h2

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Table 21 MCS and Data Type List (Continued)

MCS Command/Parameter		W/R	Host to R61523 Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
			DCS no para	DCS 1 para	DCS -	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set maximum return packet size
E0h	NVM Access Control	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
E1h	set_DDB_write Control	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
E2h	Frame Memory Access and Interface Setting	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
E3h	Read Checksum and ECC Error Counter	12	No	No	No	No	No	Yes	Yes	No	No	16'hC
E4h	DSI Control	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
E5h	Backlight Control 1	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
E6h	Backlight Control 2	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
F3h	Backlight Control 3	2	No	No	No	No	No	Yes	Yes	No	No	16'h2
FAh	Device Code Read	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
FCh	Test Mode	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
FDh	Test Mode	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
FEh	Test Mode	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
FFh	Reserved	-	No	No	No	No	No	No	No	No	No	-

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

System Interface Configuration (MIPI-DBI)

DBI Type B

The R61523 adopts 16-/8-bit bus display command interface to interface to high-performance host processor at high speed. The R61523 starts internal processing after storing control information of externally sent 16-/8-bit data in the command register (CDR) and the parameter register (PR). Since the internal operation of the R61523 is determined by signals sent from the host processor, command/parameter signal, read/write status signal (RDX/WRX), and internal 16-bit data bus signals (DB[15:0]) are called command.

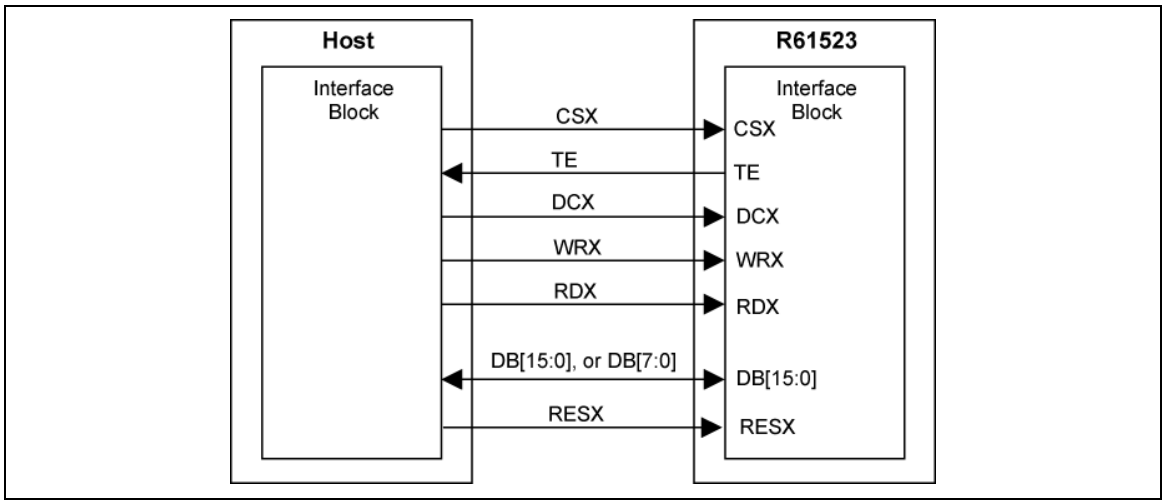


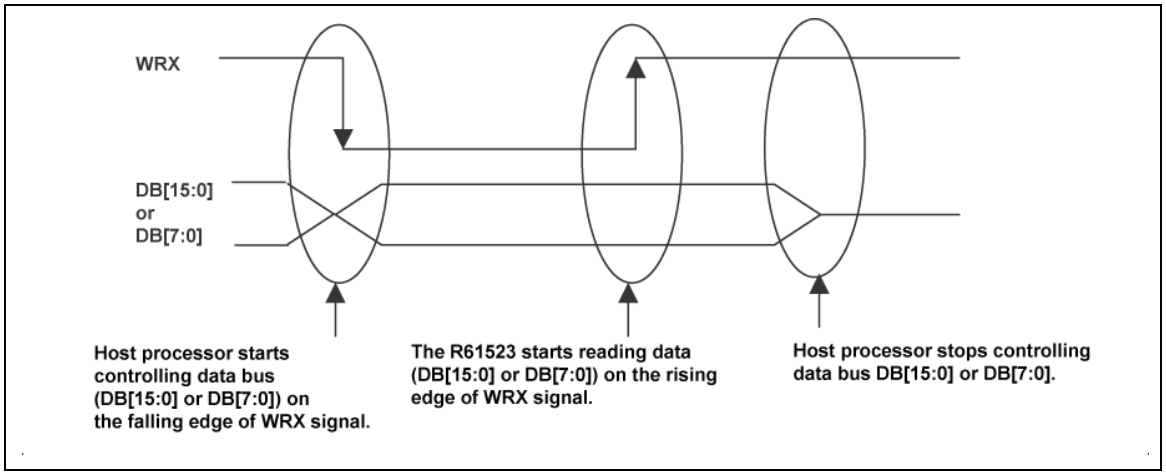
Figure 16 Example: DBI Type B

Write Cycle Sequence

In the write cycle, data and/or command are written to the R61523 via the interface between the R61523 and the host processor. Each step of write cycle sequence (WRX high, WRX low, WRX high) comprises three control signals (DCX, RDX, WRX) and 16(DB[15:0])-bit data. The DCX bit indicates a signal that is used to select command or data sent on the data bus.

When DCX=”1”, data on DB[15:0] is image data or command parameter. When DCX = 0, data on DB[7:0] are command.

Setting RDX and WRX to “Low” simultaneously is prohibited. See the figure below for the write cycle sequence.



Note: WRX is not a synchronous signal (can be halted).

Figure 17 Write Cycle Sequence

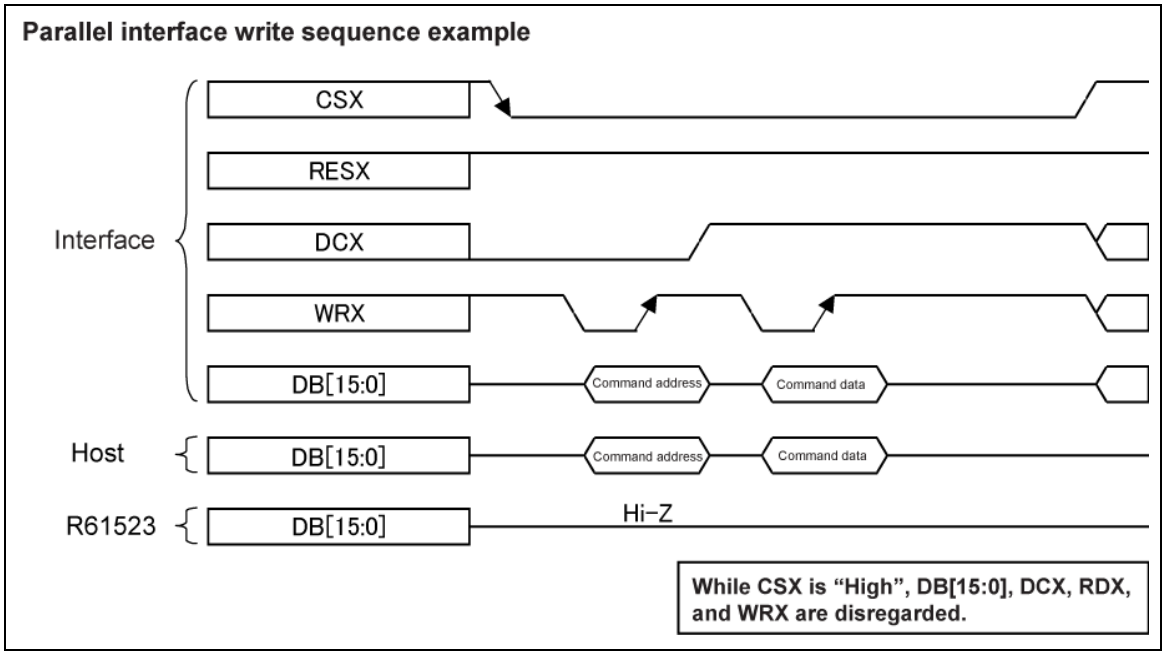
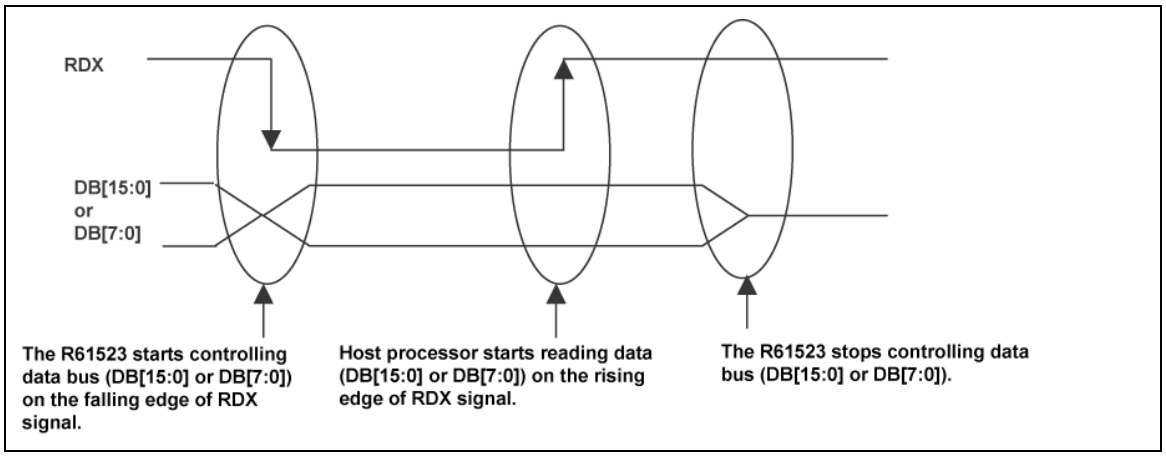


Figure 18

Read Cycle Sequence

In the read cycle, data and/or commands are read from the R61523 via the interface between the R61523 and the host processor. The data (DB[15:0] or [7:0]) are transmitted from the R61523 to the host processor on the falling edge of RDX. The host processor reads the data on the rising edge of RDX. Setting RDX and WRX to Low simultaneously is prohibited. See below for the read cycle sequence.



Note: RDX is not a synchronous signal (can be halted).

Figure 19

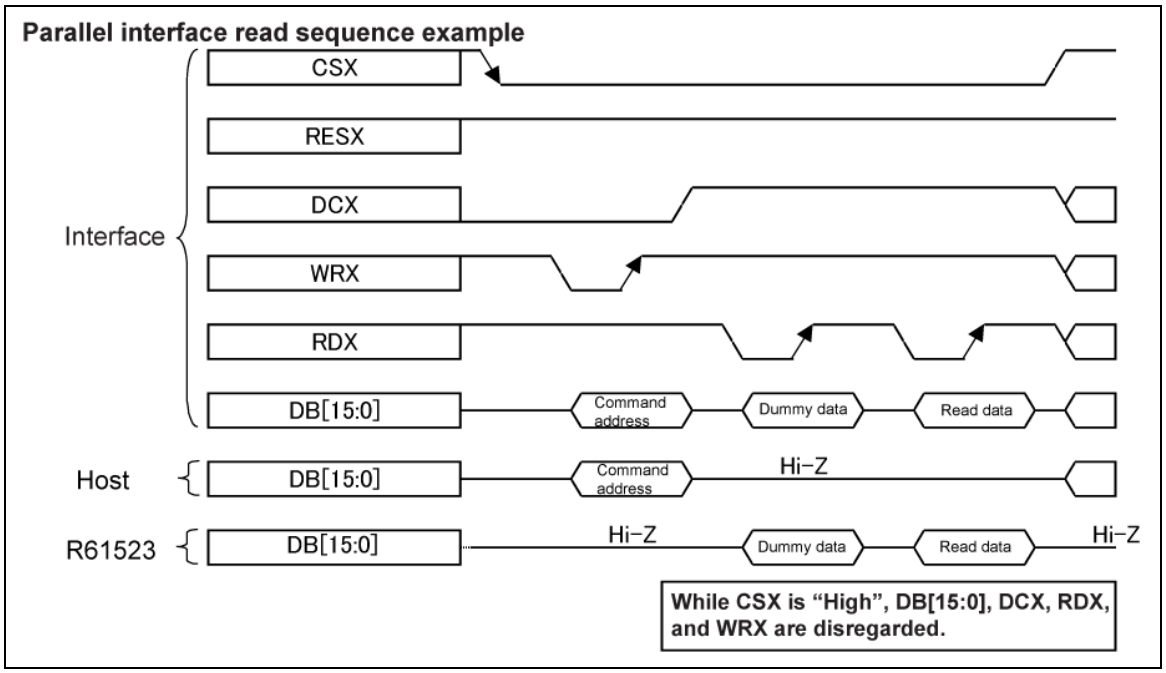


Figure 20

Data Transfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the R61523, the command parameters sent to the R61523 before a break occurs are stored in the register of the R61523 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the R61523. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when a break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

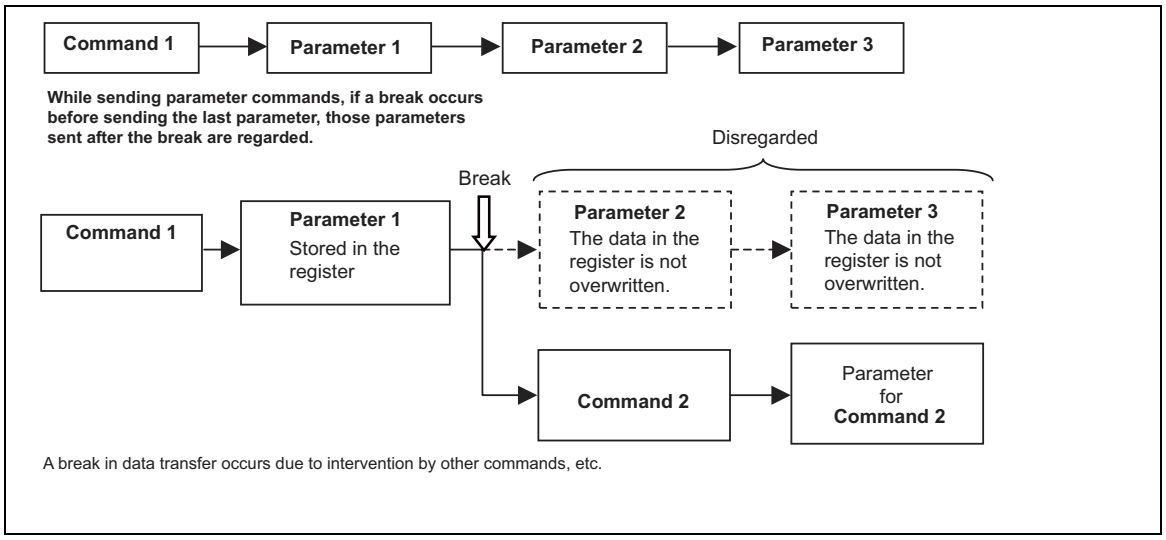


Figure 21

Note: A break occurs, for example, when another command is input.

Data Transfer Pause (Command/Pause/Command)

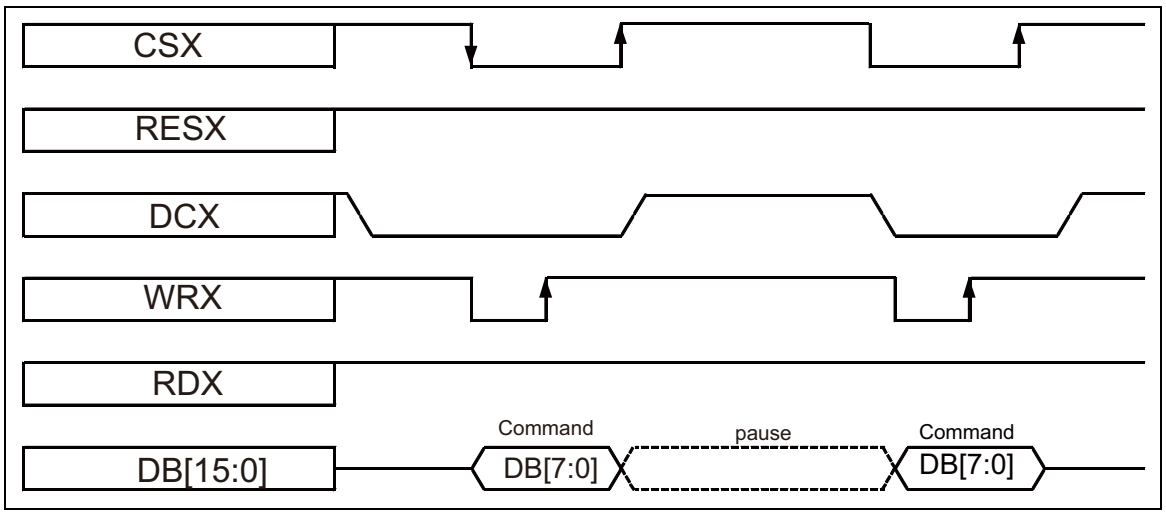


Figure 22

Data Transfer Pause (Command/Pause/Parameter)

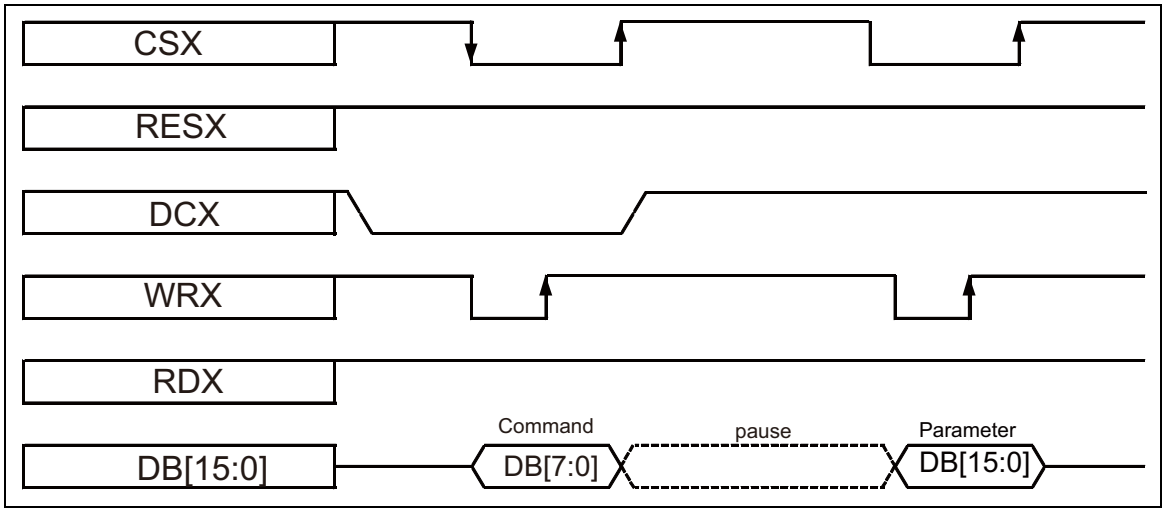


Figure 23

Data Transfer Pause (Parameter/Pause/Command)

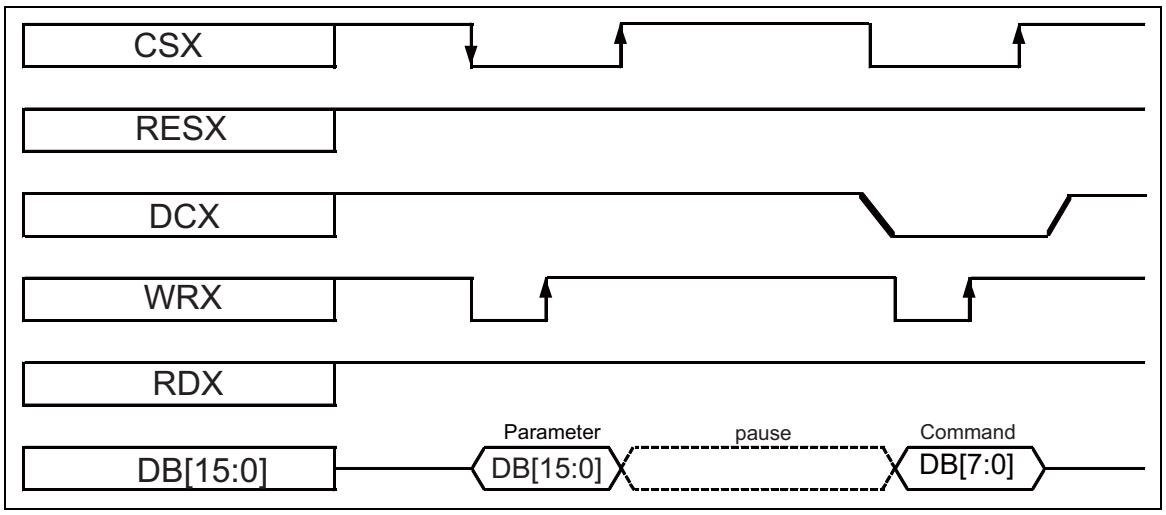


Figure 24

Data Transfer Pause (Parameter/Pause/Parameter)

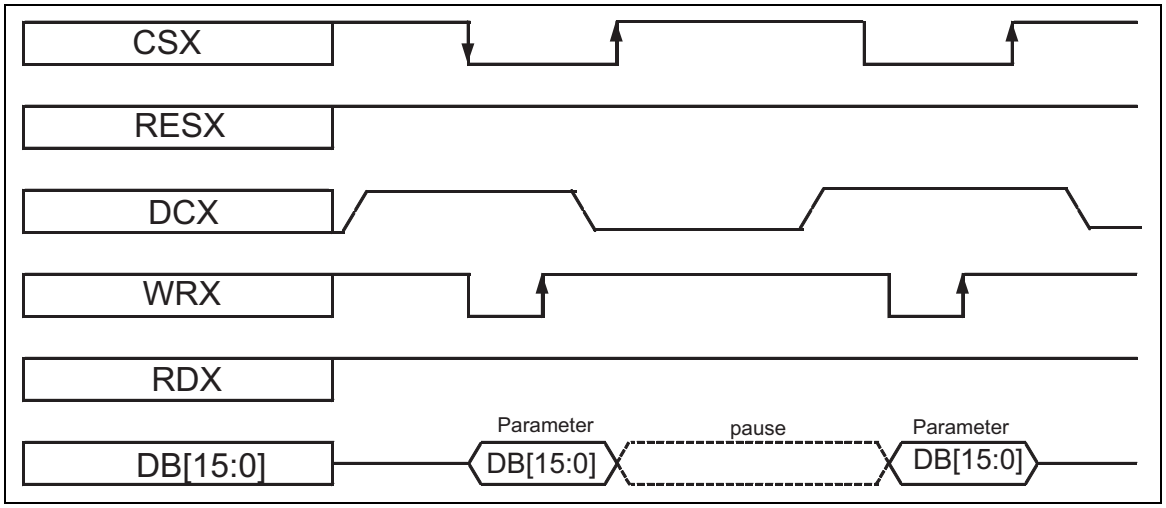


Figure 25

Data Transfer Mode

Two methods are available for writing data to the frame memory in the R61523.

(1) Write Method 1 (Default)

One frame of image data is written to the frame memory. If over one frame of data is transmitted, all the data is disregarded. The write operation of the data to the frame memory is terminated when a command intervenes in the middle of the course. The R61523 writes the image data to the next frame when write_memory_start command (2Ch) is written. Set WEMODE = 0 (Frame Memory Access and Interface Setting (B3h)).

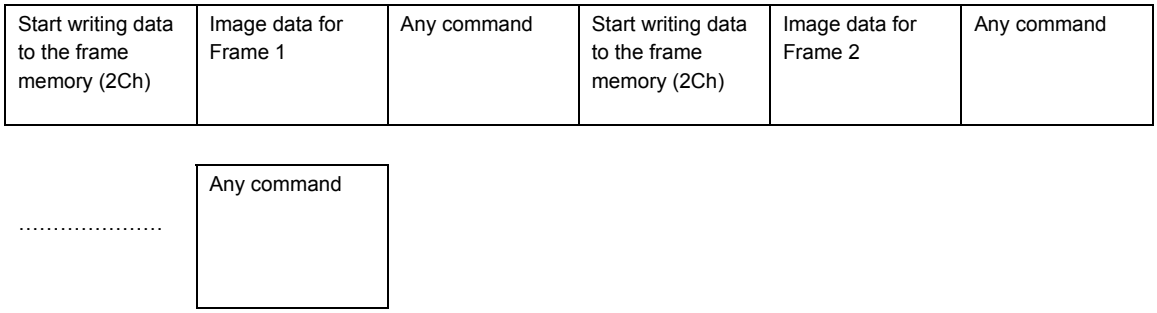


Figure 26

(2) Write Method 2

The image data are written consecutively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE =1 (Frame Memory Access and Interface setting (B3h)).

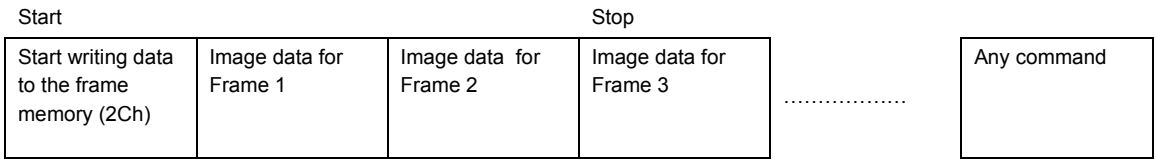


Figure 27

Notes: 1. Two write methods are available for all data transfer color modes in 16-/8-bit bus display command interface.
2. The number of pixels in one frame can be odd or even in both download methods. Only complete data sets are retained in the frame memory.
3. The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue (3Ch) is executed, the write operation can be started again from the address where the write operation is halted.

DBI Data Format

The R61523 supports color formats shown in the table below. At least one color format is supported by each of Type B 16-bit and DSI.

Table 22

Type	IM2-0	Data pin	Color format	MIPI Spec.	R61523
Type B	000	Setting inhibited	-	-	-
	010	DB[15:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp (262,144-color Option1)	Yes	Yes
			18bpp (262,144-color Option2)	Yes	Yes
			18bpp (262,144-color Option 3)	No	Yes
			24bpp (16,777,216-color Option1)	Yes	Yes
			24bpp (16,777,216-color Option2)	Yes	Yes
	001	Setting inhibited	-	-	-
	011	DB[7:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp	Yes	Yes
			24bpp	Yes	Yes
DSI	100	D0+/-, D1+/-	3bpp	Yes	No
			8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp	Yes	Yes
			24bpp	Yes	Yes

Yes: Supported

No: Unsupported

■DBI Type B Data Forma

●Data Format for 16-Bit Interface (DB[15:0] is used. IM[2:0]=010)

	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*									D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission															
	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	0	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
18bpp Frame Memory Write option1	3'h6	0	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]			G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]		
option2		1									R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		
option3		2	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]
24bpp Frame Memory Write option1	3'h7	0	R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
option2		1									R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]
24bpp Frame Memory Read	*	0	r1[7]	r1[6]	r1[5]	r1[4]	r1[3]	r1[2]	r1[1]	r1[0]	g1[7]	g1[6]	g1[5]	g1[4]	g1[3]	g1[2]	g1[1]	g1[0]
		1									r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]

			Second Transmission															
	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	0																
18bpp Frame Memory Write option1	3'h6	0	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]			R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]		
option2		1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
option3		2	B[1]	B[0]														
24bpp Frame Memory Write option1	3'h7	0	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	R2[7]	R2[6]	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]
option2		1	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
24bpp Frame Memory Read	*	0	b1[7]	b1[6]	b1[5]	b1[4]	b1[3]	b1[2]	b1[1]	b1[0]	r2[7]	r2[6]	r2[5]	r2[4]	r2[3]	r2[2]	r2[1]	r2[0]
		1	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

			Third Transmission															
	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	0																
18bpp Frame Memory Write option1	3'h6	0	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]			B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]		
option2		1																
option3		2																
24bpp Frame Memory Write option1	3'h7	0	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]
option2		1																
24bpp Frame Memory Read	*	0	g2[7]	g2[6]	g2[5]	g2[4]	g2[3]	g2[2]	g2[1]	g2[0]	b2[7]	b2[6]	b2[5]	b2[4]	b2[3]	b2[2]	b2[1]	b2[0]
		1																

●Data Format for 8-Bit Interface (DB[7:0] is used. IM[2:0]=011)

	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	0	D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	0	D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission								Second Transmission								Third Transmission							
	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	0	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]								
18bpp Frame Memory Write	3'h6	0	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
24bpp Frame Memory Write	3'h7	0	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	0	r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

●Extended Format for 24bpp Data

		Frame Memory Data (24bpp)																							
set_pixel_format	EPF	r7	r6	r5	r4	r3	r2	r1	r0	g7	g6	g5	g4	g3	g2	g1	g0	b7	b6	b5	b4	b3	b2	b1	b0
24bpp	*	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18bpp	2'h0	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
	2'h1	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
	2'h2	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[4]	B[3]	B[2]	B[1]	B[0]	0	0	0
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[4]	B[3]	B[2]	B[1]	B[0]	1	1	1
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	R[3]	R[2]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]	B[3]	B[2]

R[5:0], B[5:0] = 6'h3F → r[7:0], b[7:0] = 8'hFF, G[5:0] = 6'h3F → g[7:0] = 8'hFF,
R[5:0], B[5:0] = 6'h00 → r[7:0], b[7:0] = 8'h00, G[5:0] =6'h00 → g[7:0] = 8'h00

R[4:0], B[4:0] = 5'h1F → r[7:0], b[7:0] = 8'hFF, G[5:0] = 6'h3F → g[7:0] = 8'hFF,
R[4:0], B[4:0] = 5'h00 → r[7:0], b[7:0] = 8'h00, G[5:0] =6'h00 → g[7:0] = 8'h00

Note 1: The first Command Parameter Read and Frame Memory Read after read command is issued are invalid (dummy read).
Note 2: Data are written to the Frame Memory when data for one pixel are input. In 2-pixel 3- transfer operation (16-bit I/F 18bpp Option1), the first and second pixels are written in the 2nd and 3rd transfers respectively.
Note 3: If data transfer stops after 2nd transfer in 2-pixel 3-transfer operation, the first pixel data are written normally. This applies to the last address when number of pixel is odd according to window setting.
Note 4: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

BGR Register Setting and Write/Read Data in Frame Memory

System interface outputs write and read data in the same RGB order regardless of BGR register setting.

Example: 16-Bit Interface

●BGR=0

	First Transmission																Second Transmission								
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7-0
Write Data	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	*

↓

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Frame Memory	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

↓

	First Transmission																Second Transmission								
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7-0
Read Data	r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	*

●BGR=1

	First Transmission																Second Transmission								
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7-0
Write Data	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	*

↓

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Frame Memory	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]

↓

	First Transmission																Second Transmission								
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7-0
Read Data	r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	*

Command List

(1) User Command

Table 23 User Command

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number of Parameter	MIPI DCS Type1 Requirement	R61523 Implementation	Note
00h	nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
04h	read_DDB_start	R	5	No	Yes	
06h	get_red_channel	R	1	No	No	
07h	get_green_channel	R	1	No	No	
08h	get_blue_channel	R	1	No	No	
0Ah	get_power_mode	R	1	Yes	Yes	
0Bh	get_address_mode	R	1	Yes (Bit7-0)	Yes	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes	1
0Eh	get_signal_mode	R	1	Yes	Yes	
0Fh	get_diagnostic _result	R	1	Bit7/6: Yes Bit5/4: Optional	Yes (Bit6 Only)	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	Yes	Yes	
13h	enter_normal_mode	C	0	Yes	Yes	
20h	exit_invert_mode	C	0	Yes	No	
21h	enter_invert_mode	C	0	Yes	No	
26h	set_gamma_curve	W	1	Yes	No	1
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_address	W	4	Yes	Yes	
2Bh	set_page_address	W	4	Yes	Yes	

Table 24 User Command (Continued)

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number of Parameter	MIPI DCS Type1 Requirement	R61523 Implementation	Note
2Ch	write_memory_start	W	Variable	Yes	Yes	2
2Dh	wite_LUT	W	Variable	Optional	No	
2Eh	read_memory_start	R	Variable	Yes	Yes	2
30h	set_partial_area	W	4	Yes	Yes	
33h	set_scroll_area	W	6	Yes	No	
34h	set_tear_off	C	0	Yes	Yes	
35h	set_tear_on	W	1	Yes	Yes	
36h	set_address_mode	W	1	Yes (Bit7-0)	Yes	
37h	set_scroll_start	W	2	Yes	No	
38h	exit_idle_mode	C	0	Yes	Yes	
39h	enter_idle_mode	C	0	Yes	Yes	
3Ah	set_pixel_format	W	1	Yes	Yes	
3Ch	write_memory _continue	W	Variable	Yes	Yes	2
3Eh	read_memory _continue	R	Variable	Yes	Yes	2
44h	set_tear_scanline	W	2	Yes	Yes	
45h	get_scanline	R	2	Yes	Yes	
A1h	read_DDB_start	R	5	Yes	Yes	
A8h	read_DDB_continue	R	Variable	Yes	Yes	

Notes: 1. The R61523 supports one type of gamma curve specified by gamma adjustment register GC0. Therefore, D [2:0] bits (get_display_mode, 0Dh) are fixed at 0.

2. See “DBI Data Format” for details on data write to the frame memory and data read from the frame memory.

(2) Manufacturer Command

Table 25 Manufacturer Command

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number of Parameter	Category
B0h	Manufacturer Command Access Protect	W/R	1	Additional User Command
B1h	Low Power Mode Control	W/R	1	Additional User Command
B3h	Frame Memory Access and Interface Setting	W/R	2	Additional User Command
B5h	Read Checksum and ECC Error Count	R	3	
B6h	DSI Control	W/R	1	
B8h	Backlight Control 1	W/R	15	
B9h	Backlight Control 2	W/R	4	
BAh	Backlight Control 3	R	1	
BFh	Device Code Read	R	4	
C0h	Panel Driving Setting	W/R	7	
C1h	Display Timing Setting for Normal/Partial Mode	W/R	5	
C3h	Display Timing Setting for Idle Mode	W/R	5	
C4h	Source/VCOM/Gate Driving Timing Setting	W/R	5	
C8h	Gamma Set A	W/R	18	
C9h	Gamma Set B	W/R	18	
CAh	Gamma Set C	W/R	18	
D0h	Power Setting for Common	W/R	10	
D1h	VCOM Setting	W/R	4	
D2h	Power Setting for Normal Mode	W/R	3	
D4h	Power Setting for Idle Mode	W/R	3	
D6h	Test Mode	N/A	4	Access prohibited
D7h	Test Mode	N/A	12	Access prohibited
D9h	Test Mode	N/A	2	Access prohibited

Table 26 Manufacturer Command (Continued)

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number Of Parameter	Category
E0h	NVM Access Control	W/R	4	
E1h	set_write_DDB Control	W/R	1	
E2h	Test Mode	N/A	1	Access prohibited
E3h	Test Mode	N/A	12	Access prohibited
E4h	Test Mode	N/A	5	Access prohibited
E5h	Test Mode	N/A	1	Access prohibited
E6h	Test Mode	N/A	1	Access prohibited
F3h	Test Mode	N/A	2	Access prohibited
FAh	Test Mode	N/A	4	Access prohibited
FCh	Test Mode	N/A	5	Access prohibited
FDh	Test Mode	N/A	5	Access prohibited
FEh	Test Mode	N/A	5	Access prohibited

Command Accessibility

In the initial state, only User Command and Manufacturer Command Access Protect command (B0h) are accessible. Other commands are treated as nop.

Of Manufacturer Command (B0h-FFh) defined in the table below, additional User Commands (B1h-BFh) are accessible only when MCAP=3'h2.

Other Manufacturer Commands are accessible only when MCAP=3'h0. See description on MCAP command for details.

(1) User Command

Table 27 User Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
00h	nop	Yes	Yes	Yes	Yes	Yes
01h	soft_reset	Yes	Yes	Yes	Yes	Yes
04h	read_DDB_start	Yes	Yes	Yes	Yes	Yes
0Ah	get_power_mode	Yes	Yes	Yes	Yes	Yes
0Bh	get_address_mode	Yes	Yes	Yes	Yes	Yes
0Ch	get_pixel_format	Yes	Yes	Yes	Yes	Yes
0Dh	get_display_mode	Yes	Yes	Yes	Yes	Yes
0Eh	get_signal_mode	Yes	Yes	Yes	Yes	Yes
0Fh	get_diagnostic _result	Yes	Yes	Yes	Yes	Yes
10h	enter_sleep_mode	Yes	Yes	Yes	Yes	Yes
11h	exit_sleep_mode	Yes	Yes	Yes	Yes	Yes
12h	enter_partial_mode	Yes	Yes	Yes	Yes	Yes
13h	enter_normal_mode	Yes	Yes	Yes	Yes	Yes
20h	exit_invert_mode	N/A	N/A	N/A	N/A	N/A
21h	enter_invert_mode	N/A	N/A	N/A	N/A	N/A
28h	set_display_off	Yes	Yes	Yes	Yes	Yes
29h	set_display_on	Yes	Yes	Yes	Yes	Yes
2Ah	set_column_address	Yes	Yes	Yes	Yes	Yes
2Bh	set_page_address	Yes	Yes	Yes	Yes	Yes

Table 28 User Command (Continued)

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
2Ch	write_memory_start	Yes	Yes	Yes	Yes	Yes
2Eh	read_memory_start	Yes	Yes	Yes	Yes	Yes
30h	set_partial_area	Yes	Yes	Yes	Yes	Yes
33h	set_scroll_area	N/A	N/A	N/A	N/A	N/A
34h	set_tear_off	Yes	Yes	Yes	Yes	Yes
35h	set_tear_on	Yes	Yes	Yes	Yes	Yes
36h	set_address_mode	Yes	Yes	Yes	Yes	Yes
37h	set_scroll_start	N/A	N/A	N/A	N/A	N/A
38h	exit_idle_mode	Yes	Yes	Yes	Yes	Yes
39h	enter_idle_mode	Yes	Yes	Yes	Yes	Yes
3Ah	set_pixel_format	Yes	Yes	Yes	Yes	Yes
3Ch	write_memory_ continue	Yes	Yes	Yes	Yes	Yes
3Eh	read_memory_ continue	Yes	Yes	Yes	Yes	Yes
44h	set_tear_scanline	Yes	Yes	Yes	Yes	Yes
45h	get_scanline	Yes	Yes	Yes	Yes	No
A1h	read_DDB_start	Yes	Yes	Yes	Yes	Yes
A8h	read_DDB_continue	Yes	Yes	Yes	Yes	Yes

(2) Manufacturer Command

Table 29 Manufacturer Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
B0h	Manufacturer Command Access Protect	Yes	Yes	Yes	Yes	Yes
B1h	Low Power Mode Control	No	No	No	No	Yes
B3h	Frame Memory Access and Interface Setting	Yes	Yes	Yes	Yes	Yes
B5h	Read Checksum and ECC Error Count	Yes	Yes	Yes	Yes	Yes
B6h	DSI Control	Yes	Yes	Yes	Yes	Yes
B8h	Backlight Control 1	Yes	Yes	Yes	Yes	Yes
B9h	Backlight Control 2	Yes	Yes	Yes	Yes	Yes
BAh	Backlight Control 3	Yes	Yes	Yes	Yes	No
BFh	Device Code Read	Yes	Yes	Yes	Yes	Yes
C0h	Panel Driving Setting	Yes	Yes	Yes	Yes	Yes
C1h	Display Timing Setting for Normal/Partial Mode	Yes	Yes	Yes	Yes	Yes
C3h	Display Timing Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
C4h	LTPS Interface Mode	Yes	Yes	Yes	Yes	Yes
C8h	Gamma Set A	Yes	Yes	Yes	Yes	Yes
C9h	Gamma Set B	Yes	Yes	Yes	Yes	Yes
CAh	Gamma Set C	Yes	Yes	Yes	Yes	Yes
D0h	Power Setting for Common	Yes	Yes	Yes	Yes	Yes
D1h	VCOM Setting	Yes	Yes	Yes	Yes	Yes
D2h	Power Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
D4h	Power Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
E0h	NVM Access Control	Yes	Yes	Yes	Yes	No
E1h	set_write_DDB Control	Yes	Yes	Yes	Yes	Yes

Table 30 Manufacturer Command (Continued)

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
D6h	Test Mode	No	No	No	No	No
D7h	Test Mode	No	No	No	No	No
D9h	Test Mode	No	No	No	No	No
E2h	Test Mode	No	No	No	No	No
E3h	Test Mode	No	No	No	No	No
E4h	Test Mode	No	No	No	No	No
E5h	Test Mode	No	No	No	No	No
E6h	Test Mode	No	No	No	No	No
F3h	Test Mode	No	No	No	No	No
FAh	Test Mode	No	No	No	No	No
FCh	Test Mode	No	No	No	No	No
FDh	Test Mode	No	No	No	No	No
FEh	Test Mode	No	No	No	No	No
FFh	Test Mode	No	No	No	No	No

Default Modes and Values

(1) User Command

Table 31 User Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	nop	None	N/A	N/A	N/A
01h	soft_reset	None	N/A	N/A	N/A
04h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)
		5th	FFh	FFh	FFh
0Ah	get_power_mode	1st	08h	08h	08h
0Bh	get_address_mode	1st	00h	No Change (Note1)	00h
0Ch	get_pixel_format	1st	07h	07h	07h
0Dh	get_display_mode	1st	00h	00h	00h
0Eh	get_signal_mode	1st	00h	00h	00h
0Fh	get_diagnostic _result	1st	00h	00h	00h
10h	enter_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
11h	exit_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
12h	enter_partial_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
13h	enter_normal_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
20h	exit_invert_mode	None	N/A	N/A	N/A
21h	enter_invert_mode	None	N/A	N/A	N/A
28h	set_display_off	None	Display Off	Display Off	Display Off
29h	set_display_on	None	Display Off	Display Off	Display Off

Table 32 User Command (Continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
2Ah	set_column_address	1st/2nd SC[9:0]	000h	000h	000h
		3rd/4th EC[9:0]	167h	If set_address_mode B5=0 : 167h B5=1 : 27Fh	167h
2Bh	set_page_address	1st/2nd SP[9:0]	000h	000h	000h
		3rd/4th EP[9:0]	27Fh	If set_address_mode B5=0 : 27Fh B5=1 : 167h	27Fh
2Ch	write_memory_start	All	Random Values	Not Cleared	Not Cleared
2Eh	read_memory_start	All	Random Values	Not Cleared	Not Cleared
30h	set_partial_area	1st/2nd SR[9:0]	000h	000h	000h
		3rd/4th ER[9:0]	27Fh	27Fh	27Fh
33h	set_scroll_area	1st/2nd TFA[9:0]	N/A	N/A	N/A
		3rd/4th VSA[9:0]	N/A	N/A	N/A
		5th/6th BFA[9:0]	N/A	N/A	N/A
34h	set_tear_off	None	TE line output Off	TE line output Off	TE line output Off
35h	set_tear_on	1st	TE line output Off	TE line output Off	TE line output Off
36h	set_address_mode	1st	00h	No Change (Note1)	00h
37h	set_scroll_start	1st/2nd VSP[9:0]	N/A	N/A	N/A
38h	exit_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39h	enter_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3Ah	set_pixel_format	1st	07h	07h	07h
3Ch	write_memory _continue	All	Random Values	Not Cleared	Not Cleared
3Eh	read_memory _continue	All	Random Values	Not Cleared	Not Cleared

Table 33 User Command (Continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
44h	set_tear_scanline	1st/2nd STS[9:0]	000h	000h	000h
45h	get_scanline	1st/2nd GTS[9:0]	000h (invalid)	000h (invalid)	000h (invalid)
A1h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)
		5th	FFh	FFh	FFh
A8h	read_DDB_continue	-	See read_DDB_start	See read_DDB_start	See read_DDB_start

Notes: 1. No Change from the value before soft_reset command.

2. Data are loaded from internal NVM. If the user writes VCM register value, Supplier ID, and Supplier Elective Data to the NVM, the values are set to default.

(2) Manufacturer Command

Table 34 Manufacturer Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
B0h	Manufacturer Command Access Protect	1st	MCAP=3'h3	No Change (Note1)	MCAP=3'h3
B1h	Low Power Mode Control	1st	DSTB=0 Sleep Mode On	DSTB=0 Sleep Mode On	DSTB=0 Sleep Mode On
B3h	Frame Memory Access and Interface Setting	1st	WEMODE=0 SELDL=0	No Change (Note1)	WEMODE=0 SELDL=0
		2nd	TEI=3'h0 DFM=2'h0 EPF=2'h0	No Change (Note1)	TEI=3'h0 DFM=2'h0 EPF=2'h0
B5h	Read Checksum and ECC Error Count	1st	CSOUT=8'h00	No Change (Note1)	CSOUT=8'h00
		2nd	DSIECP=8'h00	No Change (Note1)	DSIECP=8'h00
		3rd	DSIECE=8'h00	No Change (Note1)	DSIECE=8'h00
B6h	DSI Control	1st	DSITXDIV=2'h1	No Change (Note1)	DSITXDIV=2'h1
B8h	Backlight Control 1	1st	BLCM=0 BLCON=0	No Change (Note1)	BLCM=0 BLCON=0
		2nd	THREW0=5'h00	No Change (Note1)	THREW0=5'h00
		3rd	THREW1=5'h00	No Change (Note1)	THREW1=5'h00
		4th	ULMTW0=8'h00	No Change (Note1)	ULMTW0=8'h00
		5th	ULMTW1=8'h00	No Change (Note1)	ULMTW1=8'h00
		6th	LLMTW0=8'h00	No Change (Note1)	LLMTW0=8'h00
		7th	LLMTW1=8'h00	No Change (Note1)	LLMTW1=8'h00
		8th	PITCHW=4'h0	No Change (Note1)	PITCHW=4'h0
		9th	CGAPW=5'h00	No Change (Note1)	CGAPW=5'h00
		10th	COEFK0=5'h00	No Change (Note1)	COEFK0=5'h00

Table 35 Manufacturer Command (Continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
B8h	Backlight Control 1	11th	COEFK1=5'h00	No Change (Note1)	COEFK1=5'h00
		12th	TBL3=8'h00	No Change (Note1)	TBL3=8'h00
		13th	TBL4=8'h00	No Change (Note1)	TBL4=8'h00
		14th	TBL5=8'h00	No Change (Note1)	TBL5=8'h00
		15th	TBL6=8'h00	No Change (Note1)	TBL6=8'h00
B9h	Backlight Control 2	1st	PWMON=0	No Change (Note1)	PWMON=0
		2nd	BDCV=8'h00	No Change (Note1)	BDCV=8'h00
		3rd	PWMDIV=8'h00	No Change (Note1)	PWMDIV=8'h00
		4th	DIMON=0 LEDPWMPOL=0 LEDPWME=0 PWMWM=0	No Change (Note1)	DIMON=0 LEDPWMPOL=0 LEDPWME=0 PWMWM=0
BAh	Backlight Control 3	1st	RDPWM=8'h00	RDPWM=8'h00	RDPWM=8'h00
BFh	Device Code Read	1st	8'h01	8'h01	8'h01
		2nd	8'h22	8'h22	8'h22
		3rd	8'h15	8'h15	8'h15
		4th	8'h23	8'h23	8'h23
C0h	Panel Driving Setting	1st	SS=0,BGR=0 GS=0,SM=0 REV=0	No Change (Note1)	SS=0,BGR=0 GS=0,SM=0 REV=0
		2nd	NL=8'h9F	No Change (Note1)	NL=8'h9F
		3rd	SCN=8'h00	No Change (Note1)	SCN=8'h00
		4th	NW=0	No Change (Note1)	NW=0
		5th	PTV=0 BLV=1	No Change (Note1)	PTV=0 BLV=1

Table 36 Manufacturer Command (Continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
C0h	Panel Driving Setting	6th	PTS=3'h0 PTDC=0 NDL=0,BLS=0	No Change (Note1)	PTS=3'h0 PTDC=0 NDL=0,BLS=0
		7th	ISC=4'h1 PTG=0	No Change (Note1)	ISC=4'h1 PTG=0
C1h	Display Timing Setting for Normal/Partial Mode	1st	BC0=1	No Change (Note1)	BC0=1
		2nd	8'h00	No Change (Note1)	8'h00
		3rd	RTN0=5'h19	No Change (Note1)	RTN0=5'h19
		4th	BP0=8'h08	No Change (Note1)	BP0=8'h08
		5th	FP0=8'h08	No Change (Note1)	FP0=8'h08
C3h	Display Timing Setting for Idle Mode	1st	BC2=1	No Change (Note1)	BC2=1
		2nd	8'h00	No Change (Note1)	8'h00
		3rd	RTN2=5'h19	No Change (Note1)	RTN2=5'h19
		4th	BP2=8'h08	No Change (Note1)	BP2=8'h08
		5th	FP2=8'h08	No Change (Note1)	FP2=8'h08
C4h	Source/VCOM/Gate Driving Timing Setting	1st	NOW=3'h1 SDT=3'h1	No Change (Note1)	NOW=3'h1 SDT=3'h1
		2nd	MCP=3'h1	No Change (Note1)	MCP=3'h1
		3rd	VEM=2'h3 VEQW=3'h1	No Change (Note1)	VEM=2'h3 VEQW=3'h1
		4th	SPCW=3'h1	No Change (Note1)	SPCW=3'h1
		5th	8'h00	No Change (Note1)	8'h00
C8h	Gamma Set A	1st-18th	All "0"	No Change (Note1)	All "0"
C9h	Gamma Set B	1st-18th	All "0"	No Change (Note1)	All "0"

Table 37 Manufacturer Command (Continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
CAh	Gamma Set C	1st-18th	All “0”	No Change (Note1)	All “0”
D0h	Power Setting for Common	1st	8’h00	No Change (Note1)	8’h00
		2nd	VC2=3’h4 VC3=3’h7	No Change (Note1)	VC2=3’h4 VC3=3’h7
		3rd	8’hC0	No Change (Note1)	8’hC0
		4th	VRH=5’h0F	No Change (Note1)	VRH=5’h0F
		5th	8’h01	No Change (Note1)	8’h01
		6th	8’h00	No Change (Note1)	8’h00
		7th	8’h00	No Change (Note1)	8’h00
		8th	8’h00	No Change (Note1)	8’h00
		9th	8’h07	No Change (Note1)	8’h07
		10th	8’h00	No Change (Note1)	8’h00
D1h	VCOM Setting	1st	VCVCM=0 VCVDV=0	No Change (Note1)	VCVCM=0 VCVDV=0
		2nd	8’h00	No Change (Note1)	8’h00
		3rd	NVM value	NVM value	NVM value
		4th	NVM value	NVM value	NVM value
D2h	Power Setting for Normal Mode	1st	AP0=2’h3	No Change (Note1)	AP0=2’h3
		2nd	DC00=3’h4 DC10=3’h2	No Change (Note1)	DC00=3’h4 DC10=3’h2
		3rd	DC30=3’h2	No Change (Note1)	DC30=3’h2

Table 38 Manufacturer Command (Continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
D4h	Power Setting for Idle Mode	1st	AP1=2'h3	No Change (Note1)	AP1=2'h3
		2nd	DC01=3'h4 DC11=3'h2	No Change (Note1)	DC01=3'h4 DC11=3'h2
		3rd	DC31=3'h2	No Change (Note1)	DC31=3'h2
D6h	Test Mode	1st	8'h01 (Note3)	8'h01 (Note3)	8'h01 (Note3)
		2nd	8'h30 (Note3)	8'h30 (Note3)	8'h30 (Note3)
		3rd	8'h02 (Note3)	8'h02 (Note3)	8'h02 (Note3)
		4th	8'h16 (Note3)	8'h16 (Note3)	8'h16 (Note3)
D7h	Test Mode	1st	8'h06 (Note3)	8'h06 (Note3)	8'h06 (Note3)
		2nd	8'h16 (Note3)	8'h16 (Note3)	8'h16 (Note3)
		3rd	8'h88 (Note3)	8'h88 (Note3)	8'h88 (Note3)
		4th	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		5th	8'h66 (Note3)	8'h66 (Note3)	8'h66 (Note3)
		6th	8'hAA (Note3)	8'hAA (Note3)	8'hAA (Note3)
		7th	8'h0A (Note3)	8'h0A (Note3)	8'h0A (Note3)
		8th	8'h88 (Note3)	8'h88 (Note3)	8'h88 (Note3)
		9th	8'h80 (Note3)	8'h80 (Note3)	8'h80 (Note3)
		10th	8'hCA (Note3)	8'hCA (Note3)	8'hCA (Note3)
		11th	8'h0A (Note3)	8'h0A (Note3)	8'h0A (Note3)
		12th	8'h0C (Note3)	8'h0C (Note3)	8'h0C (Note3)
D9h	Test Mode	1st	8'hFF (Note3)	8'hFF (Note3)	8'hFF (Note3)
		2nd	8'h9F (Note3)	8'h9F (Note3)	8'h9F (Note3)
E0h	NVM Access Control	1st	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		2nd	8'h18 (Note3)	8'h18 (Note3)	8'h18 (Note3)
		3rd	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		4th	8'h07 (Note3)	8'h07 (Note3)	8'h07 (Note3)
E1h	set_write_DDB Control	1st	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
E2h	Test Mode	1st	8'h00	No Change	8'h00

Table 39 Manufacturer Command (Continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
E3h	Test Mode	1st	8'h00	No Change	8'h00
		2nd	8'h00	No Change	8'h00
		3rd-12th	8'hFF	No Change	8'hFF
E4h	Test Mode	1st	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		2nd	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		3rd	8'hAA (Note3)	8'hAA (Note3)	8'hAA (Note3)
		4th	8'hAA (Note3)	8'hAA (Note3)	8'hAA (Note3)
		5th	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
E5h	Test Mode	1st	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
E6h	Test Mode	1st	8'h00	No Change	8'h00
F3h	Test Mode	1st	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		2nd	8'h20 (Note3)	8'h20 (Note3)	8'h20 (Note3)
FAh	Test Mode	1st	8'h01 (Note3)	8'h01 (Note3)	8'h01 (Note3)
		2nd	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		3rd	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		4th	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
FCh	Test Mode	1st-5th	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
FDh	Test Mode	1st	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		2nd	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		3rd	8'h01 (Note3)	8'h01 (Note3)	8'h01 (Note3)
		4th	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		5th	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
FEh	Test Mode	1st	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		2nd	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		3rd	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		4th	8'h00 (Note3)	8'h00 (Note3)	8'h00 (Note3)
		5th	8'h30 (Note3)	8'h30 (Note3)	8'h30 (Note3)

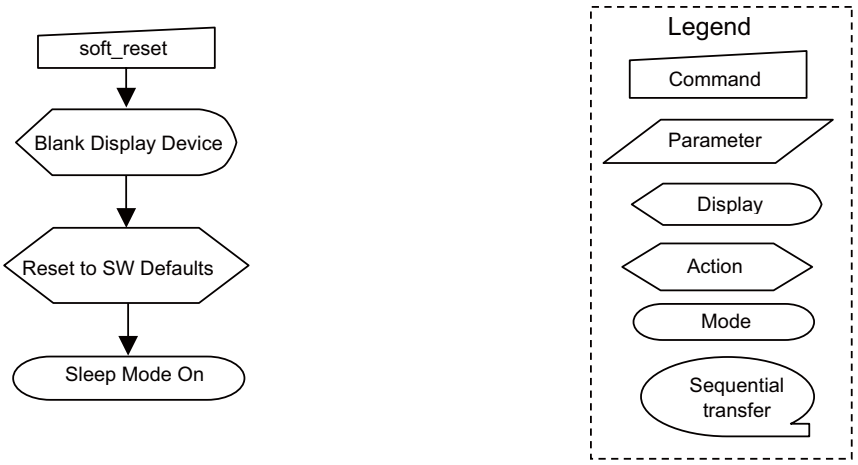
Notes: 1. Data are not changed by executing soft_reset command.
2. If data are loaded from NVM, the loaded data become default values.
3. These values are the register values when MCAP[2] is set to 0.

User Command

nop: 00h

00h	nop												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00h
Parameter	None												
Description	This command is an empty command; it has no effect on the display module. However, it can be used to terminate Frame Memory Write or Read. X = Don't Care												
Restriction	-												
Flow Chart	-												

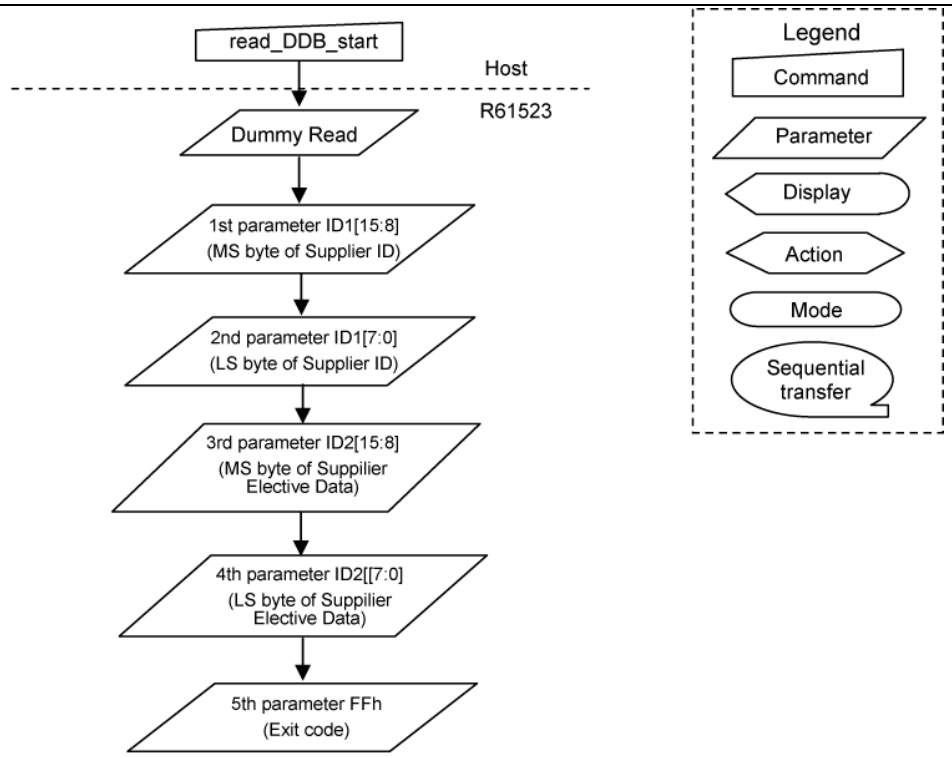
soft_reset: 01h

01H	soft_reset												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01h
Parameter	None												
Description	The display module performs a software reset. Commands and parameters are written with their SW Reset default values. (See “Default Modes and Values”.) Note: The Frame Memory contents are unaffected by this command. X = Don’t care												
Restriction	If a soft_reset is sent when the display module is in Sleep Mode, the host processor must wait 120 milliseconds before sending an exit_sleep_mode command. No soft_reset shall be sent during exit_sleep_mode sequence. No new command setting is allowed until the R61523 enters the Sleep Mode. See “State & Command sequence” for the sequence to enter Sleep Mode. If a soft_reset is sent when the display module is in Sleep Mode, data in NVM are read. No new command setting is inhibited while data are read (5ms).												
Flow Chart													

read_DDB_start: 04h

04h	read_DDB_start												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	1	0	0	A8h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	1	↑	1	X	1	1	1	1	1	1	1	1	04h
Description	The command returns information from the display module as follows: 1st parameter: upper byte (ID1[15:8]) of Supplier ID 2nd parameter: lower byte (ID[7:0]) of Supplier ID 3rd parameter: Supplier Elective Data (ID2[15:8]) 4th parameter: Supplier Elective Data (ID2[7:0]) 5th parameter: Exit Code (FFh) Supplier ID and Supplier Elective Data stored in internal NVM are read. Read values are the same as ones read by read_DDB_start (A1h) command. read_DDB_continue (A8h) command is not affected. X=Don't care												
Restriction	-												

Flow Chart



Note: When this command is read via DSI, dummy read operation is not performed.

get_power_mode: 0Ah

0Ah	get_power_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	0	1	0	0Ah
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	1	↑	1	X	0	IDM ON	PTL ON	SLP OUT	NOR ON	DSP ON	0	0	XXh

Description: The display module returns the current power mode.

Bit	Description	Comment	Command list Symbol
D7	Reserved	Set to “0”	-
D6	Idle Mode On/Off		IDMON
D5	Partial Mode On/Off		PTLON
D4	Sleep Mode On/Off		SLPOUT
D3	Display Normal Mode On/Off		NORON
D2	Display On/Off		DSPON
D1	Reserved	Set to “0”	-
D0	Reserved	Set to “0”	-

<table>
<tr><th>0Ah</th><th>get_power_mode</th></tr>
<tr><td></td><td>

Bit D7 – Reserved

This bit is not applicable. Set to “0”.

Bit D6 – Idle Mode On/Off

‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.

Bit D5 – Partial Mode On/Off

‘0’ = Partial Mode Off.
‘1’ = Partial Mode On.

Bit D4 – Sleep Mode On/Off

‘0’ = Sleep Mode On
‘1’ = Sleep Mode Off

Bit D3 – Display Normal Mode On/Off

‘0’ = Display Normal Mode Off
‘1’ = Display Normal Mode On

Bit D2 – Display On/Off

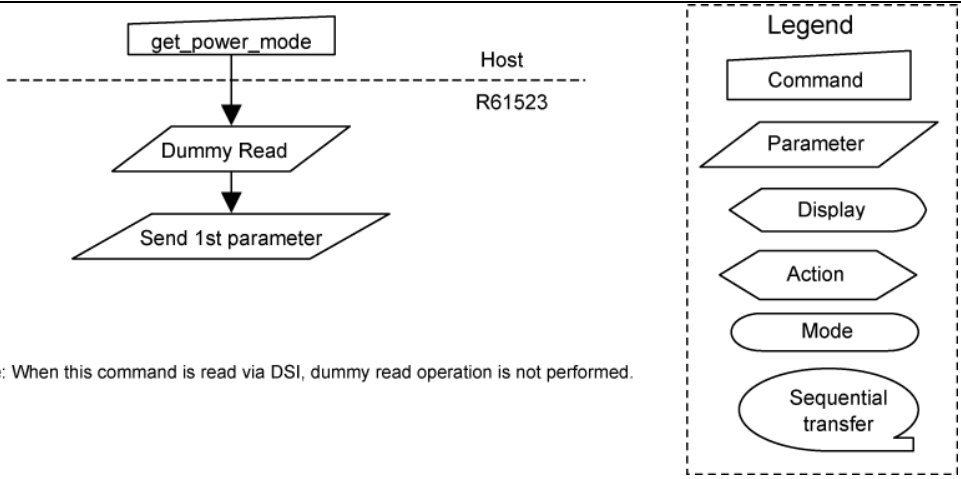
‘0’ = Display is Off
‘1’ = Display is On

Bit D1 – Reserved

This bit is not applicable. Set to “0”.

Bit D0 – Reserved

This bit is not applicable. Set to “0”.

X = Don’t care.
</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Flow chart</td><td>


Note: When this command is read via DSI, dummy read operation is not performed.
</td></tr>
</table>

get_address_mode: 0Bh

<table>
<tr><td>0Bh</td><td colspan="13">get_address_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[15:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>Dummy parameter</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>0</td><td>0</td><td>B0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below. This command setting depends on set_address_mode (36h). For B4, B3, and B0, please refer to “Appendix” for each mode.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td></td><td>B7</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td></td><td>B6</td></tr>
<tr><td>D5</td><td>Page/Column Order</td><td></td><td>B5</td></tr>
<tr><td>D4</td><td>Line Address Order</td><td></td><td>B4</td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td>Set to “0”</td><td></td></tr>
<tr><td>D2</td><td>Display Data Latch Order</td><td>Set to “0”</td><td></td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D0</td><td>Switching between Common outputs and Frame Memory</td><td></td><td>B0</td></tr>
</table>

Bit D7 - Page Address Order

‘0’ = Top to Bottom (When set_address_mode D7 = ’0’)
‘1’ = Bottom to Top (When set_address_mode D7 = ‘1’)

Bit D6 – Column Address Order

‘0’ = Left to Right (When set_address_mode D6 = ‘0’)
‘1’ = Right to Left (When set_address_mode D6 = ‘1’)

Bit D5 – Page/Column Order

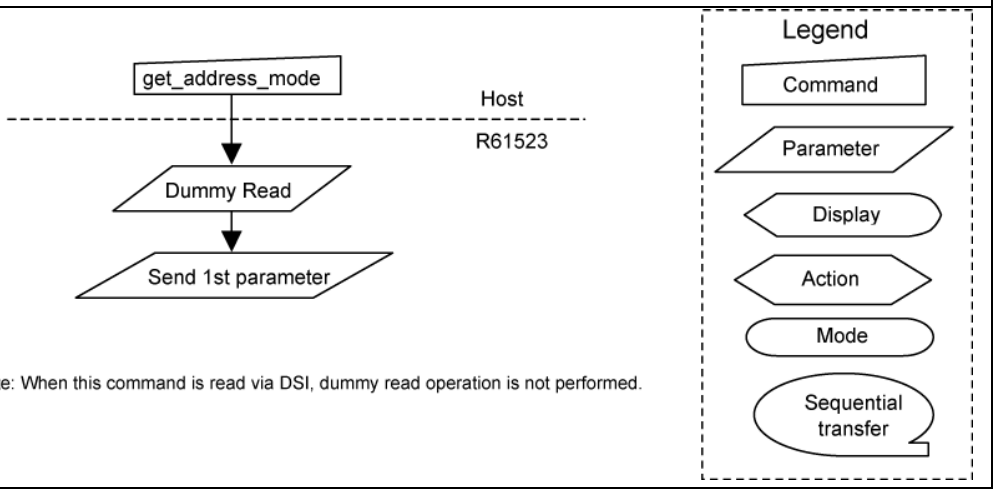
‘0’ = Normal Mode (When set_address_mode D5 = ‘0’)
‘1’ = Reverse Mode (When set_address_mode D5 = ‘1’)
Note: See “Host Processor to Memory Write/Read Direction” and “Memory Access Control: 36h” for D7 to D5 bits.

Bit D4 – Line Address Order

‘0’ = LCD Refresh Top to Bottom (When set_address_mode D4 = ‘0’)
‘1’ = LCD Refresh Bottom to Top (When set_address_mode D4 = ‘1’)
Note: See “Memory Access Control (36h)” for D4 bit.

Bit D3 – RGB/BGR Order

This bit is not applicable. Set to “0” (Not supported).</td></tr>
</table>

0Bh	get_address_mode
Description	• Bit D2 – Display Data Latch Data Order This bit is not applicable. Set to “0” (Not supported). • Bit D1 – Reserved This bit is not applicable. Set to “0” (Not supported). • Bit D0 – Switching between Common outputs and Frame Memory ‘0’ = Normal (When set_address_mode D0=’0’) ‘1’ = Flipped (When set_address_mode D0=’1’) The gate scan order is reversed. X = Don’t care.
Restriction	-
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed.

Note: See “”State Transition Diagram” for display mode transition.

get_pixel_format: 0Ch

0Ch	get_pixel_format												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	1	0	0	0Ch
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	1	↑	1	X	0	D6	D5	D4	0	D2	D1	D0	XXh

Description

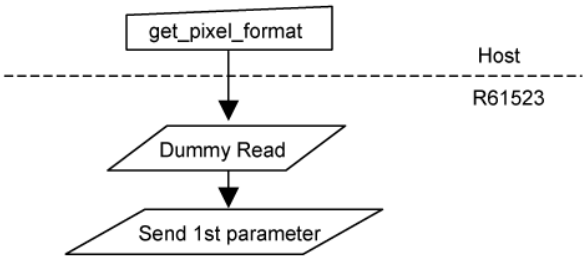
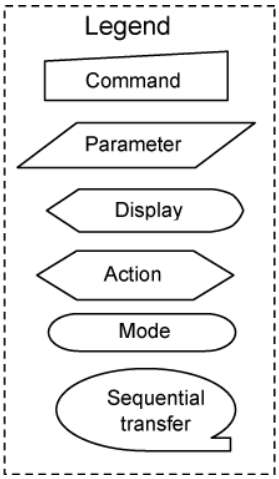
This command indicates the current status of the display as described in the table below. This command setting depends on set_pixel_format (3Ah).

Bit	Description	Comment
D7	DPI Pixel format	Set to “0”
D6	(RGB Interface Color Format)	Set to “0”
D5		Set to “0”
D4		Set to “0”
D3	DBI Pixel Format	Set to “0”
D2	(Control Interface Color Format)	D2
D1		D1
D0		D0

- Bit D[6:4] – These bits are not applicable. Set to 3’h7.
- Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection)
- Bit D7 and D3 – These bits are not applicable. Set to “0”. See description of command set_pixel_format (3Ah).

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Setting inhibited	0	0	0
Setting inhibited	0	0	1
Setting inhibited	0	1	0
Setting inhibited	0	1	1
Setting inhibited	1	0	0
16 bits/pixel (65,536 colors)	1	0	1
18 bits/pixel (262,144 colors)	1	1	0
24 bits/pixel (16,777,216 colors)	1	1	1

X = Don’t care

0Ch	get_pixel_format
	 Note: When this command is read via DSI, dummy read operation is not performed. 

get_display_mode: 0Dh

0Dh	get_display_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	1	0	1	0Dh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	1	↑	1	X	0	0	0	0	0	0	0	0	XXh

Description: The display module returns the current status of the display as described in the table below.

Bit	Description	Comment	Command list symbol
D7	Vertical Scrolling Status	Set to “0”	
D6	Reserved	Set to “0”	
D5	Inversion ON/OFF	Set to “0”	
D4	Reserved	Set to “0”	
D3	Reserved	Set to “0”	
D2	Gamma Curve Selection	Set to “0”	
D1	Gamma Curve Selection	Set to “0”	
D0	Gamma Curve Selection	Set to “0”	

- Bit D7

  This bit is not applicable. Set to “0”.

- Bit D6 – Reserved

  This bit is not applicable. Set to “0”.

- Bit D5

  This bit is not applicable. Set to “0”.

- Bit D4, D3 – Reserved

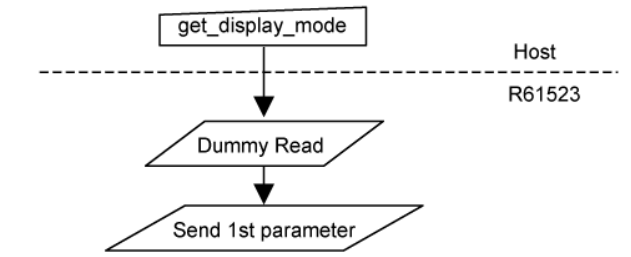
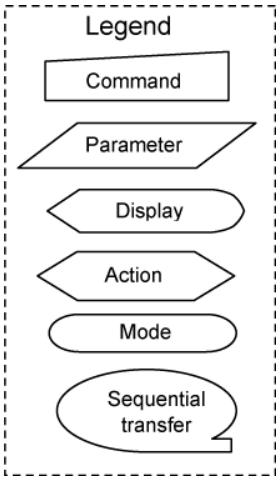
  These bits are not applicable. Set to “0”.

- Bit D2, D1, D0 – Gamma Curve Selection

  These bits are not applicable. Set to “0”.

X = Don’t care

Restriction: -

0Dh	get_display_mode
Flow Chart	 When this command is read via DSI, dummy read operation is not performed. 

get_signal_mode: 0Eh

0Eh	get_signal_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	1	1	0	0Eh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	1	↑	1	X	TE ON	TEL OM	0	0	0	0	0	0	XXh

Description: The display module returns the Display Signal Mode as described in the table below.

Bit	Description	Comment	Command list symbol
D7	Tearing Effect line ON/OFF		TEON
D6	Tearing Effect line Output Mode		TELOM
D5	Reserved	Set to “0”	-
D4	Reserved	Set to “0”	-
D3	Reserved	Set to “0”	-
D2	Reserved	Set to “0”	-
D1	Reserved	Set to “0”	-
D0	Reserved	Set to “0”	-

- Bit D7 – Tearing Effect Line On/Off

  ‘0’ = Tearing Effect Line Off
  ‘1’ = Tearing Effect On

- Bit D6 – Tearing Effect Line Output Mode (See “set_tear_on: 35h”).

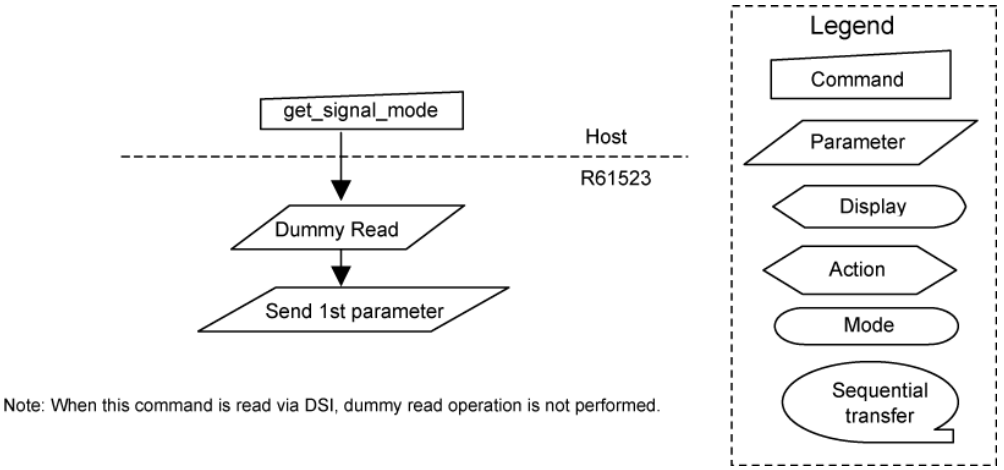
  ‘0’ = Mode1
  ‘1’ = Mode2

- Bit D5-D0 – Reserved

  These bits are not applicable. Set to “0”.

X = Don’t care

Restriction: -

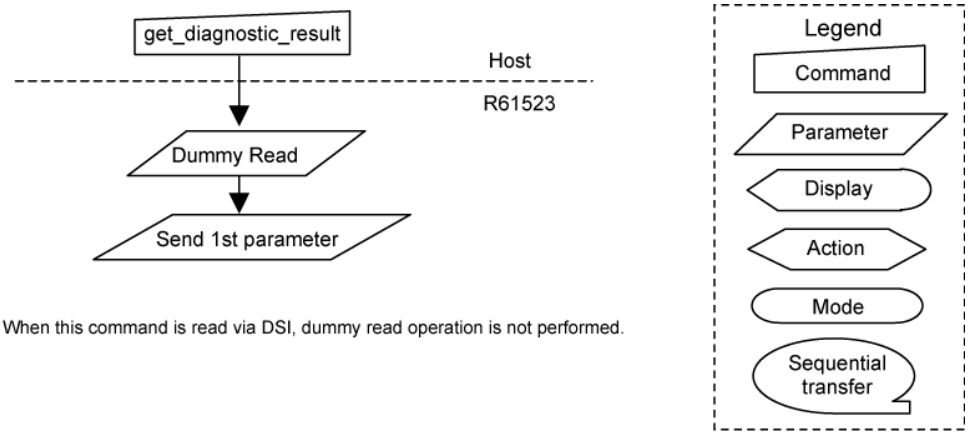
0Eh	get_signal_mode
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed.

get_diagnostic_result:0Fh

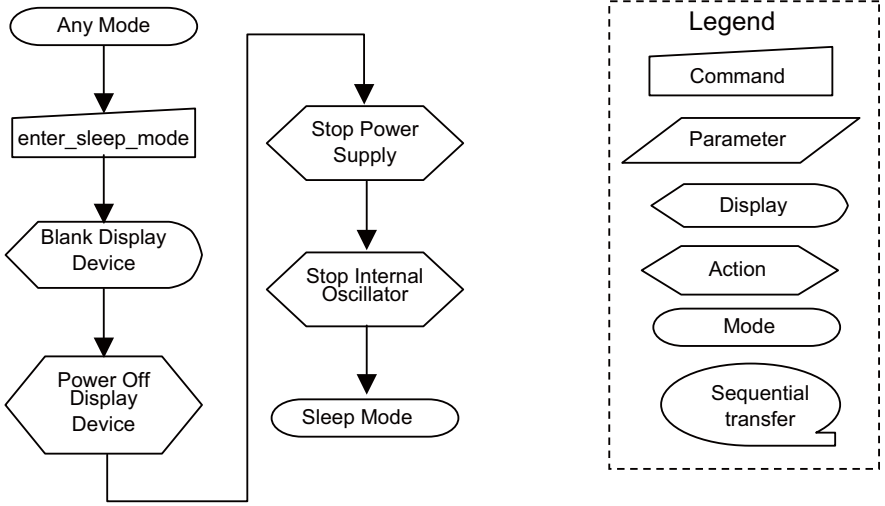
<table>
<tr><td>0Fh</td><td colspan="13">get_diagnostic_result</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[15:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0Fh</td></tr>
<tr><td>Dummy parameter</td><td>0</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>1st Parameter</td><td>0</td><td>↑</td><td>1</td><td>X</td><td>0</td><td>FUN CD</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command List Symbol</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td>Set to 0</td><td></td></tr>
<tr><td>D6</td><td>Functionality Detection</td><td></td><td>FUNCD</td></tr>
<tr><td>D5</td><td>Chip Attachment Detection</td><td>Set to 0</td><td>-</td></tr>
<tr><td>D4</td><td>Display Glass Break Detection</td><td>Set to 0</td><td>-</td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to 0</td><td>-</td></tr>
<tr><td>D2</td><td>Reserved</td><td>Set to 0</td><td>-</td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to 0</td><td>-</td></tr>
<tr><td>D0</td><td>Reserved</td><td>Set to 0</td><td>-</td></tr>
</table>

The display module returns the self-diagnostic results following the exit_sleep_mode (11h) as shown in the table above.
• Bit D7 – Register Loading Detection
This bit is not applicable. Set to “0”.
• Bit D6 – Functionality Detection
Note: See Self-Diagnostic Function for D6.
• Bit D5 – Chip Attachment Detection
This bit is not applicable. Set to “0”.
• Bit D4 –Display Glass Break Detection
This bit is not applicable. Set to “0”.
• Bit D3, D2, D1, D0 – Reserved
Set to 0.

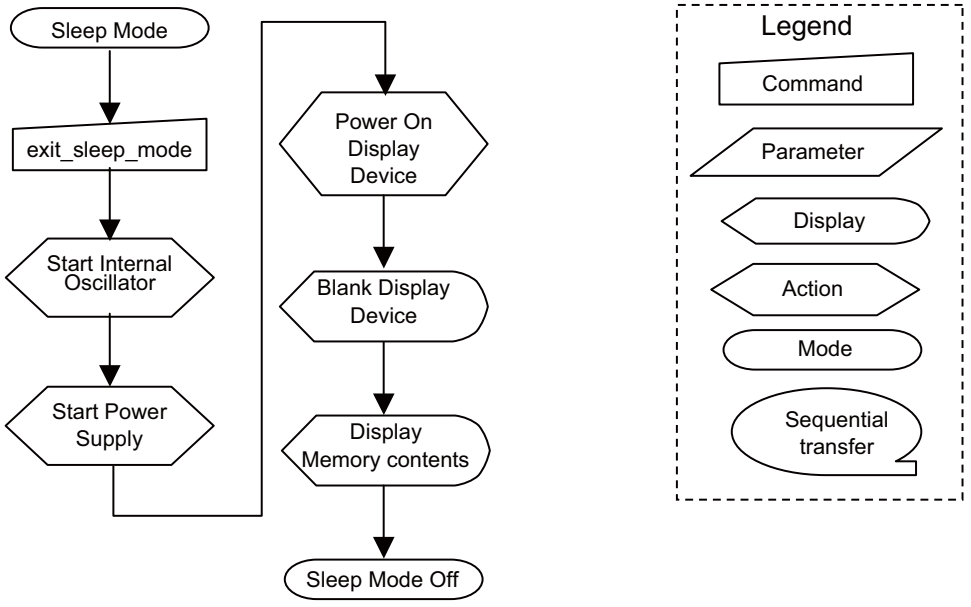
X = Don’t care
</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

0Fh	get_diagnostic_result
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed.

enter_sleep_mode: 10h

10h	enter_sleep_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	1	0	0	0	0	10h
Parameter	None												
Description	This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. See “State & Command sequence” for Sleep In sequence. DBI remains operational and the memory maintains its contents. See “State Transition Diagram” for each stage of transition. X = Don’t care												
Restriction	This command has no effect when the module is already in Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted. Sending a new command is prohibited while the R61523 performs either power supply OFF sequencer or blank scan.												
Flow Chart													

exit_sleep_mode: 11h

11h	exit_sleep_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	1	0	0	0	1	11h
Parameter	None												
Description	This command causes the display module to exit Sleep mode. DC/DC converter, internal oscillation and panel scanning start. See “State & Command sequence” for exit_sleep_mode sequence. See “State Transition Diagram” for each stage of transition. X = Don’t care												
Restriction	This command shall not cause any visual effect on display device when the display module is not in Sleep mode. No new command setting is allowed during power supply ON sequence. Operation may continue for more than 120msec due to power supply ON sequence setting. Do not send any command either in this case. The host processor must wait 120 milliseconds after sending an enter_sleep_mode command before sending an exit_sleep_mode command. The display runs the self-diagnostic function after this command is received.												
Flow Chart													

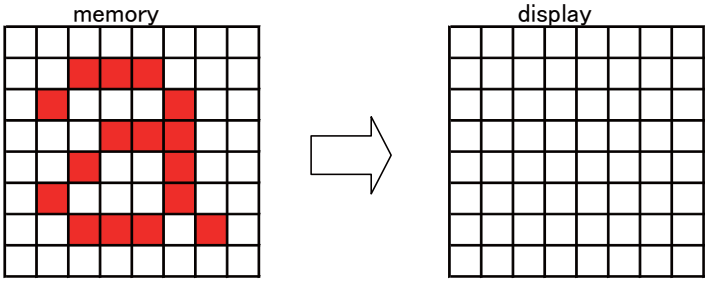
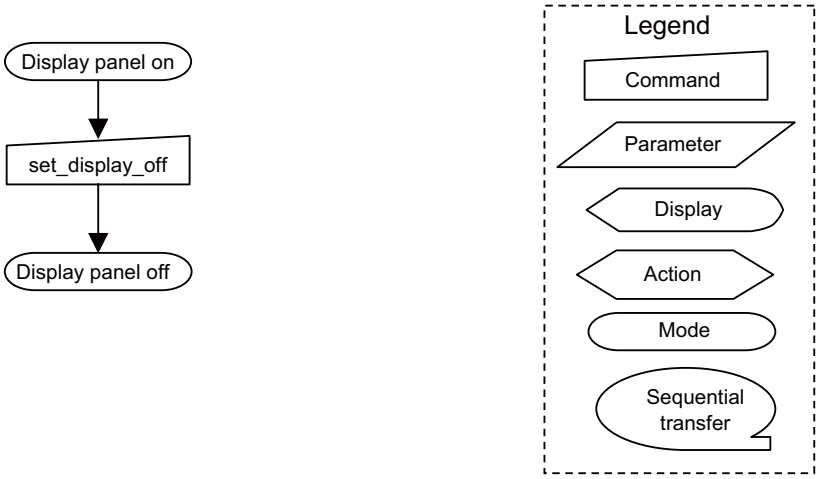
enter_partial_mode: 12h

12h	enter_partial_mode: 12h												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12h
Parameter	None												
Description	This command causes the display module to enter the Partial mode. The Partial mode window is described by the set_partial_area command (30h). To leave Partial mode, the enter_normal_mode (13h) shall be written. X = Don't care Note: When a command breaks in the middle of frame period in Normal mode, the command is enabled from the next frame period.												
Restriction	This command has no effect when the module is already in Partial mode.												
Flow Chart	See "set_partial_area: 30h".												

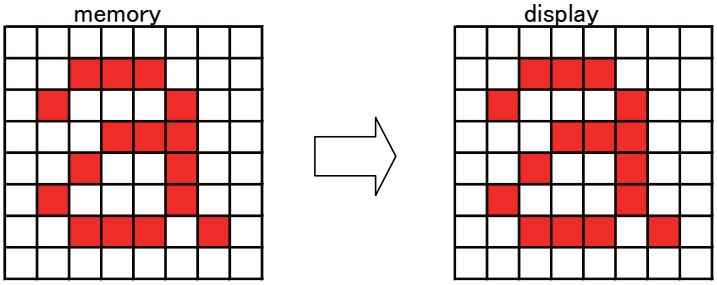
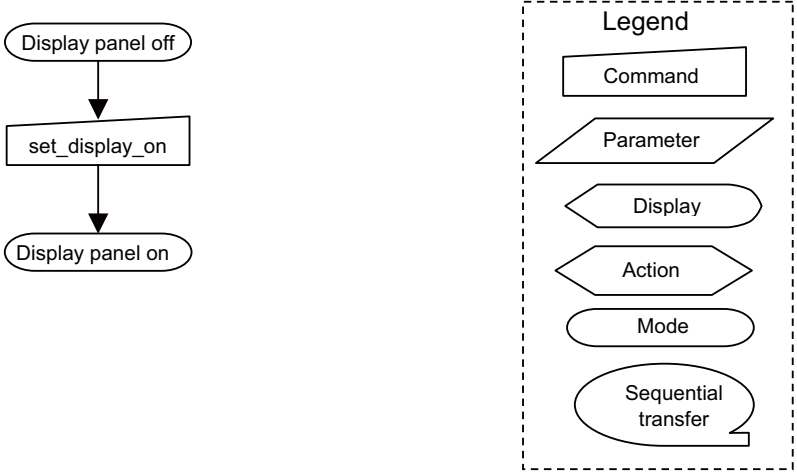
enter_normal_mode: 13h

13h	enter_normal_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	1	0	0	1	1	13h
Parameter	None												
Description	This command causes the display module to enter the Normal mode. Normal mode means Partial mode is off. X = Don't care Note: When a command breaks in the middle of frame period in Partial Mode, that command becomes valid from the next frame period.												
Restriction	This command has no effect when Normal mode is already active.												
Flow Chart	See the descriptions of commands set_partial_area (30h) when using this command.												

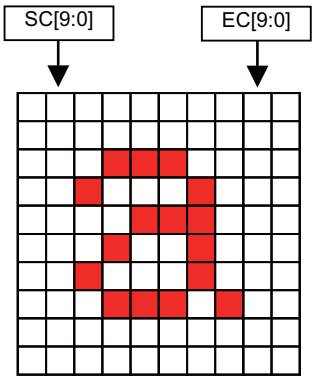
set_display_off: 28h

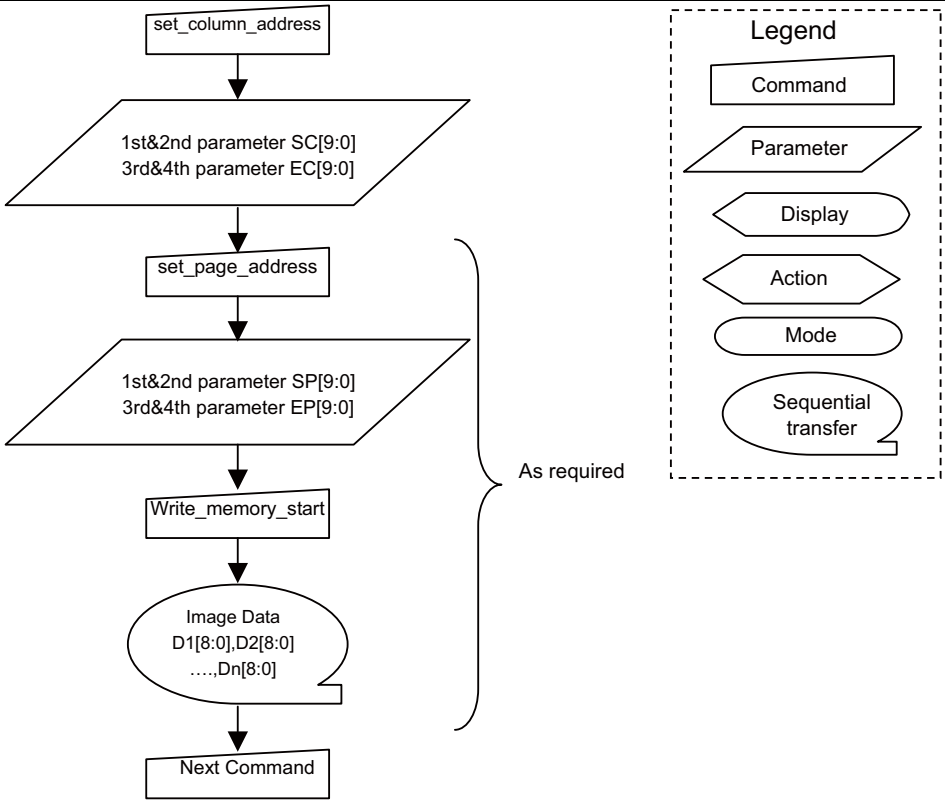
28h	set_display_off												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	0	0	0	28h
Parameter	None												
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example) memory display  For DISPOFF mode selection, see “Panel Driving Setting: C0h”. X = Don’t care												
Restriction	This command has no effect when the display panel is already off.												
Flow Chart													

set_display_on: 29h

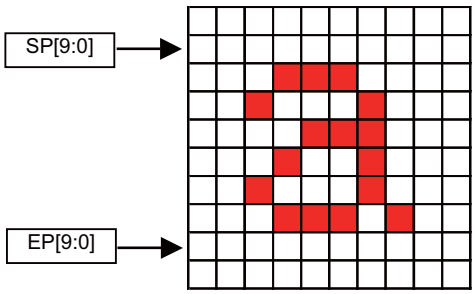
29h	**set_display_on**												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	0	1	0	0	1	29h
Parameter	None												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example) memory display 												
Restriction	This command has no effect when the display panel is already on.												
Flow Chart													

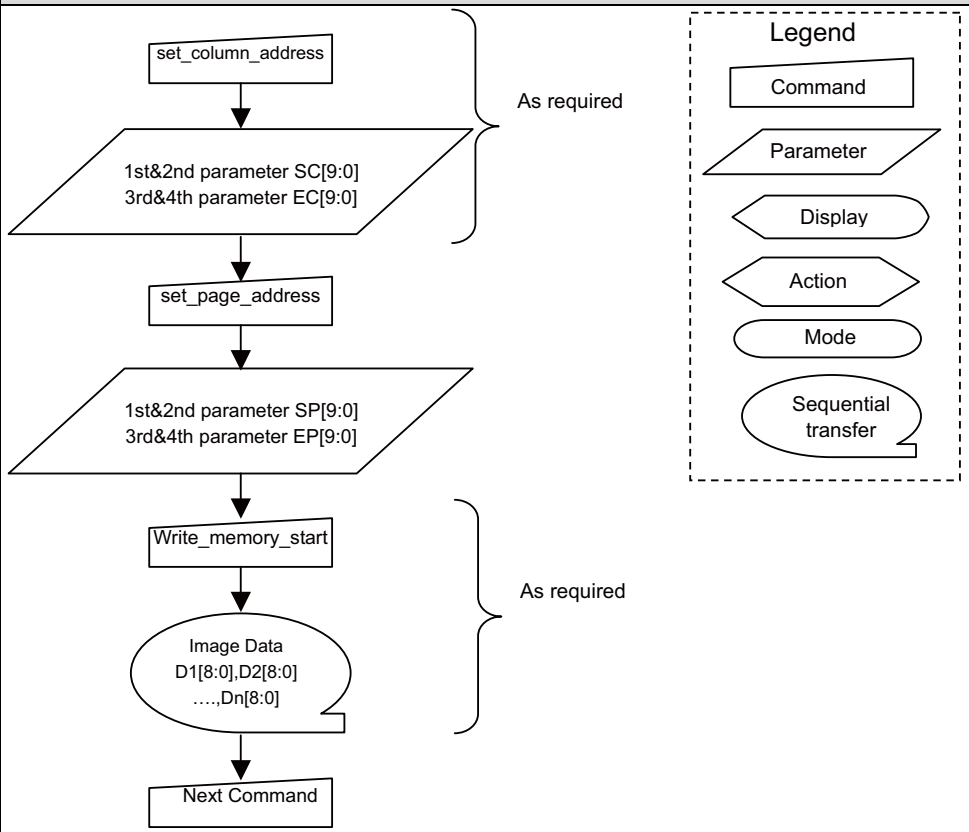
set_column_address: 2Ah

2Ah	set_column_address												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	0	1	0	2Ah
1st parameter	1	1	↑	X	0	0	0	0	0	0	SC[9]	SC[8]	XXh
2nd parameter	1	1	↑	X	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	XXh
3rd parameter	1	1	↑	X	0	0	0	0	0	0	EC[9]	EC[8]	XXh
4th parameter	1	1	↑	X	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	XXh
Description	This command defines the column extent of the frame memory accessed by the host processor. The values of SC[9:0] and EC[9:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed. Example  X=Don't care.												
Restriction	SC [9:0] must be equal to or less than EC[9:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in the following cases. • If set_address_mode B5 = 0: SC[9:0] or EC[9:0] > 167h • If set_address_mode B5 = 1: SC[9:0] or EC[9:0] > 27Fh												

2Ah	set_column_address
Flow Chart	

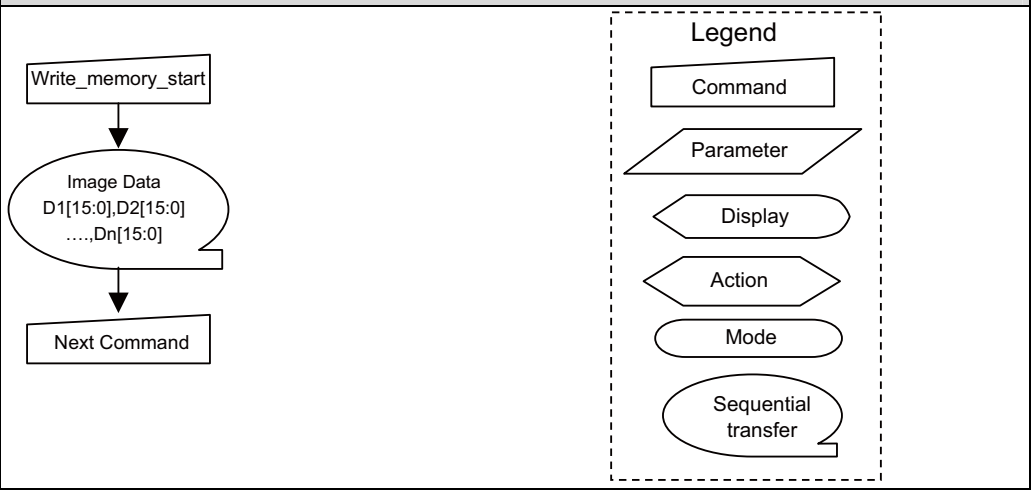
set_page_address: 2Bh

2Bh	set_page_address												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	0	1	1	2Bh
1st parameter	1	1	↑	X	0	0	0	0	0	0	SP[9]	SP[8]	XXh
2nd parameter	1	1	↑	X	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	XXh
3rd parameter	1	1	↑	X	0	0	0	0	0	0	EP[9]	EP[8]	XXh
4th parameter	1	1	↑	X	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	XXh
Description	This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed. The values of SP[9:0] and EP[9:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. Example  X = Don't care												
Restriction	SP[9:0] must always be equal to or less than EP[9:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in the following cases. • If set_address_mode B5 = 0: SP[9:0] or EP[9:0] > 27Fh • If set_address_mode B5 = 1: SP[9:0] or EP[9:0] > 167h												

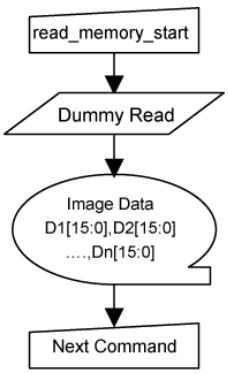
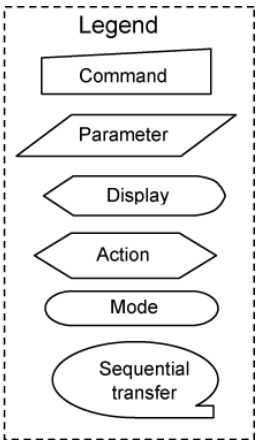
2Bh	set_page_address
Flow Chart	

write_memory_start: 2Ch

2Ch	write_memory_start												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	1	0	0	2Ch
1st pixel data	1	1	↑	D1 [15:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
: :	1	1	↑	Dx [15:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth pixel data	1	1	↑	Dn [15:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data 1 is stored in frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If Frame Memory Access and Interface setting (B3h) WEMODE = 0: If the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. If Frame Memory Access and Interface setting (B3h) WEMODE = 1 When the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are set to the Start Column and Start Page respectively. Then subsequent data are written to the frame memory. Sending any other command will stop writing to the frame memory. See DBI Data Format and DSI Data Format for write data formats in DBI Type B 16-/8-bit bus interface and DSI. X=Don't care.												
Restriction	In all color modes, there are no restrictions on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.												

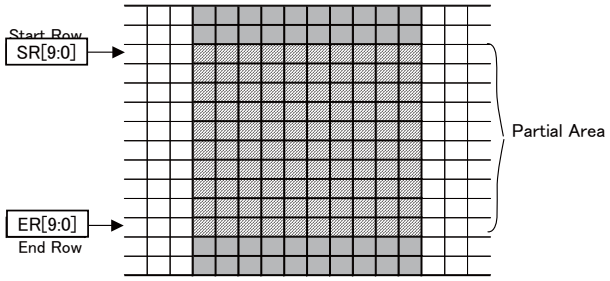
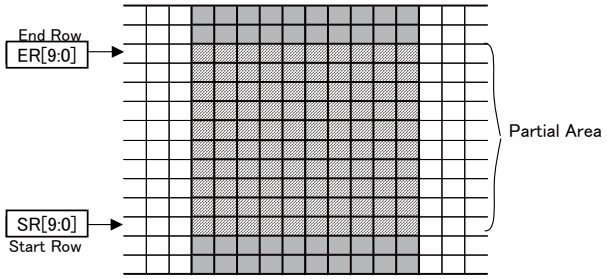
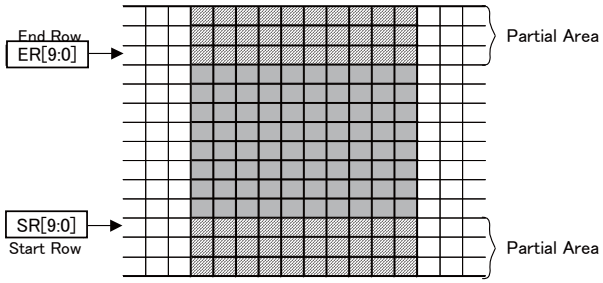
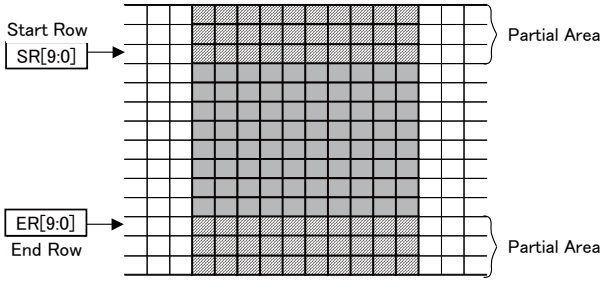
2Ch	write_memory_start
Flow Chart	

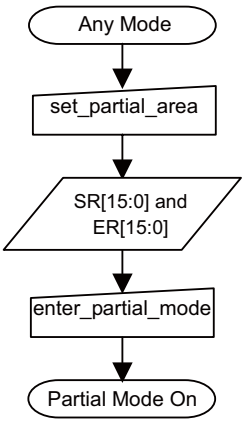
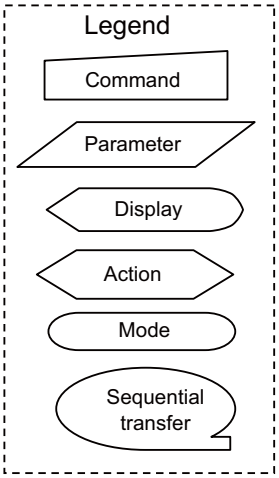
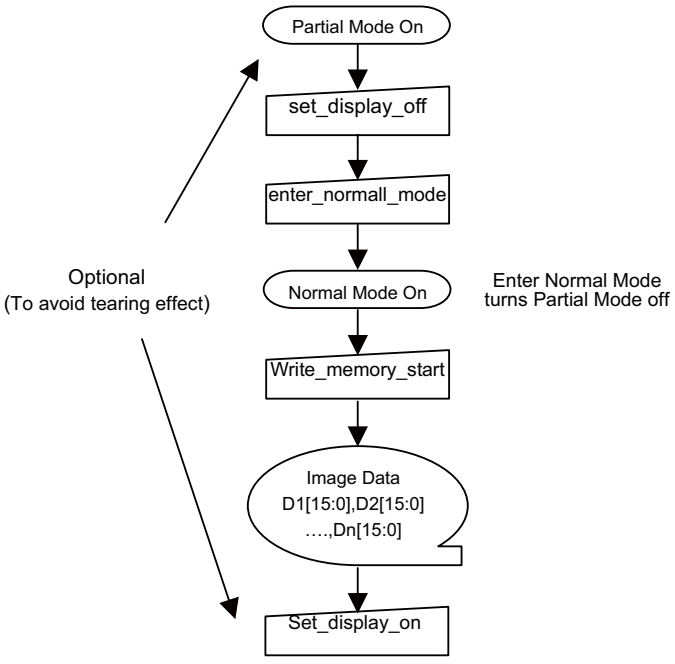
read_memory_start: 2Eh

2Eh	read_memory_start												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	1	1	0	2Eh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st pixel data	1	↑	1	D1 [15:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
:	1	↑	1	Dx [15:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth pixel data	1	↑	1	Dn [15:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the frame memory to the host processor. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data are read from the frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction." If read operation continued after (EP, EC) data were read, the last data (EP, EC) continue to be read. Any other written command stops frame memory read. See DBI Data Format and DSI Data Format for read data formats in DBI Type B 16-/8-bit bus interface and DSI, respectively. X = Don't care.												
Restriction	In all color modes, the Frame memory read is always 24 bits so there is no restriction on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.												
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed.												

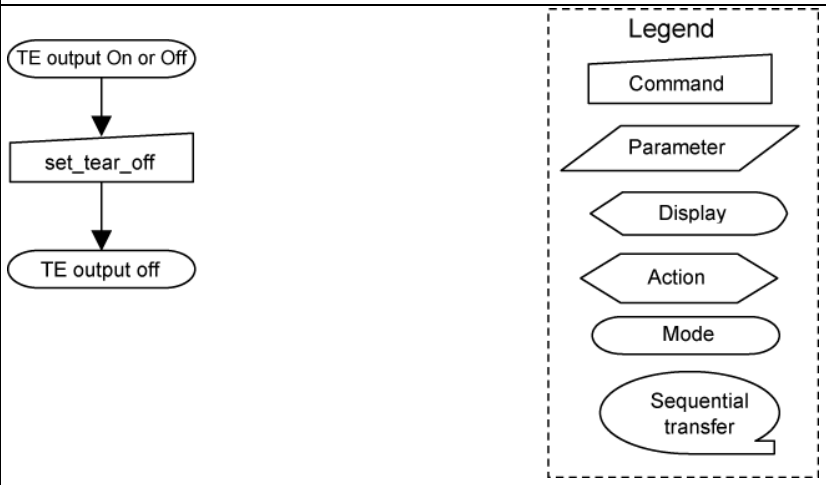
set_partial_area: 30h

30h	set_partial_area												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	0	0	0	0	30h
1st parameter	1	1	↑	X	0	0	0	0	0	0	SR[9]	SR[8]	000h
2nd parameter	1	1	↑	X	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	… 35Fh
3rd parameter	1	1	↑	X	0	0	0	0	0	0	ER[9]	ER[8]	000h
4th parameter	1	1	↑	X	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	… 35Fh

30h	set_partial_area
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command; the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. End Row > Start Row (set_address_mode(36h) B4=0)  End Row > Start Row(set_address_mode(36h) B4=1)  End Row < Start Row (set_address_mode(36h) B4=0)  End Row < Start Row (set_address_mode(36h) B4=1)  If End Row = Start Row, the partial area will be one row deep. X = Don't care.

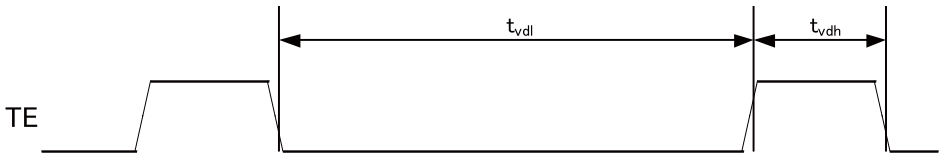
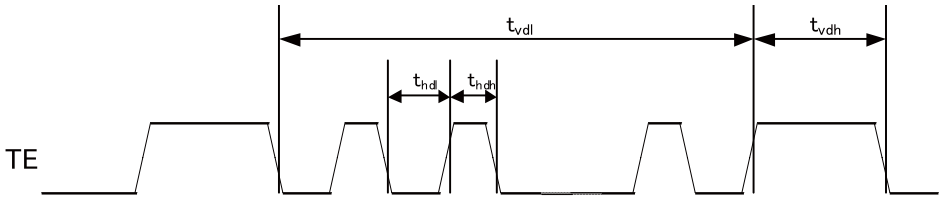
30h	set_partial_area
Restriction	SR[9:0] and ER[9:0] shall not be greater than 27Fh. The bits other than SR[9:0] and ER[9:0] are “Don’t care.”
Flow Chart	1. To enter Partial mode   2. To exit Partial mode 

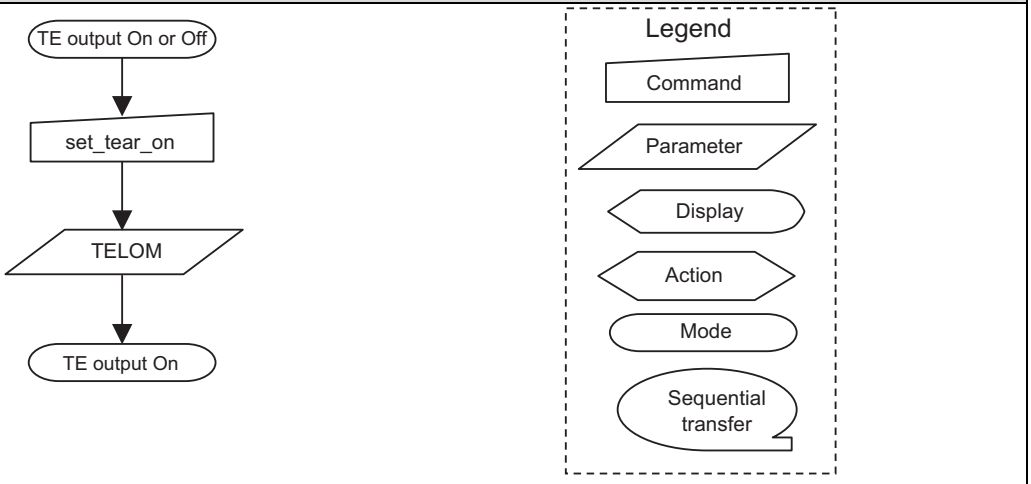
set_tear_off: 34h

34h	set_tear_off												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	0	1	0	0	34h
Parameter	None												
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already off.												
Flow Chart													

set_tear_on: 35h

<table>
<tr><td>35h</td><td colspan="13">set_tear_on</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[15:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>TEL OM</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on the display module’s Tearing Effect output signal on the TE signal line.
The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Refresh order).
The Tearing Effect Line On has one parameter, TELOM, which describes the Tearing Effect Output Line mode.
See “TE Pin Output Signal“ for details.

TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only.
The Tearing Effect Output line shall be high during vertical blanking period.
 
TELOM = 1: The tearing Effect Output line consists of both V-blanking and H-blanking information.
 
Vertical blanking period: Non-lit display period in (back porch + front porch + partial mode)
<table><tr><td>tvdl</td><td>Number of lines set by NL</td></tr><tr><td>tvdh</td><td>Number of lines set by BP + Number of lines set by FP</td></tr><tr><td>thdl</td><td>3 clocks (based on internal operation clock)</td></tr><tr><td>thdh</td><td>Number of clocks set by RTN – 3 clocks (based on internal operation clock)</td></tr></table>
Notes: 1. The Tearing Effect pin goes to the low level when Tearing Effect Line is On and Sleep mode is On.
2. TELOM=0 when DSI TE-report is used.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON. Changes in parameter TELOM are enabled from the next frame period.</td></tr>
</table>

35h	set_tear_on
Flow Chart	

set_address_mode: 36h

36h	set_address_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	1	0	1	1	0	36h
1st parameter	1	1	↑	X	B7	B6	B5	B4	0	0	0	B0	XXh

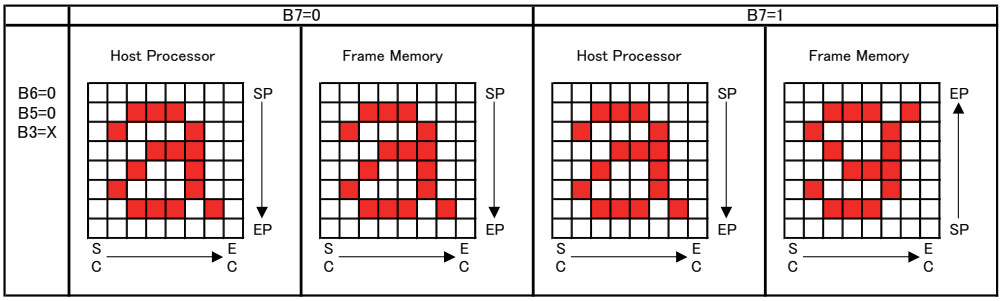
Description

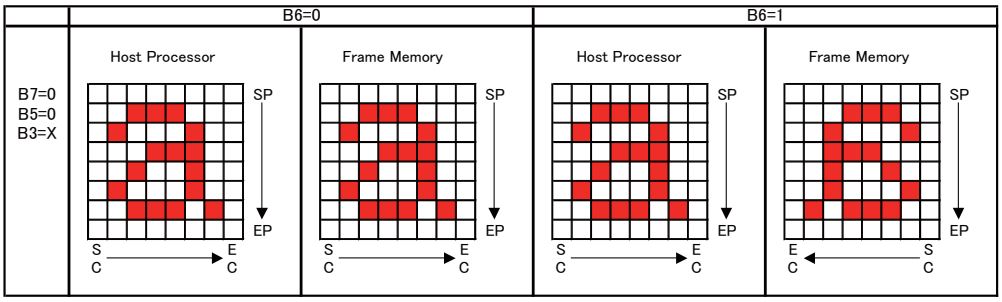
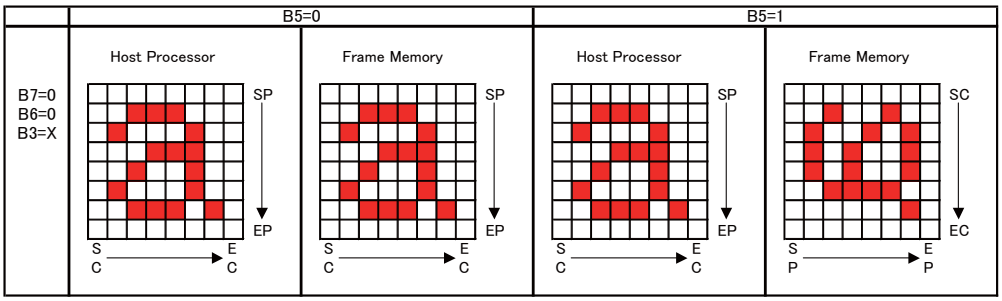
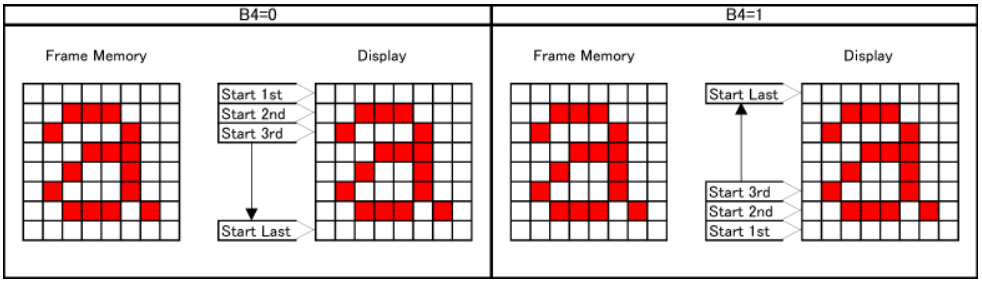
This command sets the read/write scanning direction of frame memory. No status bits are changed.

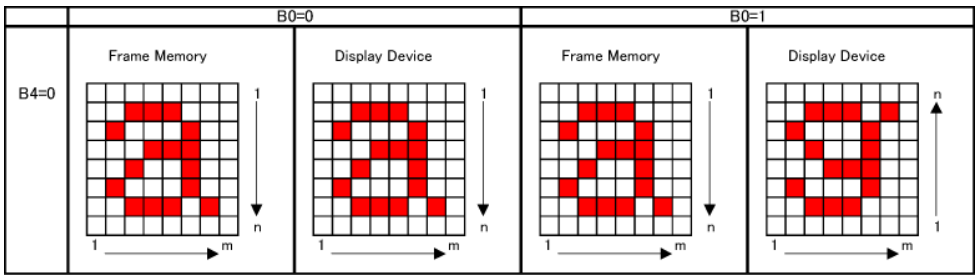
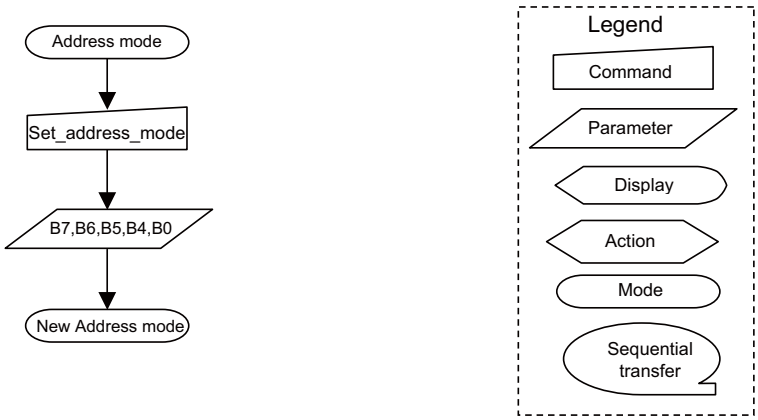
Bit	Description	Comment	Symbol
D7	Page Address Order		B7
D6	Column Address Order		B6
D5	Page/Column Addressing Order		B5
D4	Display Device Line Refresh Order		B4
D3	RGB/BGR Order	Don't care	-
D2	Display Data Latch Data Order	Don't care	-
D1	Flip Horizontal	Don't care	-
D0	Flip Vertical		B0

- Bit B7 - Page Address Order

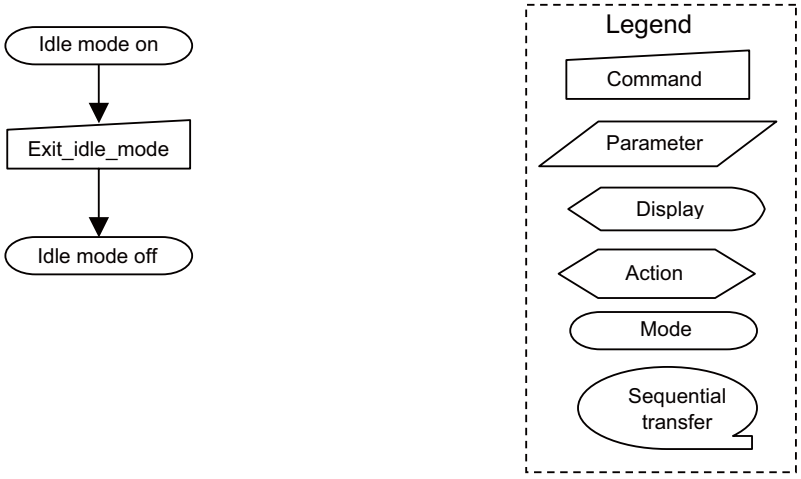
'0' = Top to Bottom
'1' = Bottom to Top



36h	set_address_mode
Description	• Bit B6 - Column Address Order '0' = Left to Right '1' = Right to Left  • Bit B5 – Page/Column Addressing Order '0' = Normal Mode '1' = Reverse Mode  Note: See Chapter "Frame Memory" for bits B7-5. • Bit B4 – Display Device Line Refresh Order '0' = LCD Refresh Top to Bottom '1' = LCD Refresh Bottom to Top (Memory reading and gate scanning directions invert simultaneously.) 

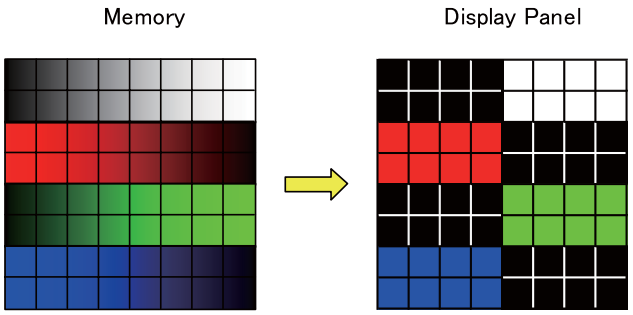
36h	set_address_mode
Description	• Bit B3 – RGB/BGR order This bit is not applicable. Set to “0”. (Not supported) • Bit B2 – Display Data Latch Data Order This bit is not applicable. Set to “0”. (Not supported) • Bit B1 – Flip Horizontal This bit is not applicable. Set to “0”. (Not supported) • Bit B0 – Flip Vertical ‘0’ = Normal ‘1’ = Flipped (Gate scanning direction inverts.)  X = Don’t care
Restriction	-
Flow Chart	

exit_idle_mode: 38h

38h	exit_idle_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	0	0	0	38h
Parameter	None												
Description	This command causes the display module to exit Idle mode. LCD can display up to 16,777,216 colors when Idle mode is off. X = Don't care												
Restriction	This command has no effect when the display module is not in Idle mode.												
Flow Chart													

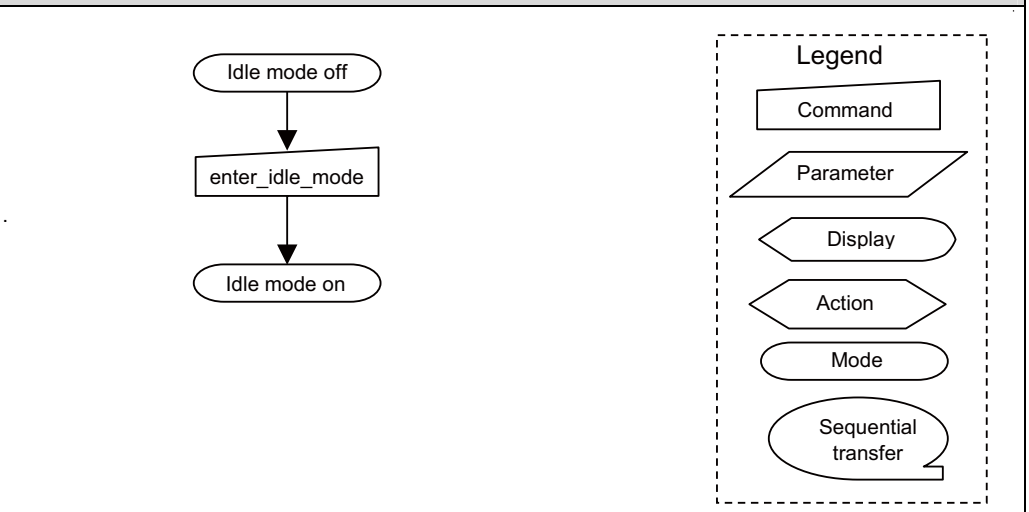
enter_idle_mode: 39h

39h	enter_idle_mode												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	0	0	1	39h
Parameter	None												
Description	This command causes the display module to enter Idle mode. In the Idle mode, color expression is reduced. Eight color depth data are displayed using MSB of each R, G and B color components in the Frame Memory. In this mode, only grayscale levels V0 and V255 are used and power supplies for other levels V1-V254 are halted, reducing power consumption. It is possible to reduce power consumption by optimizing settings for Idle Mode. In the Idle mode, the settings of Gamma Set A (C8h), Gamma Set B (C9h), and Gamma Set C (CAh) registers are applied to R, G, and B dots, respectively.												
Restriction	This command has no effect when the module is already in Idle mode.												



Memory Contents vs. Display Color			
	R[7:0]	G[7:0]	B[7:0]
Black	0 X X X X X X X	0 X X X X X X X	0 X X X X X X X
Blue	0 X X X X X X X	0 X X X X X X X	1 X X X X X X X
Red	1 X X X X X X X	0 X X X X X X X	0 X X X X X X X
Magenta	1 X X X X X X X	0 X X X X X X X	1 X X X X X X X
Green	0 X X X X X X X	1 X X X X X X X	0 X X X X X X X
Cyan	0 X X X X X X X	1 X X X X X X X	1 X X X X X X X
Yellow	1 X X X X X X X	1 X X X X X X X	0 X X X X X X X
White	1 X X X X X X X	1 X X X X X X X	1 X X X X X X X

X = Don’t care

39h	enter_idle_mode
Flow Chart	

set_pixel_format: 3Ah

3Ah	set_pixel_format												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	0	1	0	3Ah
1st parameter	1	1	↑	X	0	0	0	0	0	D2	D1	D0	XXh

Description

This command is used to define the format of RGB picture data, which are to be transferred via the DBI/DSI. The formats are shown in the following table:

Bit D[6:4] – Setting inhibited.
Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection), DSI
Bit D7 and D3 – These bits are not applicable. Set to "0".

Control Interface Color Format	D2	D1	D0
Setting inhibited	0	0	0
Setting inhibited	0	0	1
Setting inhibited	0	1	0
Setting inhibited	0	1	1
Setting inhibited	1	0	0
16 bits/pixel (65,536 colors)	1	0	1
18 bits/pixel (262,144 colors)	1	1	0
24 bits/pixel (16,777,216 colors)	1	1	1

See "DBI Data Format" for each data format.

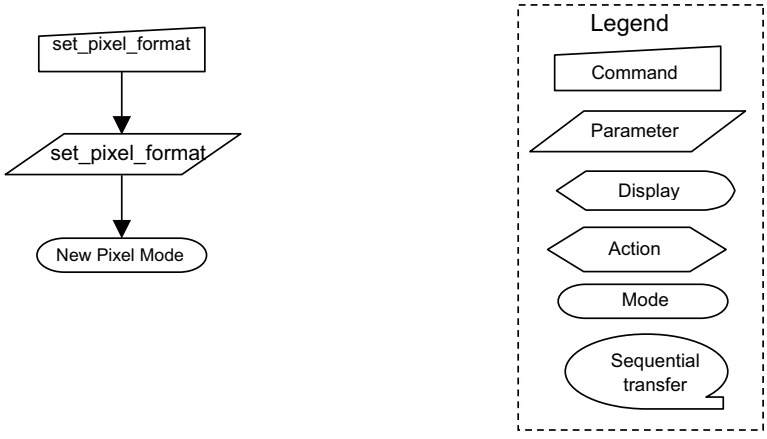
Notes 1: When "the bits settings are disabled" are set, undesirable image will be displayed on the panel.

2: Other settings than D[2:0] = 5 (16 bits/pixel), 6 (18 bits/pixel), and 7 (24 bits/pixel) are disabled in DBI Type B operation.

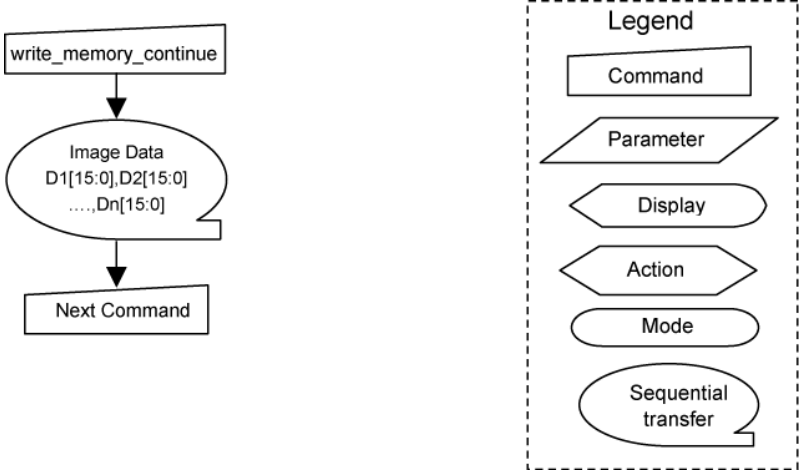
X = Don't care

Restriction: There is no visible effect until the frame memory is written.

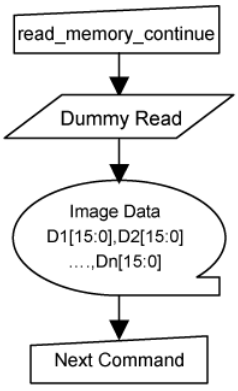
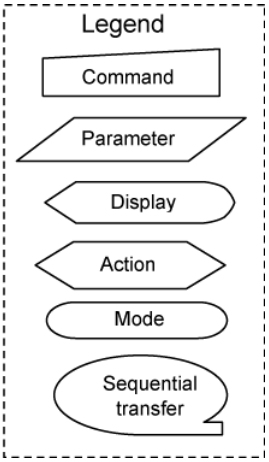
Flow Chart



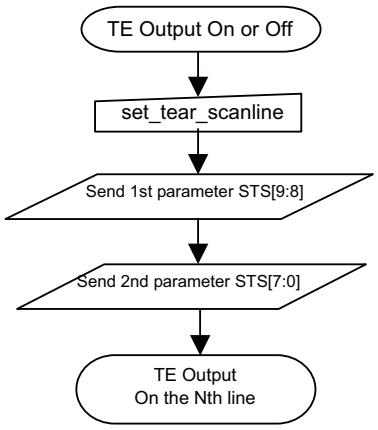
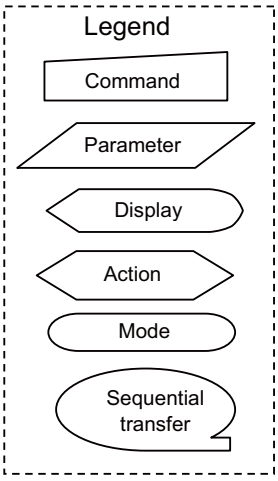
write_memory_continue: 3Ch

3Ch	write_memory_continue												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3Ch
1st pixel data	1	1	↑	D1 [15:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … FFFh
:	1	1	↑	Dx [15:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … FFFh
Nth pixel data	1	1	↑	Dn [15:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … FFFh
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Frame Memory Access and Interface setting (B3h): WEMODE = 0 If the number of pixels in the transfer data exceeds (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. Frame Memory Access and Interface setting (B3h): WEMODE = 1 When the number of pixels in the transfer data exceeds (EC-SC+1)*(EP-SP+1), the column register and the page register are reset to the Start Column/Start Page positions, and the subsequent data are written to the frame memory. X=Don't care												
Restriction	If write_memory_continue command is executed without setting set_column_address (2Ah), set_page_address (2Bh), and set_address_mode (36h), there is no guarantee that data are correctly written to the frame memory. If data is not transferred in units of pixels, the extra data is regarded as invalid.												
Flow Chart													

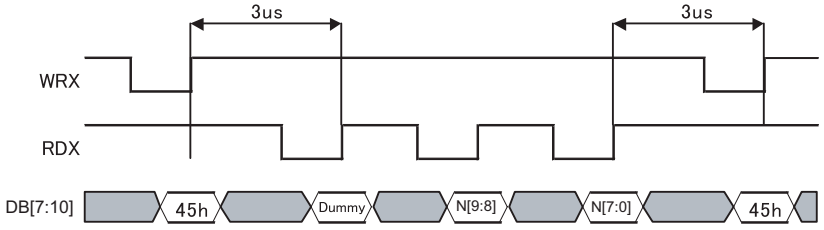
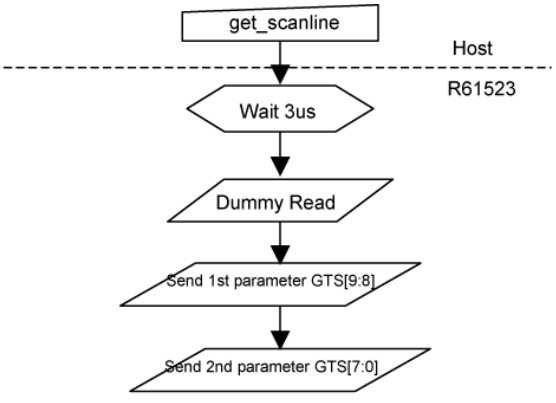
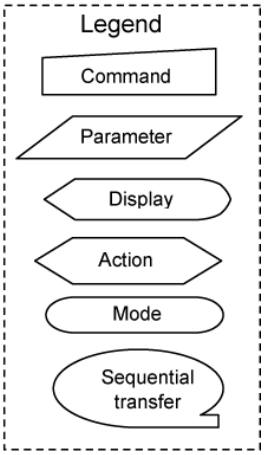
read_memory_continue: 3Eh

3Eh	read_memory_continue												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	1	1	0	3Eh
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Pixel data	1	↑	1	D1 [15:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … FFFh
:	1	↑	1	Dx [15:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … FFFh
Nth Pixel data	1	↑	1	Dn [15:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … FFFh
Description	This command transfers image data from the host processor to the display module's frame memory, continuing from the location following the previous read_memory_continue or read_memory_start command. If read operation is executed after (EP. EC) is read, the last data (EP, EC) continue to be output. After pixel data 1 is written to frame memory (SC, SP), address counter's direction differs depending on setting of set_address_mode (36h)'s Bits 5, 6, 7. See "Host Processor to Memory Write/Read Direction." X = Don't care												
Restriction	In any color mode, the format returned by read_memory_continue is always 24 bits so there is no restriction on the length of parameter. If data is not transferred in units of pixels, the extra data is regarded as invalid.												
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed. 												

set_tear_scanline:44h

44h	set_tear_scanline												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	X	0	0	0	0	0	0	STS [9]	STS [8]	0Xh
2nd Parameter	1	1	↑	X	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by STS [9:0]. TE line is unaffected by change in B4 bit of set_address_mode command. See "TE Pin Output Signal" for the relationship between the setting value and waveform. X =Don't care.												
Restriction	The command takes effect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame. Setting is disabled when TELOM=1 of set_tear_on (35h). Make sure that STS [9:0] ≤ NL (number of line) + 1.												
Flow Chart	 												

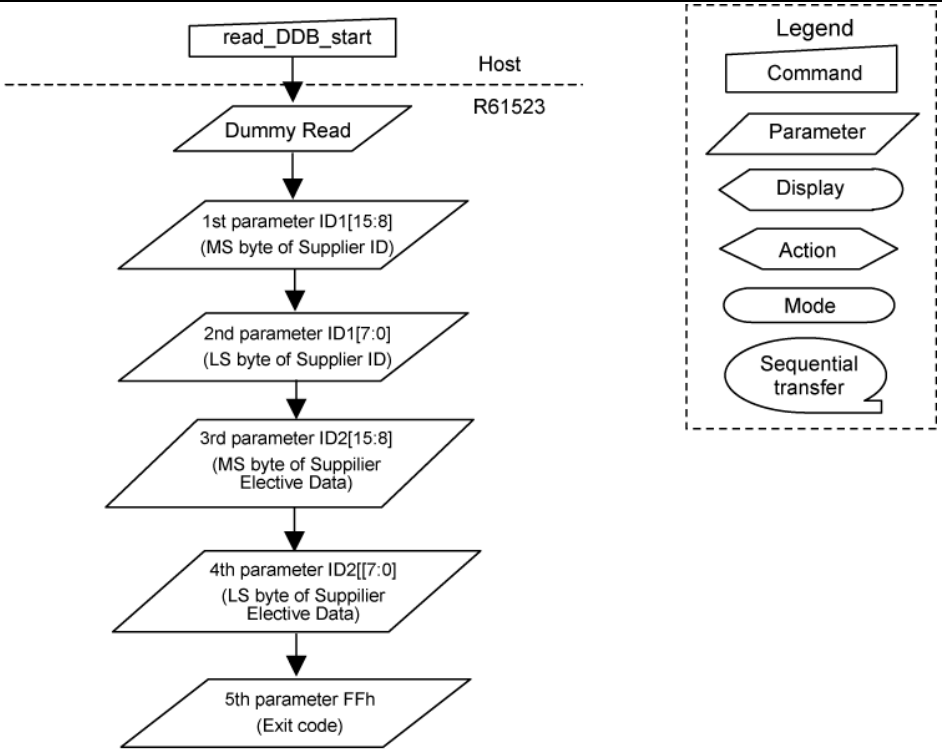
get_scanline: 45h

45h	get_scanline												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	1	45h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	1	↑	1	X	0	0	0	0	0	0	GTS [9]	GTS [8]	0Xh
2nd parameter	1	↑	1	X	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	XXh
Description	The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back porch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined. X = Don't care												
Restriction	After get_line command is input, it takes 3µs or more to read it. After parameters are read, wait 3µs or more to input this command again. 												
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed. 												

read_DDB_start: A1h

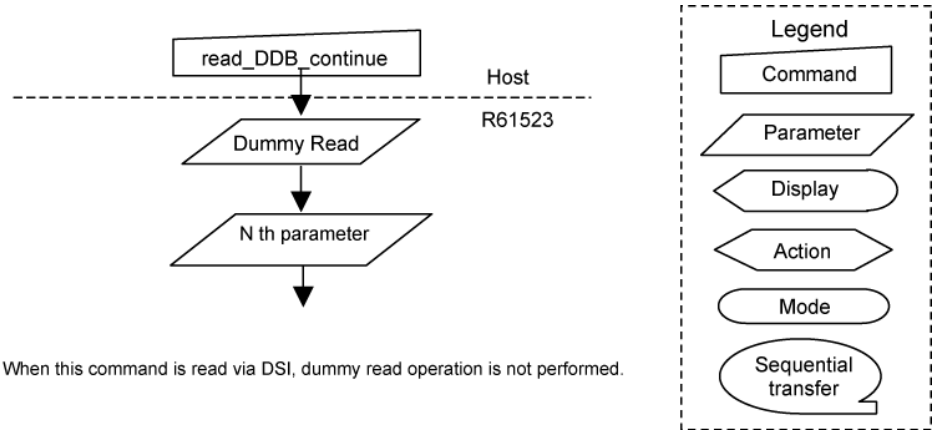
A1h	read_DDB_start												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	0	0	0	0	1	A1h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	1	↑	1	X	1	1	1	1	1	1	1	1	FFh
Description	The command returns information from the display module as follows: 1st parameter: MS byte of Supplier ID (ID1[15:8]) 2nd parameter: LS byte of Supplier ID (ID1[7:0]) 3rd parameter: Supplier Elective Data (ID2[15:8]) 4th parameter: Supplier Elective Data (ID2[7:0]) 5th parameter: Exit Code (FFh) Supplier ID stored in internal NVM is read. X=Don't care												
Restriction	-												

Flow Chart



Note: When this command is read via DSI, dummy read operation is not performed.

read_DDB_continue: A8h

A8h	read_DDB_continue												
	DCX	RDX	WRX	DB[15:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	0	1	0	0	0	A8h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	1	↑	1	X	1	1	1	1	1	1	1	1	FFh
Description	This command continues read operation from the position where the operation is halted by read_DDB_continue or read_DDB_start. For the position that information is returned, see read_DDB_start (A1h). X=Don't care												
Restriction	To fix the position that information is returned, execute read_DDB_start command and parameter read operation at least once before read_DDB_continue command is executed. If they are not executed, the value returned by read_DDB_continue command is invalid.												
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed.												

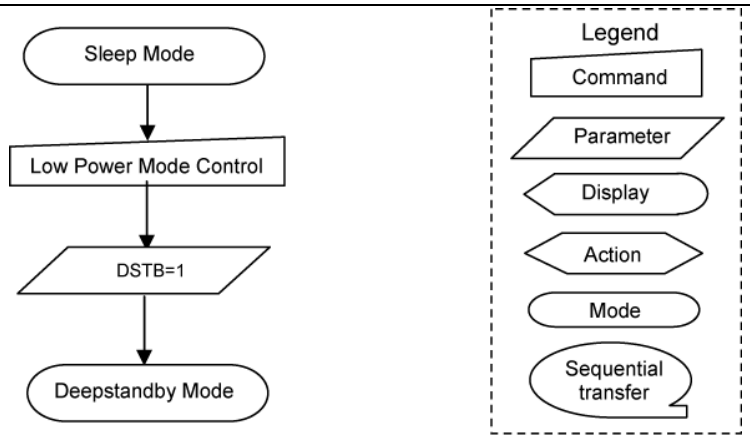
Manufacturer Command

Additional User Command

MCAP: Manufacturer Command Access Protect (B0h)

<table>
<tr><td>B0h</td><td colspan="13">MCAP (Manufacturer Command Access Protect)</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB15-8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>MCAP[2]</td><td>MCAP[1]</td><td>MCAP[0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">
Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read
(Note: When this command is read via DSI, dummy read operation is not performed.)
MCAP[2:0]
The LCD driver is required to release Access Protect before inputting a Manufacturer Command. This command releases Protect parameters so that Manufacturer Command inputs are enabled. When the conditions to release Protect, tabulated below, are met, Manufacturer Command inputs are enabled.
<table>
<tr><td rowspan="2">Command</td><td colspan="6">MCAP[2:0]</td></tr>
<tr><td>3’b000</td><td>3’b001</td><td>3’b010</td><td>3’b011 (default)</td><td>3’b100</td><td>3’b101-111</td></tr>
<tr><td>B0</td><td>Yes</td><td rowspan="4">Setting inhibited</td><td>Yes</td><td>Yes</td><td>Yes</td><td rowspan="4">Setting inhibited</td></tr>
<tr><td>B1-BFh</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td></tr>
<tr><td>C0-D4h</td><td>Yes</td><td>No</td><td>No</td><td>Yes</td></tr>
<tr><td>E0-E1h</td><td>Fixed</td><td>Fixed</td><td>Fixed</td><td>Yes</td></tr>
<tr><td>D6-D9h</td><td>Fixed</td><td rowspan="3"></td><td>Fixed</td><td>Fixed</td><td>Yes</td><td rowspan="3"></td></tr>
<tr><td>E2, E3, E6h</td><td>Yes</td><td>No</td><td>No</td><td>Yes</td></tr>
<tr><td>E4, E5, F3-FEh</td><td>Fixed</td><td>Fixed</td><td>Fixed</td><td>Yes</td></tr>
</table>
Yes: Access is enabled. (Protect Off)
No: Access is disabled. (Protect On)
Fixed: Fixed to the initial value.
Once the LCD driver enables Manufacturer Command inputs, it keeps the state until MCAP[2:0] is written so that the LCD driver enters Protect ON state again. D6h-D9h and E2h-FEh are test registers. Do not access this command via them.
</td></tr>
<tr><td>Restriction</td><td colspan="13">After H/W Reset or exiting Deep Standby Mode, accessing a Manufacturer Command is restricted so that Manufacture Commands B1h-BFh inputs are identified as nop command.</td></tr>
</table>

Low Power Mode Control (B1h)

B1h	Low Power Mode Control												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	0	0	0	1	B1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	DSTB	XXh
Description	Write #A="1" #B=" ↑ " Read #A=" ↑ " #B=" 1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.) This command is used to enter the Deep Standby Mode. **DSTB** The Deep Standby Mode is entered when DSTB=1. Internal logic power supply circuit (VDD) is turned off, enabling low power consumption. In the Deep Standby mode, data stored in the Frame Memory and the Instructions are not retained. Rewrite them after the Deep Standby mode is exited. Do not input SW-Reset or other commands during the Deep Standby mode. See "State and Command Sequence" for Deep Standby Mode On/Off Sequence.												
Restriction	DSTB can be entered only from the Sleep mode. Access to DSTB when the Sleep mode is off has no effect (treated as nop).												
Flow Chart													

Frame Memory Access and Interface Setting (B3h)

B3h	Frame Memory Access and Interface Setting												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	1	B3h
1st parameter	1	#A	#B	X	1	0	0	SEL DL	0	0	WE MODE	0	XXh
2nd parameter	1	#A	#B	X	EPF [1]	EPF [0]	DFM [1]	DFM [0]	0	TEI [2]	TEI [1]	TEI [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is performed.)												

WEMODE

After frame memory write operation reaches the end of window address area, the next write start position is selected.

WEMODE = 0: The write start position is not reset to the start of window address, and the subsequent data are disregarded. (Default)

WEMODE = 1: The write start position is reset to the start of window address area to overwrite the subsequent data to the previous data.

TEI [2:0]

These bits are used to define interval between outputs of TE signal. Set in accordance with update cycle and transfer rate of the display data.

TEI[2]	TEI[1]	TEI[0]	Interval
0	0	0	Every frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other setting			Setting inhibited

EPF[1:0]

These bits are used to set data format when 16/18bpp (R, G, B) data are converted to 24bpp (r, g, b) stored in internal frame memory.

EPF[1:0]	16bpp(R,G,B) → 24bpp(r,g,b)	18bpp(R,G,B) → 24bpp(r,g,b)
2'h0	"0" is written to the LSB. r[7:0]={ R[4:0], 3'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[4:0], 3'h0 } Note that the data are converted as follows: R[4:0], B[4:0]=5'h1F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF	"0" is written to the LSB. r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 } Note that the data are converted as follows: R[5:0], B[5:0]=6'h3F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF
2'h1	"1" is written to the LSB. r[7:0]={ R[4:0], 3'h7 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[4:0], 3'h7 } Note that the data are converted as follows: R[4:0], B[4:0]=5'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00	"1" is written to the LSB. r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 } Note that the data are converted as follows: R[5:0], B[5:0]=6'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00
2'h2	The MSB value is written to the LSB. r[7:0]={ R[4:0], R[4:2] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[4:0], B[4:2] }	The MSB value is written to the LSB. r[7:0]={ R[5:0], R[5:4] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[5:0], B[5:4] }
2'h3	Setting inhibited	Setting inhibited

DFM[1:0]

The bit is used to define image data write/read format to the Frame Memory in DBI Type B 16 bit bus interface operation. See "DBI Data Format" for details.

SELDL

SELDL is used to adjust the number of DSI Data lanes when DSI is selected.

SELDL=0: DSI Data 2 lanes
SELDL=1: DSI Data 1 lane

Connect to unused DSI pins (DSID1PLVL, DSID1NLVL, DSID1P, DSI1N)
When DSI is selected, access this command in the Escape mode.

How to change the number of DSI Data Lane

Change the number of DSI Data Lane right after a reset using SELDL.

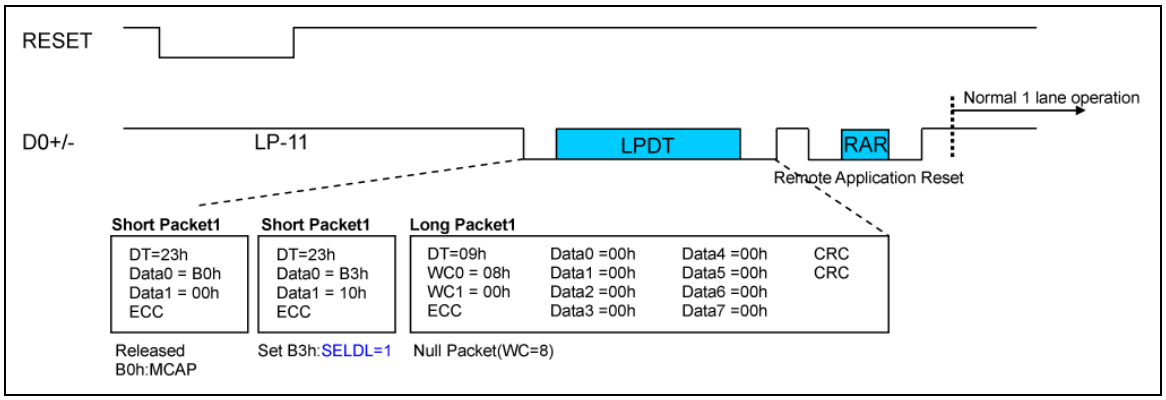


Figure 28

Read Checksum and ECC Error Counter (B5h)

B5h	Read Checksum and ECC Error Counter												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	0	1	0	1	B5h
1st parameter	1	#A	1	X	CSOUT[7]	CSOUT[6]	CSOUT[5]	CSOUT[4]	CSOUT[3]	CSOUT[2]	CSOUT[1]	CSOUT[0]	XXh
2nd parameter	1	#A	1	X	DSIECP[7]	DSIECP[6]	DSIECP[5]	DSIECP[4]	DSIECP[3]	DSIECP[2]	DSIECP[1]	DSIECP[0]	XXh
3rd parameter	1	#A	1	X	DSIECE[7]	DSIECE[6]	DSIECE[5]	DSIECE[4]	DSIECE[3]	DSIECE[2]	DSIECE[1]	DSIECE[0]	XXh
Description	Read #A=" ↑ " #B=" 1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.)												

CSOUT[7:0]
These bits read checksum error count values. When checksum error occurs in DSI Long Packet reception, the value is counted up. When these bits are read, they are cleared to 8'h00.

DSIECP[7:0]
These bits read single-bit ECC error count values. When 1-bit ECC error occurs in DSI Packet Header reception, the value is counted up. When these bits are read, they are cleared to 8'h00.

DSIECE[7:0]
These bits read multi-bit ECC error count values. When 2-bit-or-more ECC error occurs in DSI Packet Header reception, the value is counted up. When these bits are read, they are cleared to 8'h00.

DSI Control (B6)

B6h	DSI Control												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	0	1	1	0	B6h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	DSITXDIV [1]	DSITXDIV [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: No dummy read when a read operation is performed using DSI.)												

DSITXDIV[1:0]

The bits are used to define the division ratio to generate transmit clock in LP mode. If DSICLK stops, data is transmitted by using the internal oscillator (14MHz).

Table 40

DSITXDIV[1:0]	DSICLK division ratio
2'b00	fDSICLK/4
2'b01	fDSICLK/8 (default)
2'b10	fDSICLK/16
2'b11	fDSICLK/32

Table 41 DSITXDIV Setting Example

Status of Clock Lane	Host to R61523		R61523 to Host		
	Bit Rate [Mbps]	fDSICLK [MHz]	Setting of DSITXDIV [1:0]	fTXCLK [MHz]	Bit rate [Mbps]
Active	300	150	2'b01	9.375	4.69
	200	100		12.5	6.25
	160	80	2'b00	20	10.0
	100	50		12.5	6.25
Inactive (Stop)	-	-	-	14.0 (fOSCCLK)	7.0

Back Light Control 1 (B8h)

B8h	Back Light Control 1												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	0	0	0	B8h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	BLCM	BLCON	XXh
2nd parameter	1	#A	#B	X	0	0	0	THREW0[4]	THREW0[3]	THREW0[2]	THREW0[1]	THREW0[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	THREW1[4]	THREW1[3]	THREW1[2]	THREW1[1]	THREW1[0]	XXh
4th parameter	1	#A	#B	X	ULMTW0[7]	ULMTW0[6]	ULMTW0[5]	ULMTW0[4]	ULMTW0[3]	ULMTW0[2]	ULMTW0[1]	ULMTW0[0]	XXh
5th parameter	1	#A	#B	X	ULMTW1[7]	ULMTW1[6]	ULMTW1[5]	ULMTW1[4]	ULMTW1[3]	ULMTW1[2]	ULMTW1[1]	ULMTW1[0]	XXh
6th parameter	1	#A	#B	X	LLMTW0[7]	LLMTW0[6]	LLMTW0[5]	LLMTW0[4]	LLMTW0[3]	LLMTW0[2]	LLMTW0[1]	LLMTW0[0]	XXh
7th parameter	1	#A	#B	X	LLMTW1[7]	LLMTW1[6]	LLMTW1[5]	LLMTW1[4]	LLMTW1[3]	LLMTW1[2]	LLMTW1[1]	LLMTW1[0]	XXh
8th parameter	1	#A	#B	X	0	0	0	0	PITCHW[3]	PITCHW[2]	PITCHW[1]	PITCHW[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	CGAPW[4]	CGAPW[3]	CGAPW[2]	CGAPW[1]	CGAPW[0]	XXh
10th parameter	1	#A	#B	X	0	0	0	COEFK0[4]	COEFK0[3]	COEFK0[2]	COEFK0[1]	COEFK0[0]	XXh
11th parameter	1	#A	#B	X	0	0	0	COEFK1[4]	COEFK1[3]	COEFK1[2]	COEFK1[1]	COEFK1[0]	XXh
12th parameter	1	#A	#B	X	TBL3[7]	TBL3[6]	TBL3[5]	TBL3[4]	TBL3[3]	TBL3[2]	TBL3[1]	TBL3[0]	XXh
13th parameter	1	#A	#B	X	TBL4[7]	TBL4[6]	TBL4[5]	TBL4[4]	TBL4[3]	TBL4[2]	TBL4[1]	TBL4[0]	XXh
14th parameter	1	#A	#B	X	TBL5[7]	TBL5[6]	TBL5[5]	TBL5[4]	TBL5[3]	TBL5[2]	TBL5[1]	TBL5[0]	XXh
15th parameter	1	#A	#B	X	TBL6[7]	TBL6[6]	TBL6[5]	TBL6[4]	TBL6[3]	TBL6[2]	TBL6[1]	TBL6[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.)												
Restriction	Note: Make sure that BLC function is turned off (B8h: BLCON=0) when changing register values on the 1st to 15th parameters and switching BLC modes (B8h: BLCM).												

BLCM

The bit is used to select BLC mode. There are two sets for each of THREW, ULMTW, LLMTW, and COEFK registers, enabling different settings for different display images. Before changing BLCM value, turn BLC function off (B8h: BLCON=0).

Table 42

BLCM	BLC mode	Enabled register			
0	Mode 0	THREW0 [4:0]	ULMTW0 [7:0]	LLMTW0 [7:0]	COEFK0 [4:0]
1	Mode 1	THREW1 [4:0]	ULMTW1 [7:0]	LLMTW1 [7:0]	COEFK1 [4:0]

BLCON

The bit is used to turn the BLC function ON/OFF.

Table 43

BLCON	BLC function
0	OFF
1	ON

The BLC function is disabled when the Partial, Idle, or Display Invert mode is On. To use the BLC function (BLCON=1), make sure that the Normal mode is entered and the Idle and Display Invert modes are exited.

THREW0[4:0], THREW1[4:0]
These bits are used to specify percentage from the threshold to grayscale number 255 in the total of grayscale data. This is the ratio (percentage) of the maximum number of pixels that makes display image white (= data “255”) to the total of pixels by image processing.

Percentage of pixels =

Number of pixels with the grayscale from the threshold to grayscale number 255/ Number of all pixels

THREW0 is enabled when BLCM=0.
THREW1 is enabled when BLCM=1.

Table 44

THREW0[4:0] THREW1[4:0]	Percentage of pixels	THREW0[4:0] THREW1[4:0]	Percentage of pixels
5’h00	0%	5’h10	32%
5’h01	2%	5’h11	34%
5’h02	4%	5’h12	36%
5’h03	6%	5’h13	38%
5’h04	8%	5’h14	40%
5’h05	10%	5’h15	42%
5’h06	12%	5’h16	44%
5’h07	14%	5’h17	46%
5’h08	16%	5’h18	48%
5’h09	18%	5’h19	50%
5’h0A	20%	5’h1A	52%
5’h0B	22%	5’h1B	54%
5’h0C	24%	5’h1C	56%
5’h0D	26%	5’h1D	58%
5’h0E	28%	5’h1E	60%
5’h0F	30%	5’h1F	62%

ULMTW0[7:0], ULMTW1[7:0]

The possible maximum value of the threshold grayscale value (Dth) that makes display image white is set in units of one grayscale.

ULMTW0 is enabled when BLCM=0. ULMTW1 is enabled when BLCM=1.

Table 45

ULMTW0 [7:0] ULMTW1 [7:0]	**Maximum grayscale level (Frame Memory data)**	ULMTW0 [7:0] ULMTW1 [7:0]	**Maximum grayscale level** (Frame Memory data)	ULMTW0 [7:0] ULMTW1 [7:0]	**Maximum grayscale level** (Frame Memory data)	ULMTW0 [7:0] ULMTW1 [7:0]	**Maximum grayscale level** (Frame Memory data)
8'h00	8'h00	8'h40	8'h40	8'h80	8'h80	8'hC0	8'hC0
8'h01	8'h01	8'h41	8'h41	8'h81	8'h81	8'hC1	8'hC1
8'h02	8'h02	8'h42	8'h42	8'h82	8'h82	8'hC2	8'hC2
8'h03	8'h03	8'h43	8'h43	8'h83	8'h83	8'hC3	8'hC3
8'h04	8'h04	8'h44	8'h44	8'h84	8'h84	8'hC4	8'hC4
8'h05	8'h05	8'h45	8'h45	8'h85	8'h85	8'hC5	8'hC5
8'h06	8'h06	8'h46	8'h46	8'h86	8'h86	8'hC6	8'hC6
8'h07	8'h07	8'h47	8'h47	8'h87	8'h87	8'hC7	8'hC7
8'h08	8'h08	8'h48	8'h48	8'h88	8'h88	8'hC8	8'hC8
8'h09	8'h09	8'h49	8'h49	8'h89	8'h89	8'hC9	8'hC9
8'h0A	8'h0A	8'h4A	8'h4A	8'h8A	8'h8A	8'hCA	8'hCA
8'h0B	8'h0B	8'h4B	8'h4B	8'h8B	8'h8B	8'hCB	8'hCB
8'h0C	8'h0C	8'h4C	8'h4C	8'h8C	8'h8C	8'hCC	8'hCC
8'h0D	8'h0D	8'h4D	8'h4D	8'h8D	8'h8D	8'hCD	8'hCD
8'h0E	8'h0E	8'h4E	8'h4E	8'h8E	8'h8E	8'hCE	8'hCE
8'h0F	8'h0F	8'h4F	8'h4F	8'h8F	8'h8F	8'hCF	8'hCF
8'h10	8'h10	8'h50	8'h50	8'h90	8'h90	8'hD0	8'hD0
8'h11	8'h11	8'h51	8'h51	8'h91	8'h91	8'hD1	8'hD1
8'h12	8'h12	8'h52	8'h52	8'h92	8'h92	8'hD2	8'hD2
8'h13	8'h13	8'h53	8'h53	8'h93	8'h93	8'hD3	8'hD3
8'h14	8'h14	8'h54	8'h54	8'h94	8'h94	8'hD4	8'hD4
8'h15	8'h15	8'h55	8'h55	8'h95	8'h95	8'hD5	8'hD5
8'h16	8'h16	8'h56	8'h56	8'h96	8'h96	8'hD6	8'hD6
8'h17	8'h17	8'h57	8'h57	8'h97	8'h97	8'hD7	8'hD7
8'h18	8'h18	8'h58	8'h58	8'h98	8'h98	8'hD8	8'hD8
8'h19	8'h19	8'h59	8'h59	8'h99	8'h99	8'hD9	8'hD9
8'h1A	8'h1A	8'h5A	8'h5A	8'h9A	8'h9A	8'hDA	8'hDA
8'h1B	8'h1B	8'h5B	8'h5B	8'h9B	8'h9B	8'hDB	8'hDB
8'h1C	8'h1C	8'h5C	8'h5C	8'h9C	8'h9C	8'hDC	8'hDC
8'h1D	8'h1D	8'h5D	8'h5D	8'h9D	8'h9D	8'hDD	8'hDD
8'h1E	8'h1E	8'h5E	8'h5E	8'h9E	8'h9E	8'hDE	8'hDE
8'h1F	8'h1F	8'h5F	8'h5F	8'h9F	8'h9F	8'hDF	8'hDF
8'h20	8'h20	8'h60	8'h60	8'hA0	8'hA0	8'hE0	8'hE0
8'h21	8'h21	8'h61	8'h61	8'hA1	8'hA1	8'hE1	8'hE1
8'h22	8'h22	8'h62	8'h62	8'hA2	8'hA2	8'hE2	8'hE2
8'h23	8'h23	8'h63	8'h63	8'hA3	8'hA3	8'hE3	8'hE3
8'h24	8'h24	8'h64	8'h64	8'hA4	8'hA4	8'hE4	8'hE4
8'h25	8'h25	8'h65	8'h65	8'hA5	8'hA5	8'hE5	8'hE5
8'h26	8'h26	8'h66	8'h66	8'hA6	8'hA6	8'hE6	8'hE6
8'h27	8'h27	8'h67	8'h67	8'hA7	8'hA7	8'hE7	8'hE7
8'h28	8'h28	8'h68	8'h68	8'hA8	8'hA8	8'hE8	8'hE8
8'h29	8'h29	8'h69	8'h69	8'hA9	8'hA9	8'hE9	8'hE9
8'h2A	8'h2A	8'h6A	8'h6A	8'hAA	8'hAA	8'hEA	8'hEA
8'h2B	8'h2B	8'h6B	8'h6B	8'hAB	8'hAB	8'hEB	8'hEB
8'h2C	8'h2C	8'h6C	8'h6C	8'hAC	8'hAC	8'hEC	8'hEC
8'h2D	8'h2D	8'h6D	8'h6D	8'hAD	8'hAD	8'hED	8'hED
8'h2E	8'h2E	8'h6E	8'h6E	8'hAE	8'hAE	8'hEE	8'hEE
8'h2F	8'h2F	8'h6F	8'h6F	8'hAF	8'hAF	8'hEF	8'hEF
8'h30	8'h30	8'h70	8'h70	8'hB0	8'hB0	8'hF0	8'hF0
8'h31	8'h31	8'h71	8'h71	8'hB1	8'hB1	8'hF1	8'hF1
8'h32	8'h32	8'h72	8'h72	8'hB2	8'hB2	8'hF2	8'hF2
8'h33	8'h33	8'h73	8'h73	8'hB3	8'hB3	8'hF3	8'hF3
8'h34	8'h34	8'h74	8'h74	8'hB4	8'hB4	8'hF4	8'hF4
8'h35	8'h35	8'h75	8'h75	8'hB5	8'hB5	8'hF5	8'hF5
8'h36	8'h36	8'h76	8'h76	8'hB6	8'hB6	8'hF6	8'hF6
8'h37	8'h37	8'h77	8'h77	8'hB7	8'hB7	8'hF7	8'hF7
8'h38	8'h38	8'h78	8'h78	8'hB8	8'hB8	8'hF8	8'hF8
8'h39	8'h39	8'h79	8'h79	8'hB9	8'hB9	8'hF9	8'hF9
8'h3A	8'h3A	8'h7A	8'h7A	8'hBA	8'hBA	8'hFA	8'hFA
8'h3B	8'h3B	8'h7B	8'h7B	8'hBB	8'hBB	8'hFB	8'hFB
8'h3C	8'h3C	8'h7C	8'h7C	8'hBC	8'hBC	8'hFC	8'hFC
8'h3D	8'h3D	8'h7D	8'h7D	8'hBD	8'hBD	8'hFD	8'hFD
8'h3E	8'h3E	8'h7E	8'h7E	8'hBE	8'hBE	8'hFE	8'hFE
8'h3F	8'h3F	8'h7F	8'h7F	8'hBF	8'hBF	8'hFF	8'hFF

LLMTW0[7:0], LLMTW1[7:0]

The possible minimum value of the threshold grayscale value (Dth) that makes display image white is set in units of one grayscale.

LLMTW0 is enabled when BLCM=0. LLMTW1 is enabled when BLCM=1.

Table 46

LLMTW0 [7:0] LLMTW1 [7:0]	Minimum grayscale level (Frame Memory data)	LLMTW0 [7:0] LLMTW1 [7:0]	Minimum grayscale level (Frame Memory data)	LLMTW0 [7:0] LLMTW1 [7:0]	Minimum grayscale level (Frame Memory data)	LLMTW0 [7:0] LLMTW1 [7:0]	Minimum grayscale level (Frame Memory data)
8'h00	8'h00	8'h40	8'h40	8'h80	8'h80	8'hC0	8'hC0
8'h01	8'h01	8'h41	8'h41	8'h81	8'h81	8'hC1	8'hC1
8'h02	8'h02	8'h42	8'h42	8'h82	8'h82	8'hC2	8'hC2
8'h03	8'h03	8'h43	8'h43	8'h83	8'h83	8'hC3	8'hC3
8'h04	8'h04	8'h44	8'h44	8'h84	8'h84	8'hC4	8'hC4
8'h05	8'h05	8'h45	8'h45	8'h85	8'h85	8'hC5	8'hC5
8'h06	8'h06	8'h46	8'h46	8'h86	8'h86	8'hC6	8'hC6
8'h07	8'h07	8'h47	8'h47	8'h87	8'h87	8'hC7	8'hC7
8'h08	8'h08	8'h48	8'h48	8'h88	8'h88	8'hC8	8'hC8
8'h09	8'h09	8'h49	8'h49	8'h89	8'h89	8'hC9	8'hC9
8'h0A	8'h0A	8'h4A	8'h4A	8'h8A	8'h8A	8'hCA	8'hCA
8'h0B	8'h0B	8'h4B	8'h4B	8'h8B	8'h8B	8'hCB	8'hCB
8'h0C	8'h0C	8'h4C	8'h4C	8'h8C	8'h8C	8'hCC	8'hCC
8'h0D	8'h0D	8'h4D	8'h4D	8'h8D	8'h8D	8'hCD	8'hCD
8'h0E	8'h0E	8'h4E	8'h4E	8'h8E	8'h8E	8'hCE	8'hCE
8'h0F	8'h0F	8'h4F	8'h4F	8'h8F	8'h8F	8'hCF	8'hCF
8'h10	8'h10	8'h50	8'h50	8'h90	8'h90	8'hD0	8'hD0
8'h11	8'h11	8'h51	8'h51	8'h91	8'h91	8'hD1	8'hD1
8'h12	8'h12	8'h52	8'h52	8'h92	8'h92	8'hD2	8'hD2
8'h13	8'h13	8'h53	8'h53	8'h93	8'h93	8'hD3	8'hD3
8'h14	8'h14	8'h54	8'h54	8'h94	8'h94	8'hD4	8'hD4
8'h15	8'h15	8'h55	8'h55	8'h95	8'h95	8'hD5	8'hD5
8'h16	8'h16	8'h56	8'h56	8'h96	8'h96	8'hD6	8'hD6
8'h17	8'h17	8'h57	8'h57	8'h97	8'h97	8'hD7	8'hD7
8'h18	8'h18	8'h58	8'h58	8'h98	8'h98	8'hD8	8'hD8
8'h19	8'h19	8'h59	8'h59	8'h99	8'h99	8'hD9	8'hD9
8'h1A	8'h1A	8'h5A	8'h5A	8'h9A	8'h9A	8'hDA	8'hDA
8'h1B	8'h1B	8'h5B	8'h5B	8'h9B	8'h9B	8'hDB	8'hDB
8'h1C	8'h1C	8'h5C	8'h5C	8'h9C	8'h9C	8'hDC	8'hDC
8'h1D	8'h1D	8'h5D	8'h5D	8'h9D	8'h9D	8'hDD	8'hDD
8'h1E	8'h1E	8'h5E	8'h5E	8'h9E	8'h9E	8'hDE	8'hDE
8'h1F	8'h1F	8'h5F	8'h5F	8'h9F	8'h9F	8'hDF	8'hDF
8'h20	8'h20	8'h60	8'h60	8'hA0	8'hA0	8'hE0	8'hE0
8'h21	8'h21	8'h61	8'h61	8'hA1	8'hA1	8'hE1	8'hE1
8'h22	8'h22	8'h62	8'h62	8'hA2	8'hA2	8'hE2	8'hE2
8'h23	8'h23	8'h63	8'h63	8'hA3	8'hA3	8'hE3	8'hE3
8'h24	8'h24	8'h64	8'h64	8'hA4	8'hA4	8'hE4	8'hE4
8'h25	8'h25	8'h65	8'h65	8'hA5	8'hA5	8'hE5	8'hE5
8'h26	8'h26	8'h66	8'h66	8'hA6	8'hA6	8'hE6	8'hE6
8'h27	8'h27	8'h67	8'h67	8'hA7	8'hA7	8'hE7	8'hE7
8'h28	8'h28	8'h68	8'h68	8'hA8	8'hA8	8'hE8	8'hE8
8'h29	8'h29	8'h69	8'h69	8'hA9	8'hA9	8'hE9	8'hE9
8'h2A	8'h2A	8'h6A	8'h6A	8'hAA	8'hAA	8'hEA	8'hEA
8'h2B	8'h2B	8'h6B	8'h6B	8'hAB	8'hAB	8'hEB	8'hEB
8'h2C	8'h2C	8'h6C	8'h6C	8'hAC	8'hAC	8'hEC	8'hEC
8'h2D	8'h2D	8'h6D	8'h6D	8'hAD	8'hAD	8'hED	8'hED
8'h2E	8'h2E	8'h6E	8'h6E	8'hAE	8'hAE	8'hEE	8'hEE
8'h2F	8'h2F	8'h6F	8'h6F	8'hAF	8'hAF	8'hEF	8'hEF
8'h30	8'h30	8'h70	8'h70	8'hB0	8'hB0	8'hF0	8'hF0
8'h31	8'h31	8'h71	8'h71	8'hB1	8'hB1	8'hF1	8'hF1
8'h32	8'h32	8'h72	8'h72	8'hB2	8'hB2	8'hF2	8'hF2
8'h33	8'h33	8'h73	8'h73	8'hB3	8'hB3	8'hF3	8'hF3
8'h34	8'h34	8'h74	8'h74	8'hB4	8'hB4	8'hF4	8'hF4
8'h35	8'h35	8'h75	8'h75	8'hB5	8'hB5	8'hF5	8'hF5
8'h36	8'h36	8'h76	8'h76	8'hB6	8'hB6	8'hF6	8'hF6
8'h37	8'h37	8'h77	8'h77	8'hB7	8'hB7	8'hF7	8'hF7
8'h38	8'h38	8'h78	8'h78	8'hB8	8'hB8	8'hF8	8'hF8
8'h39	8'h39	8'h79	8'h79	8'hB9	8'hB9	8'hF9	8'hF9
8'h3A	8'h3A	8'h7A	8'h7A	8'hBA	8'hBA	8'hFA	8'hFA
8'h3B	8'h3B	8'h7B	8'h7B	8'hBB	8'hBB	8'hFB	8'hFB
8'h3C	8'h3C	8'h7C	8'h7C	8'hBC	8'hBC	8'hFC	8'hFC
8'h3D	8'h3D	8'h7D	8'h7D	8'hBD	8'hBD	8'hFD	8'hFD
8'h3E	8'h3E	8'h7E	8'h7E	8'hBE	8'hBE	8'hFE	8'hFE
8'h3F	8'h3F	8'h7F	8'h7F	8'hBF	8'hBF	8'hFF	8'hFF

PITCHW[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one half of the grayscale. Make sure CGAPW[4:0] ≥ PITCHW[3:0] when setting.

Table 47

PITCHW [3:0]	Amount of change (grayscale)
4'h0	Setting inhibited
4'h1	1/2
4'h2	2/2
4'h3	3/2
4'h4	4/2
4'h5	5/2
4'h6	6/2
4'h7	7/2
4'h8	8/2
4'h9	9/2
4'hA	10/2
4'hB	11/2
4'hC	12/2
4'hD	13/2
4'hE	14/2
4'hF	15/2

CGAPW[4:0]

The difference of the two grayscales counted by the threshold counter is set in units of one half of the grayscale. Make sure CGAPW[4:0] ≥ PITCHW[3:0] when setting.

Table 48

CGAPW [4:0]	Grayscale difference	CGAPW [4:0]	Grayscale difference
5'h00	Setting inhibited	5'h10	16/2
5'h01	1/2	5'h11	17/2
5'h02	2/2	5'h12	18/2
5'h03	3/2	5'h13	19/2
5'h04	4/2	5'h14	20/2
5'h05	5/2	5'h15	21/2
5'h06	6/2	5'h16	22/2
5'h07	7/2	5'h17	23/2
5'h08	8/2	5'h18	24/2
5'h09	9/2	5'h19	25/2
5'h0A	10/2	5'h1A	26/2
5'h0B	11/2	5'h1B	27/2
5'h0C	12/2	5'h1C	28/2
5'h0D	13/2	5'h1D	29/2
5'h0E	14/2	5'h1E	30/2
5'h0F	15/2	5'h1F	31/2

COEFK0[4:0], COEFK1[4:0]

This register sets the range of the grayscale that prevents display image from turning white, according to the ratio of the grayscale listed below to the grayscale number that makes data white.

Table 49

COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from turning white	LLMTW x Min.	COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from turning white	LLMTW x Min.
5'h00	0%	8'h00	5'h10	100.00%	8'h80
5'h01	6.25%	8'h0F	5'h11	Setting inhibited	-
5'h02	12.50%	8'h1C	5'h12	Setting inhibited	-
5'h03	18.75%	8'h28	5'h13	Setting inhibited	-
5'h04	25.00%	8'h33	5'h14	Setting inhibited	-
5'h05	31.25%	8'h3D	5'h15	Setting inhibited	-
5'h06	37.50%	8'h46	5'h16	Setting inhibited	-
5'h07	43.75%	8'h4E	5'h17	Setting inhibited	-
5'h08	50.00%	8'h55	5'h18	Setting inhibited	-
5'h09	56.25%	8'h5C	5'h19	Setting inhibited	-
5'h0A	62.50%	8'h62	5'h1A	Setting inhibited	-
5'h0B	68.75%	8'h68	5'h1B	Setting inhibited	-
5'h0C	75.00%	8'h6D	5'h1C	Setting inhibited	-
5'h0D	81.25%	8'h72	5'h1D	Setting inhibited	-
5'h0E	87.50%	8'h77	5'h1E	Setting inhibited	-
5'h0F	93.75%	8'h7B	5'h1F	Setting inhibited	-

Note: LLMTW0[7:0] and LLMTW1[7:0] values are restricted as listed above according to COEFK0[4:0] and COEFK1[4:0] values. Make sure to follow the minimum LLMTW*[7:0] setting to each COEFK[4:0] value.

TBL3[7:0], TBL4[7:0], TBL5[7:0], TBL6[7:0]

The reference values used for interpolation calculation in gamma conversion table are set by TBL_*.

Table 50

TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value
8'h00	8'h00	8 'h20	8 'h20	8 'h40	8 'h40	8 'h60	8 'h60
8'h01	8'h01	8 'h21	8 'h21	8 'h41	8 'h41	8 'h61	8 'h61
8'h02	8'h02	8 'h22	8 'h22	8 'h42	8 'h42	8 'h62	8 'h62
8'h03	8'h03	8 'h23	8 'h23	8 'h43	8 'h43	8 'h63	8 'h63
8'h04	8'h04	8 'h24	8 'h24	8 'h44	8 'h44	8 'h64	8 'h64
8'h05	8'h05	8 'h25	8 'h25	8 'h45	8 'h45	8 'h65	8 'h65
8'h06	8'h06	8 'h26	8 'h26	8 'h46	8 'h46	8 'h66	8 'h66
8'h07	8'h07	8 'h27	8 'h27	8 'h47	8 'h47	8 'h67	8 'h67
8'h08	8'h08	8 'h28	8 'h28	8 'h48	8 'h48	8 'h68	8 'h68
8'h09	8'h09	8 'h29	8 'h29	8 'h49	8 'h49	8 'h69	8 'h69
8'h0A	8'h0A	8 'h2A	8 'h2A	8 'h4A	8 'h4A	8 'h6A	8 'h6A
8'h0B	8'h0B	8 'h2B	8 'h2B	8 'h4B	8 'h4B	8 'h6B	8 'h6B
8'h0C	8'h0C	8 'h2C	8 'h2C	8 'h4C	8 'h4C	8 'h6C	8 'h6C
8'h0D	8'h0D	8 'h2D	8 'h2D	8 'h4D	8 'h4D	8 'h6D	8 'h6D
8'h0E	8'h0E	8 'h2E	8 'h2E	8 'h4E	8 'h4E	8 'h6E	8 'h6E
8'h0F	8'h0F	8 'h2F	8 'h2F	8 'h4F	8 'h4F	8 'h6F	8 'h6F
8'h10	8'h10	8 'h30	8 'h30	8 'h50	8 'h50	8 'h70	8 'h70
8'h11	8'h11	8 'h31	8 'h31	8 'h51	8 'h51	8 'h71	8 'h71
8'h12	8'h12	8 'h32	8 'h32	8 'h52	8 'h52	8 'h72	8 'h72
8'h13	8'h13	8 'h33	8 'h33	8 'h53	8 'h53	8 'h73	8 'h73
8'h14	8'h14	8 'h34	8 'h34	8 'h54	8 'h54	8 'h74	8 'h74
8'h15	8'h15	8 'h35	8 'h35	8 'h55	8 'h55	8 'h75	8 'h75
8'h16	8'h16	8 'h36	8 'h36	8 'h56	8 'h56	8 'h76	8 'h76
8'h17	8'h17	8 'h37	8 'h37	8 'h57	8 'h57	8 'h77	8 'h77
8'h18	8'h18	8 'h38	8 'h38	8 'h58	8 'h58	8 'h78	8 'h78
8'h19	8'h19	8 'h39	8 'h39	8 'h59	8 'h59	8 'h79	8 'h79
8'h1A	8'h1A	8 'h3A	8 'h3A	8 'h5A	8 'h5A	8 'h7A	8 'h7A
8'h1B	8'h1B	8 'h3B	8 'h3B	8 'h5B	8 'h5B	8 'h7B	8 'h7B
8'h1C	8'h1C	8 'h3C	8 'h3C	8 'h5C	8 'h5C	8 'h7C	8 'h7C
8'h1D	8'h1D	8 'h3D	8 'h3D	8 'h5D	8 'h5D	8 'h7D	8 'h7D
8'h1E	8'h1E	8 'h3E	8 'h3E	8 'h5E	8 'h5E	8 'h7E	8 'h7E
8'h1F	8'h1F	8 'h3F	8 'h3F	8 'h5F	8 'h5F	8 'h7F	8 'h7F

Table 51

TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value
8'h80	8'h80	8'hA0	8'hA0	8'hC0	8'hC0	8'hE0	8'hE0
8'h81	8'h81	8'hA1	8'hA1	8'hC1	8'hC1	8'hE1	8'hE1
8'h82	8'h82	8'hA2	8'hA2	8'hC2	8'hC2	8'hE2	8'hE2
8'h83	8'h83	8'hA3	8'hA3	8'hC3	8'hC3	8'hE3	8'hE3
8'h84	8'h84	8'hA4	8'hA4	8'hC4	8'hC4	8'hE4	8'hE4
8'h85	8'h85	8'hA5	8'hA5	8'hC5	8'hC5	8'hE5	8'hE5
8'h86	8'h86	8'hA6	8'hA6	8'hC6	8'hC6	8'hE6	8'hE6
8'h87	8'h87	8'hA7	8'hA7	8'hC7	8'hC7	8'hE7	8'hE7
8'h88	8'h88	8'hA8	8'hA8	8'hC8	8'hC8	8'hE8	8'hE8
8'h89	8'h89	8'hA9	8'hA9	8'hC9	8'hC9	8'hE9	8'hE9
8'h8A	8'h8A	8'hAA	8'hAA	8'hCA	8'hCA	8'hEA	8'hEA
8'h8B	8'h8B	8'hAB	8'hAB	8'hCB	8'hCB	8'hEB	8'hEB
8'h8C	8'h8C	8'hAC	8'hAC	8'hCC	8'hCC	8'hEC	8'hEC
8'h8D	8'h8D	8'hAD	8'hAD	8'hCD	8'hCD	8'hED	8'hED
8'h8E	8'h8E	8'hAE	8'hAE	8'hCE	8'hCE	8'hEE	8'hEE
8'h8F	8'h8F	8'hAF	8'hAF	8'hCF	8'hCF	8'hEF	8'hEF
8'h90	8'h90	8'hB0	8'hB0	8'hD0	8'hD0	8'hF0	8'hF0
8'h91	8'h91	8'hB1	8'hB1	8'hD1	8'hD1	8'hF1	8'hF1
8'h92	8'h92	8'hB2	8'hB2	8'hD2	8'hD2	8'hF2	8'hF2
8'h93	8'h93	8'hB3	8'hB3	8'hD3	8'hD3	8'hF3	8'hF3
8'h94	8'h94	8'hB4	8'hB4	8'hD4	8'hD4	8'hF4	8'hF4
8'h95	8'h95	8'hB5	8'hB5	8'hD5	8'hD5	8'hF5	8'hF5
8'h96	8'h96	8'hB6	8'hB6	8'hD6	8'hD6	8'hF6	8'hF6
8'h97	8'h97	8'hB7	8'hB7	8'hD7	8'hD7	8'hF7	8'hF7
8'h98	8'h98	8'hB8	8'hB8	8'hD8	8'hD8	8'hF8	8'hF8
8'h99	8'h99	8'hB9	8'hB9	8'hD9	8'hD9	8'hF9	8'hF9
8'h9A	8'h9A	8'hBA	8'hBA	8'I	8'I	8'hFA	8'hFA
8'h9B	8'h9B	8'hBB	8'hBB	8'hDB	8'hDB	8'hFB	8'hFB
8'h9C	8'h9C	8'hBC	8'hBC	8'hDC	8'hDC	8'hFC	8'hFC
8'h9D	8'h9D	8'hBD	8'hBD	8'hDD	8'hDD	8'hFD	8'hFD
8'h9E	8'h9E	8'hBE	8'hBE	8'hDE	8'hDE	8'hFE	8'hFE
8'h9F	8'h9F	8'hBF	8'hBF	8'hDF	8'hDF	8'hFF	8'hFF

Back Light Control 2 (B9h)

B9h	Back Light Control 2												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	0	0	1	B9h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	PWM ON	XXh
2nd parameter	1	#A	#B	X	BDCV [7]	BDCV [6]	BDCV [5]	BDCV [4]	BDCV [3]	BDCV [2]	BDCV [1]	BDCV [0]	XXh
3rd parameter	1	#A	#B	X	PWM DIV [7]	PWM DIV [6]	PWM DIV [5]	PWM DIV [4]	PWM DIV [3]	PWM DIV [2]	PWM DIV [1]	PWM DIV [0]	XXh
4th parameter	1	#A	#B	X	0	0	0	PWM WM	LED PWM E	LED PWM POL	0	DIM ON	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.)												

PWMWM, PWMON

PWMWM = 0: Controls On/Off of the PWM output according to Display On/Off state.
PWMWM = 1: Controls On/Off of the PWM output according to PWMON setting. Note that LEDPWM is Off when the Sleep mode is On regardless of PWMON value.

LEDPWME

LEDPWM pin output enable bit. In the system configuration using no LEDPWM pin, set the bit to 0. In the system configuration using LEDPWM pin, set the bit to 1. This setting can be changed only when Sleep Mode is On.

Table 52

LEDPWME	PWMWM	PWMON	BLCON	RDPWM	LEDPWM output	
0	0	*	0	BDCV	0%	
			1	BLC*BDCV	0%	
	1	0	0	0%	0%	
			1	Setting inhibited	Setting inhibited	
		1	0	BDCV	0%	
			1	BLC*BDCV	0%	*2
1	0	*	0	BDCV	BDCV	*1
			1	BLC*BDCV	BLC*BDCV	*1
	1	0	0	0%	0%	
			1	Setting inhibited	Setting inhibited	
		1	0	BDCV	BDCV	
			1	BLC*BDCV	BLC*BDCV	*2

Notes: 1. If PWMWM = 0, On/Off of the PWM output is automatically controlled according to display ON/Off state.
Display Off: Sleep Mode On + set_display_off
Display On: Sleep Mode Off + set_display_on
2. If PWMWM = 1, RDPWM and LEDPWM outputs cause BDCV value to be read during Display Off.

BDCV[7:0]
PWM signal's width is selected from 256 values between 8'hFF and 8'h00 when LED is adjusted externally.

When BLCON=0, PWM signals are output according to BDCV values.
When BLCON=1, PWM signals are output according to calculated values by BDCV*BLC.

Table 53

BDCV[7:0]	Amount of light
8'h00	None (0%)
8'h01	1/255
8'h02	2/255
8'h03	3/255
:	:
8'hFE	254/255
8'hFF	255/255 (100%)

PWMDIV[7:0]

These bits are used to define frequency of PWM signal that is output from LEDPWM pin.

Table 54

PWMDIV[7:0]	LEDPWM frequency	PWMDIV[7:0]	LEDPWM frequency
8'h00	33.3KHz	8'h10-8'h1E	Setting inhibited
8'h01	27.4KHz	8'h1F	1.72KHz
8'h02	18.3KHz	8'h20-8'h3E	Setting inhibited
8'h03	13.7KHz	8'h3F	0.86KHz
8'h04-8'h06	Setting inhibited	8'h40-8'h7E	Setting inhibited
8'h07	6.86KHz	8'h7F	0.43KHz
8'h08-8'h0E	Setting inhibited	8'h80-8'hFE	Setting inhibited
8'h0F	3.43KHz	8'hFF	0.21KHz

Notes: 1. The values in the above table are typical ones. There shall be variance of maximum ±7% in the actual operation.

2. When PWMDIV is set to 8'h00 (33.3KHz), PWM signal's width is selected from maximum 210 values

LEDPWMPOL

The bit is used to define polarity of LEDPWM signal.

Table 55

LEDPWPOL	LEDPWM pin	
	Lit period	Non-lit period
0	High	Low
1	Low	High

DIMON

DIMON bit is used to enable / disable LEDPWM's DIMMING function.

The bit is used to control change in brightness (change in LEDPWM signal) when BCDV register is rewritten or LEDPWM pin is turned on.

Table 56

DIMON	DIMMING function	Brightness
0	OFF	Changes immediately
1	ON	Changes gradually in approximately 500ms.

Note: This bit is applied to BDCV register setting and not to brightness change by the BLC function.

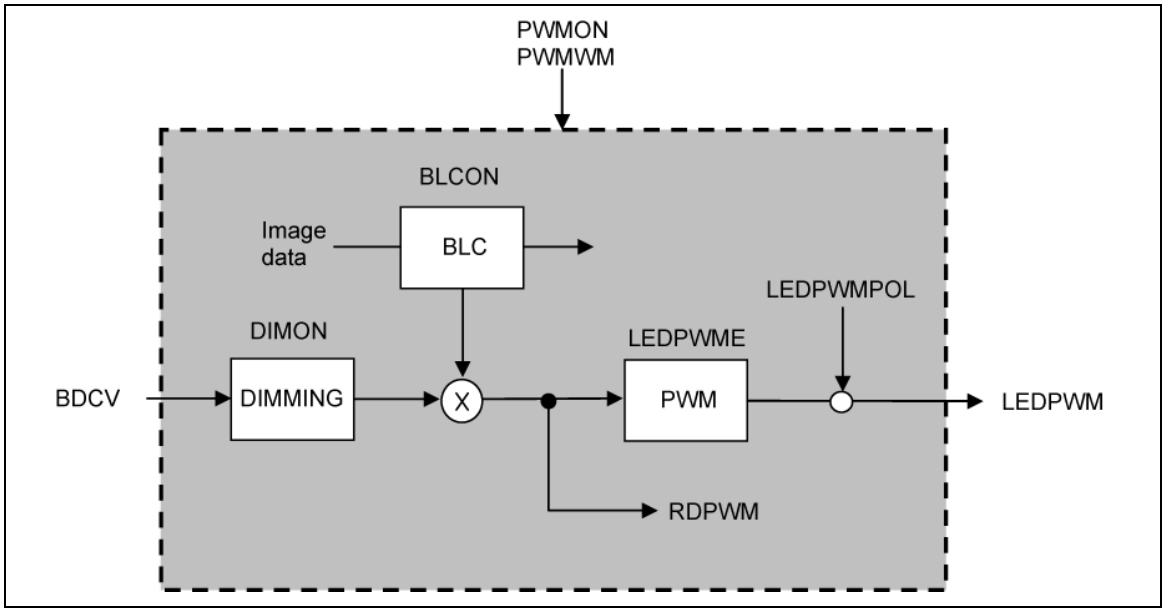
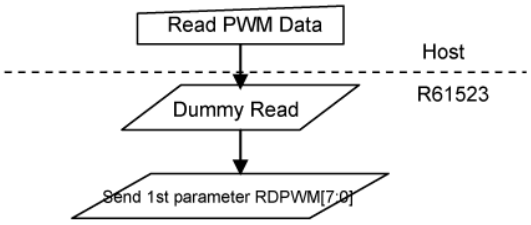
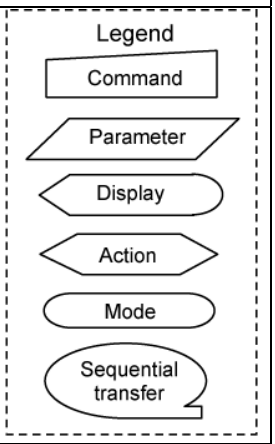


Figure 29

Back Light Control 3 (BAh)

BAh	Back Light Control 3 (Read PWM Data)												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	0	1	0	Bah
Dummy Parameter	1	↑	1	X	x	x	x	x	x	x	x	x	XXh
1st parameter	1	↑	1	X	RD PWM [7]	RD PWM [6]	RD PWM [5]	RD PWM [4]	RD PWM [3]	RD PWM [2]	RD PWM [1]	RD PWM [0]	XXh
Description	**RDPWM[7:0]** The command is used to read LED brightness data for LEDPWM signal. X = Don't care												
Flow Chart	 Note: When this command is read via DSI, dummy read operation is not performed. 												
Restriction	Data read is disabled when Sleep mode is On.												

Device Code Read (BFh)

BFh	Device Code Read												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	1	1	1	BFh
Dummy parameter	1	↑	1	X	x	x	x	x	x	x	x	x	XXh
1st parameter	1	↑	1	X	0	0	0	0	0	0	0	1	01h
2nd parameter	1	↑	1	X	0	0	1	0	0	0	1	0	22h
3rd parameter	1	↑	1	X	0	0	0	1	0	1	0	1	15h
4th parameter	1	↑	1	X	0	0	1	0	0	0	1	1	23h
Description	The parameters are used to read the information as follows: 1st parameter: Returns the upper byte "01h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 2nd parameter: Returns the lower byte "22h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 3rd parameter: Returns the upper byte "15h" of product code of this LSI. 4th parameter: Returns the lower byte "23h" of product code of this LSI. X = Don't care												
Restriction	-												
Flow Chart	Note : When this command is read via DSI, dummy read operation is not performed.												

Panel Control Command

Panel Driving Setting (C0h)

C0h	Panel Driving Setting												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	0	C0h
1st parameter	1	#A	#B	X	0	0	0	REV	SM	GS	BGR	SS	XXh
2nd parameter	1	#A	#B	X	NL [7]	NL [6]	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	XXh
3rd parameter	1	#A	#B	X	SCN [7]	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	XXh
4th parameter	1	#A	#B	X	0	0	0	0	0	0	0	NW [0]	XXh
5th parameter	1	#A	#B	X	0	0	0	0	0	0	BLV	PTV	XXh
6th parameter	1	#A	#B	X	0	0	BLS	NDL	PTDC	PTS [2]	PTS [1]	PTS [0]	XXh
7th parameter	1	#A	#B	X	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.)												

REV

The grayscale is reversed by setting REV = 1. This enables the R61523 to display the same image from the same set of data on both normally black and white panels. The source output levels during the retrace period and non-lit display period are determined by register settings, BLS and NDL, respectively.

Table 57

REV	Frame memory data	Source output level in display area	
		Positive polarity	Negative polarity
0	24'h00000	V255	V0
	:	:	:
	24'hFFFFF	V0	V255
1	24'h00000	V0	V255
	:	:	:
	24'hFFFFF	V255	V0

SM
SM=0: Left/right interchanging scan
SM=1: Left/right one-side scan

GS
GS=0: Forward scan
GS=1: Reverse scan

The R61523 allows changing gate driver assignment and the scan mode by combination of SM and GS bits. Set these bits in accordance with the configuration of the module. For details, see "Scan Mode Setting."

BGR
The bit is used to reverse 18-bit write data in the Frame Memory from RGB to BGR. Set in accordance with arrangement of color filters.

BGR=0: Data are written to the Frame Memory in the order of RGB. (Default)
BGR=1: Data are written to the Frame Memory in the order of BGR.

SS
The bit is used to select the shifting direction of the source driver output. Set in accordance with mounting position of the R61523 to the panel.

SS=0: S1 to S1080 (Default)
SS=1: S1080 to S1

To change the RGB order, set SS and BGR bits.

SS=0, BGR=0: RGB
SS=1, BGR=1: BGR

NL[7:0]

These bits select the number of lines to drive the LCD from 480 to 640 lines. The frame memory address mapping is not affected by the number of NL[7:0]. The number of lines shall be set according to the panel size.

Table 58

NL[7:0]	Number of drive lines
8'h00-8'h9E	Setting inhibited
8'h77	480 lines
8'h78	484 lines
8'h79	488 lines
8'h7A	492 lines
8'h7B	496 lines
8'h7C	500 lines
8'h7D	504 lines
8'h7E	508 lines
8'h7F	512 lines
8'h80	516 lines
8'h81	520 lines
8'h82	524 lines
8'h83	528 lines
8'h84	532 lines

NL[7:0]	Number of drive lines
8'h85	536 lines
8'h86	540 lines
8'h87	544 lines
8'h88	548 lines
8'h89	552 lines
8'h8A	556 lines
8'h8B	560 lines
8'h8C	564 lines
8'h8D	568 lines
8'h8E	572 lines
8'h8F	576 lines
8'h90	580 lines
8'h91	584 lines
8'h92	588 lines
8'h93	592 lines

NL[7:0]	Number of drive lines
8'h94	596 lines
8'h95	600 lines
8'h96	604 lines
8'h97	608 lines
8'h98	612 lines
8'h99	616 lines
8'h9A	620 lines
8'h9B	624 lines
8'h9C	628 lines
8'h9D	632 lines
8'h9E	636 lines
8'h9F	640 lines
8'hA0-8'hFF	Setting inhibited

SCN[7:0]

These bits are used to set the gate scanning start position.

Table 59

SCN[7:0]	Gate Scan Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
8'h00	G1	G(N)	G1	G(2N－640)
8'h01-8'hFF	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

N: Number of line(s) defined by NL[7:0].

To set SCN, follow the restriction below.

Table 60

SM	GS	Restriction
0	0	(Gate scan start position -1) + (Number of line set by NL) ≤ 640
0	1	Gate scan start position ≤ 640
1	0	Gate scan start position -1)/2 + (Number of line set by NL) ≤ 640
1	1	Gate scan start position ≤ 640

NW[0]

This bit sets the number of lines for inversion liquid crystal drive by line inversion waveform (BCn=1, Display Timing Setting for Normal Mode (C1h) and Display Timing Setting for Idle Mode (C3h)). The polarity of waveform inverts in every 1 or 2 line(s).

Table 61

NW[0]	Number of line(s)
0	1 line
1	2 lines

BLV

The bit selects line or frame inversion during the retrace period.

BLV=0: Line inversion is selected for the retrace period when line inversion is selected by BCn=1, C1h - C3h.
BLV=1: Frame inversion is selected for the retrace period.

Table 62

BCn	BLV	Retrace period
0	-	Frame inversion
1	0	Line inversion
	1	Frame inversion

PTV

The bit is used to define inversion in the non-lit display area.
PTV=1: Frame inversion is selected for the non-lit display area when line inversion is selected (BCn=1).

Table 63

BCn	PTV	Inversion in non-lit display area
0	*	Frame inversion
1	0	Line inversion
	1	Frame inversion

"Retrace period" indicates back and front porches.

"Non-lit display area" indicates:

Non-display area other than the Partial Area defined by SR[8:0] and ER[8:0].

Display area when Sleep mode is off and the display operation is off.

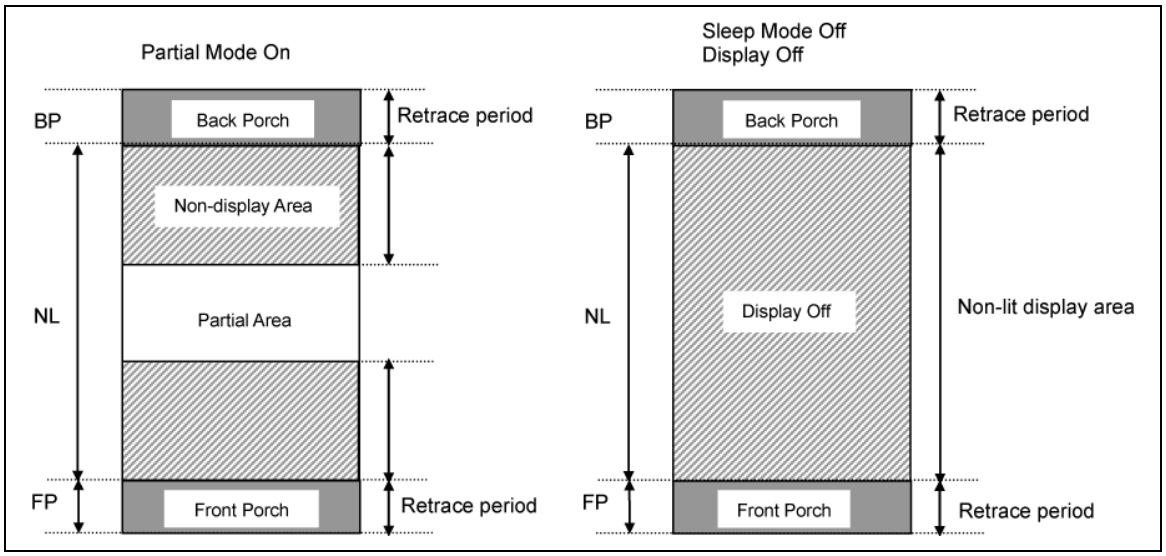


Figure 30

BLS

The bit is used to define source output level in the Retrace Period. The polarity of grayscale voltage in the Retrace period is inverted.

Table 64

BLS	Retrace period	
	Positive polarity	Negative polarity
0	V255	V0
1	V0	V255

NDL

The bit is used to define source output level in the non-lit display area. The polarity of grayscale voltage is inverted.

Table 65

NDL	Non-lit display area	
	Positive polarity	Negative polarity
0	V255	V0
1	V0	V255

PTS[2:0], PTDC

These bits are used to define low-power consumption operation. PTS[1:0] defines output level in the retrace period and the non-lit display area. PTS[2] defines the operation of the grayscale amplifier and the step-up clock frequency while PTDC defines step-up clock frequency.

Table 66

PTDC	PTS [2]	PTS [1:0]	Source output in the non-lit display area (Note)		Grayscale amplifier's operation in the non-lit display area	Step-up clock frequency in the non-lit display area (DDVDHA and DDVDHB)
			Positive polarity	Negative polarity		
–	0	00	V255	V0	V0 to V255	Normal operation
		01	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
		10	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
		11	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
0	1	00	V255	V0	V0,V255	Normal operation
		01	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
		10	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
		11	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
1	1	00	V255	V0	V0,V255	Low-speed operation
		01	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
		10	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited
		11	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

Note: The polarity of the source output level in non-lit display area is set by NDL (C0h). The polarity of the source output level during the retrace period is defined by BLS (C0h). If PTDC=1, step-up operation may not be executed properly depending on DC0n and RTNn values.

PTG

The bit is used to select gate scan mode in non-lit display area.

Table 67

PTG	Gate output in non-lit display area
0	Normal scan
1	Interval scan

Note: Set BCn=0 and select frame inversion in interval scan operation.

ISC[3:0]

These bits are used to set gate interval scan when PTG bit sets interval scan in non-lit display area. The scan interval is always of odd number. The polarity of liquid crystal drive waveform is inverted in the same timing as the interval scan.

Table 68

ISC[3:0]	Scan cycle
4'h0	Setting inhibited
4'h1	3 frames
4'h2	5 frames
4'h3	7 frames
4'h4	9 frames
4'h5	11 frames
4'h6	13 frames
4'h7	15 frames
4'h8	17 frames
4'h9	19 frames
4'hA	21 frames
4'hB	23 frames
4'hC	25 frames
4'hD	27 frames
4'hE	29 frames
4'hF	31 frames

Display Timing Setting for Normal / Partial Mode (C1h)

Display Timing Setting for Idle Mode (C3h)

C1h	Display Timing Setting for Normal / Partial Mode												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	1	C1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	BC0	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	0	0	0	XXh
3rd parameter	1	#A	#B	X	0	0	RTN0 [5]	RTN0 [4]	RTN0 [3]	RTN0 [2]	RTN0 [1]	RTN0 [0]	XXh
4th parameter	1	#A	#B	X	BP0 [7]	BP0 [6]	BP0 [5]	BP0 [4]	BP0 [3]	BP0 [2]	BP0 [1]	BP0 [0]	XXh
5th parameter	1	#A	#B	X	FP0 [7]	FP0 [6]	FP0 [5]	FP0 [4]	FP0 [3]	FP0 [2]	FP0 [1]	FP0 [0]	XXh
C3h	**Display Timing Setting for Idle Mode**												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	1	1	C3h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	BC2	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	0	0	0	XXh
3rd parameter	1	#A	#B	X	0	0	RTN2 [5]	RTN2 [4]	RTN2 [3]	RTN2 [2]	RTN2 [1]	RTN2 [0]	XXh
4th parameter	1	#A	#B	X	BP2 [7]	BP2 [6]	BP2 [5]	BP2 [4]	BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]	XXh
5th parameter	1	#A	#B	X	FP2 [7]	FP2 [6]	FP2 [5]	FP2 [4]	FP2 [3]	FP2 [2]	FP2 [1]	FP2 [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When these commands are read via DSI, dummy read operation is not performed.) Timings can be defined separately for different modes. C1h: Enabled when Normal Mode is On and Idle Mode is Off, or when Partial Mode is On and Idle Mode is Off. C3h: Enabled when Normal Mode is On and Idle Mode is On, or when Partial Mode is On and Idle Mode is On.												

Restriction	Make sure to set BP and FP so that the restriction below is satisfied. BP ≥ 4 lines FP ≥ 4 lines FP+BP ≤ 256 lines

Display Mode and Valid Register

Display_Setting commands (C1h and C3h) can be set separately for different display modes.

Table 69

Display mode	Number of clock per 1H (RTN)	Back porch (BP)	Front porch (FP)	Liquid crystal alternating cycle (BC)
(Normal / Partial mode) + Idle mode off	C1h:RTN0	C1h:BP0	C1h:FP0	C1h:BC0
Idle mode on + (Normal / Partial mode)	C3h:RTN2	C3h:BP2	C3h:FP2	C3h:BC2

BC0, BC2
These bits define liquid crystal drive waveform inversion.

BCn = 0: Frame inversion waveform is selected.
BCn = 1: Line inversion waveform is selected.

For details, see “Line Inversion AC Drive”.

RTN0[5:0], RTN2[5:0]

These bits set the number of clocks in one line period.

Table 70

RTNn[5:0]	Number of clocks per line	RTNn[5:0]	Number of clocks per line	RTNn[5:0]	Number of clocks per line
6'h00-6'h0F	Setting inhibited	6'h20	32	6'h30	48
6'h10	Setting inhibited	6'h21	33	6'h31	49
6'h11	Setting inhibited	6'h22	34	6'h32	50
6'h12	18	6'h23	35	6'h33	51
6'h13	19	6'h24	36	6'h34	52
6'h14	20	6'h25	37	6'h35	53
6'h15	21	6'h26	38	6'h36	54
6'h16	22	6'h27	39	6'h37	55
6'h17	23	6'h28	40	6'h38	56
6'h18	24	6'h29	41	6'h39	57
6'h19	25	6'h2A	42	6'h3A	58
6'h1A	26	6'h2B	43	6'h3B	59
6'h1B	27	6'h2C	44	6'h3C	60
6'h1C	28	6'h2D	45	6'h3D	61
6'h1D	29	6'h2E	46	6'h3E	62
6'h1E	30	6'h2F	47	6'h3F	63
6'h1F	31				

FP0[7:0], FP2[7:0], BP0[7:0], BP2[7:0]

These parameters define the retrace period (i.e. front and back porches) which appears before and after the display area. FPn bits define the number of front porch lines while BPn bits define the number of back porch lines.

Table 71

FPn[7:0] BPn[7:0]	Font porch Number of lines	Back porch Number of lines
8'h00	Setting inhibited	Setting inhibited
8'h01	Setting inhibited	Setting inhibited
8'h02	Setting inhibited	Setting inhibited
8'h03	Setting inhibited	Setting inhibited
8'h04	4	4
8'h05	5	5
8'h06	6	6
8'h07	7	7
8'h08	8	8
8'h09	9	9
8'h0A	10	10
8'h0B	11	11
8'h0C	12	12
8'h0D	13	13
8'h0E	14	14
8'h0F	15	15
:	:	:
8'h7F	127	127
8'h80	128	128
8'h81	Setting inhibited	Setting inhibited
:	:	:
8'hFF	Setting inhibited	Setting inhibited

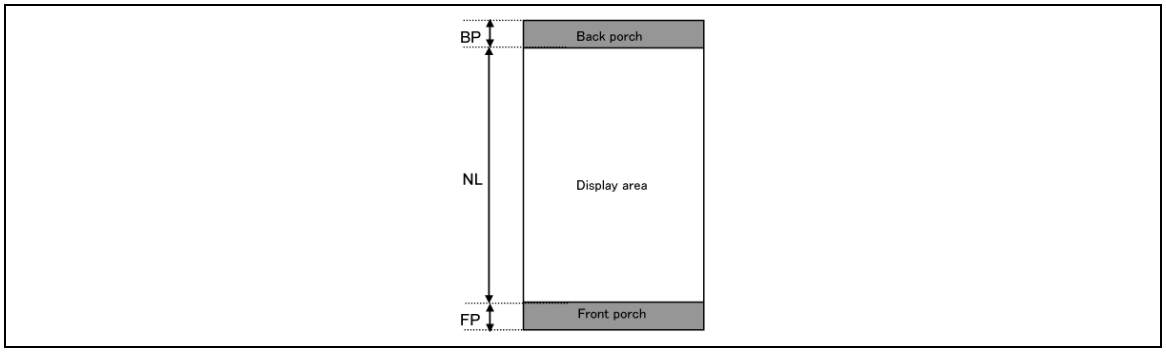


Figure 31

Source/VCOM/Gate Driving Timing Setting (C4h)

C4h	Source/VCOM/Gate Driving Timing Setting												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	1	0	0	C4h
1st parameter	1	#A	#B	X	0	SDT [2]	SDT [1]	SDT [0]	0	NOW [2]	NOW [1]	NOW [0]	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	MCP [2]	MCP [1]	MCP [0]	XXh
3rd parameter	1	#A	#B	X	0	VEQW [2]	VEQW [1]	VEQW [0]	0	0	VEM [1]	VEM [0]	XXh
4th parameter	1	#A	#B	X	0	0	0	0	0	SPCW [2]	SPCW [1]	SPCW [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.)												
Restriction													

SDT [2:0]

These bits are used to set the source output alternating position in one line period.

Table 72

SDT[2:0]	Source output alternating position (clocks)
3'h0	Setting inhibited
3'h1	1
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

NOW[2:0]
These bits set the gate output start position (non-overlap period) in one line period.

Table 73

NOW[2:0]	Gate drive start position (clocks)
3'h0	Setting inhibited
3'h1	1
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

MCP [2:0]
These bits are used to set the VCOM output alternating position in one line period.

Table 74

MCP[2:0]	VCOM alternating position (clocks)
3'h0	Setting inhibited
3'h1	1
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

VEQW[2:0]
These bits define VCOM equalize period. Equalizing is performed during the period defined by VEQW[2:0] starting from the VCOM alternating position.

Table 75

VEQW[2:0]	VCOM equalize period (clocks)
3'h0	Setting inhibited
3'h1	1
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

VEM[1:0]
VEM[0]: VCOMH equalize switch
VEM[0] = 1: When VCOMH level falls from VCOMH to VCOML level, the level first falls to the GND level and then to the VCOML level.

VEM[1]: VCOML equalize switch
VEM[1] = 1: When VCOMH level rises from VCOML level to VCOMH level, the level first goes up to the VCI level and then to the VCOMH level.

These bits reduce power consumption during VCOM drive period.

Table 76

VEM[1:0]	Operation
2'h0	Setting inhibited
2'h1	Setting inhibited
2'h2	Setting inhibited
2'h3	VCOMH/VCOML equalize

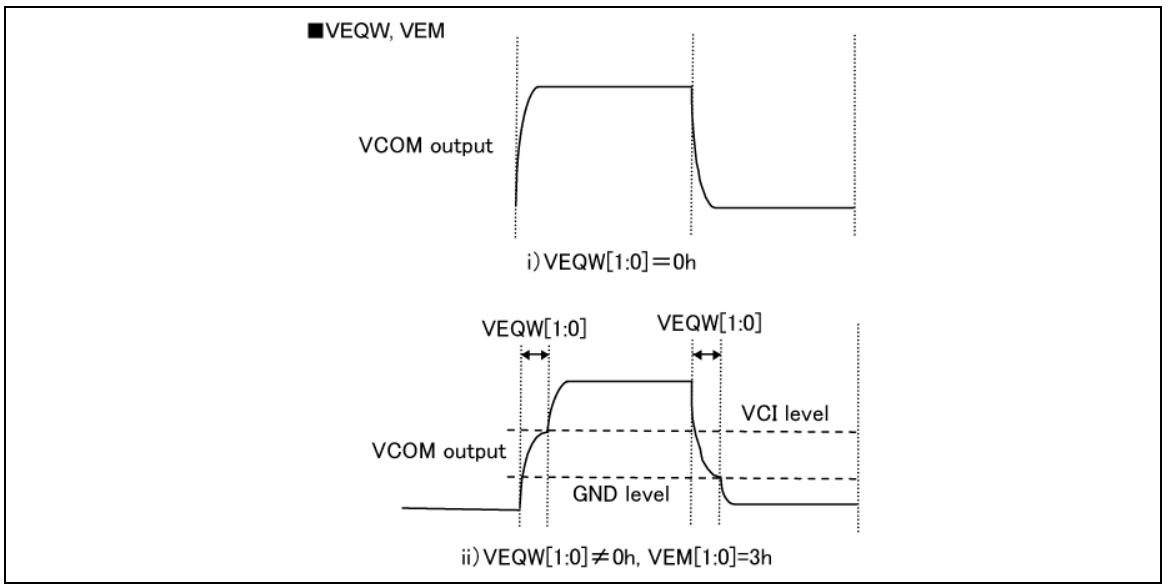


Figure 32

SPCW[2:0]
These bits are used to set source pre-charge period in one line period. Pre-charge period is set by SPCW[2:0] starting from the source output alternating position defined by SDT [2:0]. Source output is precharged only on the line where liquid crystal waveform inverts.

This function realizes power consumption reduction depending on image data. Check actual image quality and effect on the panel.

Table 77

SPCW[2:0]	Source pre-charge period (clocks)
3'h0	Setting inhibited
3'h1	1
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

Gamma Control

Gamma Set A (C8h)

C8h	Gamma Set A												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	0	0	C8h
1st parameter	1	1	↑	X	0	0	0	PR0P_R[4]	PR0P_R[3]	PR0P_R[2]	PR0P_R[1]	PR0P_R[0]	XXh
2nd parameter	1	1	↑	X	0	0	0	PR1P_R[4]	PR1P_R[3]	PR1P_R[2]	PR1P_R[1]	PR1P_R[0]	XXh
3rd parameter	1	1	↑	X	PR3P_R[3]	PR3P_R[2]	PR3P_R[1]	PR3P_R[0]	PR2P_R[3]	PR2P_R[2]	PR2P_R[1]	PR2P_R[0]	XXh
4th parameter	1	1	↑	X	PR5P_R[3]	PR5P_R[2]	PR5P_R[1]	PR5P_R[0]	PR4P_R[3]	PR4P_R[2]	PR4P_R[1]	PR4P_R[0]	XXh
5th parameter	1	1	↑	X	0	0	0	0	PR6P_R[3]	PR6P_R[2]	PR6P_R[1]	PR6P_R[0]	XXh
6th parameter	1	1	↑	X	PR8P_R[3]	PR8P_R[2]	PR8P_R[1]	PR8P_R[0]	PR7P_R[3]	PR7P_R[2]	PR7P_R[1]	PR7P_R[0]	XXh
7th parameter	1	1	↑	X	PR10P_R[3]	PR10P_R[2]	PR10P_R[1]	PR10P_R[0]	PR9P_R[3]	PR9P_R[2]	PR9P_R[1]	PR9P_R[0]	XXh
8th parameter	1	1	↑	X	0	0	0	PR11P_R[4]	PR11P_R[3]	PR11P_R[2]	PR11P_R[1]	PR11P_R[0]	XXh
9th parameter	1	1	↑	X	0	0	0	PR12P_R[4]	PR12P_R[3]	PR12P_R[2]	PR12P_R[1]	PR12P_R[0]	XXh
10th parameter	1	1	↑	X	0	0	0	PR0N_R[4]	PR0N_R[3]	PR0N_R[2]	PR0N_R[1]	PR0N_R[0]	XXh
11th parameter	1	1	↑	X	0	0	0	PR1N_R[4]	PR1N_R[3]	PR1N_R[2]	PR1N_R[1]	PR1N_R[0]	XXh
12th parameter	1	1	↑	X	PR3N_R[3]	PR3N_R[2]	PR3N_R[1]	PR3N_R[0]	PR2N_R[3]	PR2N_R[2]	PR2N_R[1]	PR2N_R[0]	XXh
13th parameter	1	1	↑	X	PR5N_R[3]	PR5N_R[2]	PR5N_R[1]	PR5N_R[0]	PR4N_R[3]	PR4N_R[2]	PR4N_R[1]	PR4N_R[0]	XXh
14th parameter	1	1	↑	X	0	0	0	0	PR6N_R[3]	PR6N_R[2]	PR6N_R[1]	PR6N_R[0]	XXh
15th parameter	1	1	↑	X	PR8N_R[3]	PR8N_R[2]	PR8N_R[1]	PR8N_R[0]	PR7N_R[3]	PR7N_R[2]	PR7N_R[1]	PR7N_R[0]	XXh
16th parameter	1	1	↑	X	PR10N_R[3]	PR10N_R[2]	PR10N_R[1]	PR10N_R[0]	PR9N_R[3]	PR9N_R[2]	PR9N_R[1]	PR9N_R[0]	XXh

17th parameter	1	1	↑	X	0	0	0	PR11N_R[4]	PR11N_R[3]	PR11N_R[2]	PR11N_R[1]	PR11N_R[0]	XXh
18th parameter	1	1	↑	X	0	0	0	PR12N_R[4]	PR12N_R[3]	PR12N_R[2]	PR12N_R[1]	PR12N_R[0]	XXh
Description	Gamma Set A registers are applied to source pins numbered S(3n + 1) (n=0, 1, ..., 359) when they output frame memory data [23:16]. See "γ Correction Function" for detailed description of the parameters.												

Gamma Set B (C9h)

C9h	Gamma Set B												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	0	1	C9h
1st parameter	1	1	↑	X	0	0	0	PR0P_G[4]	PR0P_G[3]	PR0P_G[2]	PR0P_G[1]	PR0P_G[0]	XXh
2nd parameter	1	1	↑	X	0	0	0	PR1P_G[4]	PR1P_G[3]	PR1P_G[2]	PR1P_G[1]	PR1P_G[0]	XXh
3rd parameter	1	1	↑	X	PR3P_G[3]	PR3P_G[2]	PR3P_G[1]	PR3P_G[0]	PR2P_G[3]	PR2P_G[2]	PR2P_G[1]	PR2P_G[0]	XXh
4th parameter	1	1	↑	X	PR5P_G[3]	PR5P_G[2]	PR5P_G[1]	PR5P_G[0]	PR4P_G[3]	PR4P_G[2]	PR4P_G[1]	PR4P_G[0]	XXh
5th parameter	1	1	↑	X	0	0	0	0	PR6P_G[3]	PR6P_G[2]	PR6P_G[1]	PR6P_G[0]	XXh
6th parameter	1	1	↑	X	PR8P_G[3]	PR8P_G[2]	PR8P_G[1]	PR8P_G[0]	PR7P_G[3]	PR7P_G[2]	PR7P_G[1]	PR7P_G[0]	XXh
7th parameter	1	1	↑	X	PR10P_G[3]	PR10P_G[2]	PR10P_G[1]	PR10P_G[0]	PR9P_G[3]	PR9P_G[2]	PR9P_G[1]	PR9P_G[0]	XXh
8th parameter	1	1	↑	X	0	0	0	PR11P_G[4]	PR11P_G[3]	PR11P_G[2]	PR11P_G[1]	PR11P_G[0]	XXh
9th parameter	1	1	↑	X	0	0	0	PR12P_G[4]	PR12P_G[3]	PR12P_G[2]	PR12P_G[1]	PR12P_G[0]	XXh
10th parameter	1	1	↑	X	0	0	0	PR0N_G[4]	PR0N_G[3]	PR0N_G[2]	PR0N_G[1]	PR0N_G[0]	XXh
11th parameter	1	1	↑	X	0	0	0	PR1N_G[4]	PR1N_G[3]	PR1N_G[2]	PR1N_G[1]	PR1N_G[0]	XXh
12th parameter	1	1	↑	X	PR3N_G[3]	PR3N_G[2]	PR3N_G[1]	PR3N_G[0]	PR2N_G[3]	PR2N_G[2]	PR2N_G[1]	PR2N_G[0]	XXh
13th parameter	1	1	↑	X	PR5N_G[3]	PR5N_G[2]	PR5N_G[1]	PR5N_G[0]	PR4N_G[3]	PR4N_G[2]	PR4N_G[1]	PR4N_G[0]	XXh
14th parameter	1	1	↑	X	0	0	0	0	PR6N_G[3]	PR6N_G[2]	PR6N_G[1]	PR6N_G[0]	XXh
15th parameter	1	1	↑	X	PR8N_G[3]	PR8N_G[2]	PR8N_G[1]	PR8N_G[0]	PR7N_G[3]	PR7N_G[2]	PR7N_G[1]	PR7N_G[0]	XXh
16th parameter	1	1	↑	X	PR10N_G[3]	PR10N_G[2]	PR10N_G[1]	PR10N_G[0]	PR9N_G[3]	PR9N_G[2]	PR9N_G[1]	PR9N_G[0]	XXh

17th parameter	1	1	↑	X	0	0	0	PR11N_G[4]	PR11N_G[3]	PR11N_G[2]	PR11N_G[1]	PR11N_G[0]	XXh
18th parameter	1	1	↑	X	0	0	0	PR12N_G[4]	PR12N_G[3]	PR12N_G[2]	PR12N_G[1]	PR12N_G[0]	XXh
Description	Gamma Set B registers are applied to source pins numbered S(3n + 2) (n=0, 1, ..., 359) when they output frame memory data [15:8]. See "γ Correction Function" for detailed description of the parameters.												

Gamma Set C (CAh)

CAh	Gamma Set C												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	1	0	CAh
1st parameter	1	1	↑	X	0	0	0	PR0P_B[4]	PR0P_B[3]	PR0P_B[2]	PR0P_B[1]	PR0P_B[0]	XXh
2nd parameter	1	1	↑	X	0	0	0	PR1P_B[4]	PR1P_B[3]	PR1P_B[2]	PR1P_B[1]	PR1P_B[0]	XXh
3rd parameter	1	1	↑	X	PR3P_B[3]	PR3P_B[2]	PR3P_B[1]	PR3P_B[0]	PR2P_B[3]	PR2P_B[2]	PR2P_B[1]	PR2P_B[0]	XXh
4th parameter	1	1	↑	X	PR5P_B[3]	PR5P_B[2]	PR5P_B[1]	PR5P_B[0]	PR4P_B[3]	PR4P_B[2]	PR4P_B[1]	PR4P_B[0]	XXh
5th parameter	1	1	↑	X	0	0	0	0	PR6P_B[3]	PR6P_B[2]	PR6P_B[1]	PR6P_B[0]	XXh
6th parameter	1	1	↑	X	PR8P_B[3]	PR8P_B[2]	PR8P_B[1]	PR8P_B[0]	PR7P_B[3]	PR7P_B[2]	PR7P_B[1]	PR7P_B[0]	XXh
7th parameter	1	1	↑	X	PR10P_B[3]	PR10P_B[2]	PR10P_B[1]	PR10P_B[0]	PR9P_B[3]	PR9P_B[2]	PR9P_B[1]	PR9P_B[0]	XXh
8th parameter	1	1	↑	X	0	0	0	PR11P_B[4]	PR11P_B[3]	PR11P_B[2]	PR11P_B[1]	PR11P_B[0]	XXh
9th parameter	1	1	↑	X	0	0	0	PR12P_B[4]	PR12P_B[3]	PR12P_B[2]	PR12P_B[1]	PR12P_B[0]	XXh
10th parameter	1	1	↑	X	0	0	0	PR0N_B[4]	PR0N_B[3]	PR0N_B[2]	PR0N_B[1]	PR0N_B[0]	XXh
11th parameter	1	1	↑	X	0	0	0	PR1N_B[4]	PR1N_B[3]	PR1N_B[2]	PR1N_B[1]	PR1N_B[0]	XXh
12th parameter	1	1	↑	X	PR3N_B[3]	PR3N_B[2]	PR3N_B[1]	PR3N_B[0]	PR2N_B[3]	PR2N_B[2]	PR2N_B[1]	PR2N_B[0]	XXh
13th parameter	1	1	↑	X	PR5N_B[3]	PR5N_B[2]	PR5N_B[1]	PR5N_B[0]	PR4N_B[3]	PR4N_B[2]	PR4N_B[1]	PR4N_B[0]	XXh
14th parameter	1	1	↑	X	0	0	0	0	PR6N_B[3]	PR6N_B[2]	PR6N_B[1]	PR6N_B[0]	XXh
15th parameter	1	1	↑	X	PR8N_B[3]	PR8N_B[2]	PR8N_B[1]	PR8N_B[0]	PR7N_B[3]	PR7N_B[2]	PR7N_B[1]	PR7N_B[0]	XXh
16th parameter	1	1	↑	X	PR10N_B[3]	PR10N_B[2]	PR10N_B[1]	PR10N_B[0]	PR9N_B[3]	PR9N_B[2]	PR9N_B[1]	PR9N_B[0]	XXh

17th parameter	1	1	↑	X	0	0	0	PR11N_B[4]	PR11N_B[3]	PR11N_B[2]	PR11N_B[1]	PR11N_B[0]	XXh
18th parameter	1	1	↑	X	0	0	0	PR12N_B[4]	PR12N_B[3]	PR12N_B[2]	PR12N_B[1]	PR12N_B[0]	XXh
Description	Gamma Set C registers are applied to source pins numbered S(3n + 3) (n=0, 1, ..., 359) when they output frame memory data [7:0]. See "γ Correction Function" for detailed description of the parameters.												

Power Control

Power Setting for Common (D0h)

D0h	Power Setting for Common												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	0	D0h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	0	XXh
2nd parameter	1	#A	#B	X	0	VC3 [2]	VC3 [1]	VC3 [0]	0	VC2 [2]	VC2 [1]	VC2 [0]	XXh
3rd parameter	1	#A	#B	X	1	1	0	0	0	0	0	0	XXh
4th parameter	1	#A	#B	X	1	0	0	VRH [4]	VRH [3]	VRH [2]	VRH [1]	VRH [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.)												

VC2[2:0]

These bits are used to define VCI2 level using VCIR level. VCI2 is the reference voltage of VGH and VGL voltages.

Table 78

VC2[2:0]	VCI2 voltage (Step-up output reference voltage)
3'h0	Setting inhibited
3'h1	VCIR × 1.36
3'h2	VCIR × 1.44
3'h3	VCIR × 1.52
3'h4	VCIR × 1.60
3'h5	VCIR × 1.68
3'h6	Setting inhibited
3'h7	Setting inhibited

Note: VGH=VCI2 x 4. VGL= -(VCI2 x 2＋VCI3).

VC3[2:0]

These bits are used to define VCI3 level using VCIR level. VCI3 is the reference voltage of VGL.

Table 79

VC3[2:0]	VCI3 voltage (Step-up output reference voltage)
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	Setting inhibited
3'h3	VCIR x 0.800
3'h4	Setting inhibited
3'h5	VCIR x 0.889
3'h6	Setting inhibited
3'h7	VCIR x 1.000

Note: VGL= -(VCI2×2+VCI3)

VRH[4:0]

Sets VREG1 voltage from 1.475 x VCIR to 1.875 x VCIR. VCIR is the internal reference power supply.

Table 80

VRH[4:0]	VREG1	VRH[4:0]	VREG1
5'h00-5'h0A	Setting inhibited	5'h15	VCIR × 1.725
5'h0B	VCIR × 1.475	5'h16	VCIR × 1.750
5'h0C	VCIR × 1.500	5'h17	VCIR × 1.775
5'h0D	VCIR × 1.525	5'h18	VCIR × 1.800
5'h0E	VCIR × 1.550	5'h19	VCIR × 1.825
5'h0F	VCIR × 1.575	5'h1A	VCIR × 1.850
5'h10	VCIR × 1.600	5'h1B	VCIR × 1.875
5'h11	VCIR × 1.625	5'h1C	VCIR × 1.900
5'h12	VCIR × 1.650	5'h1D	VCIR × 1.925
5'h13	VCIR × 1.675	5'h1E	VCIR × 1.950
5'h14	VCIR × 1.700	5'h1F	VCIR × 1.975

Note: Make sure that VREG1≦DDVDH*-0.5V(*=A,B).

VCOM Setting (D1h)

D1h	VCOM Setting												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	1	D1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	WCVDV	WCVCM	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	0	0	0	XXh
3rd parameter	1	#A	#B	X	1	VCM [6]	VCM [5]	VCM [4]	VCM [3]	VCM [2]	VCM [1]	VCM [0]	XXh
4th parameter	1	#A	#B	X	1	1	1	VDV [4]	VDV [3]	VDV [2]	VDV [1]	VDV [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When this command is read via DSI, dummy read operation is not performed.)												

WCVCM

WCVCM=1: Used to enable writing to 2nd parameter's VCM [6:0]. To set NVM write data, write WCVCM=1.

WCVCM=0: Used to disable writing to 2nd parameter's VCM [6:0]. Values loaded from NVM are retained even if this parameter is written.

WCVDV

WCVDC=1: Used to enable writing to the 3rd parameter's VDV[4:0]. To set NVM write data, write WCVDC=1.

WCVDC=0: Used to disable writing to the 3rd parameter's VDV[4:0]. Values loaded from NVM are retained even if this parameter is written.

VCM[6:0]

These bits are used to set the amplification factor of VCOMH using VREG1.

Table 81

VCM[6:0]	VCOMH voltage	VCM[6:0]	VCOMH voltage	VCM[6:0]	VCOMH voltage
7'h00	VREG1 x 0.492	7'h2B	VREG1 x 0.664	7'h56	VREG1 x 0.836
7'h01	VREG1 x 0.496	7'h2C	VREG1 x 0.668	7'h57	VREG1 x 0.840
7'h02	VREG1 x 0.500	7'h2D	VREG1 x 0.672	7'h58	VREG1 x 0.844
7'h03	VREG1 x 0.504	7'h2E	VREG1 x 0.676	7'h59	VREG1 x 0.848
7'h04	VREG1 x 0.508	7'h2F	VREG1 x 0.680	7'h5A	VREG1 x 0.852
7'h05	VREG1 x 0.512	7'h30	VREG1 x 0.684	7'h5B	VREG1 x 0.856
7'h06	VREG1 x 0.516	7'h31	VREG1 x 0.688	7'h5C	VREG1 x 0.860
7'h07	VREG1 x 0.520	7'h32	VREG1 x 0.692	7'h5D	VREG1 x 0.864
7'h08	VREG1 x 0.524	7'h33	VREG1 x 0.696	7'h5E	VREG1 x 0.868
7'h09	VREG1 x 0.528	7'h34	VREG1 x 0.700	7'h5F	VREG1 x 0.872
7'h0A	VREG1 x 0.532	7'h35	VREG1 x 0.704	7'h60	VREG1 x 0.876
7'h0B	VREG1 x 0.536	7'h36	VREG1 x 0.708	7'h61	VREG1 x 0.880
7'h0C	VREG1 x 0.540	7'h37	VREG1 x 0.712	7'h62	VREG1 x 0.884
7'h0D	VREG1 x 0.544	7'h38	VREG1 x 0.716	7'h63	VREG1 x 0.888
7'h0E	VREG1 x 0.548	7'h39	VREG1 x 0.720	7'h64	VREG1 x 0.892
7'h0F	VREG1 x 0.552	7'h3A	VREG1 x 0.724	7'h65	VREG1 x 0.896
7'h10	VREG1 x 0.556	7'h3B	VREG1 x 0.728	7'h66	VREG1 x 0.900
7'h11	VREG1 x 0.560	7'h3C	VREG1 x 0.732	7'h67	VREG1 x 0.904
7'h12	VREG1 x 0.564	7'h3D	VREG1 x 0.736	7'h68	VREG1 x 0.908
7'h13	VREG1 x 0.568	7'h3E	VREG1 x 0.740	7'h69	VREG1 x 0.912
7'h14	VREG1 x 0.572	7'h3F	VREG1 x 0.744	7'h6A	VREG1 x 0.916
7'h15	VREG1 x 0.576	7'h40	VREG1 x 0.748	7'h6B	VREG1 x 0.920
7'h16	VREG1 x 0.580	7'h41	VREG1 x 0.752	7'h6C	VREG1 x 0.924
7'h17	VREG1 x 0.584	7'h42	VREG1 x 0.756	7'h6D	VREG1 x 0.928
7'h18	VREG1 x 0.588	7'h43	VREG1 x 0.760	7'h6E	VREG1 x 0.932
7'h19	VREG1 x 0.592	7'h44	VREG1 x 0.764	7'h6F	VREG1 x 0.936
7'h1A	VREG1 x 0.596	7'h45	VREG1 x 0.768	7'h70	VREG1 x 0.940
7'h1B	VREG1 x 0.600	7'h46	VREG1 x 0.772	7'h71	VREG1 x 0.944
7'h1C	VREG1 x 0.604	7'h47	VREG1 x 0.776	7'h72	VREG1 x 0.948
7'h1D	VREG1 x 0.608	7'h48	VREG1 x 0.780	7'h73	VREG1 x 0.952
7'h1E	VREG1 x 0.612	7'h49	VREG1 x 0.784	7'h74	VREG1 x 0.956
7'h1F	VREG1 x 0.616	7'h4A	VREG1 x 0.788	7'h75	VREG1 x 0.960
7'h20	VREG1 x 0.620	7'h4B	VREG1 x 0.792	7'h76	VREG1 x 0.964
7'h21	VREG1 x 0.624	7'h4C	VREG1 x 0.796	7'h77	VREG1 x 0.968
7'h22	VREG1 x 0.628	7'h4D	VREG1 x 0.800	7'h78	VREG1 x 0.972
7'h23	VREG1 x 0.632	7'h4E	VREG1 x 0.804	7'h79	VREG1 x 0.976
7'h24	VREG1 x 0.636	7'h4F	VREG1 x 0.808	7'h7A	VREG1 x 0.980
7'h25	VREG1 x 0.640	7'h50	VREG1 x 0.812	7'h7B	VREG1 x 0.984
7'h26	VREG1 x 0.644	7'h51	VREG1 x 0.816	7'h7C	VREG1 x 0.988
7'h27	VREG1 x 0.648	7'h52	VREG1 x 0.820	7'h7D	VREG1 x 0.992
7'h28	VREG1 x 0.652	7'h53	VREG1 x 0.824	7'h7E	VREG1 x 0.996
7'h29	VREG1 x 0.656	7'h54	VREG1 x 0.828	7'h7F	VREG1 x 1.000
7'h2A	VREG1 x 0.660	7'h55	VREG1 x 0.832		

VDV[4:0]

These bits are used to set VCOM alternating amplitude as tabulated below.

Table 82

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	VREG1×1.32	5'h10	VREG1×1.00
5'h01	VREG1×1.30	5'h11	VREG1×0.98
5'h02	VREG1×1.28	5'h12	VREG1×0.96
5'h03	VREG1×1.26	5'h13	VREG1×0.94
5'h04	VREG1×1.24	5'h14	VREG1×0.92
5'h05	VREG1×1.22	5'h15	VREG1×0.90
5'h06	VREG1×1.20	5'h16	VREG1×0.88
5'h07	VREG1×1.18	5'h17	VREG1×0.86
5'h08	VREG1×1.16	5'h18	VREG1×0.84
5'h09	VREG1×1.14	5'h19	VREG1×0.82
5'h0A	VREG1×1.12	5'h1A	VREG1×0.80
5'h0B	VREG1×1.10	5'h1B	VREG1×0.78
5'h0C	VREG1×1.08	5'h1C	VREG1×0.76
5'h0D	VREG1×1.06	5'h1D	VREG1×0.74
5'h0E	VREG1×1.04	5'h1E	VREG1×0.72
5'h0F	VREG1×1.02	5'h1F	VREG1×0.70

Note: Make sure that VCOM amplitude is 6.0V or less.

Power Setting for Normal/Partial Mode (D2h)

Power Setting for Idle Mode (D4h)

D2h	**Power Setting for Normal/Partial Mode**												
	DCX	RDX	WR X	DB 15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	0	D2h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	AP0 [0]	AP0 [0]	XXh
2nd parameter	1	#A	#B	X	0	DC10 [2]	DC10 [1]	DC10 [0]	0	DC00 [2]	DC00 [1]	DC00 [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DC30 [2]	DC30 [1]	DC30 [0]	XXh
D4h	**Power Setting for Idle Mode**												
	DCX	RDX	WR X	DB 15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	1	0	0	D4h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	AP2 [0]	AP2 [0]	XXh
2nd parameter	1	#A	#B	X	0	DC12 [2]	DC12 [1]	DC12 [0]	0	DC02 [2]	DC02 [1]	DC02 [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DC32 [2]	DC32 [1]	DC32 [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When these commands are read via DSI, dummy read operation is not performed.) Power control is definable for each mode. D2h is enabled when Normal/Partial Mode is On and Idle Mode is Off. D4h is enabled when Normal/Partial Mode is On and Idle Mode is On.												

AP0[1:0] Normal/Partial mode
AP2[1:0] Idle mode
These bits adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current will enhance the drivability of the LCD, however more current will be consumed. Adjust the constant current considering the trade-off between the display quality and the current consumption.

Table 83

AP0[1:0] AP2[1:0]	Constant current in operational amplifier in LCD power supply circuit
2'h0	Halt operational amplifier and step-up circuits
2'h1	0.5
2'h2	0.75
2'h3	1

Note: The values represent the ratios of constant current in respective APn[1:0] settings to the constant current when APn[1:0] is set to 2'h3.

DC00[2:0] Normal/Idle mode
DC02[2:0] Idle mode

These bits are used to set the step-up clock frequency of the step-up circuit that generates DDVDHA/DDVDHB.

Table 84

DC00[2:0] DC02[2:0]	Step-up clock frequency (f_{DCDC1})	
	PTDC=0 (Normal operation)	PTDC=1 (Low-speed operation)
3'h0	f_{osc}/8	f_{osc}/10
3'h1	f_{osc}/10	f_{osc}/12
3'h2	f_{osc} /12	f_{osc} /16
3'h3	f_{osc} /16	f_{osc} /20
3'h4	f_{osc}/20	f_{osc}/24
3'h5	f_{osc}/24	f_{osc}/32
3'h6	The step-up circuit halts	The step-up circuit halts
3'h7	f_{osc}/32	f_{osc}/32

DC10[2:0]: Normal / Partial mode
DC12[2:0]: Idle mode

These bits are used to define the step-up clock frequency of the step-up circuit that generates VGH and VGL.

Table 85

DC10[2:0] DC12[2:0]	Step-up clock frequency (f_{DCDC2})
3'h0	Line frequency / 2
3'h1	Line frequency / 4
3'h2	Line frequency / 8
3'h3	Line frequency / 16
3'h4	Line frequency / 32
3'h5	Setting inhibited
3'h6	The step-up circuit halts
3'h7	Setting inhibited

DC30[2:0] Normal / Partial mode
DC32[2:0] Idle mode

These bits are used to define the step-up clock frequency of the step-up circuit that generates VCL.

Table 86

DC30[2:0] DC32[2:0]	Step-up clock frequency (f_{DCDC3})
3'h0	f_{OSC}/16
3'h1	f_{OSC}/20
3'h2	f_{OSC}/24
3'h3	Frequency set by DC00/DC02
3'h4	Line frequency / 2
3'h5	Line frequency / 4
3'h6	The step-up circuit halts
3'h7	Line frequency / 8

NVM Control

NVM Access Control (E0h)

E0h	NVM Access Control												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	0	E0h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	NVAE	XXh
2nd parameter	1	#A	#B	X	0	FTT	0	1	1	0	0	NVAD [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	TEM [0]	0	0	VERIF LGWR	VERIF LGER	XXh
4th parameter	1	#A	#B	X	0	0	0	0	0	1	1	1	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note : When this command is read via DSI, dummy read operation is not performed.)												

NVAE:
The bit is used to enable access to NVM when NVAE=1.

FTT:
NVM control register. When FTT=1, NVM write/erase is triggered. The bit is set to 0 when NVM write and verify is finished.

NVAD[0]:

The bit decides which command is used to write data to NVM.

Table 87

NVAD[0]	Command used to write data to NVM
0	A1h: DDB0-DDB3[7:0]
1	D1h: VCM[6:0], VDV[4:0]

VERIFLGER
This bit is used for data read only. Writing data to this bit is ignored. Data erase and erase verify are executed before performing a data write. This bit is written according to the result of the erase verify.

If the result of erase verify is good: VERIFLGER=1
If the result of erase verify is not good: VERIFLGER=0

VERIFLGWR
This bit is used for data read only. Writing data to this bit is ignored. Data write and write verify are executed before performing a data erase. This bit is written according to the result of the write verify.

If the result of write verify is good: VERIFLGWR=1
If the result of write verify is not good: VERIFLGWR=0

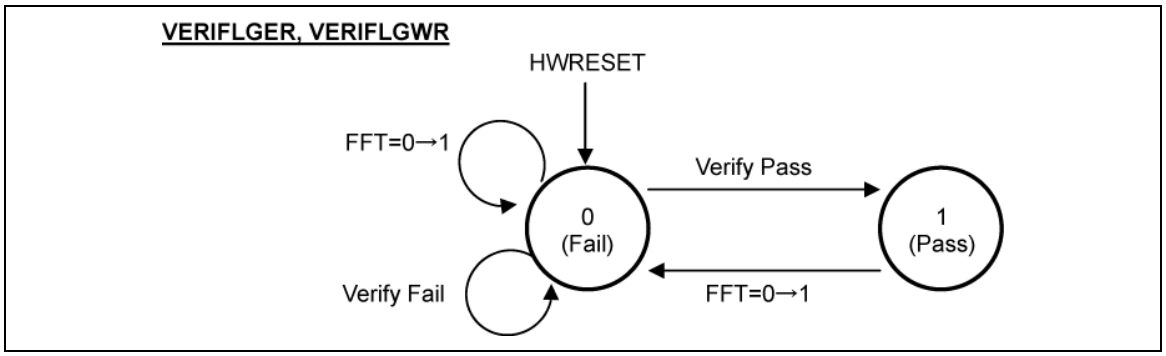


Figure 33

TEM [0]
This bit is used to define TE output.

Table 88

TEM[0]	TE output
1'h0	Tearing Effect
1'h1	TE is used to output the result of automatic NVM write data verify. (VERIFLGWR) TE = 0 The write data was correct. TE = 1 The write data was not correct.

Note: The TE pin output is fixed at the low level when Sleep mode is on or Tearing Effect output is off.

set_DDB_write_control (E1h)

E1h	set_DDB_write_control												
	DCX	RDX	WRX	DB15-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	1	E1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	WCDDB	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read (Note: When reading by DSI, there is no dummy read.)												

WCDDB

WCDDB=1: Writing to A1h's ID1[15:0] and ID2[15:0] is enabled. The data written to A1h: ID1[15:0] and ID2[15:0] can be written to NVM. ID2[15:0]≠16'hFFFF shall be set. No data can be written using read_DDB_continue (A8h).

WCDDB=0: Writing data to A1h's ID1[15:0] and ID2[15:0] cannot be performed. Write WCDDB=0 except when writing to the NVM.

Reset

The R61523 internal initial setting is done with a RESET input. During the RESET period, no access, whether it is command write or frame memory data write operation, is accepted. The source driver unit and the power supply circuit unit are also reset to the respective initial states when RESET signal is inputted to the R61523.

Initial state of command

The initial state of command is shown in Default Modes and Values table in Command List. See "Default Modes and Values." The command setting is initialized to the default value when a Hardware Reset is executed.

Initial state of Frame Memory data

The Frame Memory data is not automatically initialized by inputting RESET. It needs to be initialized by software during Display Off period.

Initial state of input/output pin

Table 89

Pin name	After H/W reset	Pin name	After H/W reset
S1-1080	GND	C11AP/C11AM	Hi-Z/Hi-Z
G1-640	GND	C11BP/C11BM	Hi-Z/Hi-Z
VCOM	GND	C12AP/C12AM	Hi-Z/Hi-Z
VCOMH	VCI	C12BP/C12BM	Hi-Z/Hi-Z
VCOML	GND	C13P/ C13M	Hi-Z/Hi-Z
VCL	GND	C21P/C21M	VCI/GND
VGH	VCI	C22P/C22M	VCI/GND
VGL	GND	C23P/C23M	VCI/GND
VREG1	VGS	C31P/C31M	VCI/GND
DDVDHA	VCI		
DDVDHB	VCI		
TE	GND		
LEDPWM	GND		
VDD	1.5V		

Frame Memory

The frame memory retains image data of up to 5,529,600 bits (640 x 360 x 24 bits).

Address Mapping from Memory to Display

Normal Display On or Partial Mode On

In this mode, a content of the frame memory within an area where column pointer is 0000h to 0167h and page pointer is 0000h to 027Fh is displayed.

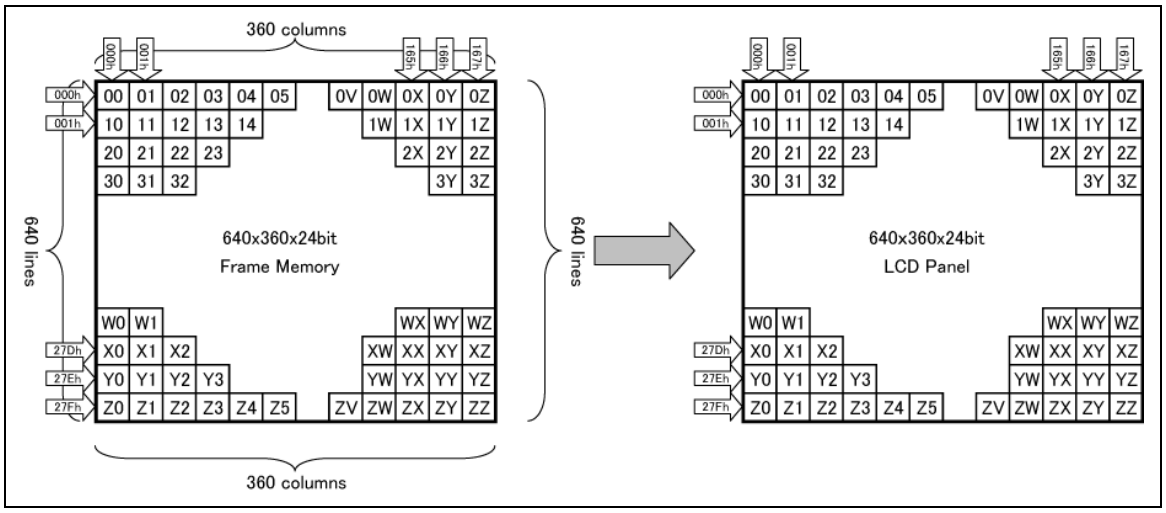


Figure 34

Write/Read Direction from/to Host Processor

The figure below illustrates data stream from the host processor.

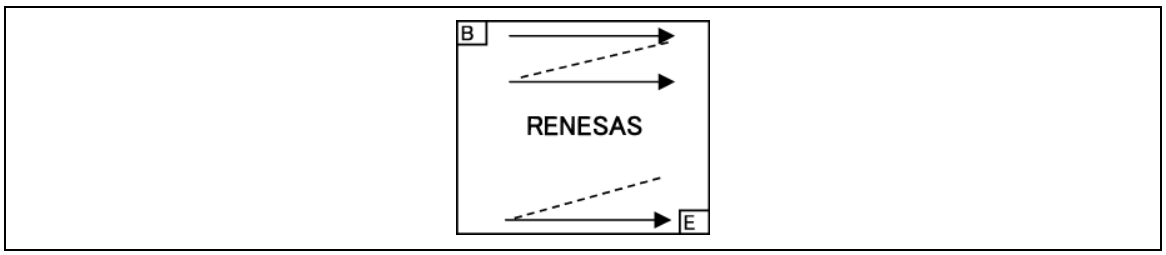


Figure 35

The data is written in the order illustrated above. The Counter which dictates write position on the physical memory is controlled by "set_address_mode (36h)" command Bits B5, B6, B7 as illustrated below.

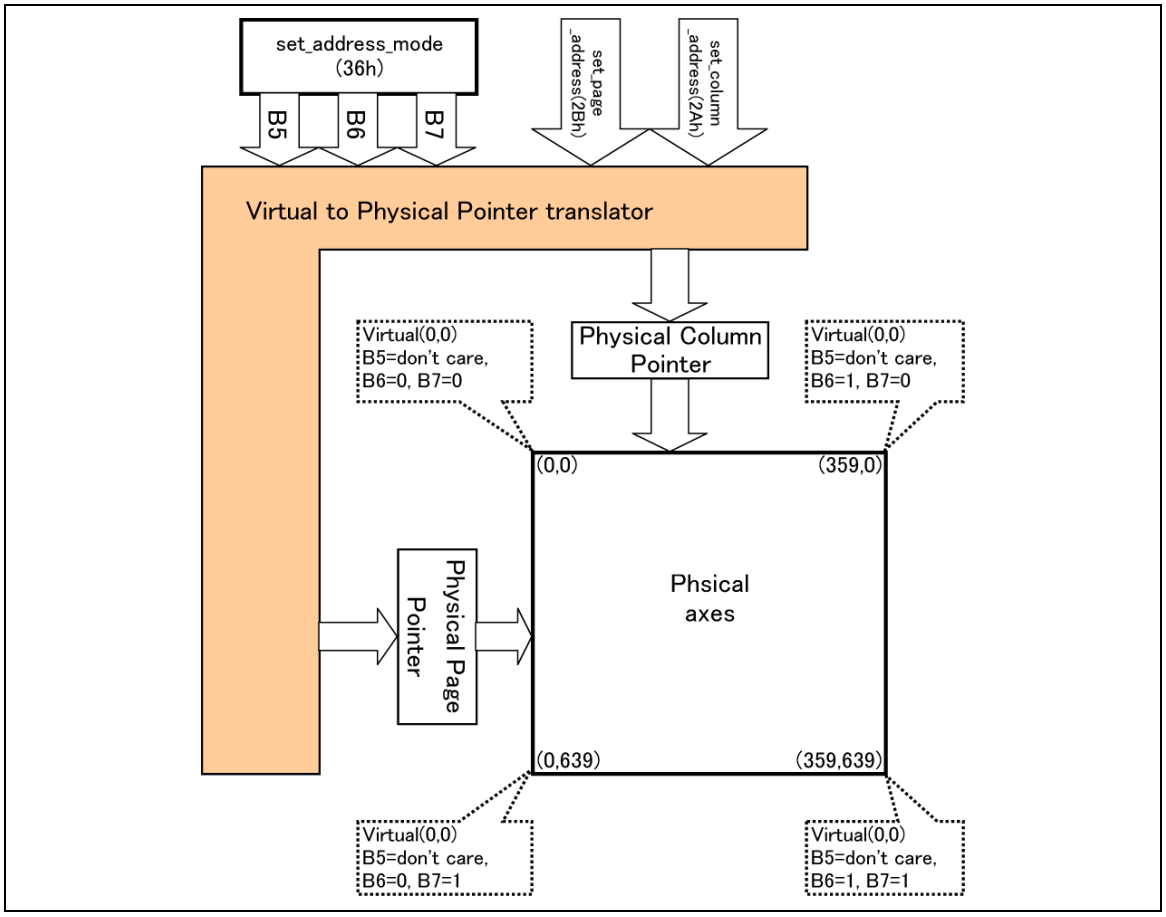


Figure 36

Table 90

B5	B6	B7	Column Address	Page Address
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (639-Physical Page Pointer)
0	1	0	Direct to (359-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (359-Physical Column Pointer)	Direct to (639-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (639-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (359-Physical Column Pointer)
1	1	1	Direct to (639-Physical Page Pointer)	Direct to (359-Physical Column Pointer)

For each image orientation, the controls on the columns and page counters apply as below.

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by set_address_mode (36h) bits B7, B6 and B5. The write order for each pixel unit is as follows:

Table 91

D23	D22	D21	D20	D19	D18	D17	D16
R7	R6	R5	R4	R3	R2	R1	R0

D15	D14	D13	D12	D11	D10	D9	D8
G7	G6	G5	G4	G3	G2	G1	G0

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

Table 92

Condition	Column counter	Page counter	Note
When commands write_memory_start (2Ch) and read_memory_start (2Eh) are received.	Back to Start Column	Back to Start Page	
Execute Pixel Read/Write	Increment by 1	No change	
When column counter value is larger than ”End Column”	Back to Start Column	Increment by 1	
When column counter value is larger than ”End Column” and page counter value is larger than “End Page”	STOP	STOP	Entry Mode(B3h) WEMODE=0
	Back to Start Column	Back to Start Page	Entry Mode(B3h) WEMODE=1

One pixel unit represents 1 column and 1 page counter value on the Frame Memory. See the next page for the resultant image for each orientation setting.

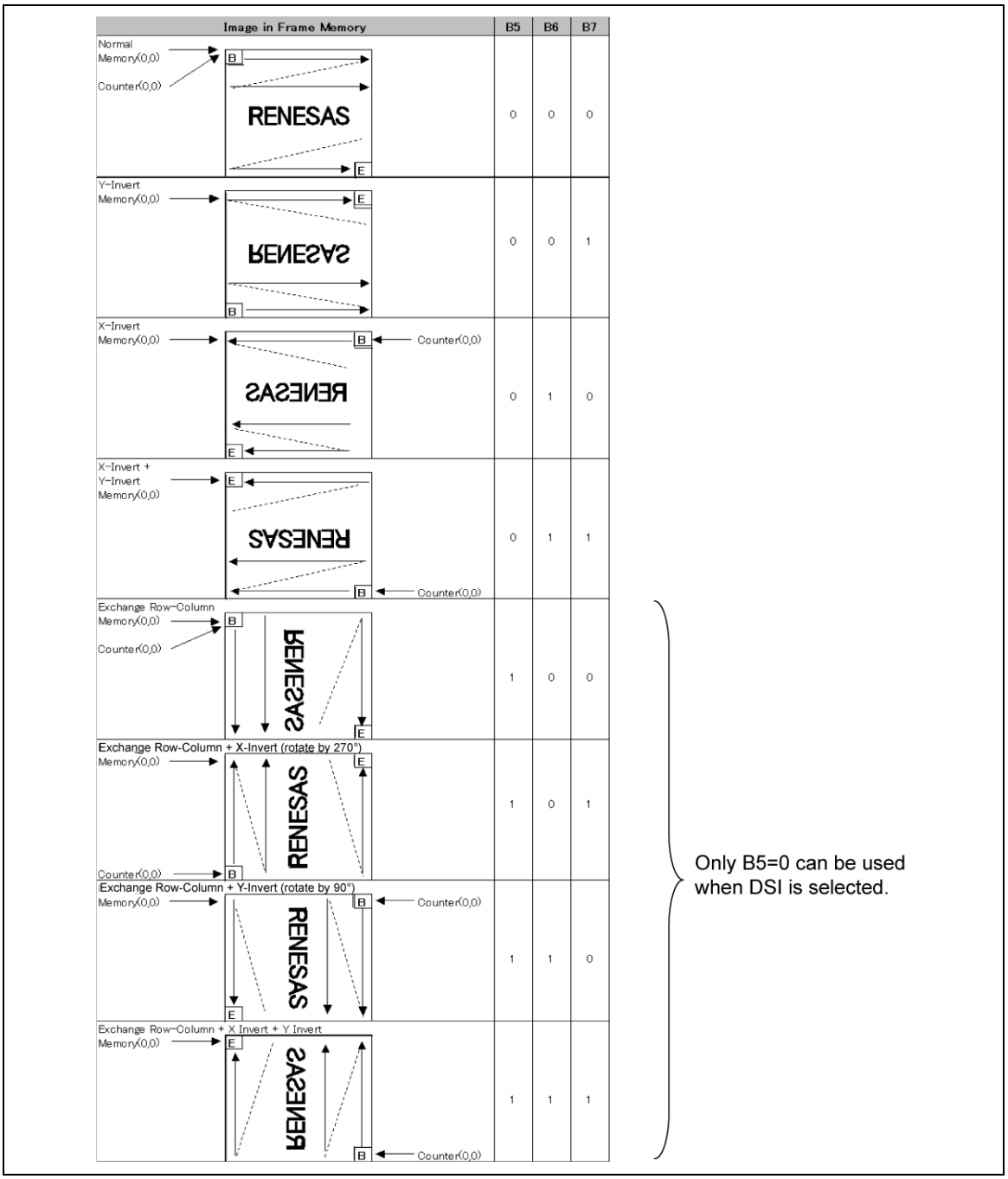


Figure 37

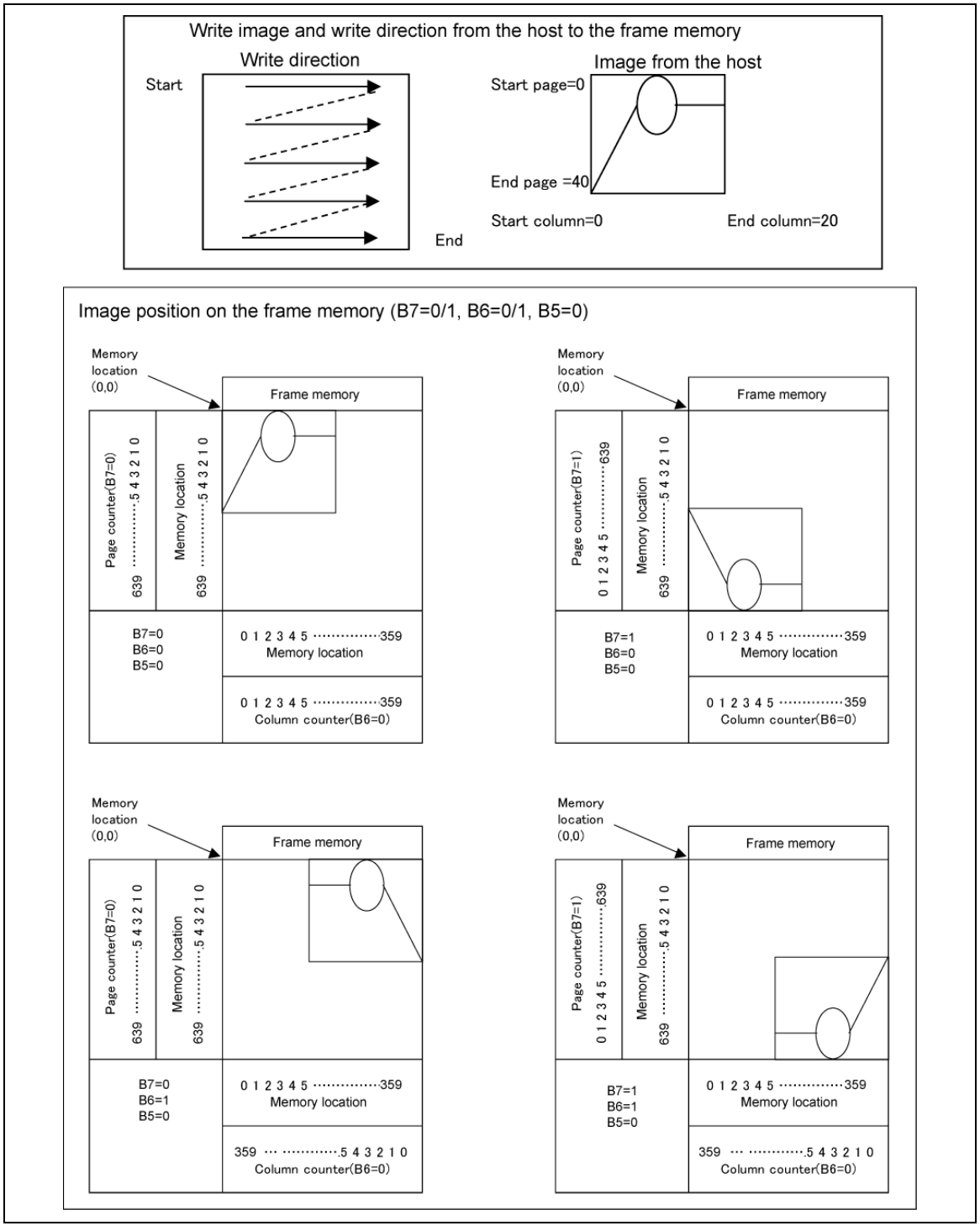


Figure 38

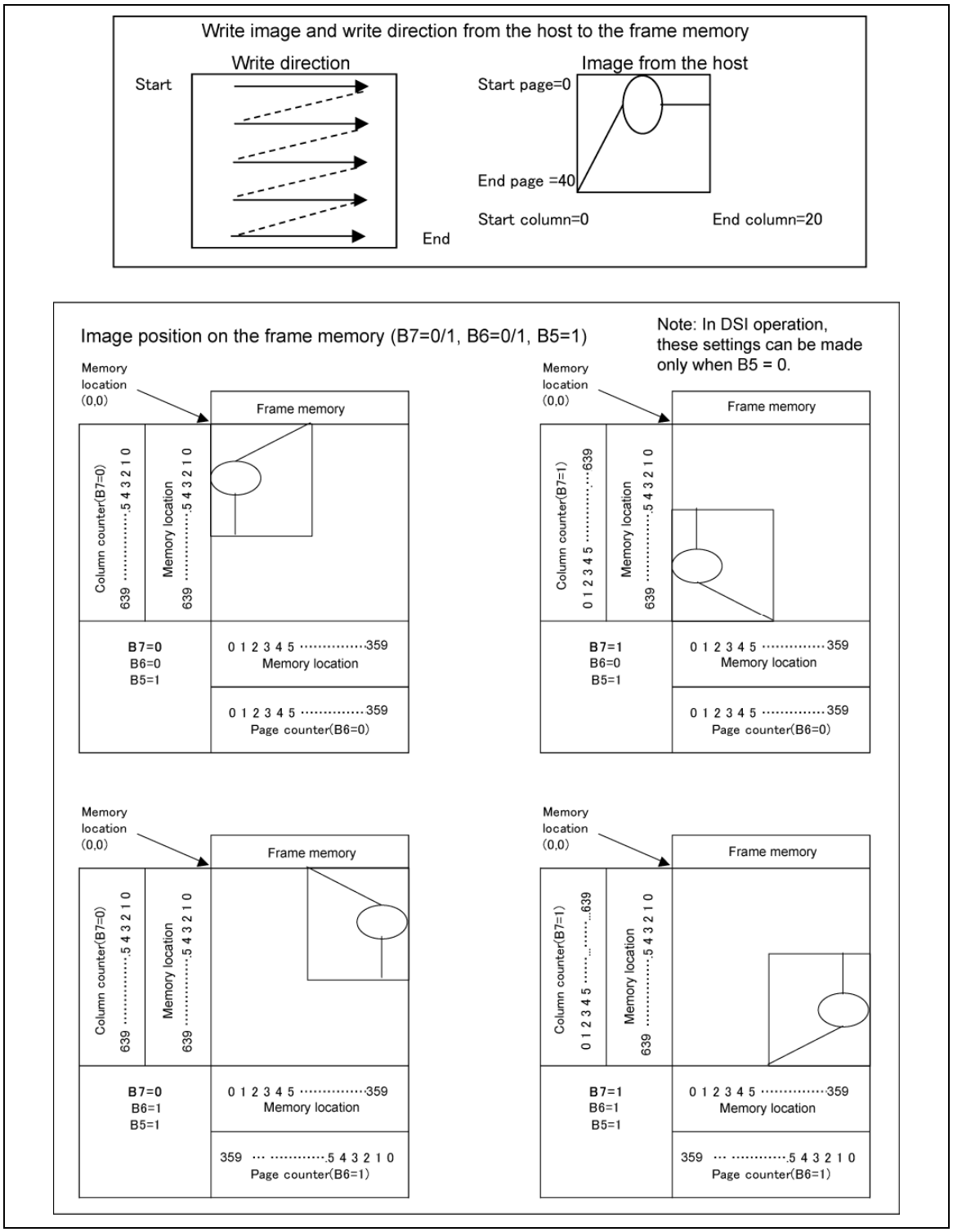


Figure 39

Self-Diagnostic Function

The R61523 supports the self-diagnostic functions. Set get_diagnostic_result (0Fh) 1st parameter's D6 bit according to the following flow chart.

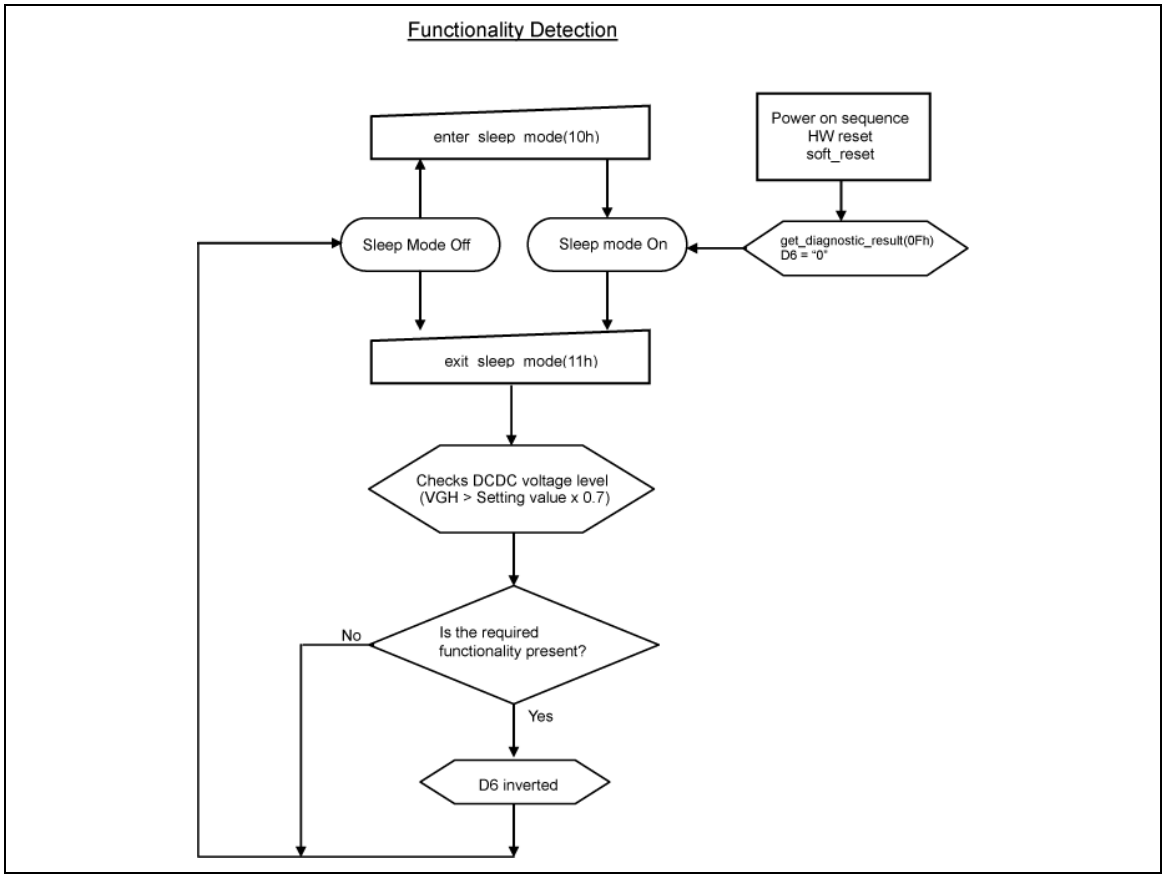


Figure 40

Dynamic Backlight Control Function

The R61523 supports BLC (backlight control) function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The display image is dynamically controlled by BLC function. The availability of this function ranges from moving picture such as TV image to still picture such as menu. The histogram of display data is analyzed by BLC function, according to the brightness range of backlight set by parameters. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image.

Notes 1: The BLC function is enabled by BLCON bit setting (B8h: Back Light Control).
2: The effect of BLC function on power efficiency and display quality depends on image data and the setting. Check display quality on the panel.

- Control backlight dynamically according to the image histogram.
- PWM pin for LED backlight adjustment (LEDPWM)
- PWM signal control register set by the host processor. Backlight dimmer is adjusted by calculating internally decided PWM value and maximum PWM value from the host processor.

System Configuration

1. The PWM signal is used to directly connect the R61523 and LED driver IC. The LED driver IC is controlled entirely via the R61523.

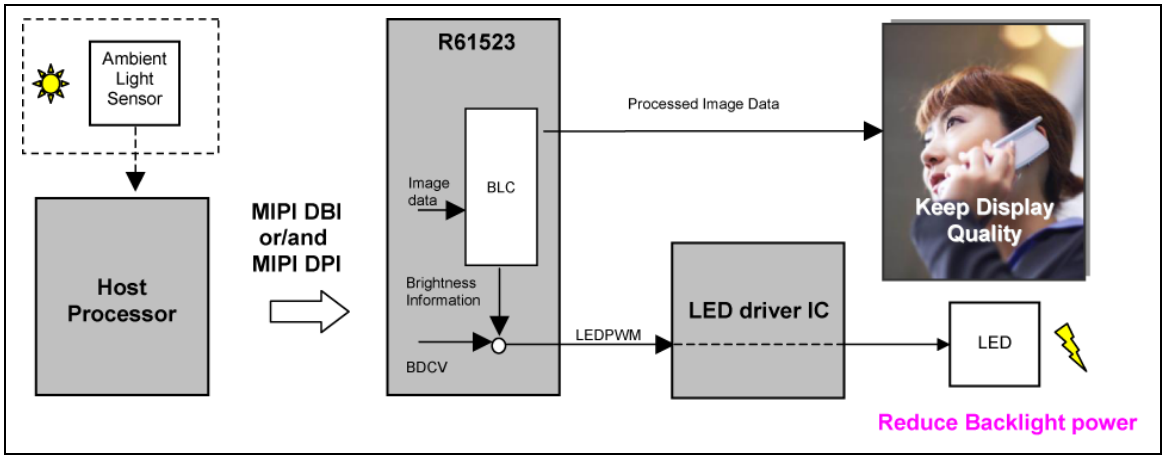


Figure 41

2. The host processor reads LED brightness information internally generated by BLC processing from the R61523 via MIPI DBI. Then, the LED driver IC is controlled from the host processor. There is the time difference between brightness adjustment by PWM and displaying data processed from the R61523. Check the effect on the image.

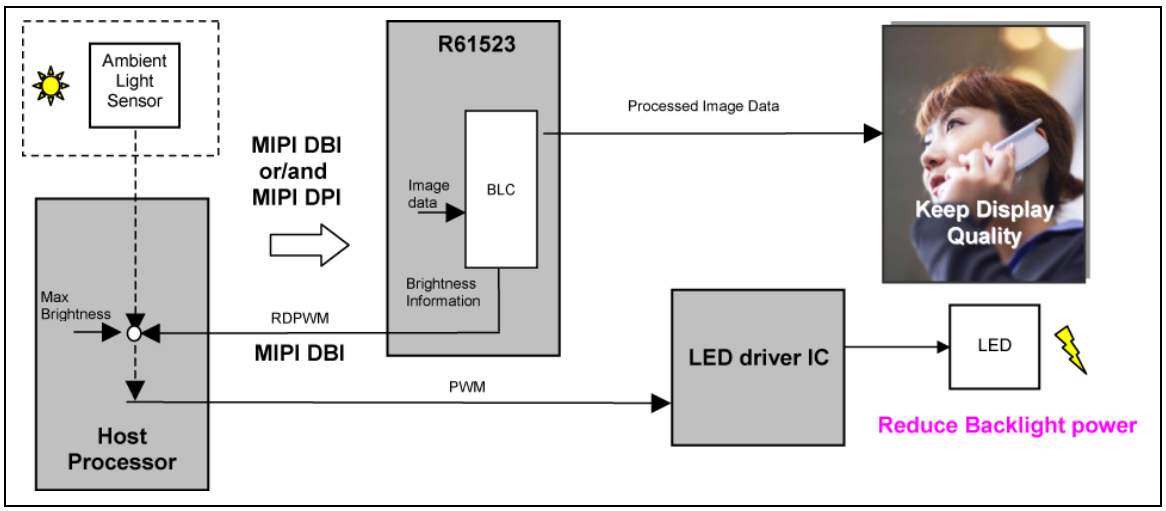


Figure 42

BLC Parameter Setting

The backlight control function has the following two functions.

- Image processing and backlight control processing
- Processing for retaining the grayscale of the display image that has turned white

These functions are set by the following parameters.

(1) BLC operating threshold (THREW)

(2) Amount of change of threshold grayscale value (Dth) per frame (PITCHW)

(3) Difference between two grayscale values counted by the histogram counter (CGAPW)

(4) Backlight brightness adjustment range (ULMTW and LLMTW)

(5) Gamma conversion table (TBL_MIN and TBLx[7:0])

(6) Interpolation to prevent display image from turning white (COEFK)

(1) THREW[4:0]

This parameter sets the ratio (percentage) of the maximum number of pixels that makes display image white (= data “255”) to the total of pixels by image processing. The ratio can be set from 0 to 62% in units of two percent. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (Dth) that makes display image white is set so that the number of the pixels set by this parameter does not change.

To reduce the power by about 30%, set the above ratio to 30% (THREW = 5’h0F). When the value set by this parameter exceeds the range of Dth to be stated later, the priority is given to the range of threshold grayscale value (Dth).

According to the relationship between threshold grayscale value (Dth) and gamma conversion table (see (5)), the rate of backlight brightness reduction (= the rate of power reduction) and image correction factor are set.

- The larger THREW value tends to enhance the effect of reducing backlight power, and increases the image correction factor. In this case, the effect on image quality tends to increase (see note 1).
- The smaller THREW value tends to reduce the effect of reducing backlight power, and decreases the image correction factor. In this case, the effect on image quality tends to decrease (see note 1).

Notes: 1. The tendency for backlight power reduction and the effect on image by BLC function depend on image data. Check actual display quality.
2. The results of the above histogram analysis are enabled from the next frame.

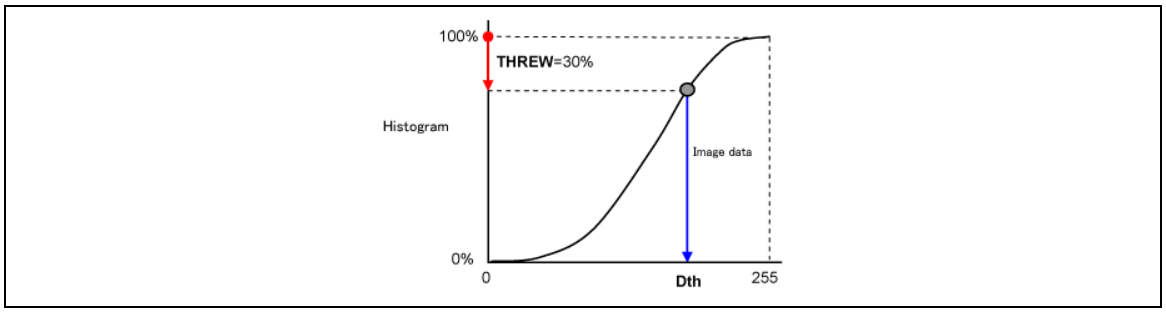


Figure 43

(2) PITCHW[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one half of the grayscale. When the target (Dth_t) is changed by the histogram change of input image including video image, this parameter can adjust the amount of changing threshold grayscale value (Dth). So, this parameter is effective in reducing a sharp change of backlight brightness. Make sure CGAPW[4:0] ≥ PITCHW[3:0] when setting.

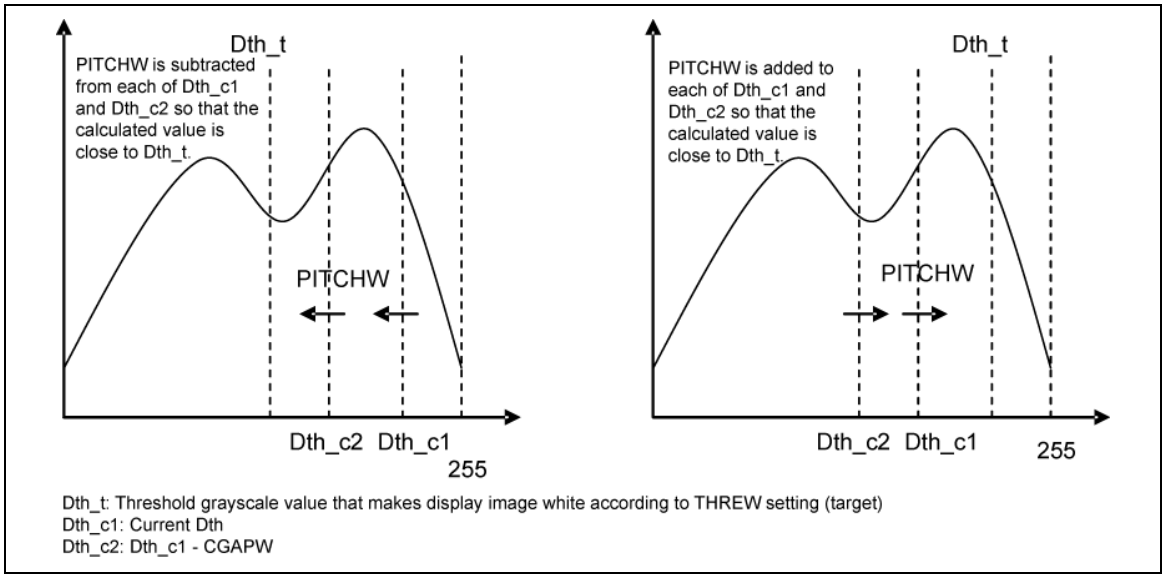


Figure 44

(3) CGAPW[4:0]

The difference of the two grayscales (Dth_c1 and Dth_c2) counted by the present threshold counter is set in units of one half of the grayscale. This parameter is effective in slowing the change of threshold grayscale value (Dth). So, the speed of the change of Dth is adjusted to reduce subtle changes and flickers. Make sure CGAPW[4:0] ≥ PITCHW[3:0] when setting.

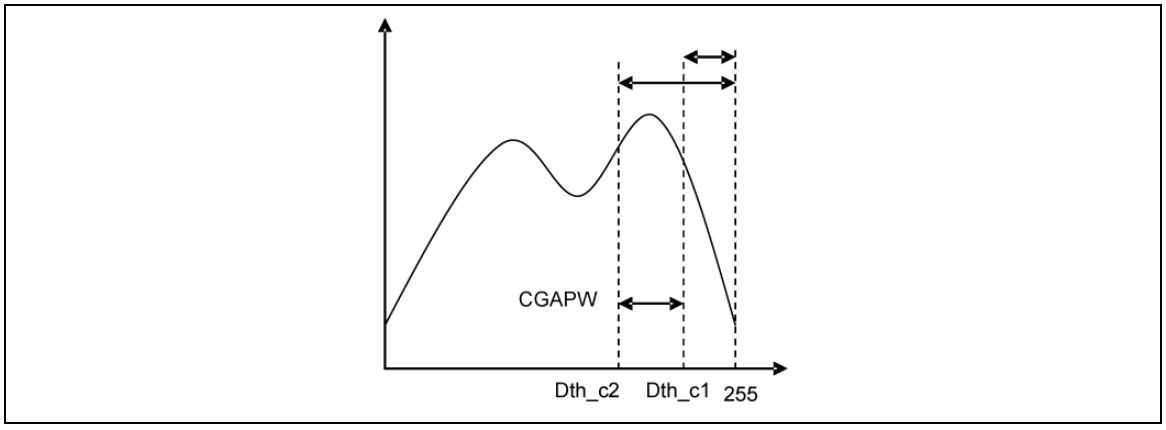


Figure 45

(4) ULMTW[7:0], LLMTW[7:0]

The possible range of the threshold grayscale value (Dth) that makes display image white is set in units of one grayscale. ULMTW and LLMTW set the maximum grayscale and the minimum grayscale, respectively. Dth can be changed within the range set by ULMTW and LLMTW.

When there is no effect on power saving due to a large number of pixels displaying white color, that is, in cases such as GUI, the R61523 can save power consumption by setting ULMTW lower than the maximum grayscale if saving power consumption precedes the display quality.

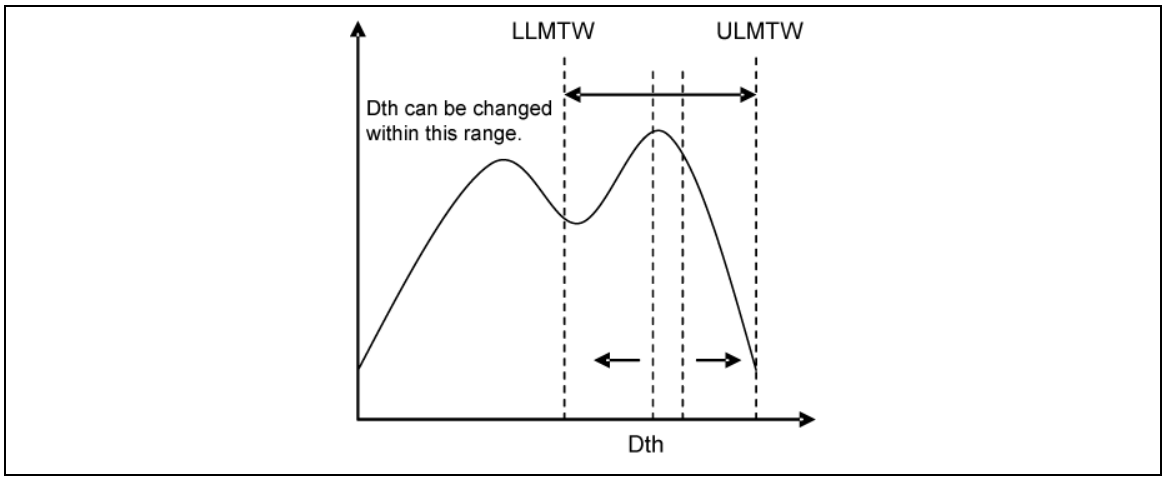


Figure 46

(5) TBL_*[7:0]

The reference values used for interpolation calculation in the gamma conversion table are set by 8-bit TBL_*[7:0]. Interpolation is performed as follows: First, four grayscale values are specified by TBL_*[7:0]. Then, the output data corresponding to the input data to 31 grayscale values specified at even interval between the adjacent two grayscale values of the four grayscale values specified by TBL_*[7:0] is calculated by linear interpolation.

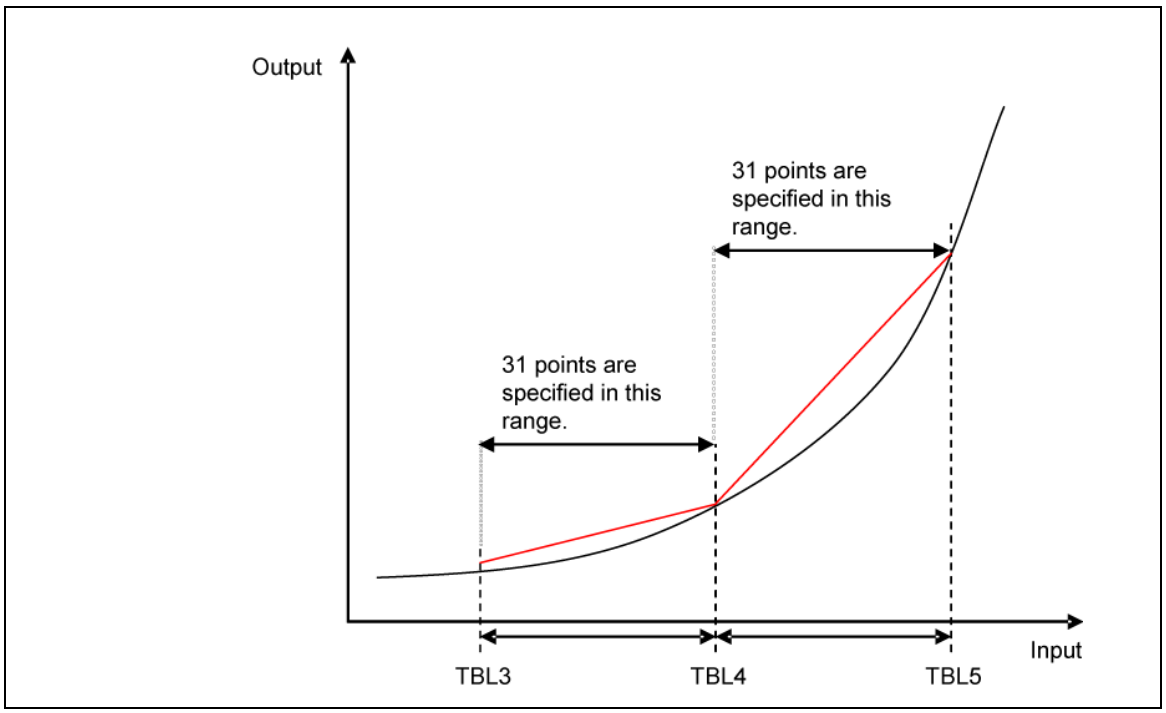


Figure 47

The table setting value is calculated by the following formula according to panel gamma value.

Table setting value = 255 x (table input grayscale / 255) ^ gamma

As the input table grayscale, the above calculation formula is applied to the five grayscale values (grayscales 127, 159, 191, 223, and 255) to calculate the table values. The table value is set as TBL*. The following table is applied to the case that gamma is set to 2.2.

Table 93

Register	TBL3	TBL4	TBL5	TBL6
Table input grayscale	127	159	191	223
Table setting value	55	90	135	190

(6) COEFK[4:0]

This register sets the range of the grayscale that prevents display image from turning white, according to the ratio of the grayscale stated here to the grayscale number that makes data white. The ratio can be set from 0% to 100%. The first grayscale (S) that starts grayscale interpolation to prevent display image from turning white is calculated by this register and Dth. Then, the number of grayscales between this grayscale (S) and the maximum grayscale is calculated by interpolation function, and it is used as image processing pixel value.

The larger COEFK[4:0] setting value increases the number of grayscales available in interpolation and relatively decreases the contrast between interpolation sections. As a result, the gamma value changes, and then, the brightness decreases. Also, the color of the section changes. In interpolation factor, there is a trade-off between contrast between interpolation section and the interpolation that the gamma value changes.

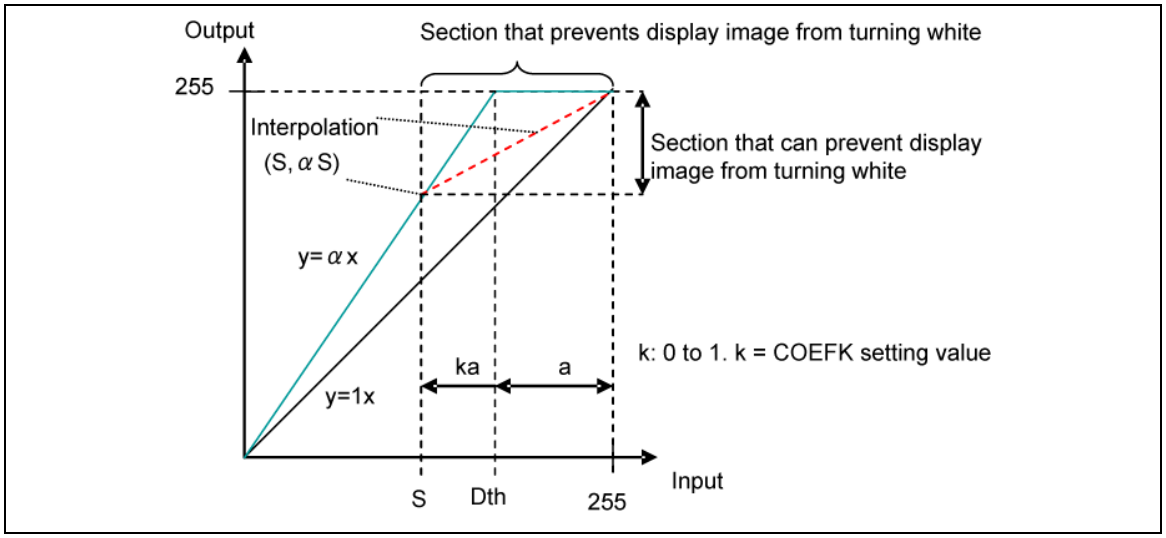


Figure 48

PWM Signal Setting

The PWM signal is output from the LEDPWM pin according to BDCV[7:0] bit settings and brightness information (8 bits) that is output from BLC control circuit.

PWM output specification (When LEDPWMPOL = 0)

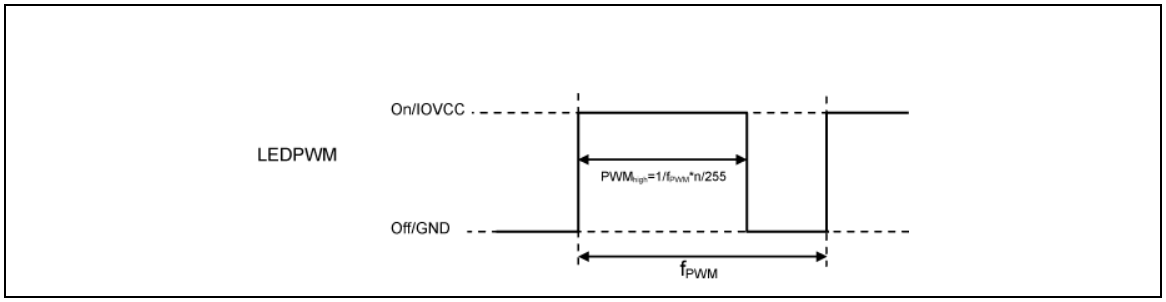


Figure 49

Table 94

PWMDIV[7:0]	LEDPWM frequency (f_{PWM})
8'h00	33.3KHz
8'h01	27.4KHz
8'h02	18.3KHz
8'h03	13.7KHz
8'h07	6.86 KHz
8'h0F	3.43 KHz
8'h1F	1.72 KHz
8'h3F	0.86 KHz
8'h7F	0.43 KHz
8'hFF	0.21 KHz

Table 95

Dimming data	$Duty_{PWM}$
8'h00	0(fixed Low)
8'h01	1/255
8'h02	2/255
8'h03	3/255
: :	: :
8'h0D	253/255
8'h0E	254/255
8'hFF	1(fixed High)

Note: These are typical values. The maximum variance is ±7%.

Scan Mode Setting

The relationship among driver arrangement, GS, SM, SS and BGR register settings and the Frame Memory Address

(1) Left/Right interchanging scan (SM=0): When the bits are written with their default values, the start address is left top (00, 000) and the scan direction is from top to bottom.

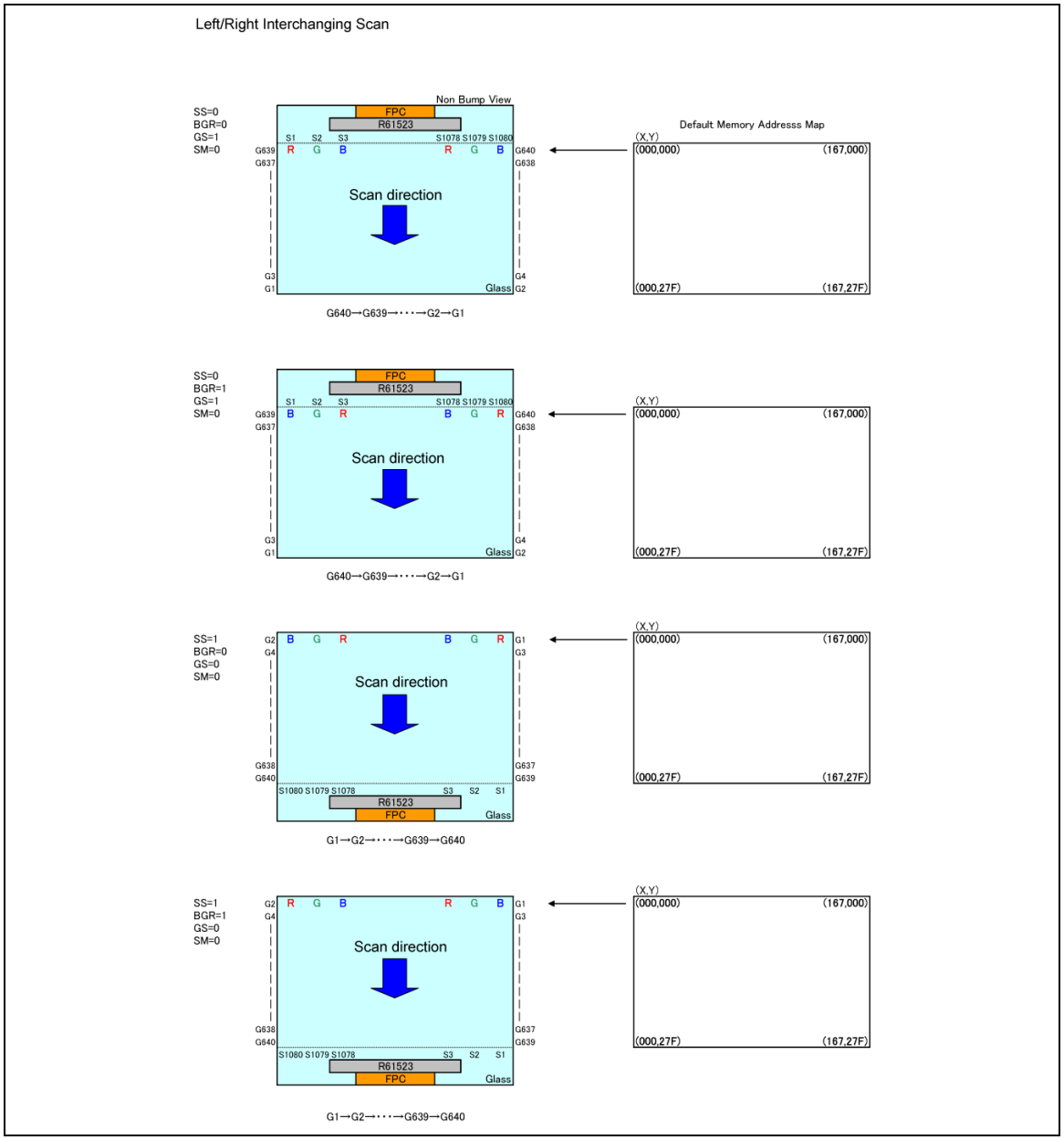


Figure 50 SM=0

(2) Left/Right one-side scan (SM=1): When the bits are written with their default values, the start address is left top (00, 000) and the scan direction is from top to bottom.

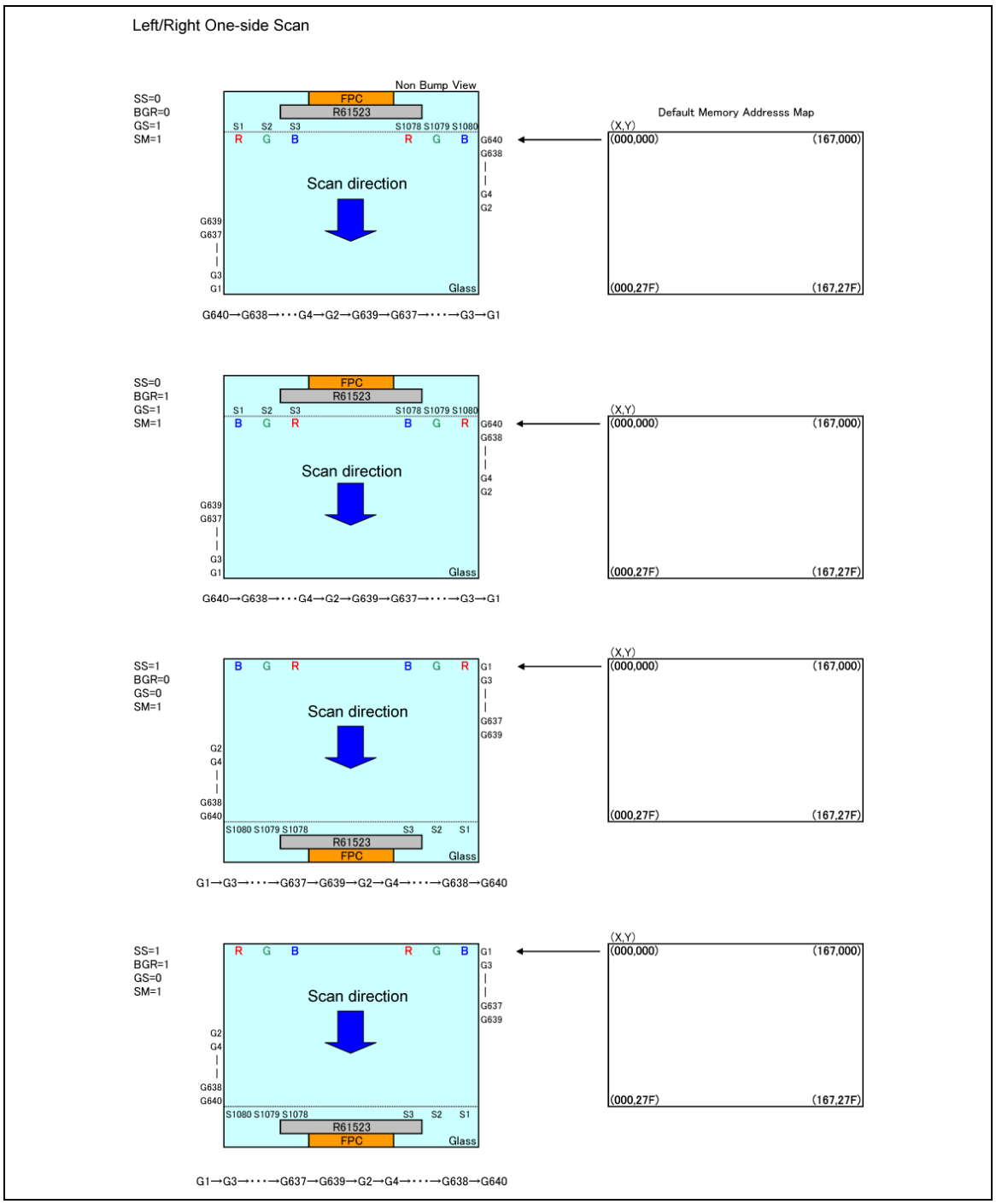


Figure 51 SM=1

Frame Frequency Adjustment Function

The R61523 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting Display Timing Setting (RTN bits) without changing the oscillation frequency.

It is possible to set a low frame frequency for saving power consumption when displaying a still picture and set a high frame frequency when displaying video image.

Also, the R61523 has frame-frequency adjustment parameters which can set frame frequency according to display modes (Normal, partial and Idle modes).

Relationship between the Liquid Crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated by the following equation. The frame frequency can be changed by setting the number of clocks per line period (RTN).

Equation for calculating frame frequency

$$FrameFrequency[f_{FLM}] = \frac{fosc}{NumberofClocks/line \times (NL + FP + BP)}[Hz]$$

fosc: Internal operation clock frequency (1000kHz)
Number of clocks per line: RTN
Line: Number of lines to drive the LCD: NL
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when Maximum Frame Frequency = 60 Hz

fosc: 1000 kHz
Number of lines: 640 lines
1H period: 25 clock cycles (RTN = 6'h19)
Front porch: 4 lines
Back porch: 4 lines

$$\therefore f_{FLM} = \frac{1000kHz}{25clocks \times (640 + 4 + 4)} \approx 60Hz$$

Line Inversion AC Drive

The R61523, in addition to frame-inversion liquid crystal alternating current drive, supports line-inversion alternating current drive.

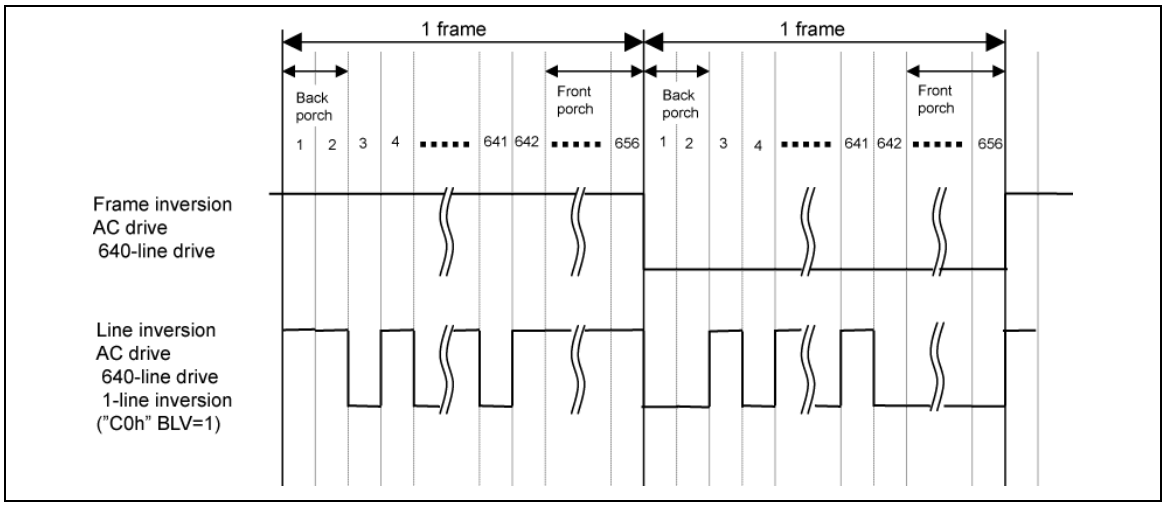


Figure 52

Alternating Timing

The following figure illustrates the liquid-crystal polarity inversion timing of different LCD driving methods.

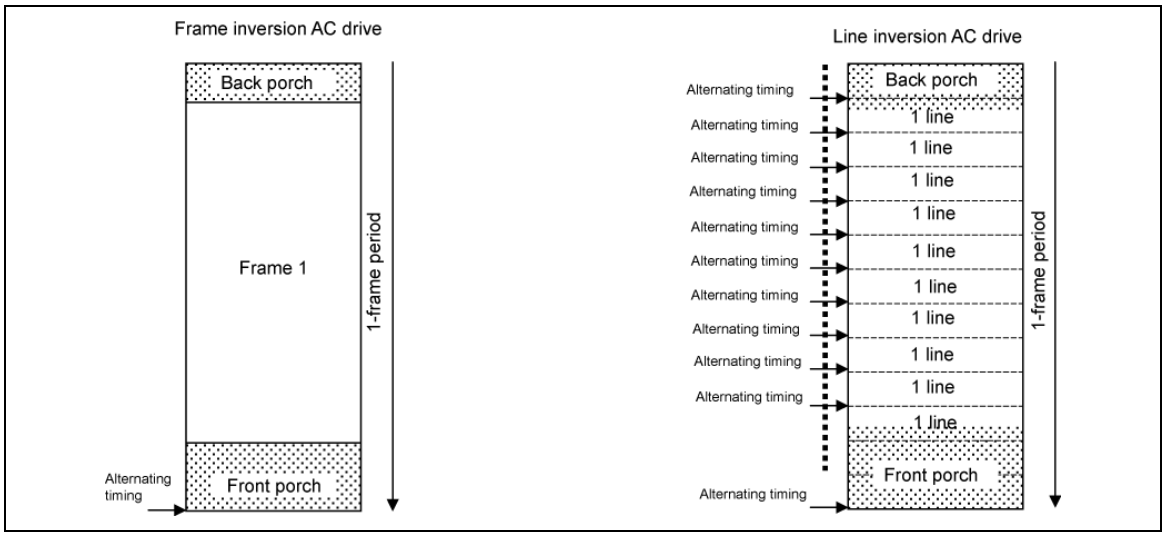


Figure 53

TE Pin Output Signal

Tearing Effect Line signals can be output from TE pin as frame memory data transfer synchronous signals. The signals are the trigger for frame memory write operation to enable data transfer in sync with the scanning operation. They are turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

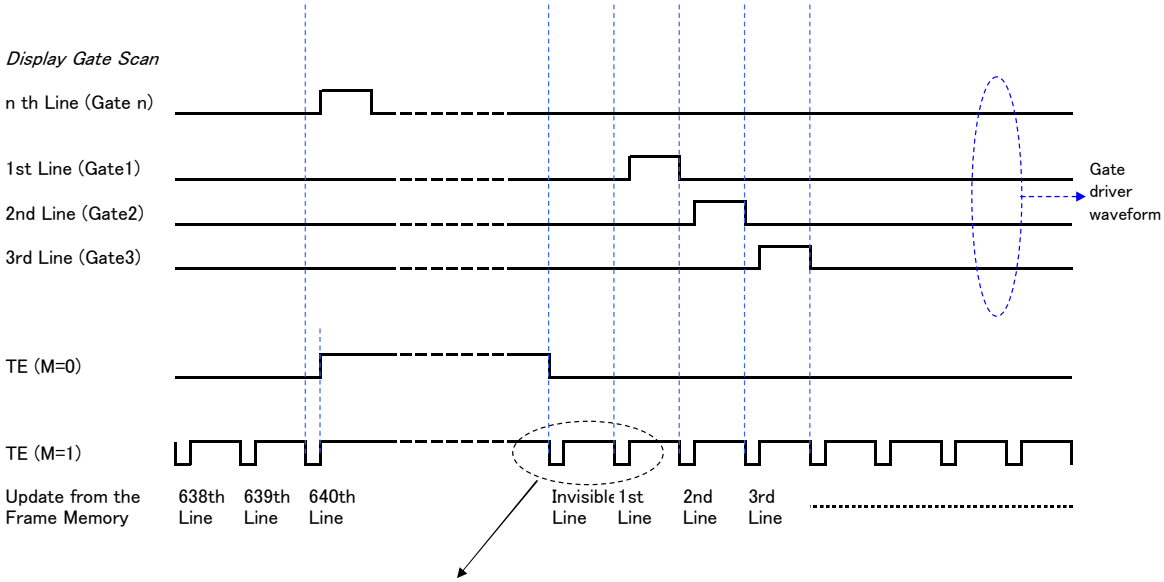
Table 96

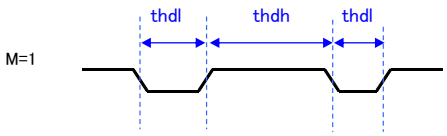
TEON (represents status of 35h command)	TELOM (35h1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode1)
1	1	TE (Mode2)

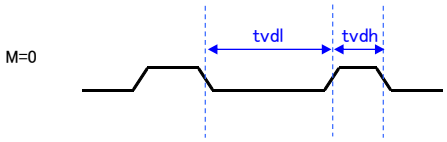
Tearing Effect signal mode is defined by TELOM, D0 parameter of set_tear_on (35h).

Write TELOM=0 when using DSI TE report function.

35h set_tear_on command







Definition

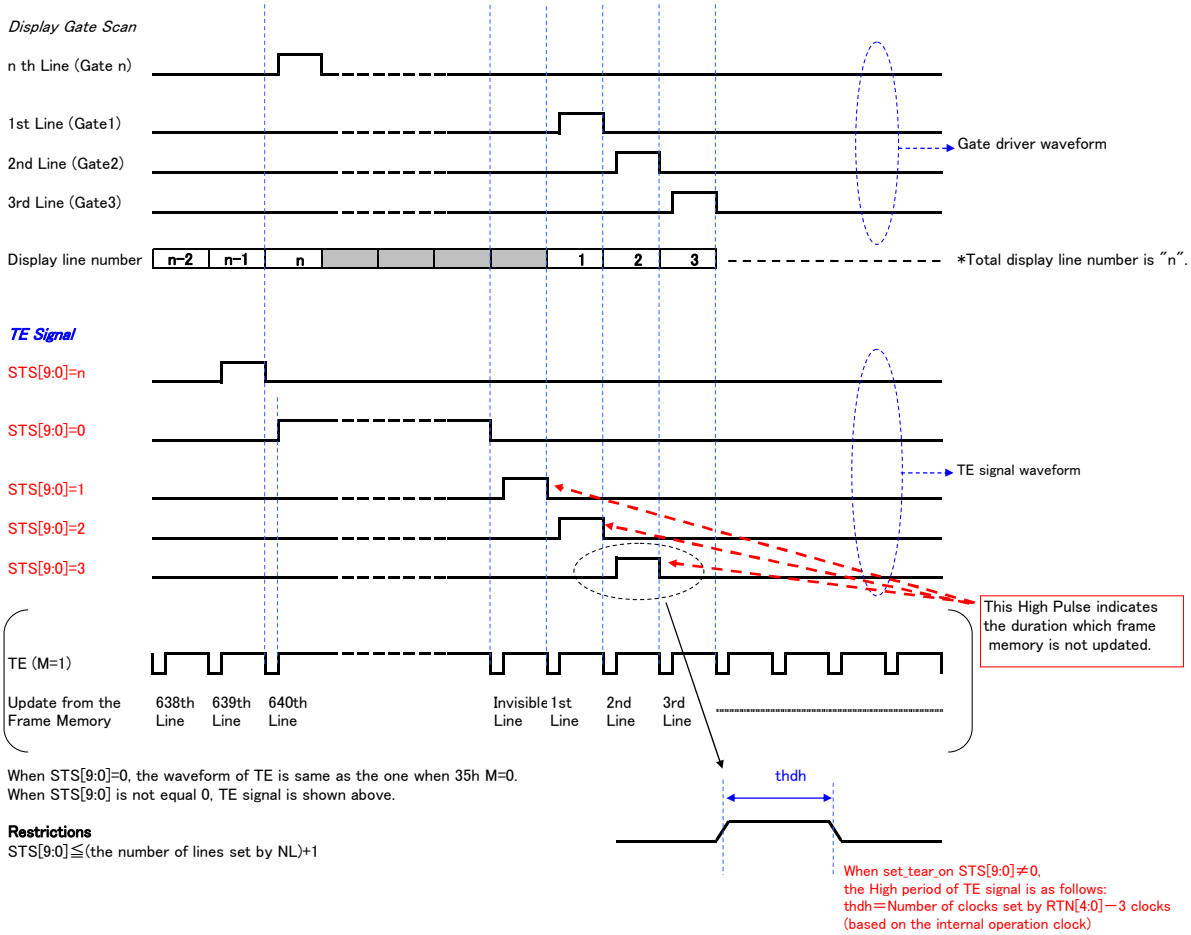
thdh : The LCD Display is not updated from the Frame Memory.
thdl : The LCD Display is updated from the Frame Memory.

tvdh : The LCD Display is not updated from the Frame Memory.
tvdl : The LCD Display is updated from the Frame Memory.

Note) TE wavaform depends on the SDT register setting.

44h set tear scanline command

STS[9:0] Setting (0～n)



When STS[9:0]=0, the waveform of TE is same as the one when 35h M=0.
When STS[9:0] is not equal 0, TE signal is shown above.

Restrictions
STS[9:0]≦(the number of lines set by NL)+1

Liquid Crystal Panel Interface Timing

Liquid Crystal Panel Interface Timing in Internal Clock Operation

The following figure shows the timing of DPI and liquid crystal panel interface signals in DPI operation.

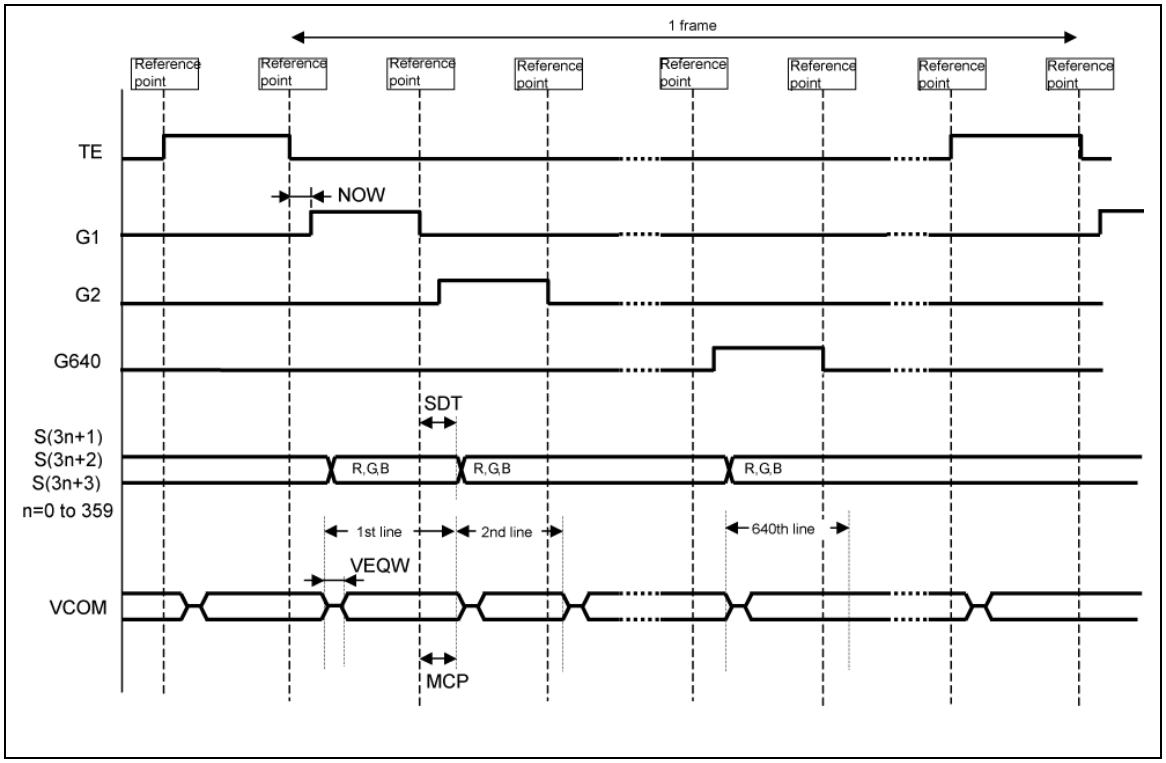


Figure 54

VCOM and source output alternating positions can be defined separately.

Notes 1. The TE waveform has values M=0, set_tear_scanline STS[9:0]=1.
2. The VCOM waveform has values BCn=1, BLV=1.

Setting range
MCP[2:0]: 1 to 7clks
SDT[2:0]: 1 to 7clks
NOW[2:0]: 1 to 7clks
Units: 1clk

State Transition Diagram

Definitions of Display modes

The state transition diagram of the R61523 is compliant with MIPI DCS.

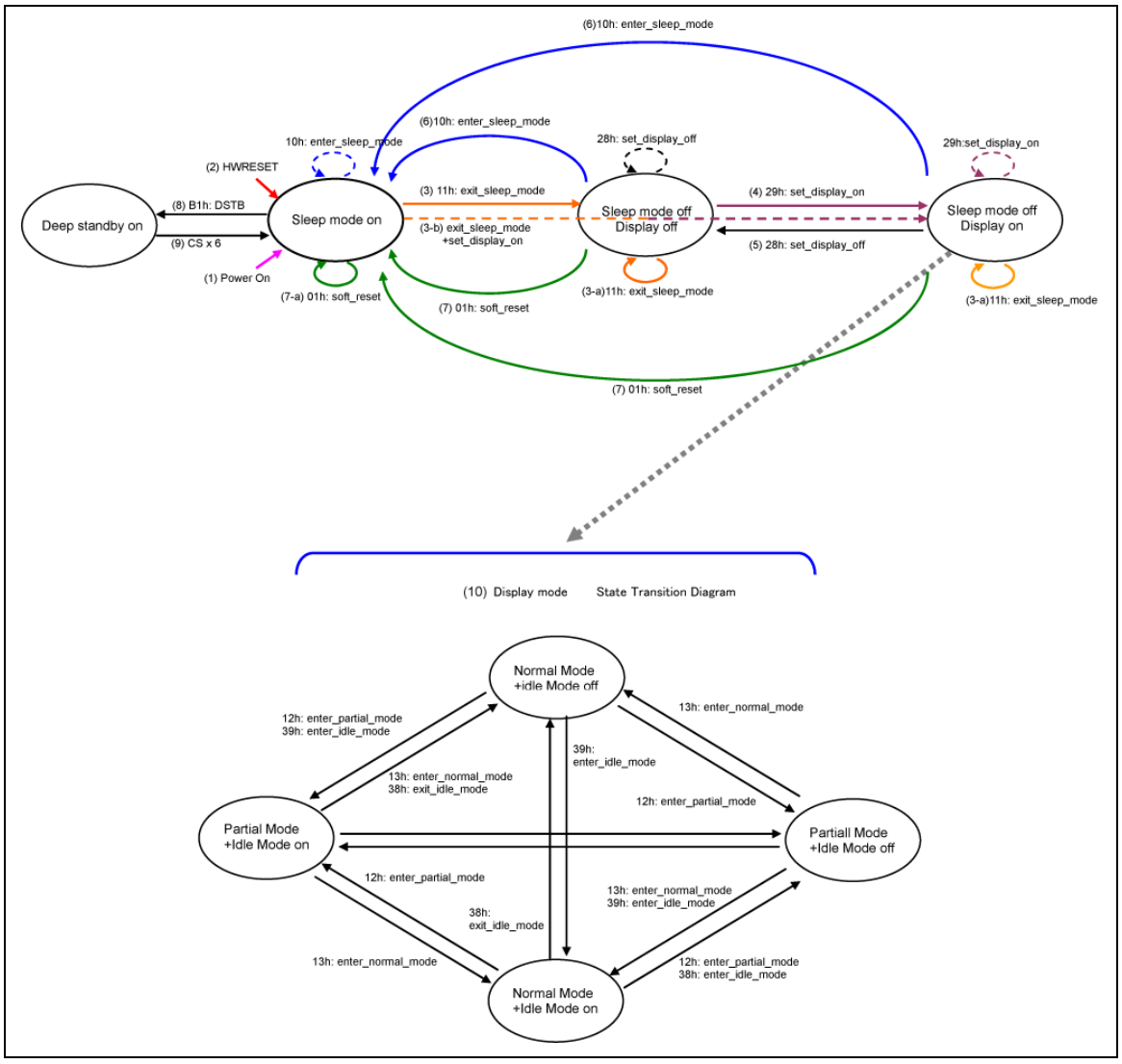


Figure 55

Notes 1: When the status of the LSI changes, designated sequences are performed. For details, see descriptions for each sequence.

2: Do not execute state transitions other than those illustrated above.

Table 97 Transition Sequences of Operation Modes

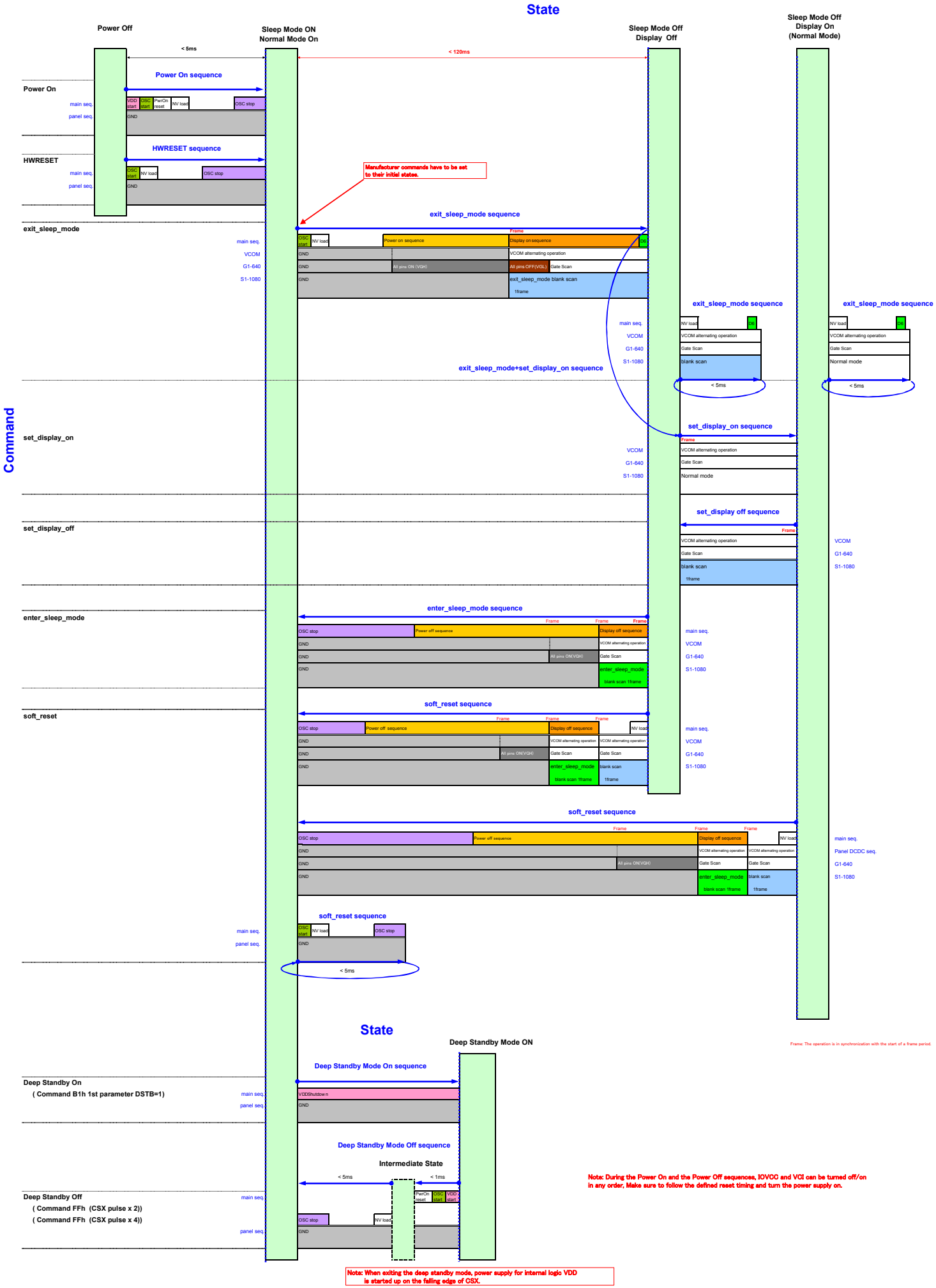
Sequence		Command	State	
			From	To
(1)	Power On sequence	-	-	Sleep mode on
(2)	HWRESET sequence	-	-	Sleep mode on
(3)	exit_sleep_mode sequence	11h:exit_sleep_mode	Sleep mode on	Sleep out Display off
(3-a)			Sleep mode off Display off/on	Sleep mode off Display off/on
(3-b)	exit_sleep_mode+ display_on sequence	11h:exit_sleep_mode	Sleep mode on	Sleep mode off Display on
(4)	set_display_on sequence	29h:set_display_on	Sleep mode off Display off	Sleep mode off Display on
(5)	set_display_off sequence	28h:set_display_off	Sleep mode off Display on	Sleep mode off Display off
(6)	enter_sleep_mode sequence	10h:enter_sleep_mode	Sleep mode off Display off/on	Sleep mode on
(7)	soft_reset sequence	01h:soft_reset	Sleep out Display off/on	Sleep mode on
(7-a)			Sleep mode on	Sleep mode on
(8)	Deep standby mode on sequence	B1h: DSTB	Sleep mode on	Deep standby on
(9)	Deep standby mode off sequence	CSX x 6	Deep standby on	Sleep mode on

Table 98 Transition Sequences of Display Modes

Sequence		Command	State	
			From	To
(10)	Display mode sequence	12h:enter_partial_mode 13h:enter_normal_mode 39h:enter_idle_mode 38h:exit_idle_mode	previous Display mode (Normal/Partial/Idle)	target Display mode (Normal/Partial/Idle)

■ R61523 State & Command sequence

Rev0.1



Example of Power and Display ON/OFF Sequence

The following figure illustrates the Power and Display ON sequence.

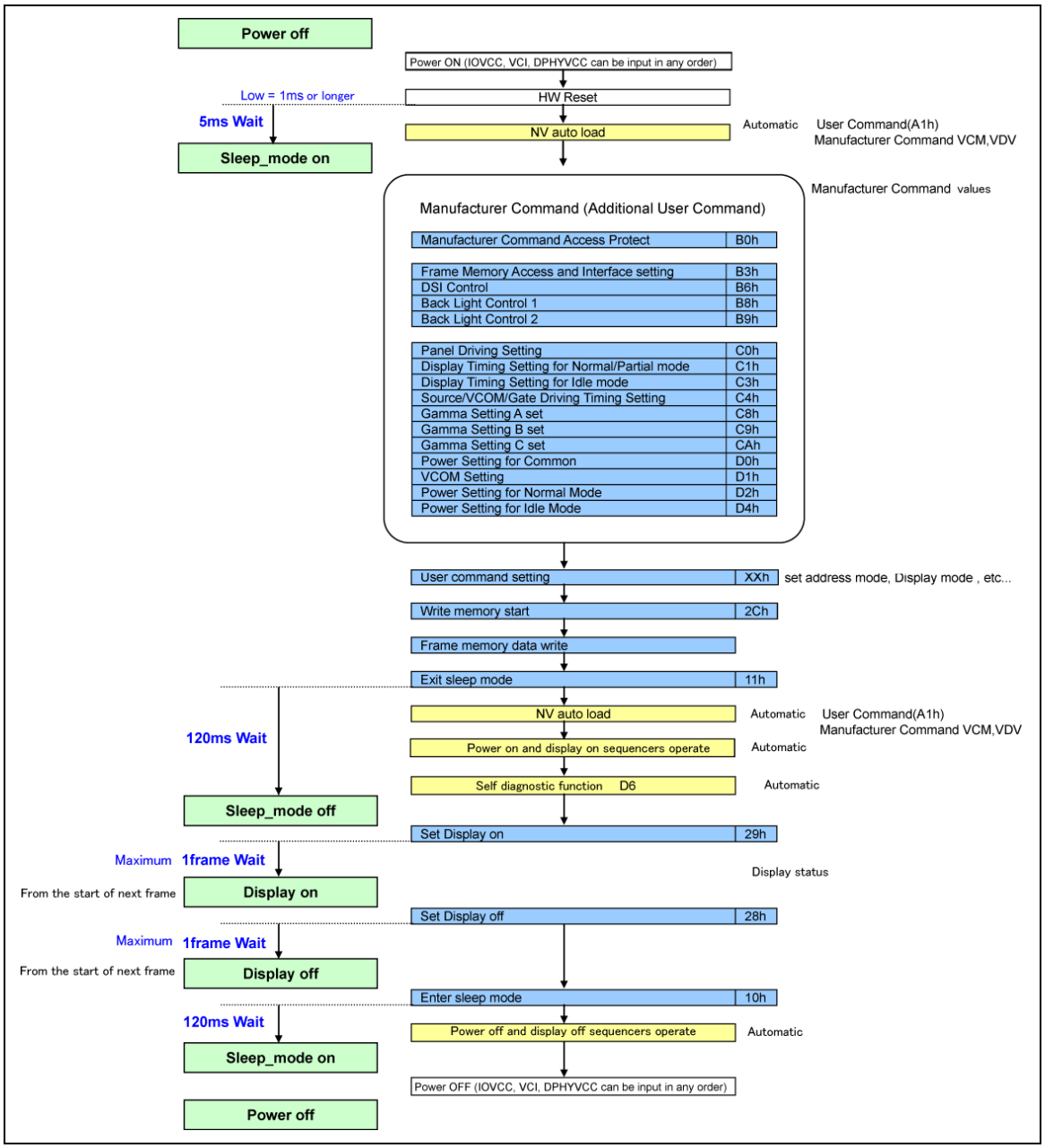


Figure 56

Command	Type	Value	Comment	Restriction
Manufacturer Command Access Protect	C	B0h		
	P1	XXh	User Setting	
Low Power Mode Control	C	B1h		
	P1	XXh	User Setting	
Frame Memory Access and Interface setting	C	B3h		
	P1	XXh	Manufacturer Setting	D7 must be "1"
	P2	XXh		
Read Checksum and ECC Error Count	C	B5h	Read Only	
	P1	–		
	P2	–		
	P3	–		
DSI Control	C	B6h		
	P1	XXh	Manufacturer Setting	
Back Light Control 1	C	B8h		
	P1	XXh	User Setting	
	P2	XXh	Manufacturer Setting	
	P3	XXh		
	P4	XXh		
	P5	XXh		
	P6	XXh		
	P7	XXh		
	P8	XXh		
	P9	XXh		
	P10	XXh		
	P11	XXh		
	P12	XXh		
	P13	XXh		
	P14	XXh		
	P15	XXh		
Back Light Control 2	C	B9h		
	P1	XXh	User Setting	
	P2	XXh		
	P3	XXh	Manufacturer Setting	
	P4	XXh		
Back Light Control 3	C	BAh	Read Only	
	P1	–		
Device Code Read	C	BFh	Read Only	
	P1	–		
	P2	–		
	P3	–		
	P4	–		
Panel Driving Setting	C	C0h		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		
	P4	XXh		
	P5	XXh		
	P6	XXh		
	P7	XXh		
Display Timing Setting for Normal/Partial Mode	C	C1h		
	P1	XXh	Manufacturer Setting	
	P2	00h	Test Mode	D7-0 must be 8'h00
	P3	XXh	Manufacturer Setting	
	P4	XXh		
	P5	XXh		
Display Timing Setting for Idle Mode	C	C3h		
	P1	XXh	Manufacturer Setting	
	P2	00h	Test Mode	D7-0 must be 8'h00
	P3	XXh	Manufacturer Setting	
	P4	XXh		
	P5	XXh		
Source/VCOM/Gate Driving Timing Setting	C	C4h		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		
	P4	XXh		
	P5	XXh		
Gamma Setting A set	C	C8h		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		
	P4	XXh		
	P5	XXh		
	P6	XXh		
	P7	XXh		
	P8	XXh		
	P9	XXh		
	P10	XXh		
	P11	XXh		
	P12	XXh		
	P13	XXh		
	P14	XXh		
	P15	XXh		
	P16	XXh		
	P17	XXh		
	P18	XXh		
Gamma Setting B set	C	C9h		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		
	P4	XXh		
	P5	XXh		
	P6	XXh		
	P7	XXh		
	P8	XXh		
	P9	XXh		
	P10	XXh		
	P11	XXh		
	P12	XXh		
	P13	XXh		
	P14	XXh		
	P15	XXh		
	P16	XXh		
	P17	XXh		
	P18	XXh		
Gamma Setting C set	C	CAh		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		
	P4	XXh		
	P5	XXh		
	P6	XXh		
	P7	XXh		
	P8	XXh		
	P9	XXh		
	P10	XXh		
	P11	XXh		
	P12	XXh		
	P13	XXh		
	P14	XXh		
	P15	XXh		
	P16	XXh		
	P17	XXh		
	P18	XXh		

Command	Type	Value	Comment	Restriction
Power Setting for Common	C	D0h		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		D7,D6 must be "1"
	P4	XXh		D7 must be "1"
	P5	01h	Test Mode	D7-0 must be 8'h01
	P6	00h		D7-0 must be 8'h00
	P7	00h		D7-0 must be 8'h00
	P8	00h		D7-0 must be 8'h00
	P9	07h		D7-0 must be 8'h07
	P10	00h		D7-0 must be 8'h00
VCOM Setting	C	D1h		
	P1	XXh	Manufacturer Setting	
	P2	00h	Test Mode	
	P3	XXh	Manufacturer Setting	D7 must be "1"
	P4	XXh		D7,D6,D5 must be "1"
Power Setting for Normal/Partial Mode	C	D2h		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		
Power Setting for Idle Mode	C	D4h		
	P1	XXh	Manufacturer Setting	
	P2	XXh		
	P3	XXh		
Test Mode	C	D6h		
	P1	01h		Fixed by MCAP=011
	P2	30h		Fixed by MCAP=011
	P3	02h		Fixed by MCAP=011
	P4	16h		Fixed by MCAP=011
Test Mode	C	D7h		
	P1	06h		Fixed by MCAP=011
	P2	16h		Fixed by MCAP=011
	P3	88h		Fixed by MCAP=011
	P4	00h		Fixed by MCAP=011
	P5	66h		Fixed by MCAP=011
	P6	AAh		Fixed by MCAP=011
	P7	0Ah		Fixed by MCAP=011
	P8	88h		Fixed by MCAP=011
	P9	80h		Fixed by MCAP=011
	P10	CAh		Fixed by MCAP=011
	P11	0Ah		Fixed by MCAP=011
	P12	0Ch		Fixed by MCAP=011
Test Mode	C	D9h		
	P1	FFh		Fixed by MCAP=011
	P2	9Fh		Fixed by MCAP=011
NV Memory Access Control	C	E0h		
	P1	XXh	Manufacturer Setting	Fixed by MCAP=011
	P2	XXh		Fixed by MCAP=011, D4,D3 must be "1"
	P3	XXh		Fixed by MCAP=011
	P4	07h	Test Mode	Fixed by MCAP=011, D7-0 must be 8'h00
set_DDB write control	C	E1h		
	P1	XXh	Manufacturer Setting	Fixed by MCAP=011
Test Mode	C	E2h		
	P1	00h		
Test Mode	C	E3h		
	P1	00h		
	P2	00h		
	P3	FFh		
	P4	FFh		
	P5	FFh		
	P6	FFh		
	P7	FFh		
	P8	FFh		
	P9	FFh		
	P10	FFh		
	P11	FFh		
	P12	FFh		
Test Mode	C	E4h		
	P1	00h		Fixed by MCAP=011
	P2	00h		Fixed by MCAP=011
	P3	AAh		Fixed by MCAP=011
	P4	AAh		Fixed by MCAP=011
	P5	00h		Fixed by MCAP=011
Test Mode	C	E5h		
	P1	00h		Fixed by MCAP=011
Test Mode	C	E6h		
	P1	00h		
Test Mode	C	F3h		
	P1	00h		Fixed by MCAP=011
	P2	20h		Fixed by MCAP=011
Test Mode	C	FAh		
	P1	01h		Fixed by MCAP=011
	P2	00h		Fixed by MCAP=011
	P3	00h		Fixed by MCAP=011
	P4	00h		Fixed by MCAP=011
Test Mode	C	FCh		
	P1	00h		Fixed by MCAP=011
	P2	00h		Fixed by MCAP=011
	P3	00h		Fixed by MCAP=011
	P4	00h		Fixed by MCAP=011
	P5	00h		Fixed by MCAP=011
Test Mode	C	FDh		
	P1	00h		Fixed by MCAP=011
	P2	00h		Fixed by MCAP=011
	P3	01h		Fixed by MCAP=011
	P4	00h		Fixed by MCAP=011
	P5	00h		Fixed by MCAP=011
Test Mode	C	FEh		
	P1	00h		Fixed by MCAP=011
	P2	00h		Fixed by MCAP=011
	P3	00h		Fixed by MCAP=011
	P4	00h		Fixed by MCAP=011
	P5	30h		Fixed by MCAP=011

Deep Standby Mode ON/OFF Sequence

1) Enter Deep Standby Mode Sequence

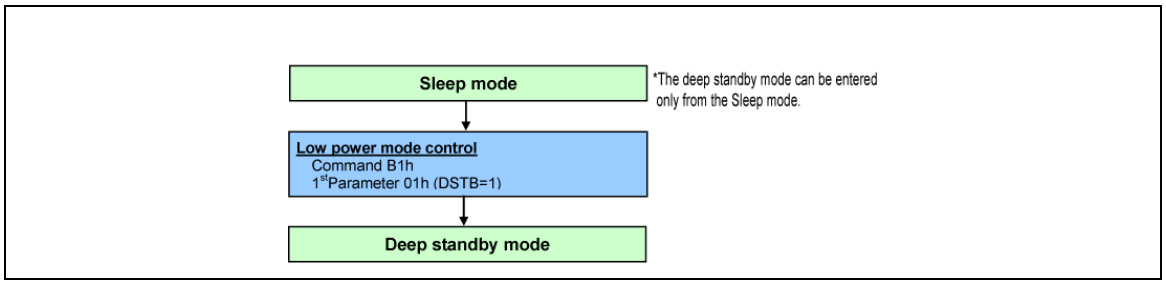


Figure 57

2) Exit Deep Standby Mode Sequence

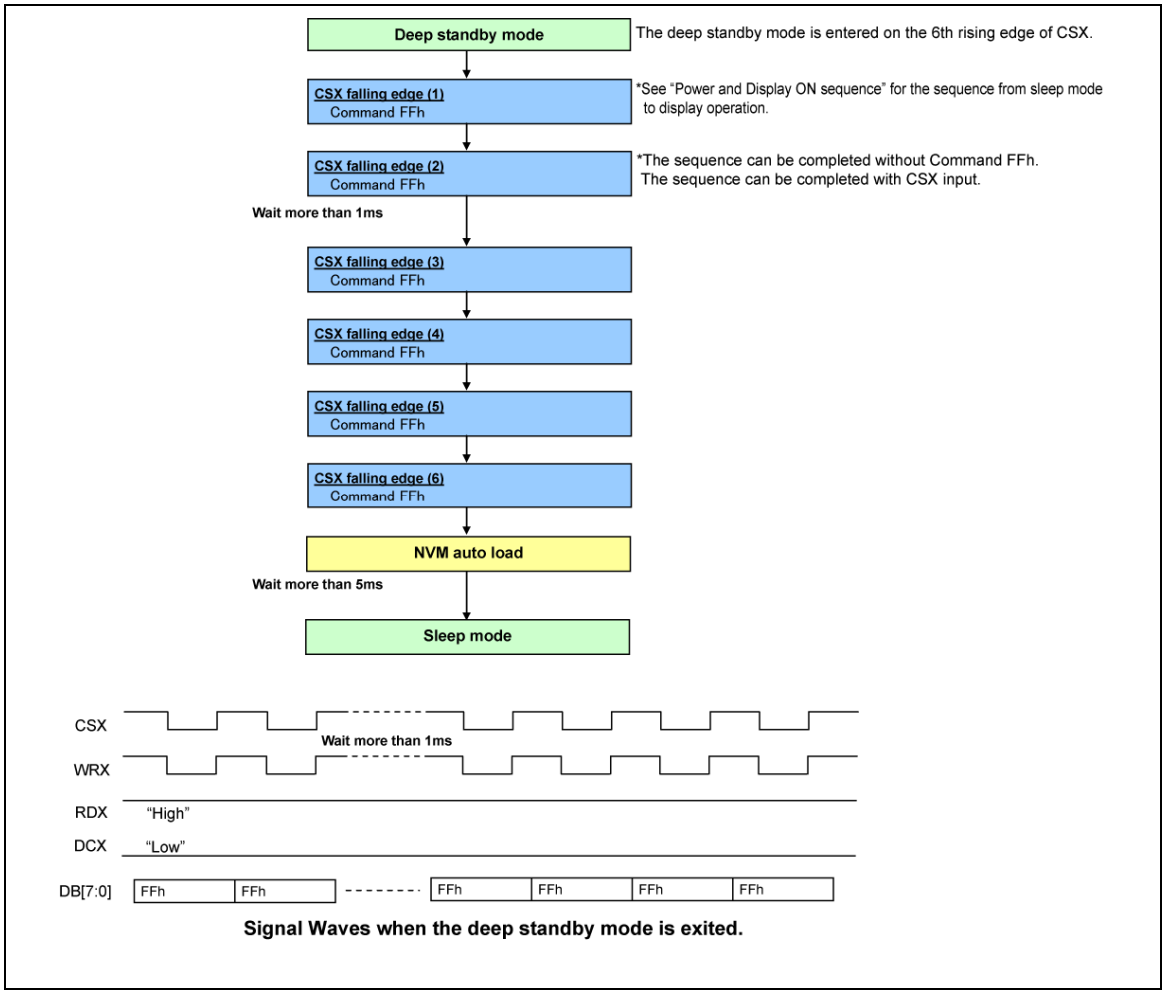


Figure 58

γ Correction Function

γ Correction Function

The R61523 supports γ correction function to make optimal colors according to the characteristics of the LCD panel. The R61523 has registers for positive and negative polarities to allow different settings for R, G, and B dots.

γ Correction Circuit

The following figure shows the γ correction circuit. The voltage between VREG and VGS is divided into 10 grayscale voltages by the first ladder resistor, and the reference voltages (V0 and V255) are specified by selectors. The voltage between V0 and V255 is divided into 10 grayscale voltages by the second ladder resistor, and the grayscale reference voltages (V4, V8, V15, V32, V80, V172, V220, V240, V247, and V251) are specified. The other grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltages, see "Grayscale Voltage Calculation Formula."

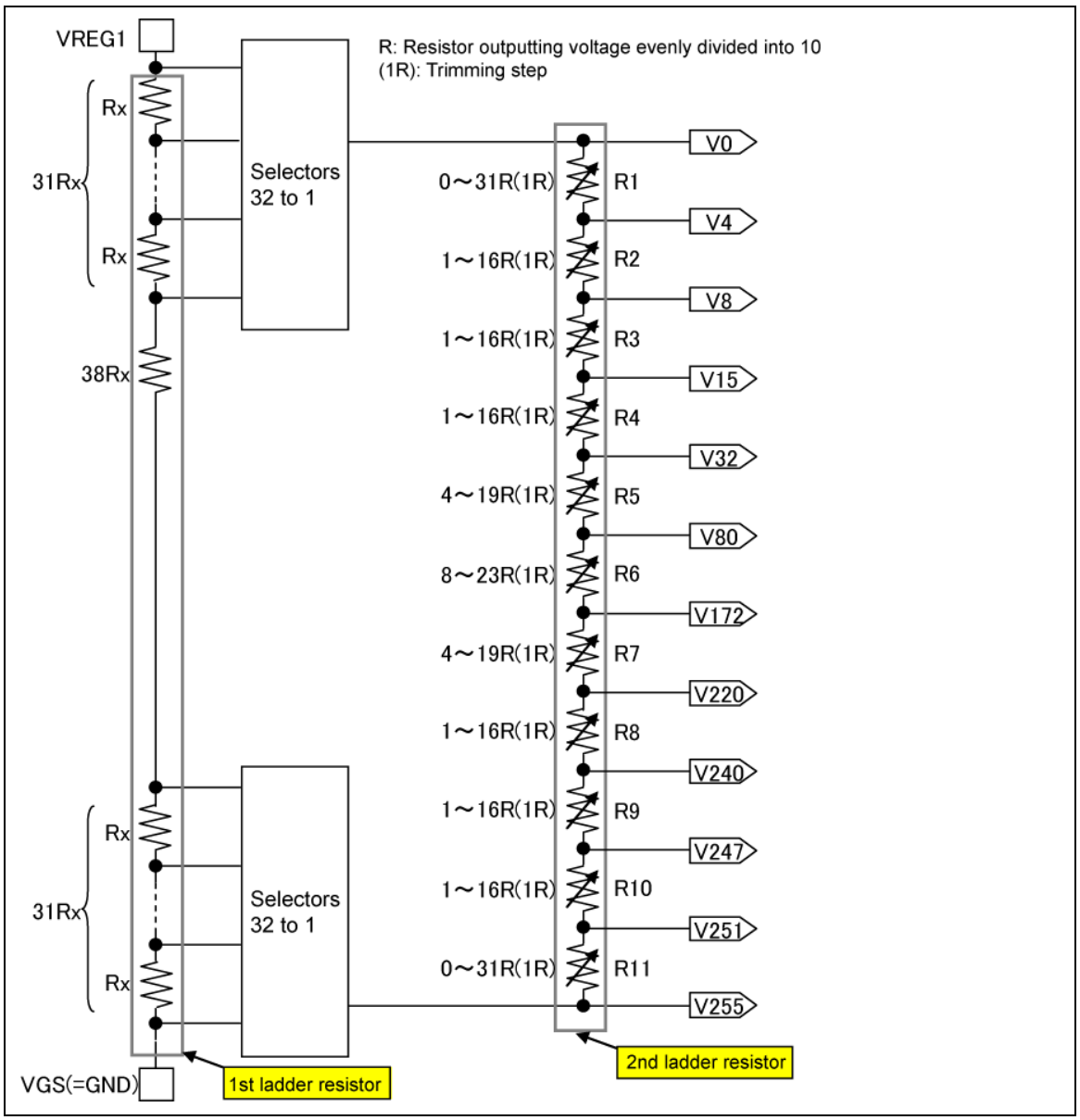


Figure 59

γ Correction Registers

The γ correction registers include 56-bit reference level adjustment registers per R, G, and B dots (positive polarity and negative polarity).

Reference level Adjustment Registers

Table 99 Reference Level Adjustment Registers

Resistor	Gamma Set A		Gamma Set B		Gamma Set C	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity	Positive polarity	Negative polarity
-	PR0P_R[4:0]	PR0N_R[4:0]	PR0P_G[4:0]	PR0N_G[4:0]	PR0P_B[4:0]	PR0N_B[4:0]
R1	PR1P_R[4:0]	PR1N_R[4:0]	PR1P_G[4:0]	PR1N_G[4:0]	PR1P_B[4:0]	PR1N_B[4:0]
R2	PR2P_R[3:0]	PR2N_R[3:0]	PR2P_G[3:0]	PR2N_G[3:0]	PR2P_B[3:0]	PR2N_B[3:0]
R3	PR3P_R[3:0]	PR3N_R[3:0]	PR3P_G[3:0]	PR3N_G[3:0]	PR3P_B[3:0]	PR3N_B[3:0]
R4	PR4P_R[3:0]	PR4N_R[3:0]	PR4P_G[3:0]	PR4N_G[3:0]	PR4P_B[3:0]	PR4N_B[3:0]
R5	PR5P_R[3:0]	PR5N_R[3:0]	PR5P_G[3:0]	PR5N_G[3:0]	PR5P_B[3:0]	PR5N_B[3:0]
R6	PR6P_R[3:0]	PR6N_R[3:0]	PR6P_G[3:0]	PR6N_G[3:0]	PR6P_B[3:0]	PR6N_B[3:0]
R7	PR7P_R[3:0]	PR7N_R[3:0]	PR7P_G[3:0]	PR7N_G[3:0]	PR7P_B[3:0]	PR7N_B[3:0]
R8	PR8P_R[3:0]	PR8N_R[3:0]	PR8P_G[3:0]	PR8N_G[3:0]	PR8P_B[3:0]	PR8N_B[3:0]
R9	PR9P_R[3:0]	PR9N_R[3:0]	PR9P_G[3:0]	PR9N_G[3:0]	PR9P_B[3:0]	PR9N_B[3:0]
R10	PR10P_R[3:0]	PR10N_R[3:0]	PR10P_G[3:0]	PR10N_G[3:0]	PR10P_B[3:0]	PR10N_B[3:0]
R11	PR11P_R[4:0]	PR11N_R[4:0]	PR11P_G[4:0]	PR11N_G[4:0]	PR11P_B[4:0]	PR11N_B[4:0]
-	PR12P_R[4:0]	PR12N_R[4:0]	PR12P_G[4:0]	PR12N_G[4:0]	PR12P_B[4:0]	PR12N_B[4:0]

Table 100 Reference Level (V4, V8, V15, V32, V80, V172, V220, V240, V247, and V251) Adjustment Registers and Resistors

Resistor	Register		Resistance	Resistor	Register		Resistance
	Name	Value			Name	Value	
R1	PR1*_*[4:0]	5'h00	0R	R7	PR7*_*[3:0]	4'h0	4R
		5'h01	1R			4'h1	5R
		5'h02	2R			4'h2	6R
		⋮	⋮			⋮	⋮
		5'h1F	31R			4'hF	19R
R2	PR2*_*[3:0]	4'h0	1R	R8	PR8*_*[3:0]	4'h0	1R
		4'h1	2R			4'h1	2R
		4'h2	3R			4'h2	3R
		⋮	⋮			⋮	⋮
		4'hF	16R			4'hF	16R
R3	PR3*_*[3:0]	4'h0	1R	R9	PR9*_*[3:0]	4'h0	1R
		4'h1	2R			4'h1	2R
		4'h2	3R			4'h2	3R
		⋮	⋮			⋮	⋮
		4'hF	16R			4'hF	16R
R4	PR4*_*[3:0]	4'h0	1R	R10	PR10*_*[3:0]	4'h0	1R
		4'h1	2R			4'h1	2R
		4'h2	3R			4'h2	3R
		⋮	⋮			⋮	⋮
		4'hF	16R			4'hF	16R
R5	PR5*_*[3:0]	4'h0	4R	R11	PR11*_*[4:0]	5'h00	0R
		4'h1	5R			5'h01	1R
		4'h2	6R			5'h02	2R
		⋮	⋮			⋮	⋮
		4'hF	19R			5'h1F	31R
R6	PR6*_*[3:0]	4'h0	8R				
		4'h1	9R				
		4'h2	10R				
		⋮	⋮				
		4'hF	23R				

Note: *_* indicates P_R/N_R, P_G/N_G, or P_B/N_B.

Table 101 Reference Levels (V0 and V255) and Adjustment Resisters

Grayscale	Register		Level	Grayscale	Register		Level
	Name	Value			Name	Value	
V0	PR0*_*[4:0]	5'h00	VREG1 x 100%	V255	PR12*_*[4:0]	5'h00	VREG1 x 0%
		5'h01	VREG1 x 99%			5'h01	VREG1 x 1%
		5'h02	VREG1 x 98%			5'h02	VREG1 x 2%
		⋮	⋮			⋮	⋮
		5'h1F	VREG1 x 69%			5'h1F	VREG1 x 31%

Note: *_* indicates P_R/N_R, P_G/N_G, or P_B/N_B.

Grayscale Voltage Calculation Formulas

Table 102

Grayscale voltage	Calculation formula
V0	-
V1	V4 + (V0 – V4) x 3/4
V2	V4 + (V0 – V4) x 2/4
V3	V4 + (V0 – V4) x 1/4
V4	Δ V x ∑ (R2~R11)/SUMR+V255
V5	V8 + (V4 – V8) x 3/4
V6	V8 + (V4 – V8) x 2/4
V7	V8 + (V4 – V8) x 1/4
V8	Δ V x ∑ (R3~R11)/SUMR+V255
V9	V15 + (V8 – V15) x 6/7
V10	V15 + (V8 – V15) x 5/7
V11	V15 + (V8 – V15) x 4/7
V12	V15 + (V8 – V15) x 3/7
V13	V15 + (V8 – V15) x 2/7
V14	V15 + (V8 – V15) x 1/7
V15	Δ V x ∑ (R4~R11)/SUMR+V255
V16	V32 + (V15 – V32) x 16/17
V17	V32 + (V15 – V32) x 15/17
V18	V32 + (V15 – V32) x 14/17
V19	V32 + (V15 – V32) x 13/17
V20	V32 + (V15 – V32) x 12/17
V21	V32 + (V15 – V32) x 11/17
V22	V32 + (V15 – V32) x 10/17
V23	V32 + (V15 – V32) x 9/17
V24	V32 + (V15 – V32) x 8/17
V25	V32 + (V15 – V32) x 7/17
V26	V32 + (V15 – V32) x 6/17
V27	V32 + (V15 – V32) x 5/17
V28	V32 + (V15 – V32) x 4/17
V29	V32 + (V15 – V32) x 3/17
V30	V32 + (V15 – V32) x 2/17
V31	V32 + (V15 – V32) x 1/17

Grayscale voltage	Calculation formula
V32	Δ V x ∑ (R5~R11)/SUMR+V255
V33	V80 + (V32 – V80) x 47/48
V34	V80 + (V32 – V80) x 46/48
V35	V80 + (V32 – V80) x 45/48
V36	V80 + (V32 – V80) x 44/48
V37	V80 + (V32 – V80) x 43/48
V38	V80 + (V32 – V80) x 42/48
V39	V80 + (V32 – V80) x 41/48
V40	V80 + (V32 – V80) x 40/48
V41	V80 + (V32 – V80) x 39/48
V42	V80 + (V32 – V80) x 38/48
V43	V80 + (V32 – V80) x 37/48
V44	V80 + (V32 – V80) x 36/48
V45	V80 + (V32 – V80) x 35/48
V46	V80 + (V32 – V80) x 34/48
V47	V80 + (V32 – V80) x 33/48
V48	V80 + (V32 – V80) x 32/48
V49	V80 + (V32 – V80) x 31/48
V50	V80 + (V32 – V80) x 30/48
V51	V80 + (V32 – V80) x 29/48
V52	V80 + (V32 – V80) x 28/48
V53	V80 + (V32 – V80) x 27/48
V54	V80 + (V32 – V80) x 26/48
V55	V80 + (V32 – V80) x 25/48
V56	V80 + (V32 – V80) x 24/48
V57	V80 + (V32 – V80) x 23/48
V58	V80 + (V32 – V80) x 22/48
V59	V80 + (V32 – V80) x 21/48
V60	V80 + (V32 – V80) x 20/48
V61	V80 + (V32 – V80) x 19/48
V62	V80 + (V32 – V80) x 18/48
V63	V80 + (V32 – V80) x 17/48

Table 103

Grayscale voltage	Calculation formula	Grayscale voltage	Calculation formula
V64	V80 + (V32 – V80) x 16/48	V96	V172 + (V80 – V172) x 76/92
V65	V80 + (V32 – V80) x 15/48	V97	V172 + (V80 – V172) x 75/92
V66	V80 + (V32 – V80) x 14/48	V98	V172 + (V80 – V172) x 74/92
V67	V80 + (V32 – V80) x 13/48	V99	V172 + (V80 – V172) x 73/92
V68	V80 + (V32 – V80) x 12/48	V100	V172 + (V80 – V172) x 72/92
V69	V80 + (V32 – V80) x 11/48	V101	V172 + (V80 – V172) x 71/92
V70	V80 + (V32 – V80) x 10/48	V102	V172 + (V80 – V172) x 70/92
V71	V80 + (V32 – V80) x 9/48	V103	V172 + (V80 – V172) x 69/92
V72	V80 + (V32 – V80) x 8/48	V104	V172 + (V80 – V172) x 68/92
V73	V80 + (V32 – V80) x 7/48	V105	V172 + (V80 – V172) x 67/92
V74	V80 + (V32 – V80) x 6/48	V106	V172 + (V80 – V172) x 66/92
V75	V80 + (V32 – V80) x 5/48	V107	V172 + (V80 – V172) x 65/92
V76	V80 + (V32 – V80) x 4/48	V108	V172 + (V80 – V172) x 64/92
V77	V80 + (V32 – V80) x 3/48	V109	V172 + (V80 – V172) x 63/92
V78	V80 + (V32 – V80) x 2/48	V110	V172 + (V80 – V172) x 62/92
V79	V80 + (V32 – V80) x 1/48	V111	V172 + (V80 – V172) x 61/92
V80	$\Delta V \times \sum$ (R6~R11)/SUMR+V255	V112	V172 + (V80 – V172) x 60/92
V81	V172 + (V80 – V172) x 91/92	V113	V172 + (V80 – V172) x 59/92
V82	V172 + (V80 – V172) x 90/92	V114	V172 + (V80 – V172) x 58/92
V83	V172 + (V80 – V172) x 89/92	V115	V172 + (V80 – V172) x 57/92
V84	V172 + (V80 – V172) x 88/92	V116	V172 + (V80 – V172) x 56/92
V85	V172 + (V80 – V172) x 87/92	V117	V172 + (V80 – V172) x 55/92
V86	V172 + (V80 – V172) x 86/92	V118	V172 + (V80 – V172) x 54/92
V87	V172 + (V80 – V172) x 85/92	V119	V172 + (V80 – V172) x 53/92
V88	V172 + (V80 – V172) x 84/92	V120	V172 + (V80 – V172) x 52/92
V89	V172 + (V80 – V172) x 83/92	V121	V172 + (V80 – V172) x 51/92
V90	V172 + (V80 – V172) x 82/92	V122	V172 + (V80 – V172) x 50/92
V91	V172 + (V80 – V172) x 81/92	V123	V172 + (V80 – V172) x 49/92
V92	V172 + (V80 – V172) x 80/92	V124	V172 + (V80 – V172) x 48/92
V93	V172 + (V80 – V172) x 79/92	V125	V172 + (V80 – V172) x 47/92
V94	V172 + (V80 – V172) x 78/92	V126	V172 + (V80 – V172) x 46/92
V95	V172 + (V80 – V172) x 77/92	V127	V172 + (V80 – V172) x 45/92

Table 104

Grayscale voltage	Calculation formula	Grayscale voltage	Calculation formula
V128	V172 + (V80 – V172) x 44/92	V160	V172 + (V80 – V172) x 12/92
V129	V172 + (V80 – V172) x 43/92	V161	V172 + (V80 – V172) x 11/92
V130	V172 + (V80 – V172) x 42/92	V162	V172 + (V80 – V172) x 10/92
V131	V172 + (V80 – V172) x 41/92	V163	V172 + (V80 – V172) x 9/92
V132	V172 + (V80 – V172) x 40/92	V164	V172 + (V80 – V172) x 8/92
V133	V172 + (V80 – V172) x 39/92	V165	V172 + (V80 – V172) x 7/92
V134	V172 + (V80 – V172) x 38/92	V166	V172 + (V80 – V172) x 6/92
V135	V172 + (V80 – V172) x 37/92	V167	V172 + (V80 – V172) x 5/92
V136	V172 + (V80 – V172) x 36/92	V168	V172 + (V80 – V172) x 4/92
V137	V172 + (V80 – V172) x 35/92	V169	V172 + (V80 – V172) x 3/92
V138	V172 + (V80 – V172) x 34/92	V170	V172 + (V80 – V172) x 2/92
V139	V172 + (V80 – V172) x 33/92	V171	V172 + (V80 – V172) x 1/92
V140	V172 + (V80 – V172) x 32/92	V172	$\Delta V \times \sum$ (R7~R11)/SUMR+V255
V141	V172 + (V80 – V172) x 31/92	V173	V220 + (V172 – V220) x 47/48
V142	V172 + (V80 – V172) x 30/92	V174	V220 + (V172 – V220) x 46/48
V143	V172 + (V80 – V172) x 29/92	V175	V220 + (V172 – V220) x 45/48
V144	V172 + (V80 – V172) x 28/92	V176	V220 + (V172 – V220) x 44/48
V145	V172 + (V80 – V172) x 27/92	V177	V220 + (V172 – V220) x 43/48
V146	V172 + (V80 – V172) x 26/92	V178	V220 + (V172 – V220) x 42/48
V147	V172 + (V80 – V172) x 25/92	V179	V220 + (V172 – V220) x 41/48
V148	V172 + (V80 – V172) x 24/92	V180	V220 + (V172 – V220) x 40/48
V149	V172 + (V80 – V172) x 23/92	V181	V220 + (V172 – V220) x 39/48
V150	V172 + (V80 – V172) x 22/92	V182	V220 + (V172 – V220) x 38/48
V151	V172 + (V80 – V172) x 21/92	V183	V220 + (V172 – V220) x 37/48
V152	V172 + (V80 – V172) x 20/92	V184	V220 + (V172 – V220) x 36/48
V153	V172 + (V80 – V172) x 19/92	V185	V220 + (V172 – V220) x 35/48
V154	V172 + (V80 – V172) x 18/92	V186	V220 + (V172 – V220) x 34/48
V155	V172 + (V80 – V172) x 17/92	V187	V220 + (V172 – V220) x 33/48
V156	V172 + (V80 – V172) x 16/92	V188	V220 + (V172 – V220) x 32/48
V157	V172 + (V80 – V172) x 15/92	V189	V220 + (V172 – V220) x 31/48
V158	V172 + (V80 – V172) x 14/92	V190	V220 + (V172 – V220) x 30/48
V159	V172 + (V80 – V172) x 13/92	V191	V220 + (V172 – V220) x 29/48

Table 105

Grayscale voltage	Calculation formula
V192	V220 + (V172 – V220) x 28/48
V193	V220 + (V172 – V220) x 27/48
V194	V220 + (V172 – V220) x 26/48
V195	V220 + (V172 – V220) x 25/48
V196	V220 + (V172 – V220) x 24/48
V197	V220 + (V172 – V220) x 23/48
V198	V220 + (V172 – V220) x 22/48
V199	V220 + (V172 – V220) x 21/48
V200	V220 + (V172 – V220) x 20/48
V201	V220 + (V172 – V220) x 19/48
V202	V220 + (V172 – V220) x 18/48
V203	V220 + (V172 – V220) x 17/48
V204	V220 + (V172 – V220) x 16/48
V205	V220 + (V172 – V220) x 15/48
V206	V220 + (V172 – V220) x 14/48
V207	V220 + (V172 – V220) x 13/48
V208	V220 + (V172 – V220) x 12/48
V209	V220 + (V172 – V220) x 11/48
V210	V220 + (V172 – V220) x 10/48
V211	V220 + (V172 – V220) x 9/48
V212	V220 + (V172 – V220) x 8/48
V213	V220 + (V172 – V220) x 7/48
V214	V220 + (V172 – V220) x 6/48
V215	V220 + (V172 – V220) x 5/48
V216	V220 + (V172 – V220) x 4/48
V217	V220 + (V172 – V220) x 3/48
V218	V220 + (V172 – V220) x 2/48
V219	V220 + (V172 – V220) x 1/48
V220	ΔV x ∑ (R8~R11)/SUMR+V255
V221	V240 + (V220 – V240) x 19/20
V222	V240 + (V220 – V240) x 18/20
V223	V240 + (V220 – V240) x 17/20

Grayscale voltage	Calculation formula
V224	V240 + (V220 – V240) x 16/20
V225	V240 + (V220 – V240) x 15/20
V226	V240 + (V220 – V240) x 14/20
V227	V240 + (V220 – V240) x 13/20
V228	V240 + (V220 – V240) x 12/20
V229	V240 + (V220 – V240) x 11/20
V230	V240 + (V220 – V240) x 10/20
V231	V240 + (V220 – V240) x 9/20
V232	V240 + (V220 – V240) x 8/20
V233	V240 + (V220 – V240) x 7/20
V234	V240 + (V220 – V240) x 6/20
V235	V240 + (V220 – V240) x 5/20
V236	V240 + (V220 – V240) x 4/20
V237	V240 + (V220 – V240) x 3/20
V238	V240 + (V220 – V240) x 2/20
V239	V240 + (V220 – V240) x 1/20
V240	ΔV x ∑ (R9~R11)/SUMR+V255
V241	V247 + (V240 – V247) x 6/7
V242	V247 + (V240 – V247) x 5/7
V243	V247 + (V240 – V247) x 4/7
V244	V247 + (V240 – V247) x 3/7
V245	V247 + (V240 – V247) x 2/7
V246	V247 + (V240 – V247) x 1/7
V247	ΔV x ∑ (R10~R11)/SUMR+V255
V248	V251 + (V247 – V251) x 3/4
V249	V251 + (V247 – V251) x 2/4
V250	V251 + (V247 – V251) x 1/4
V251	ΔV x R11/SUMR+V255
V252	V255 + (V251 – V255) x 3/4
V253	V255 + (V251 – V255) x 2/4
V254	V255 + (V251 – V255) x 1/4
V255	-

Note: Make sure that
ΔV = V0 – V255
SUMR = ∑(R1 ~ R11) ≥ 70R.
V255 ≥ 0.2V

Frame Memory Data and Grayscale Voltage

Table 106

RAM data	Grayscale voltage			
	REV = 1		REV = 0	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity
8'h00	V0	V255	V255	V0
8'h01	V1	V254	V254	V1
8'h02	V2	V253	V253	V2
8'h03	V3	V252	V252	V3
8'h04	V4	V251	V251	V4
8'h05	V5	V250	V250	V5
8'h06	V6	V249	V249	V6
8'h07	V7	V248	V248	V7
8'h08	V8	V247	V247	V8
8'h09	V9	V246	V246	V9
8'h0A	V10	V245	V245	V10
8'h0B	V11	V244	V244	V11
8'h0C	V12	V243	V243	V12
8'h0D	V13	V242	V242	V13
8'h0E	V14	V241	V241	V14
8'h0F	V15	V240	V240	V15
8'h10	V16	V239	V239	V16
8'h11	V17	V238	V238	V17
8'h12	V18	V237	V237	V18
8'h13	V19	V236	V236	V19
8'h14	V20	V235	V235	V20
8'h15	V21	V234	V234	V21
8'h16	V22	V233	V233	V22
8'h17	V23	V232	V232	V23
8'h18	V24	V231	V231	V24
8'h19	V25	V230	V230	V25
8'h1A	V26	V229	V229	V26
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.

Table 107 (Continued)

RAM data	Grayscale voltage			
	REV = 1		REV = 0	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity
.	.	.	.	.
.	.	.	.	.
8'hE5	V229	V26	V26	V229
8'hE6	V230	V25	V25	V230
8'hE7	V231	V24	V24	V231
8'hE8	V232	V23	V23	V232
8'hE9	V233	V22	V22	V233
8'hEA	V234	V21	V21	V234
8'hEB	V235	V20	V20	V235
8'hEC	V236	V19	V19	V236
8'hED	V237	V18	V18	V237
8'hEE	V238	V17	V17	V238
8'hEF	V239	V16	V16	V239
8'hF0	V240	V15	V15	V240
8'hF1	V241	V14	V14	V241
8'hF2	V242	V13	V13	V242
8'hF3	V243	V12	V12	V243
8'hF4	V244	V11	V11	V244
8'hF5	V245	V10	V10	V245
8'hF6	V246	V9	V9	V246
8'hF7	V247	V8	V8	V247
8'hF8	V248	V7	V7	V248
8'hF9	V249	V6	V6	V249
8'hFA	V250	V5	V5	V250
8'hFB	V251	V4	V4	V251
8'hFC	V252	V3	V3	V252
8'hFD	V253	V2	V2	V253
8'hFE	V254	V1	V1	V254
8'hFF	V255	V0	V0	V255

Power Supply Circuit

The following figure illustrates the configuration of R61523 LCD drive voltage generating circuit.

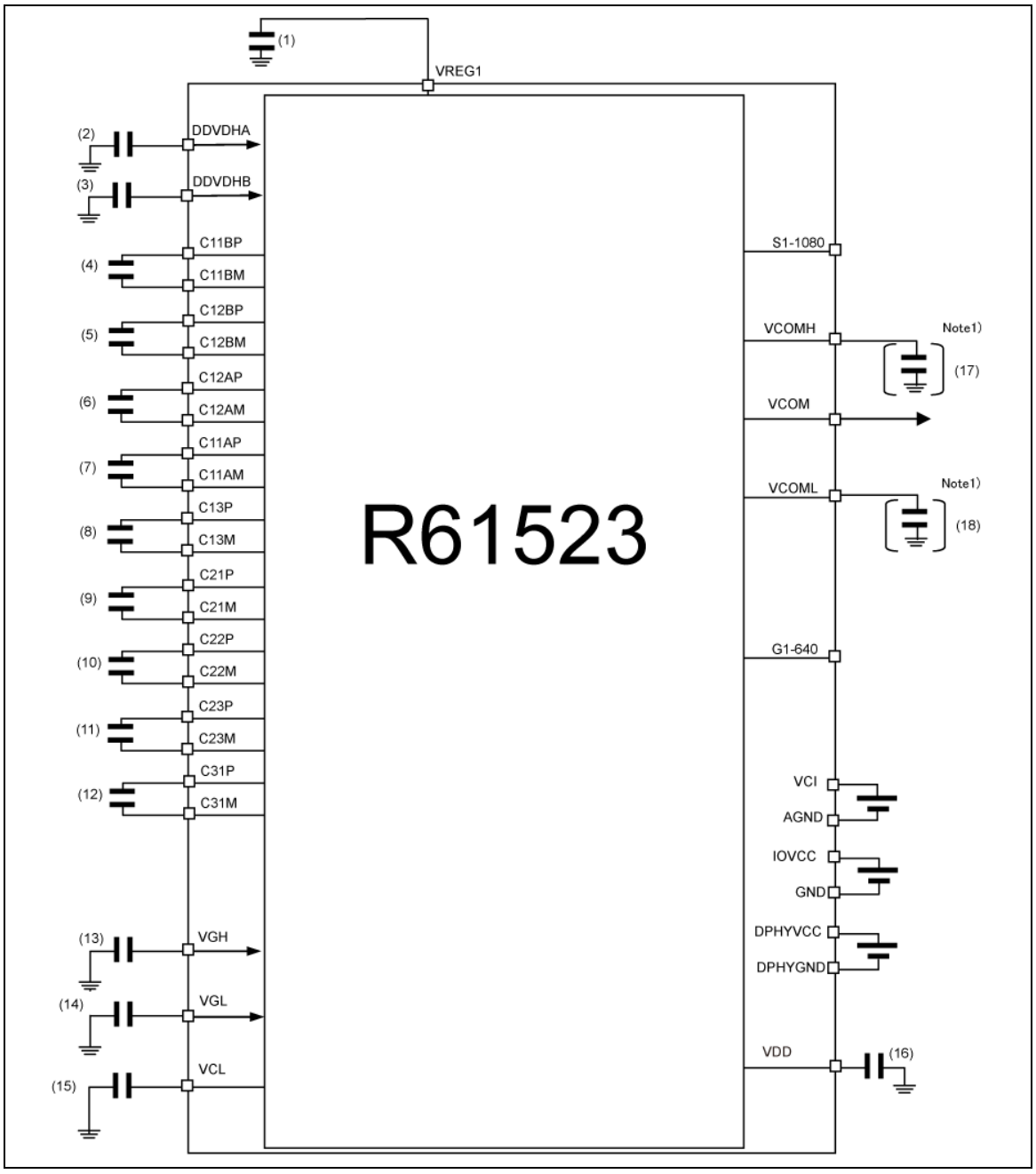


Figure 60

Note: Evaluate image quality on the panel to decide whether the stabilizing capacitances connected to VCOMH and VCOML may be removed.

Specifications of External Elements Connected to the Power Supply Circuit

The following table shows the specifications of external elements connected to the R61523 power supply circuit. The numbers of the connection pins correspond to the numbers shown in the Configuration of Power Supply Circuit.

Table 108 Capacitor Connected to LCD Power Supply Circuit

Capacity	Recommended voltage	Connection pins
1µF (B characteristics)	6V	(1)VREG1, (4)C11BP/M, (5) C12BP/M, (6)C12AM/P, (7)C11AP/M, (8)C13P/M, (15)VCL, (16)VDD
	10V	(2)DDVDHA, (3)DDVDHB, (9)C21P/M (10)C22P/M (11)C23P/M, (12) C31P/M, (17)VCOMH, (18)VCOML
	25V	(13)VGH, (14)VGL

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61523 and the relationship between TFT display application voltage waveforms and electrical potential.

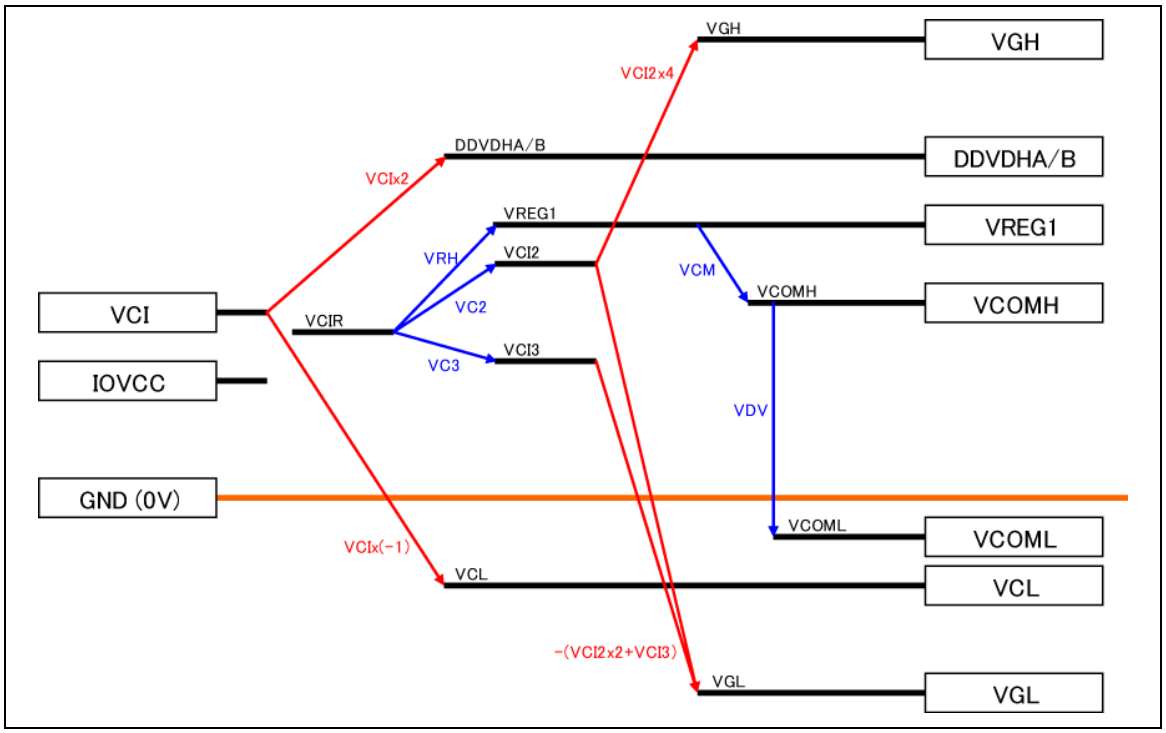


Figure 61

Note: The DDVDH, VGH, VGL, VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at respective outputs. When the alternating cycle of VCOM is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

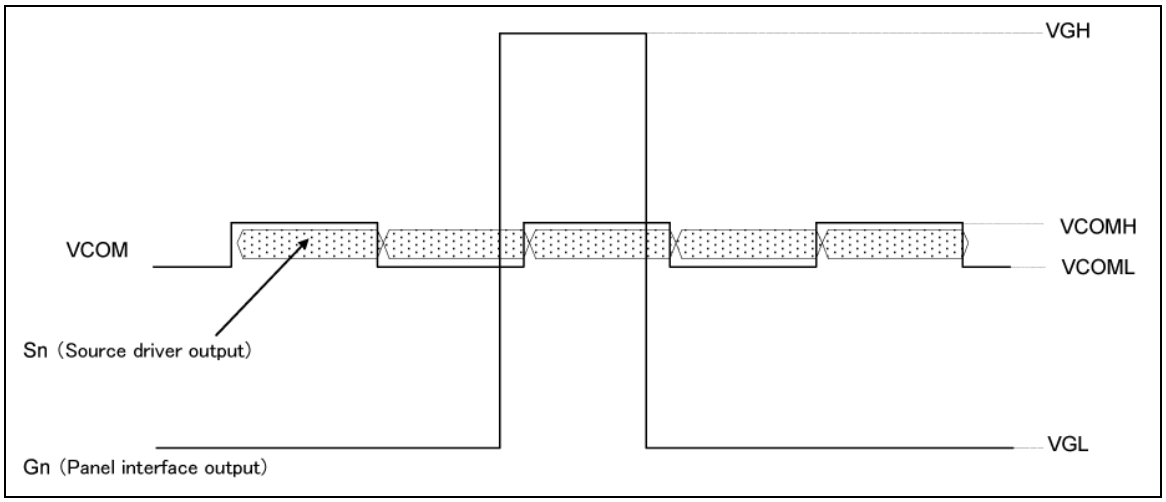


Figure 62 Voltage Application to TFT Display

NVM Control

The R61523 incorporates 44-bit NVM for user's use.

The following are read using read_DDB_start command.

- 16 bits for Supplier ID
- 16 bits for Supplier Elective Data
- 12 bits for VCOM adjustment (VCM[6:0] and VDV[4:0])

To write, read and erase data from/to the NVM, follow the sequences below. Data on the NVM is loaded to internal registers automatically when the following sequences are performed.

Power On sequence

HW RESET sequence

exit_sleep_mode sequence

soft_reset sequence

Deep Standby Mode Off sequence

Data stored in the NVM is retained permanently even if power is turned off.

Table 109

Operation	Power supply voltage		Time	Temperature
Write/Erase	VCI	2.60~3.00V	400ms or more (after FFT (E0h) is set to 1)	+20°C~+30C°
	IOVCC	1.65~3.60V		

Note: NVM data rewrite (erase-write) operation shall be performed up to 5 times per address.

NVM Write Sequence

The register values of User/Manufacturer Commands supposed to be stored in NVM are written to NVM. When “0” is written to an address, the bit of the address is set to “0”. If the data is erased from the bit, the bit is returned to ”1”. The bit to which data is not written shall be set to “1”.

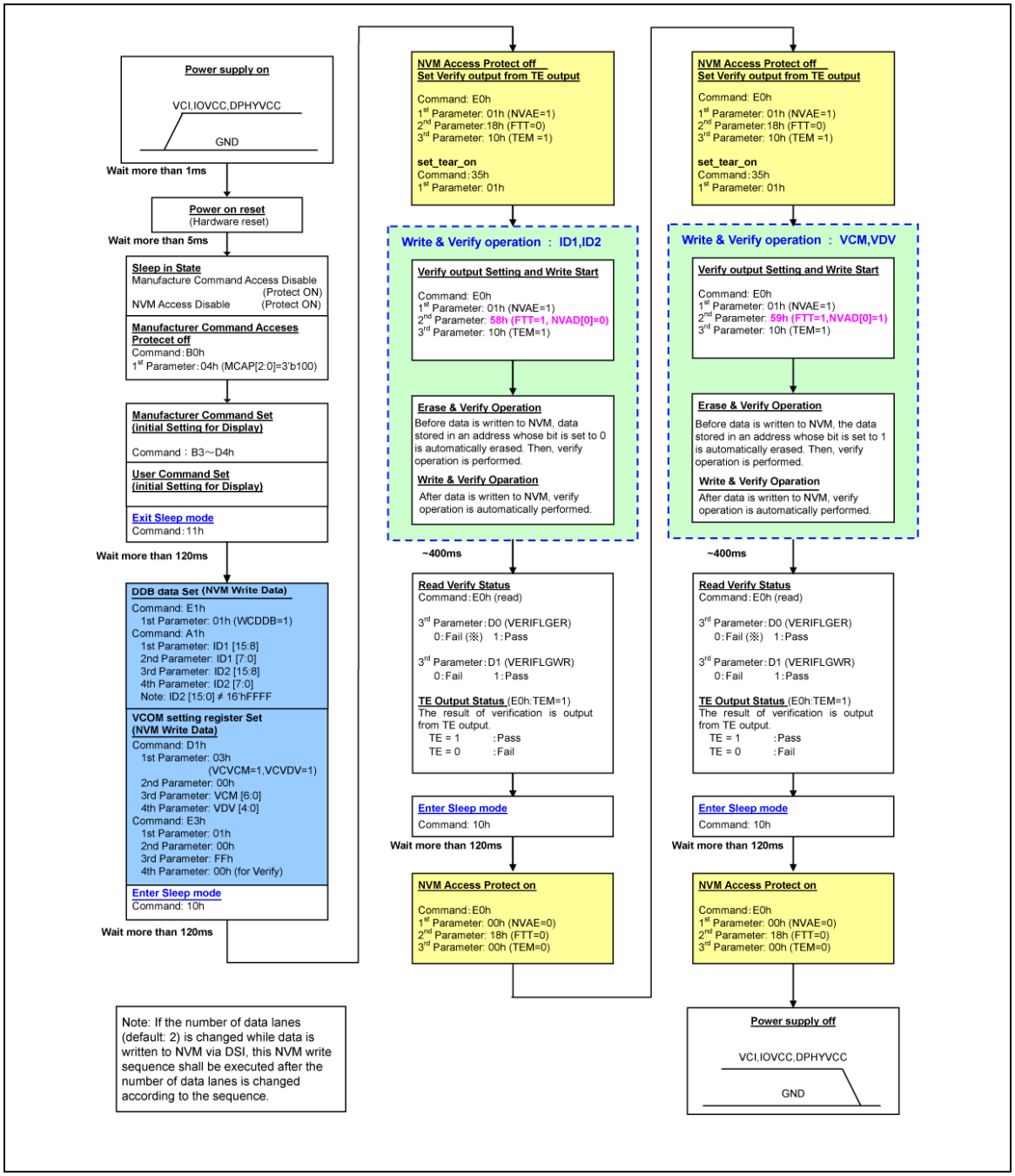


Figure 63

Absolute Maximum Rating

Table 110

Item	Symbol	Unit	Ratings	Note
Power supply voltage 1	IOVCC,DPHYVCC	V	-0.3 ~ +4.6	1, 2
Power supply voltage 2	VCI – AGND	V	-0.3 ~ +4.6	1, 3
Power supply voltage 3	DDVDHA/B– AGND	V	-0.3 ~ +6.5	1, 4
Power supply voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power supply voltage 5	AGND– VGL	V	-0.3 ~ +13.0	1, 5
Power supply voltage 6	VGH– VGL	V	-0.3 ~ +30.0	1
Power supply voltage 7	VCI – VCL	V	-0.3 ~ +6.5	1, 6
Input voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1
Operating Temperature	Topr	°C	-40 ~ +85	1, 7
Storage Temperature	Tstg	°C	-55 ~ +110	1

Notes:
1. If the LSI is used beyond the absolute maximum ratings, it may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of the LSI is not guaranteed if it is used in the conditions above the limits and it may lead to malfunction.
2. Make sure (High) IOVCC, DPHYVCC ≥ GND (Low).
3. Make sure (High) VCI ≥ AGND (Low).
4. Make sure (High) DDVDHA/B ≥ AGND (Low).
5. Make sure (High) AGND ≥ VGL (Low).
6. Make sure (High) VCI ≥ VCL (Low).
7. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Electrical Characteristics

DC characteristics

Table 111 (VCI= 2.60V~3.00V, IOVCC=1.65V~3.60V, DPHYVCC=1.65V~1.95V, Ta=-40°C~+85°C)

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Input "High" level voltage 1 (Except for RESX)		V_{IH1}	V	IOVCC=1.65V～3.60V	0.80× IOVCC	–	IOVCC	1, 2
Input "Low" level voltage 1 (Except for RESX)		V_{IL1}	V	IOVCC=1.65V～3.60V	0	–	0.20× IOVCC	1, 2
Input "High" level voltage 2 (RESX)		V_{IH2}	V	IOVCC=1.65V～3.60V	0.90× IOVCC	–	IOVCC	1, 2
Input "Low" level voltage 2 (RESX)		V_{IL2}	V	IOVCC=1.65V～3.60V	0	–	0.10× IOVCC	1, 2
Output "High" level voltage 1 (DB[15:0], TE, LEDPWM)		V_{OH1}	V	IOVCC=1.65V～3.60V, IOUT=-0.1mA	0.80× IOVCC	–	–	1
Output "Low" level voltage 1 (DB[15:0], TE, LEDPWM)		V_{OL1}	V	IOVCC=1.65V～3.60V, IOUT=0.1mA	–	–	0.20× IOVCC	1
Input "High" level current		I_{IH}	μA	Vin=IOVCC	–	–	10	4
Input "Low" level current		I_{IL}	μA	Vin=0V	-10	–	–	4
Current consumption (IOVCC-GND)	Normal Mode +Sleep out	I_{OPN}	mA	640-line drive, IOVCC=1.80V, VCI= 2.80V, fFLM=60Hz, Ta=25°C, Frame Memory Data :24'h000000, When DBI is used, BLCON=0, and frame is inverted.	-	1.0	1.4	5
	Idle Mode +Sleep out	I_{OPI}	mA	120-line partial display, IOVCC=1.80V, VCI= 2.80V, fFLM=60Hz, Ta=25°C, Frame Memory Data: 24'h000000, When DBI is used, frame is inverted.	-	0.7	1.1	5
	Deep Sleep mode	I_{DST1}	μA	IOVCC=1.80V, VCI= 2.80V, DPHYVCC = 1.80V, Ta=25°C	-	0.1	1.0	5

DSI current consumption (DPHYVCC-DPHYGND)	HS mode	I_{HS}	mA	IOVCC=1.80V, DPHYVCC=1.80V, VCI=2.80V, DSI 2lanes, DSICLK=120MHz, DSI Data:24'h000000	-	0.8	1.2	(5)
	LP mode	I_{LP}	uA	IOVCC=1.80V, DPHYVCC=1.80V, VCI =2.80V, Clock lane=LP11, Data lane=LP11	-	0.1	1.0	(5)
	Deep Sleep Mode	I_{DST2}	uA	IOVCC=DPHYVCC =1.80V, VCI= 2.80V, Ta=25°C	-	0.1	1.0	(5)
LCD power supply current (VCI-GND)	Normal Mode +Sleep out	I_{CIN}	mA	IOVCC=1.80V, VCI=2.80V, 640-line drive, fFLM=60Hz, Ta=25°C, Frame Memory Data=24'h000000, BLCON = 0, frame is inverted, No load on the panel.	-	4.0	6.0	(5)
	Idle mode +Sleep out	I_{CII}	mA	IOVCC=1.80V, VCI=2.80V, 120-line partial display, fFLM=60Hz, Ta=25°C, Frame Memory Data=24'h000000, BLCON = 0, frame is inverted, No load on the panel.	-	1.4	2.5	(5)
	Deep Sleep Mode	I_{DST3}	uA	IOVCC=1.80V, VCI= 2.80V, DPHYVCC = 1.80V, Ta=25°C	-	0.10	1.0	(5)
Output voltage dispersion	V0~V80, V176~V255	⊿Vo1	mV	-	-	-	40	(6)
	V81~V175	⊿Vo2	mV		-	-	30	(6)
Average output voltage variance		⊿V⊿	mV	-	-35	-	+35	(7)

Notes: 1. DC/AC electrical characteristics of bare die and wafer area guaranteed at +85°C.

2. The following figures illustrate the configurations of input, I/O, and output pins.

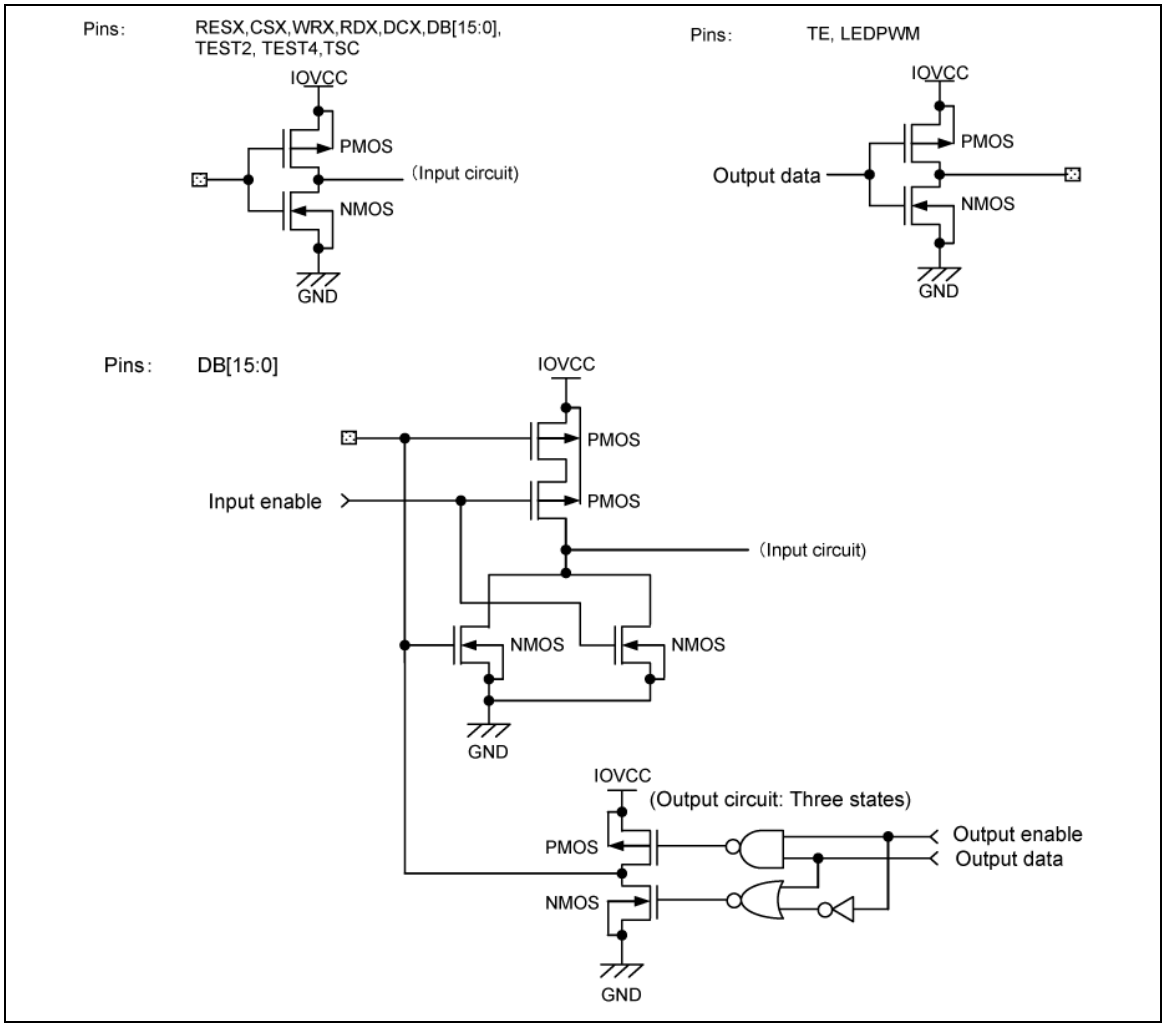


Figure 64

3. Fix pins as follows: TEST2, TEST4, VREFC, VDDTEST, and TSC to ground (GND), VPP1 to ground (AGND).
4. This excludes the current in the output drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because shoot-through current increases in the input circuit when the CMOS input level is at a mid-level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.
6. This is the difference in voltage levels between two output pins placed side by side in the same display mode. The output voltage dispersion is for reference.
7. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with the same display data.

Step-up Circuit Characteristics

Table 112

Item		Unit	Test condition	Min.	Typ.	Max.	Note
Step-up output voltage	DDVDH	V	VCI=2.80V, Ta=25°C, VC2=3'h4, VC3=3'h7, AP=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h2, I_{load} =-3[mA], No load on the panel, COG resistance=0Ω	5.30	5.45	-	(1)
Step-up output voltage	VGH	V	VCI=2.80V, Ta=25°C, VC2=3'h4, VC3=3'h7, AP=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h2, I_{load} =-100[uA], No load on the panel, COG resistance=0Ω	14.90	15.25	-	
Step-up output voltage	VGL	V	VCI=2.80V, Ta=25°C, VC2=3'h4, VC3=3'h7, AP=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h2, I_{load} =+100[uA], No load on the panel, COG resistance=0Ω	-	-9.90	-9.50	
Step-up output voltage	VCL	V	VCI=2.80V, Ta=25°C, VC2=3'h4, VC3=3'h7, AP=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h2, I_{load} =+1[mA], No load on the panel, COG resistance=0Ω	-	-2.50	-2.30	

Internal Reference Voltage

Table 113 Internal Reference Voltage (Ta=-40°C ~ +85°C, GND=AGND=0V)

Item	Symbol	Unit	Min.	Typ.	Max.	Condition
Internal Reference Voltage	VCIR	V	—	2.53	—	

Power Supply Voltage Range

Table 114 Power Supply Voltage Range (Ta=-40°C ~ +85°C, GND=AGND=0V)

Item	Symbol	Unit	Min.	Typ.	Max.	Condition
Power supply voltage	IOVCC	V	1.65	1.80	3.60	-
Power supply voltage	DPHYVCC	V	1.65	1.80	1.95	
Power supply voltage	VCI	V	2.60	2.80	3.00	-

Output Voltage Range

Table 115 Output Voltage Range （Ta=-40°C ~ +85°C, GND=AGND=0V）

Item	Symbol	Unit	Min.	Typ.	Max.	Condition
Grayscale. VCOM reference voltage	VREG1	V	-	-	DDVDH-0.5	-
Source driver		V	GND+0.2	-	VREG1	-
VCOMH output	VCOMH	V	-	-	VREG1	-
VCOML output	VCOML	V	VCL+0.5	-	-	-
VCOM amplitude		V	-	-	6.0	-
Step-up output voltage	DDVDH	V	4.5	-	6.0	-
Step-up output voltage	VGH	V	10.0	-	16.8	-
Step-up output voltage	VGL	V	-10.9	-	-4.5	-
Step-up output voltage	VCL	V	-3.0	-	-1.9	-
Voltage between VCI and VCL		V	-	-	6.0	-
Voltage between VGH and VGL		V	-	-	28.0	-

Clock Characteristics

Table 116 (Ta=-40°C ~ +85°C, VCI= 2.60V ~ 3.00V, IOVCC=1.65V~3.60V)

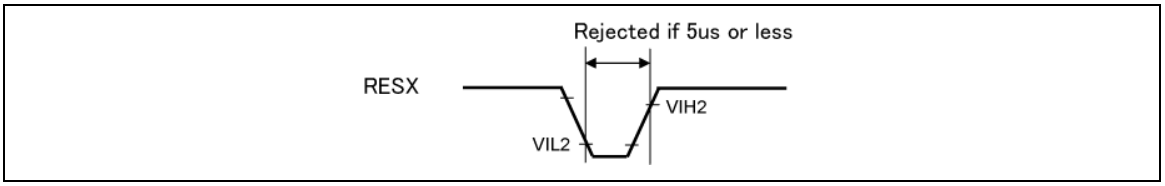
Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Oscillation clock	fosc	KHz		930	1000	1070

Reset Timing Characteristics

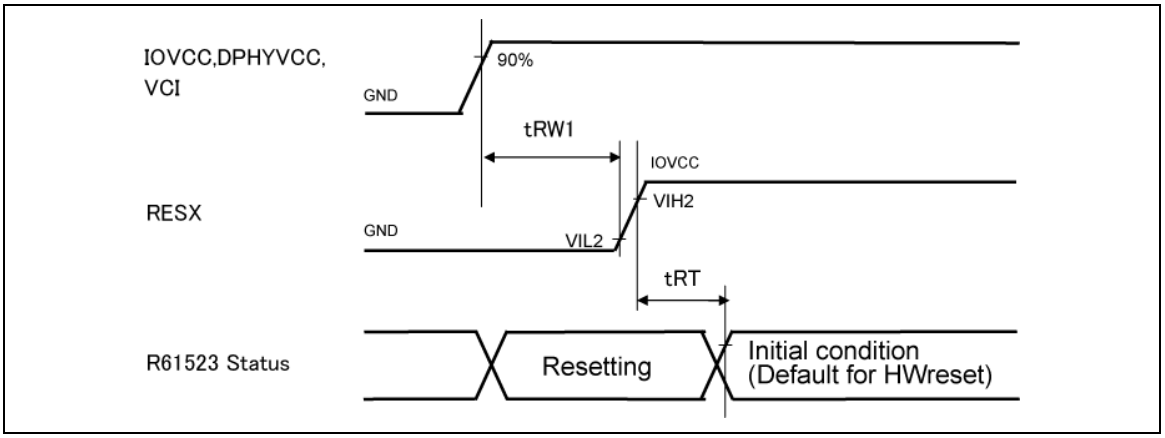
Table 117 (VCI= 2.60V~3.00V, IOVCC=1.65V~3.60V, Ta=-40°C ~ +85°C)

Item	Symbol	Unit	Test condition	Min.	Max.
Reset "Low" level width 1	tRW1	ms	Power supply on	1	–
Reset "Low" level width 2	tRW2	us	In an operating mode	10	–
Reset time	tRT	ms		–	5

Reset Reject



1) Reset Timing when power is on



2) Reset Timing during operation

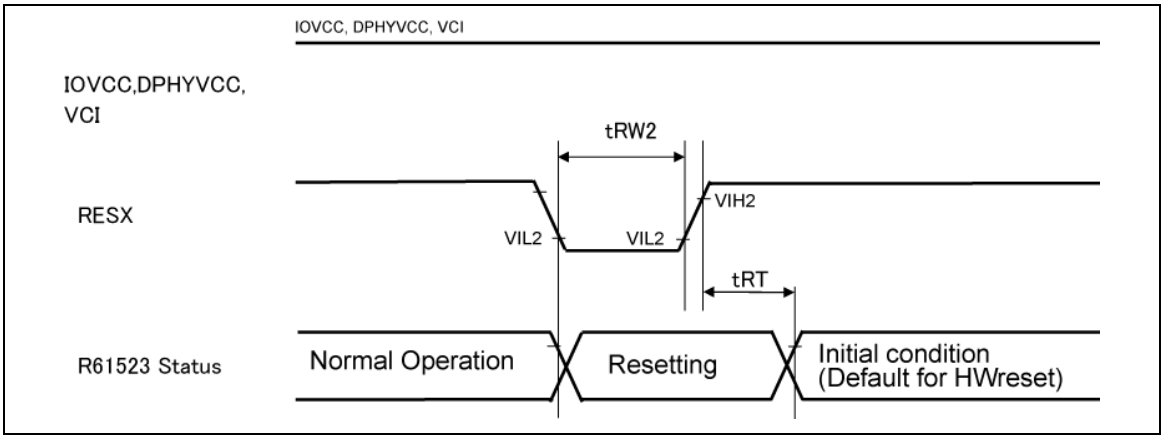


Figure 65

Liquid Crystal Driver Output Characteristics

Table 118

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
VCOM output delay time	tddv	us	IOVCC=1.8V, VCI=2.8V, Ta=25°C, BC0=1, FP=8'h08, BP=8'h08, VRH=5'h18, VCM=7'h3F, VDV=5'h15, AP=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h2, VEQW=3'h1, Time to reach the target voltage ±35mV from VCOM polarity inversion timing, load resistance R = 100Ω, load capacitance C = 20nF	–	20	25	–
Source driver output delay time	tdds	µs	IOVCC=1.8V, VCI=2.8V, Ta=25°C, BC0=1, FP=8'h08, BP=8'h08, VRH=5'h18, VCM=7'h3F, VDV=5'h15, AP=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h2, Transition time from the same grayscale at all source pins, Time to reach the target voltage level ±35mV when source output level alternates between V0 and V255, load resistance R = 10kΩ, load capacitance C = 15pF	–	15	25	See note

Note: LCD driver output delay time depends on load on the liquid crystal panel. Therefore, frame frequency and one line cycle need to be specified, checking image quality on the panel to be used.

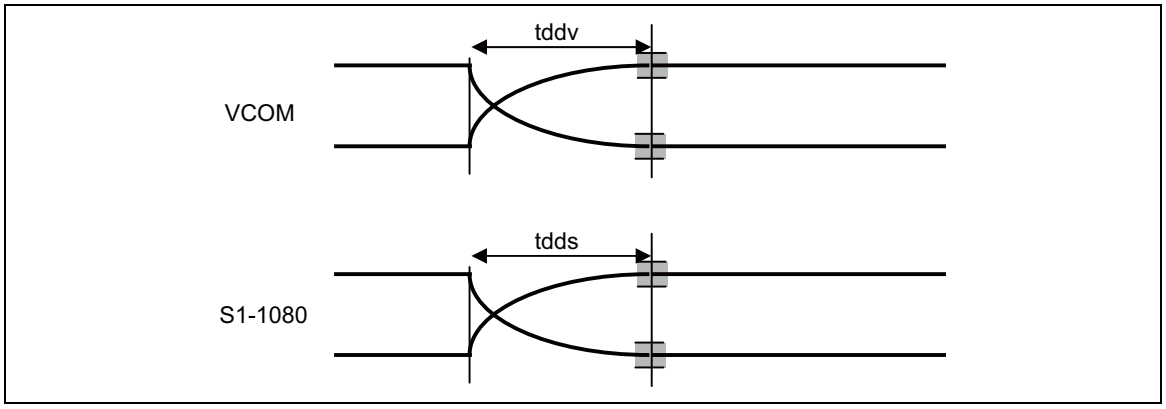


Figure 66 LCD Driver Output Timing

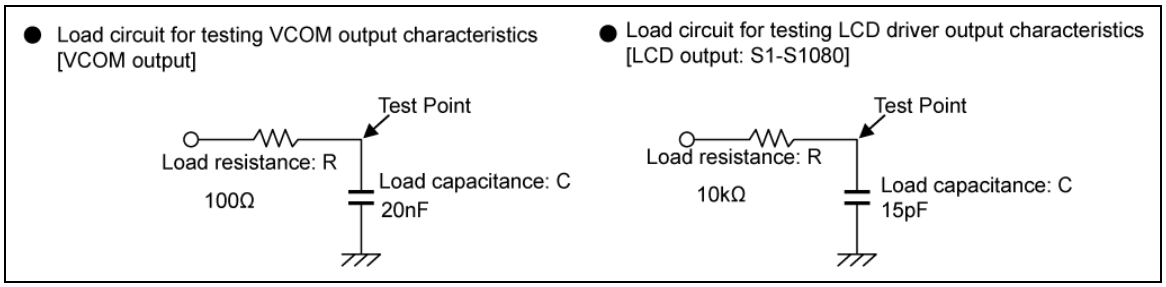


Figure 67 LCD Driver Output Characteristics Test Circuit

MIPI-DBI Type B (16/8 Bits) Timing Characteristics

Table 119 16-Bit 1, 3/2, 2 Transfers (IOVCC=1.65V~3.60V, Ta=-40°C~+85°C)

Item	Symbol		Unit	Test condition	Min.	Max.
Address setup time	DCX	tast	ns		0	-
Address hold time (Write/Read)		taht	ns		10	-
Chip select setup time (Write)	CSX	tcs	ns		30	-
Chip select setup time (Read)		trcs	ns		170	-
Chip select wait time (Write/Read)		tcsf	ns		20	-
Write cycle time	WRX	twc	ns		60	-
Write control pulse ”High” period		twrh	ns		22	-
Write control pulse ”Low” period		twrl	ns		25	-
Read cycle time	RDX	trc	ns		450	-
Read control pulse ”High” period		trdh	ns		250	-
Read control pulse “Low” period		trdl	ns		170	-
Write data setup time	DB[15:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write data hold time		twdh	ns		20	-
Read access time		tracc	ns		10	150
Output disable time		trod	ns		10	-
Rise/Fall time	-	tr/tf	ns		-	15

Table 120 8-Bit 2, 3 Transfers (IOVCC=1.65V~3.60V, Ta=-40°C~+85°C)

Item	Symbol		Unit	Test condition	Min.	Max.
Address setup time	DCX	tast	ns		0	-
Address hold time (Write/Read)		taht	ns		10	-
Chip select setup time (Write)	CSX	tcs	ns		30	-
Chip select setup time (Read)		trcs	ns		170	-
Chip select wait time (Write/Read)		tcsf	ns		20	-
Write cycle time	WRX	twc	ns		40	-
Write control pulse ”High” period		twrh	ns		18	-
Write control pulse ”Low” period		twrl	ns		18	-
Read cycle time	RDX	trc	ns		450	-
Read control pulse ”High” period		trdh	ns		250	-
Read control pulse “Low” period		trdl	ns		170	-
Write data setup time	DB[15:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write data hold time		twdh	ns		20	-
Read access time		tracc	ns		10	150
Output disable time		trod	ns		10	-
Rise/Fall time	-	tr/tf	ns		-	15

Note: 1 transfer: (1)16bit-I/F 16bpp
3/2 transfer: (1)16bit-I/F 18bpp, (2)16bit-I/F 24bpp Option1
2 transfer: (1)8bit-I/F 16bpp, (2)16bit-I/F 18bpp Option2, 3, (3)16bit-I/F 24bpp Option2
3 transfer: (1)8bit-I/F 18bpp, (2) 8bit-I/F 24bpp

DBI Type B (16/8 bit) Timing

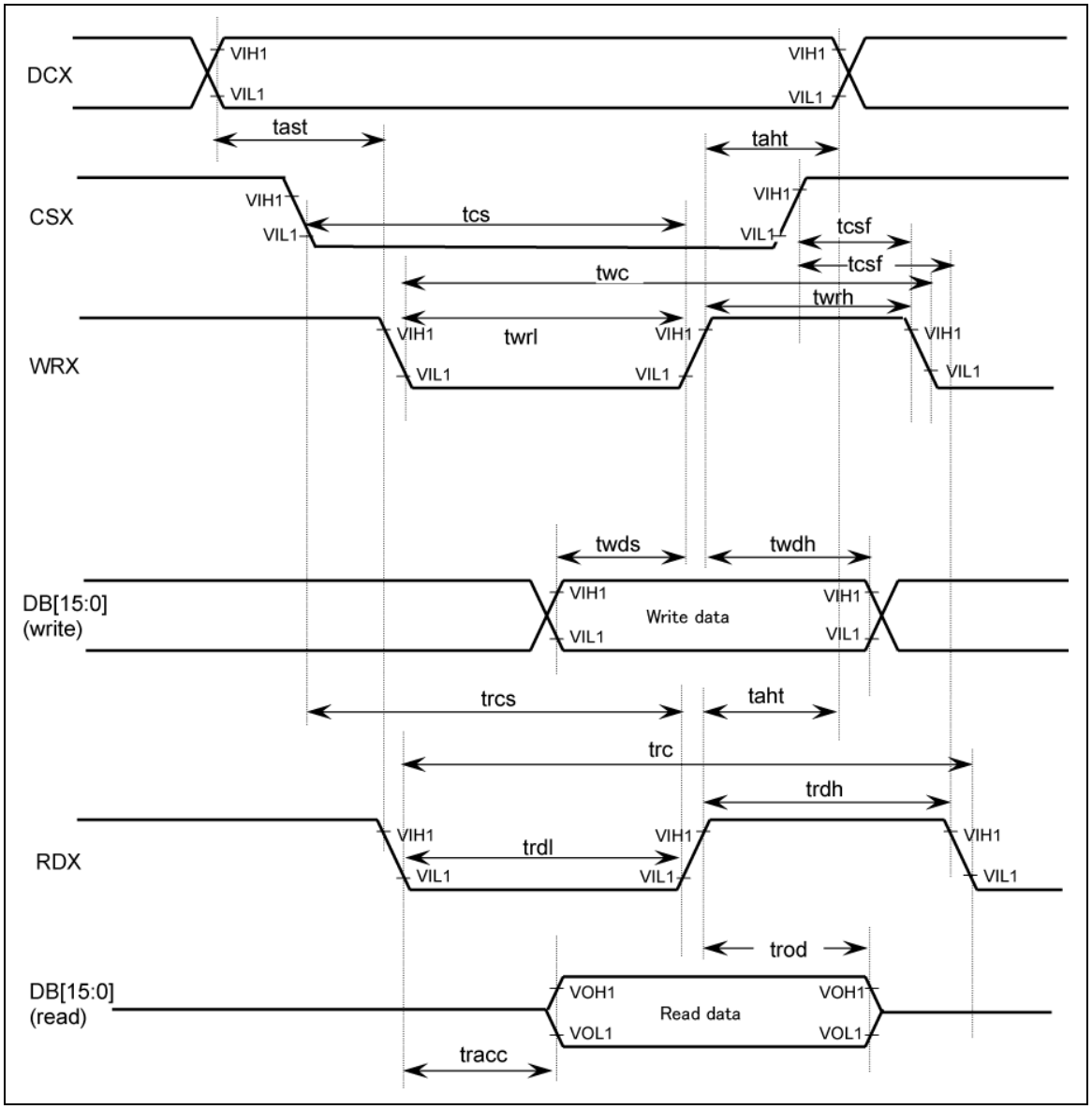


Figure 68

Note: Make sure to fix unused pins [15:0] to “IOVCC” or “GND”.

MIPI-DSI Interface DC Specifications

Table 121 (DPHYVCC=1.65V~1.95V, Ta=-40°C ~ +85°C)

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV		-	-	70	
	Differential input low threshold	VIDTL	mV		-70	-	-	
	Single-ended input low voltage	VILHS	mV		-40	-	-	
	Single-ended input high voltage	VIHHS	mV		-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV		70	-	330	1
	Differential input impedance	ZID	Ω		-	(85)	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV		-	-	550	
	Logic 1 input voltage	VIH	mV		880	-	-	
LP-TX	Thevenin output low level	VOL	mV		-50	-	50	
	Thevenin output high level	VOH	V		1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω		(110)	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV		-	-	200	
	Logic 1 contention threshold	VIHCD	mV		450	-	-	

Notes: 1. VCMRX(DC) = (VDP+VDN)/2
2. Excluding COG Resistance (Contact Resistance and ITO Wiring Resistance). The value is tentative.

HS-RX Clock and Data-Clock Specifications

Table 122 (DPHYVCC=1.65V~1.95V, Ta=-40°C~+85°C)

Item	Symbol	Unit	Timing diagram	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	-	50	-	150	
DSICLK Cycle time	tCLKP	ns	Figure A	6.7	-	20	
DSI Data Transfer Rate	tDSIR	Mbps	-	100	-	300	
Data to Clock Setup Time	tSETUP	UI	Figure A	0.15	-	-	
		ns		0.50	-	-	
Clock to Data Hold Time	tHOLD	UI	Figure A	0.15	-	-	
		ns		0.50	-	-	

LP-RX/TX Clock and Data-Clock Specifications

Table 123 (DPHYVC=1.65V~1.95V, Ta=-40°C~+85°C)

Parameter	Description	Min	Typ	Max	Unit	Timing diagram	Note
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40 ns + 4*UI	-	85ns + 6*UI	ns	Figure C	
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	–	-	ns		
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (n*8*UI, 60 ns + n*4*UI)	-	-	ns		**1,2**
$T_{HS-EXIT}$	Time to drive LP-11after HS burst	100	-	-	ns		
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPTX}$					
$T_{TA-SURE}$	Time-out before new TX side starts driving	$1*T_{LPTX}$	-	$2*T_{LPTX}$			
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPTX}$					
T_{LPX}	Length of any Low-Power state period	50	-	-	ns	Figures C, D,and E	
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between Master and Slave side	2/3	-	3/2			**5**
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60 ns + 52UI	-	-	UI	Figure D	**3**
$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	300	-	-	ns		
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI		
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns		
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns		
T_{EOT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105 ns + n*12*UI			**2**
T_{LPTX1}	Length of Low-Power TX state period in case of using DSI clock	-	n*DSITX	-	UI	Figure E	**4**
T_{LPTX2}	Length of Low-Power TX state period in case of using internal OSC clock	-	1/fosc	-	ns		

Notes: 1. If a > b then max (a, b) = a, otherwise max (a, b) = b

2. Where n = 1 for Forward-direction HS mode.
3. The R61523 operates as specified here although the last part of its internal process is left uncompleted when Clock Lane enters LP-11. However, it is favorable to have $T_{CLK\text{-}POST}$ period 256 UI or longer.
4. The R61523 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled. Here, "fosc" is the frequency of oscillator clock, typical 14 MHz.

   n*DSITX of T_{LPTX1} depends on DSIDIV setting.
5. The R61523 uses the frequency-divided DSI clock from the host processor for TX clock period.

Timing Diagram

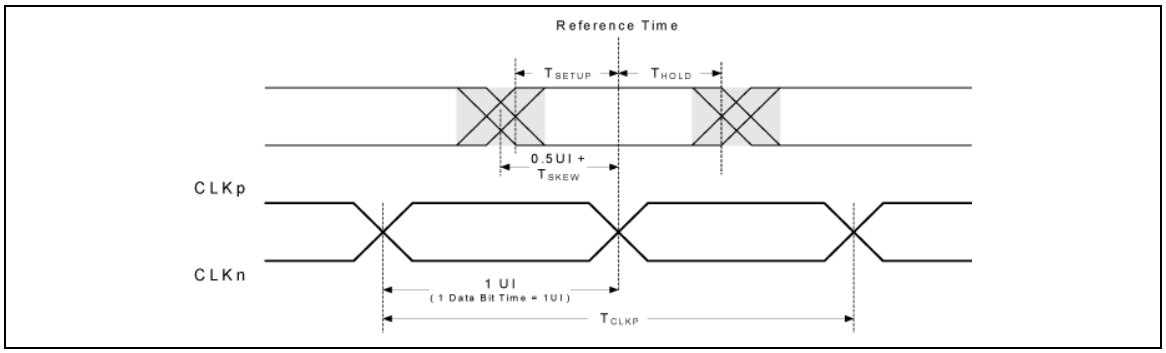


Figure A Data to Clock Timing Definition

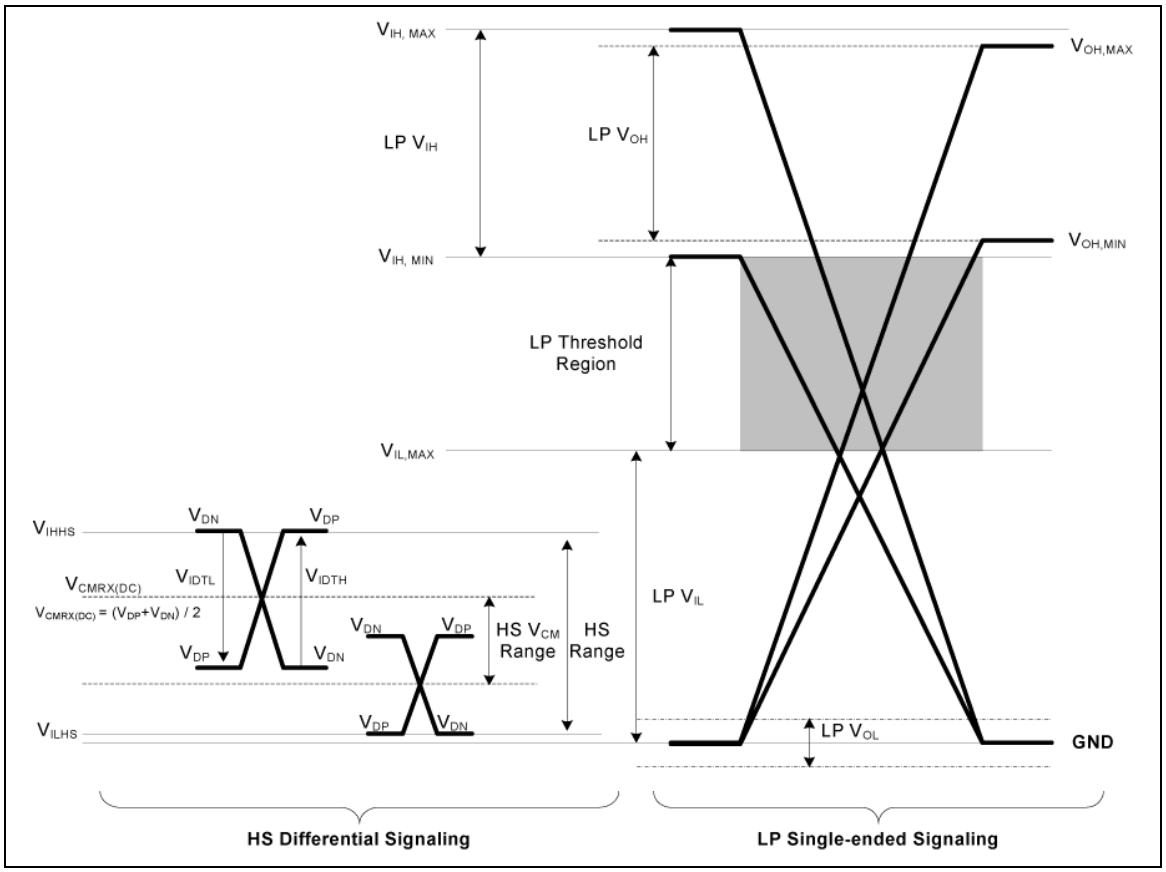
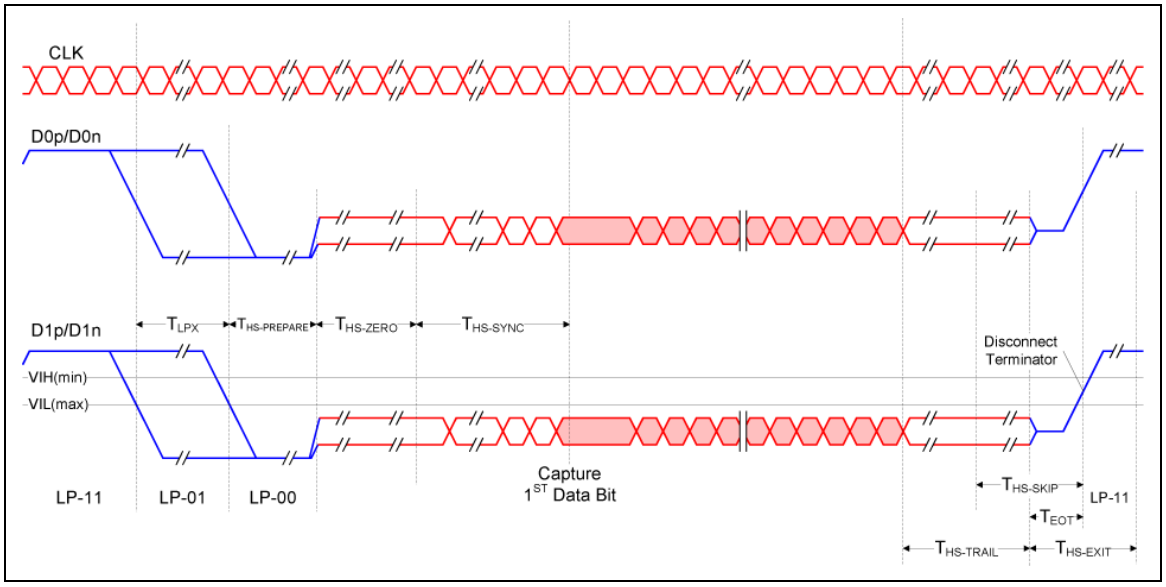


Figure B DSI LP Mode



Note: $T_{HS-SYNC}$: Proper match found for Sync sequence in HS stream, the following bits are payload data.

Figure C HS Data Transmission in Bursts

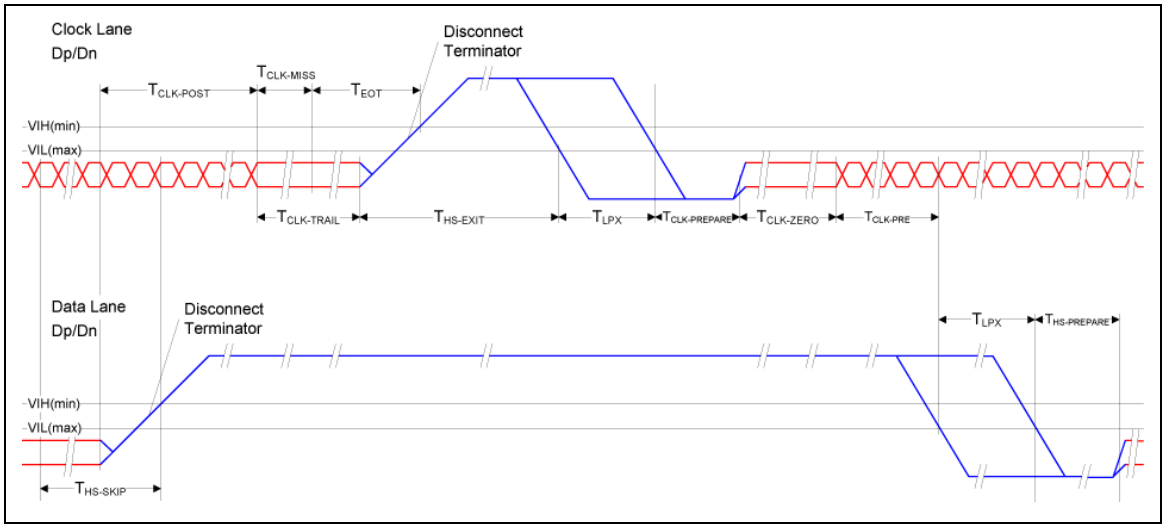


Figure D Switching the Clock Lane between Clock Transmission and LP mode

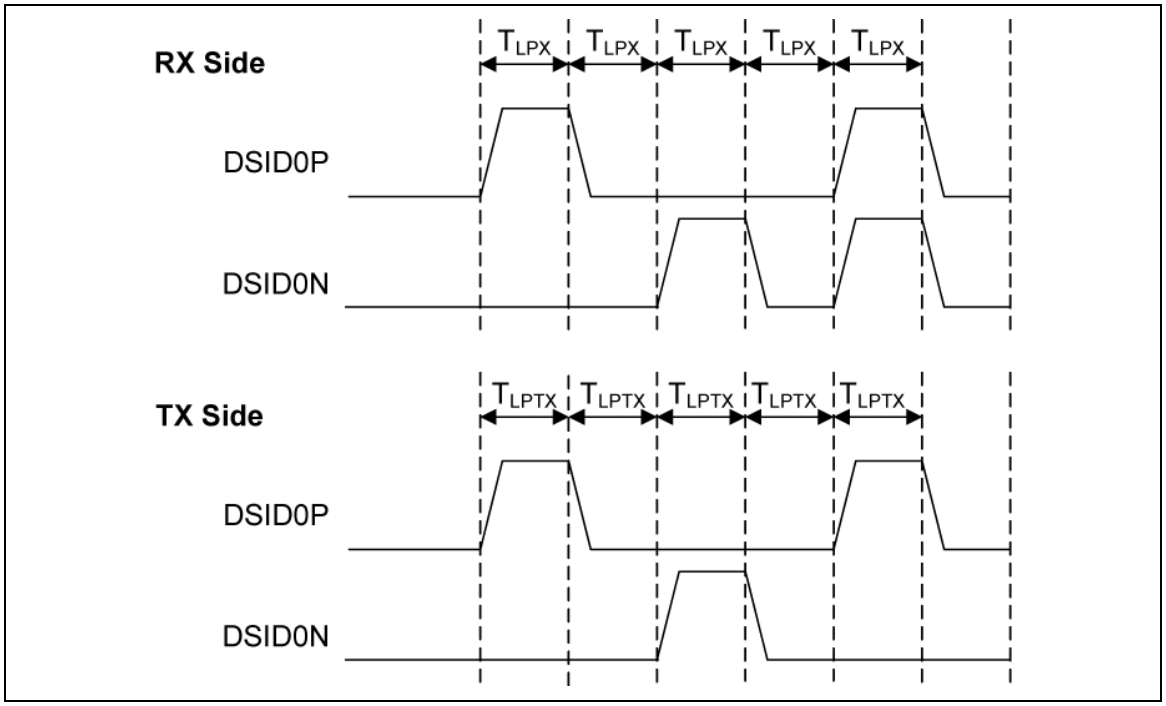


Figure E DSI LP Mode

Revision Record

Rev.	Date	Page No	Contents of Modification
0.03	February 27, 2009		First issue
0.04	April 15, 2009	6	VREG changed to VREG1.
		7	Number of VCOM adjustment bits changed from 13 to 12, description of rewriting data changed, and “Japanese Patent No. 4,226,627” added.
		9	VDDTEST1 connected to the internal logic power supply regulator deleted. (Error correction)
		11	VREG changed to VREG1.
		13	Description of DSI added in function of DPHYVCC.
		15	“step-up circuit 1” and “step-up circuit 2” changed to “step-up circuit.”
		17	“on FPC” in function of DPHYGNDDUM[1:2] and description of patent added, and function and condition of unused pin of VPP1 changed.
		18-38	Pad coordinates (Rev.0.3) defined.
		39	Bump arrangement and alignment mark defined.
		40	Recommended resistance and wiring example revised.
		47	SP changed to Spa, and TEE changed to TER. (Error correction)
		48	“Start of Identification” changed to “Start of Transmission”. (Error correction)
		55,69,73, 77	read_DDB_start (04h) command added.
		57-58	MCS and Data Type List defined.
		67	“*” changed to “0”.
		71	The numbers of parameters defined.
		72	The numbers of parameters defined, and Test Mode (FFh) command deleted.
		78	“000h” changed to “N/A” (set_scroll_start (37h)).
		80-85	Default modes and values of Manufacturer Commands defined.
		88-89	read_DDB_start (04h) command added.
		91,93,95,97,99,101,129,131,133,134	Command name in note changed. (Error correction)
		114	Note added. (Error correction)
		121	“(See Appendix)” deleted from title.
		125	Table, “Memory Contents vs. Display Color”, entirely changed.
		135	Note on dummy read operation, description of test registers added, and a table of test registers changed.
		136	Note on dummy read operation added.
		140	Description of dummy read operation added. (Error correction)
		143	ULMTW0/1[5:0] and LLMTW0/1[5:0] changed to ULMTW0/1[7:0] and LLMTW0/1[7:0].

Rev.	Date	Page No	Contents of Modification
		163	"(DDVDHA and DDVDHB)" added in a table, "DC0n,DC1n" changed to "Normal operation", and "DC0n x 1/2" changed to "Low-speed operation."
		166	Range of the number of lines set by BP and FP changed, and the equation of the total of lines set by BP and FP corrected.
		167	Settings inhibited. (RTNn[5:0]=6'h10-6'h11)
		168	Settings inhibited. (FPn[7:0]=8'h03, and BPn[7:0]=8'h02-8'h03)
		171	Settings inhibited. (VEQW[2:0]=3'h0, and VEM[1:0]=2'h0-2'h2)
		172	Setting inhibited. (SPCW[2:0]=3'h0)
		173-178	Register names and arrangements changed.
		179	Settings changed. (VC2[2:0]=3'h1-3'h5).
		180	Settings added. (VRH[4:0]=5'h1C-5'h1F)
		181	Title corrected to "VCOM Setting.", and the 2nd parameters added, and "0" of the 3rd and 4th parameters changed to "1".
		184	Title changed from "Power Setting for Normal Mode (D2h)" to "Power Setting for Normal/Partial Mode (D2h)."
		185	DC0x settings newly defined. (PTDC=1)
		186	Japanese deleted.
		187	"0" of the 2nd and 4th parameters changed to "1", and description of NVAD[0] added.
		190	"Hi-Z/GND" changed to "Hi-Z/Hi-Z" (C13P/C13M), and "Hi-Z/GND" changed to "VCI/GND" (C31P/C31M).
		198	"(DCDC > DCDC x 0.7)" changed to "VGH > Setting value x 0.7)."
		204	"four grayscales" changed to "five grayscales", and "255" added in description. (Error correction)
		210	Unit of fosc changed from Hz to kHz. (Error correction)
		213-214	Line No. corrected.
		219	DPHYVCC added in the order of inputting power supply.
		220	Register default settings defined.
		222-232	"γ Correction Function" defined.
		233	VCOMH and VCOML numbered.
		234	VCOMH and VCOML added.
		235	VREG changed to VREG1.
		237	"45-bit" changed to "44-bit", "13 bits" changed to "12 bits", and NVM operating conditions defined.
		238	NVM write sequence defined.
		239	Note on the relationship between DDVDHA/B and VCL deleted, and note No. changed.
		242	"TEST1" deleted from a figure, "TEST2" and "TEST4" added in the figure, and connection of VREFC, VDDTEST, TSC, and VPP1 to ground (GND or AGND) corrected.
		244	Table of output voltage range added. (Error correction)
		246	Spec for VCOM output delay time and VCOM waveform added, and

Rev.	Date	Page No	Contents of Modification
			some specs of source driver output delay time and test circuits changed.
		247	tcs, tcsf, twds, twdh, and tr/tf changed.
		250	tSETUP and tHOLD changed. (Unit: ns)
0.05	June 8, 2009	8	IOVCC voltage range changed, and DPHYVCC voltage range (when DSI is not used) added.
		15	“C32P,C32M” changed to “C23P,C23M.” (Error correction)
		39	Chip thickness changed.
		160	NL setting range changed.
		190	VDDPAD changed to VDD. (Error correction)
		237, 240, 243-245, 247	IOVCC voltage range changed.
		238	Parameters of D1h command corrected, ID2 changed to ID1, ID3 changed to ID2, and AD[0] changed to NVAD[0]. (Error correction)
		248	Specs of 8-bit transfer timing added.
		251-252	IOVCC changed to DPHYVCC.
1.00	September 29, 2009	All	“Preliminary Specification” changed to “Specification.”
		8, 39, 234, 240	“[T.B.D.] deleted.
		140	“Write #A= “1 “ #B= “ ↑ “” deleted (error correction).
		142	A restriction added.
		143	“LNCOM” deleted from and a sentence regarding BLC function added in the description of BLCM.
		149	The table of COEFKn changed and a note added.
		154	Note 2 added.
		167	The table of RTNn setting changed.
		186	The setting of DC30 and DC32 (3’h3) changed.
		204	“nine grayscale value” changed to “four grayscale values.”
		233	The note changed.
		240	The specs for current consumption changed.
		241	The specs for DSI current consumption, LCD power supply current, and average output voltage variance changed.
		243	The step-up circuit characteristics defined.
		244	The spec of temperature of the clock characteristics changed.
		246	The liquid crystal driver output characteristics defined.
		247	Min. of twrh changed from 25 to 22.
		251	The figure number defined and min. of tCLKP changed from 5.7 to 6.7.
		252	The figure numbers defined.
		253	Note 5 added.
1.01	December 25, 2009	10,66,94, 127,137	Setting disabled → Setting inhibited

Rev.	Date	Page No	Contents of Modification
		13	External power supply pins, GND, Function: “GND=0V” added.
		39	Chip thickness: (T.B.D.) deleted.
		69	0Bh, Note: 3 deleted.
		85	Note 2 corrected.
		91	Bit D7, D1 and D0: Not defined → Reserved
		93	Bit D0: definitions of “0” and “1” corrected.
		112, 114, 128	Command: 1st parameter, Nth parameter → 1st pixel data, Nth pixel data
		119	set_tear_on: 35h, Description: Notes corrected.
		122	Note on frame memory corrected.
		124	exit_idle_mode: 38h, Description corrected.
		127	Description, table: D6/D2 → D2, D5/D1 → D1, D4/D0 → D0
		130	set_tear_scanline: Description corrected.
		136	Low power mode control: DSTB description corrected.
		138	DFM → DFM[1:0]
		144	THREW0[4:0], THREW1[4:0]: grayscale number 63 → 255
		145	ULMTW0[5:0], ULMTW1[5:0] → ULMTW0[7:0], ULMTW1[7:0] “ULMTW0 is enabled when BLCM=0. ULMTW1 is enabled when BLCM=1.” added.
		146	LLMTW0[5:0], LLMTW1[5:0] → LLMTW0[7:0], LLMTW1[7:0] “LLMTW0 is enabled when BLCM=0. LLMTW1 is enabled when BLCM=1.” added.
		147, 148, 202	Restriction (CGAPW[4:0] ≥ PITCHW[3:0]) added.
		152	PWMWM, PWMON: Note on PWMWN setting deleted.
		153	BDCV[7:0]: BLCON definitions corrected.
		158	Title “Panel Control Command” added.
		160	NL[7:0]: …not affected by the number of NL[6:0] → NL[7:0] SCN[7:0] table: SCN[6:0] → SCN[7:0]
		163	PTS[2*0], PTDC: Table note: CD0h → DC0n
		166	Title “Display Mode and Valid Register” added.
		171	VEM[1:0]: Restrictions (VCI < VCOMH, GND > VCOML) deleted. Note on display quality deleted from under the table.
		172	Source precharge position → Source precharge period
		180	VRH → VRH[4:0]
		182	VCM[6:0] description corrected.
		187	FTT: when NVM write/erase is finished → when NVM write and verify is finished
		188	VERIFLGWR description added. TE output table: VERIFLGER&VERIFLGWR → VERIFLGWR

Rev.	Date	Page No	Contents of Modification
			Table note added.
		189	WCDDB=1: Restriction (ID2[15:0]≠16'hFFFF) added. WCDDB=0: Write WCDB=0 → Write WCDDB=0
		200	(5) Gamma conversion table: TBL[7:0] → TBLx[7:0]
		208	Left/Right interchanging scan (SM=0) added after (1)
		209	Left/Right one-side scan(SM=1) added after (2)
		219	Under the title: Figure description added. Figure, 2nd box from bottom: Power on and display on sequencers operate → Power off and display off sequencers operate
		225, 226	Note: P_B/P_N → P_B/N_B
		226	V0 Level: VREG x 100%, 99%, 98%, 69% → VREG1 x 100%, 99%, 98%, 69% V255 Level: VREG x 2%, 3%, 4%, 33% → VREG1 x 0%, 1%, 2%, 31%
		237	Exit Deep Standby Mode Sequence → Deep Standby Mode Off sequence
		238	NVM Write Sequence: DDB data set (NVM Write Data) rearranged and corrected. VCOM setting register Set (NVM Write Data) corrected. Note in the center-bottom deleted.
		243	Internal reference voltage, Typ.: 2.50 → 2.53
		244	Step-up output voltage, Typ.: 5.6 deleted.
		248	MIPI-DBI Type B, 16bit, Write data hold time, Min.: 25 → 20
		253	Ratio $T_{LPX,}$ Note: 5 added.

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