Rockwell

R6500/1E
Microprocessor Emulator Device

INTRODUCTION

The R6500/1E device provides all the features of the R6500/1 Microcomputer in a ROMless form suitable for use as an advanced microprocessor complete with 16-bit counter and 32 I/O lines, and an address and data bus for 4K of external memory.

To aid in designing R6500/1 microcomputer systems, it may also be used as an emulator device. Device architecture is basically the same as the R6500/1 except that the address, data, and associated control lines are routed off the chip for connection to an external memory.

The functions and operation of the R6500/1E device are identical to the R6500/1 except for minor differences noted in this document. The R6500/1 Product Description (Order No. 212) contains a description of R6500/1 functions and interface signals.

The R6500/1E device is available in both 64-pin ceramic DIP (R6500/1EC) and 64-pin plastic QUIP (R6500/1EQ).

ORDERING INFORMATION

Part Number	Package Type	Frequency Option	Temperature Range
R6500/1EC	Ceramic	1 MHz	0°C to 70°C
R6500/1EAC	Ceramic	2 MHz	0°C to 70°C
R6500/1EQ	Plastic	1 MHz	0°C to 70°C
R6500/1EAQ	Plastic	2 MHz	0°C to 70°C

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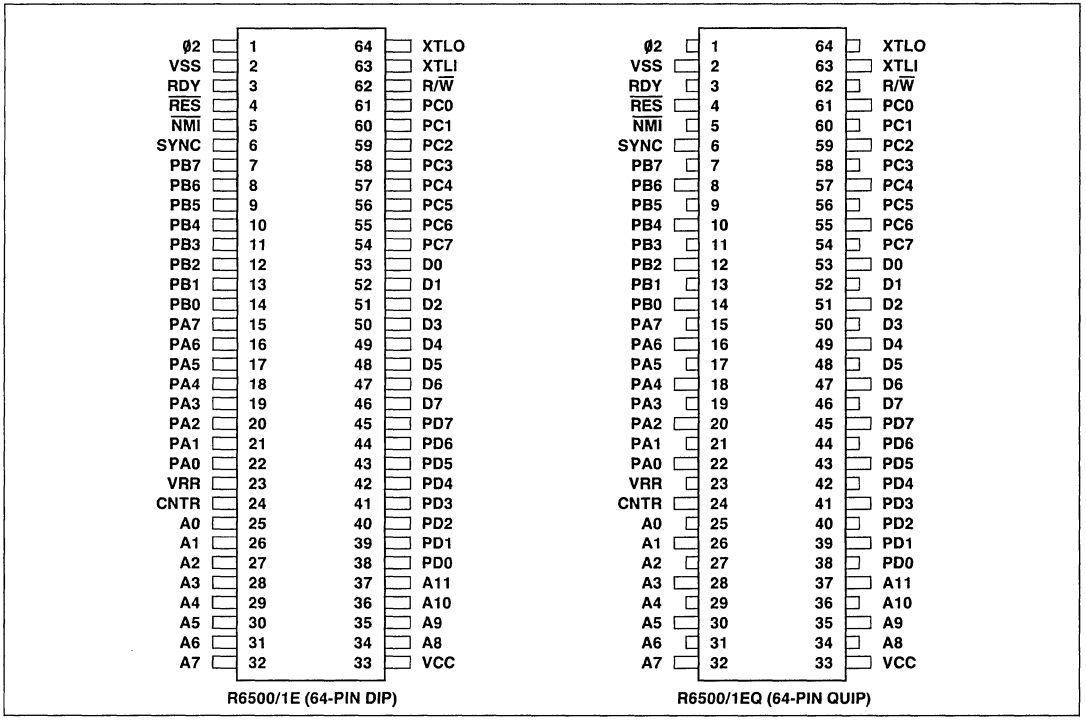


R6500/1E Pin Assignments

INTERFACE SIGNALS

All R6500/1 interface signals are available in the R6500/1E microcomputer plus the additional address (12), data (8), and control (4) lines required to extend the address bus and the data bus external to the device. The R6500/1E emulator unique interface signals are shown in Figure 1 and are described in Table 1. While the pin assignments are different in order to accommodate 64-pin DIP and QUIP packages, the interface characteristics of signals common to the R6500/1 are identical.

SYSTEM ARCHITECTURE

The architecture of the R6500/1E is identical to the R6500/1 with the following differences:

EXTERNAL ADDRESSING

ROM addressing is routed externally in the R6500/1E. The address range for internal ROM in the R6500/1 ($800-$FF9) is available externally for connection to ROM or RAM devices(s).

An additional 1024 bytes ($400-$7FF) are decoded for external memory access. Note that this address range can be used for debugging with the R6500/1E but cannot be used when the object code is transferred to masked ROM in an R6500/1 (which is restricted to $800-$FF9).

A memory map of the R6500/1E is shown in Figure 2.

INTERNAL I/O PORT PULL-UPS

The R6500/1E has the internal I/O and CNTR port pull-up resistors only. The option to delete the pull-up resistors is not available for the R6500/1E.

EARLIER I/O PORT INITIALIZATION

Ports A, B, C, D and the CNTR line in the R6500/1E are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. It is still required, however, that the $\overline{RES}$ line be held low for at least eight Ø2 clock cycles after VCC reaches operating range (Figure 3).

WRITE-ONLY MONITORING

The R6500/1E allows the user to monitor write operations to the internal RAM and I/O by routing those operations externally as well as internally. Read operations are not routed externally.

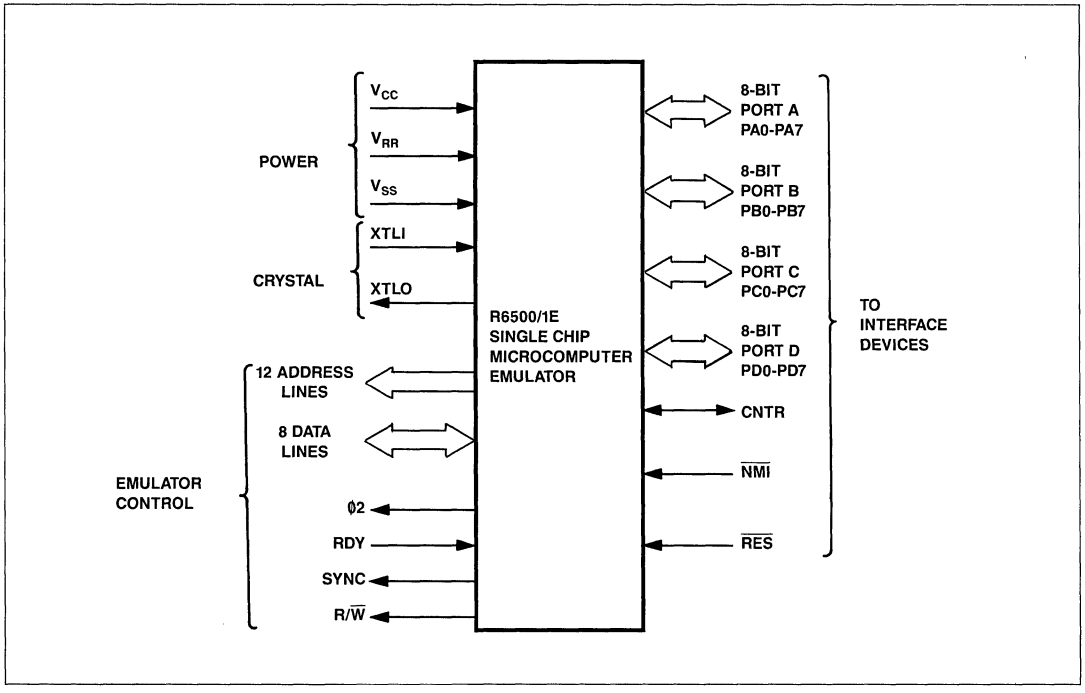


Figure 1. R6500/1E Emulator Interface Diagram

Table 1. R6500/1E Emulator Unique Signals Description

Signal Name	Pin No.	Description
R/$\overline{W}$	62	**Read/Write.** Read/Write allows the CPU to control the direction of data transfer between the R6500/1E Emulator CPU and external memory. This line is high when reading data from memory and is low when writing data to memory.
RDY	3	**Ready.** The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on all cycles except write cycles. A negative transition to the low state during the ϕ2 clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent ϕ2 clock pulse in which the RDY line is low. This feature allows the CPU to interface with memories having slow access times, such as EPROMS used with the R6500/1E during prototype system development.
SYNC	6	**Sync.** The Sync signal is provided to identify cycles in which the CPU is performing OP CODE fetch. SYNC goes high during the ϕ2 clock low pulse of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ2 clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
ϕ2	1	**Phase 2 (ϕ2) clock:** Data transfer takes place only during ϕ2 clock pulse high.
A0-A11	25-37	**Address Bus Lines.** The address bus buffers on the R6500/1E are push/pull type drivers capable of driging at least 130 pF and one standard TTL load. The address bus always contains known data. The addressing tgechnique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O address commands are also placed on these lines.
D0-D7	53-46	**Data Bus Lines.** All transfers of instructions and data between the CPU and memory, I/O, and other interfacing circuitry take place on the bidirectional data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and output buffer, with the output buffer remaining in the floating condition.

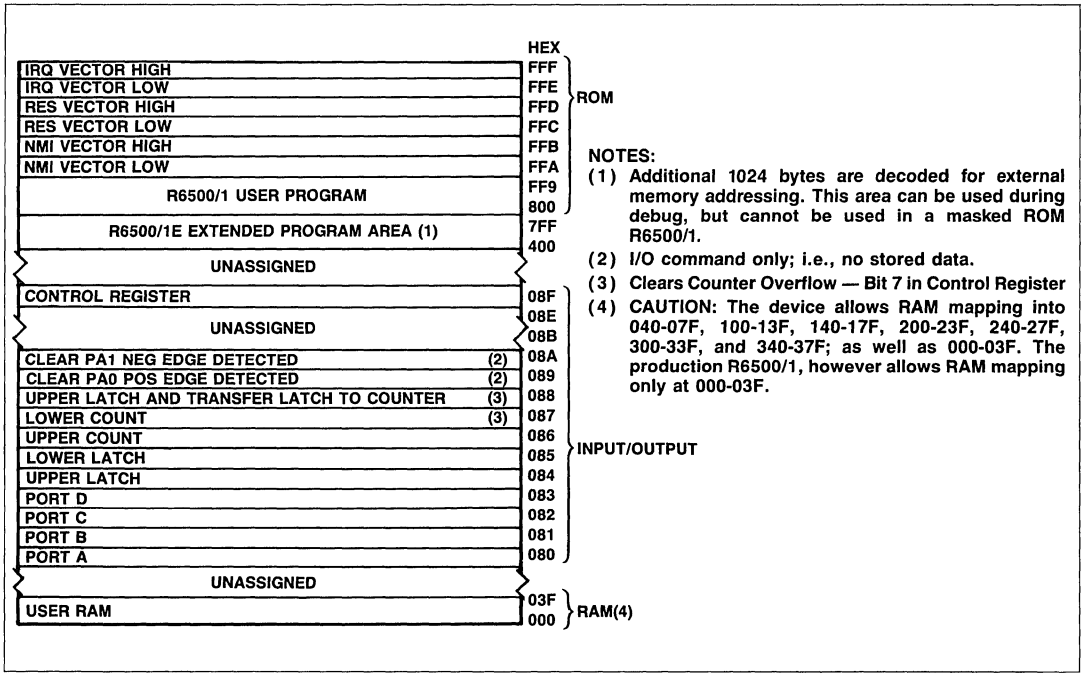


Figure 2. R6500/1E Memory Map

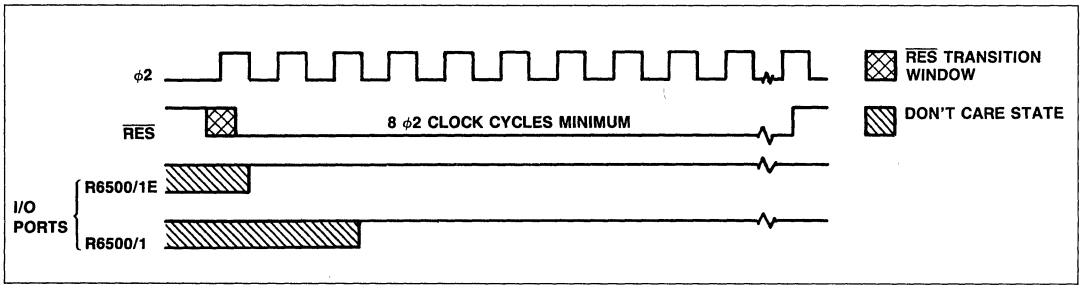


Figure 3. R6500/1E I/O Port Initialization

TYPICAL PROGRAM MEMORY INTERCONNECTIONS

Two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2732 PROMS) are illustrated. Figure 4 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

Figure 5 shows a connection to a 4K 2732 PROM. Only 3K bytes ($400-$FFF) are enabled. The upper 2K bytes correspond the production ROM space ($800-$FFF) in the R6500/1. The extra 1K ($400-$7FF) allows expanded or additional programs to be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum ($800-$FFF) before masking into R6500/1 ROM.

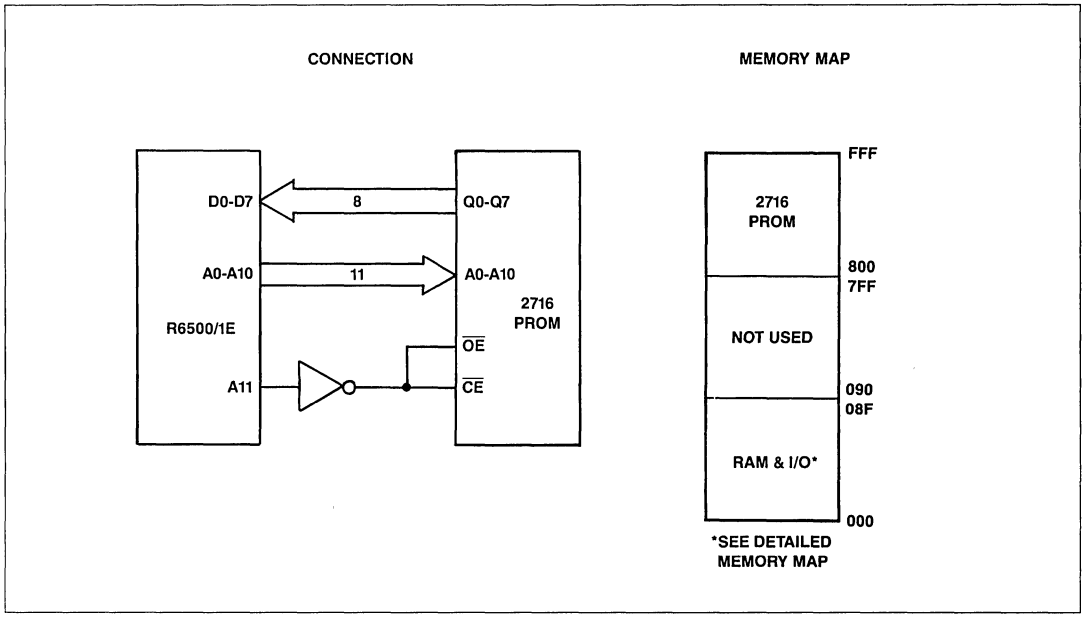


Figure 4. R6500/1E Connected to One 2716 PROM (2K Bytes)

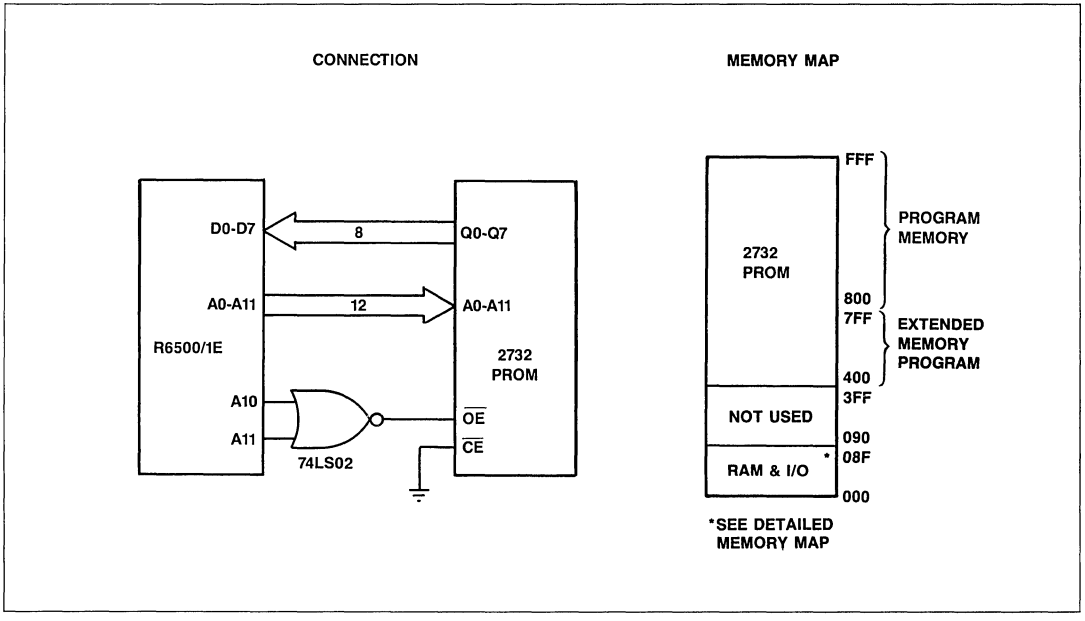


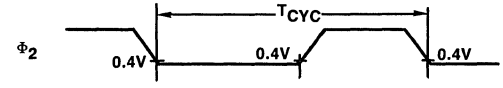
Figure 5. R6500/1E Connected to One 2732 PROM (3K Bytes)

DEVICE TIMING

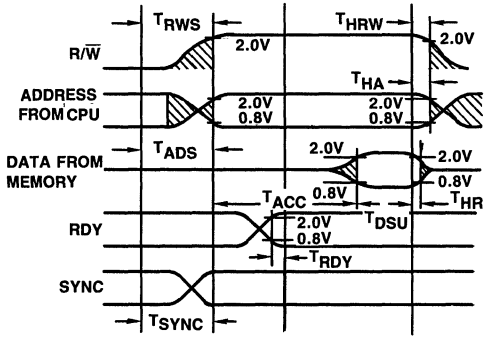
Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/$\overline{W}$ setup time from CPU	T_{RWS}		300		200	ns
Address setup time from CPU	T_{ADS}		300		200	ns
Memory read access time	T_{ACC}		525		225	ns
Data stabilization time	T_{DSU}	150		75		ns
Data hold time — Read	T_{HR}	10		10		ns
Data hold time — Write	T_{HW}	30		30		ns
Data delay time from CPU	T_{MDS}		200		150	ns
RDY setup time	T_{RDY}	100		50		ns
SYNC delay time from CPU	T_{SYNC}		350		175	ns
Address hold time	T_{HA}	30		30		ns
R/$\overline{W}$ hold time	T_{HRW}	30		30		ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

TIMING DIAGRAMS

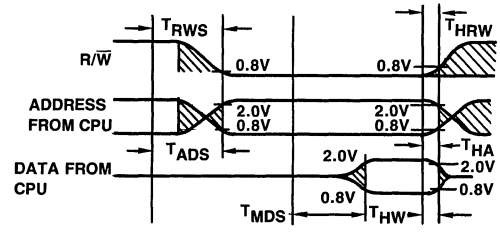
PHASE 2 (Φ2) TIMING REFERENCE



TIMING FOR READING FROM MEMORY



TIMING FOR WRITING TO MEMORY



MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device atr these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

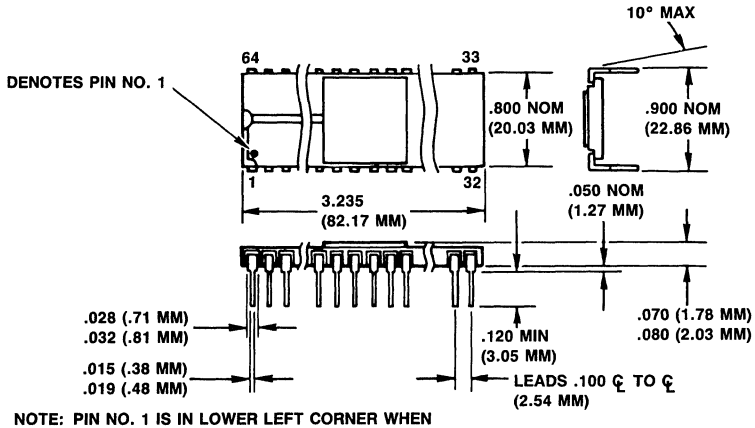
(V_{CC} = 5.0 ±5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	10	—	mA	
Input High Voltage	V_{IH}	+2.4	—	—	Vdc	
Input Low Voltage	V_{IL}	—	—	+0.8	Vdc	
Three-State (Off State) Input Current D0-D7	I_{TSI}	—	—	±10	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OH}	+2.4	—	—	Vdc	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output Low Voltage D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OL}	—	—	+0.6	Vdc	I_{LOAD} = 1.6 μA V_{CC} = 4.75V
Power Dissipation (V_{CC} = 5.5V)	P_D	—	750	1200	μW	V_{CC} = 5.5V
Input Capacitance RDY, PA, PB, PC, PD, CNTR D0-D7 XTLI, XTLO	C_{IN}	 — — —	 — — —	 10 15 50	pF	 T_A = 25°C V_{IN} = 0 f = 1 MHz
Output Capacitance A0-A11, R/$\overline{W}$, SYNC ϕ2	 C_{OUT} $C_{ϕ2}$	 — —	 —	 12 80	 pF	
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm	

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

PACKAGE DIMENSIONS

R6500/1EC 64-PIN DIP CERAMIC



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

R6500/1EQ 64-PIN QUIP PLASTIC