Rockwell

R6500/1EB and R6500/1EAB Backpack Emulator

INTRODUCTION

The Rockwell R6500/1EB and R6500/1EAB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/1 one-chip microcomputer. Like the R6500/1, the backpack device is totally upward/downward compatible with all members of the R6500/1 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, reprogrammed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/1 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/1, with some minor differences (described herein). The R6500/1 Microcomputer Product Description (Order No. 212) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/1 provides 2K bytes of read-only memory, the R6500/1EB will address 3K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

FEATURES

- PROM version of the R6500/1
- Completely pin compatible with R6500/1 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/1
- Accepts 5-volt, 24-pin industry-standard EPROMs —4K memories—2732, 2732A (3K bytes addressable)
- Use as prototyping tool or for low volume production
- 3K bytes of memory capacity (4K memories)
- 64 × 8 static RAM
- Separate power pin for RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16-bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 5 interrupts (reset, non-maskable, two external edge sensitive, counter)
- Crystal or external time base
- Single +5V power supply

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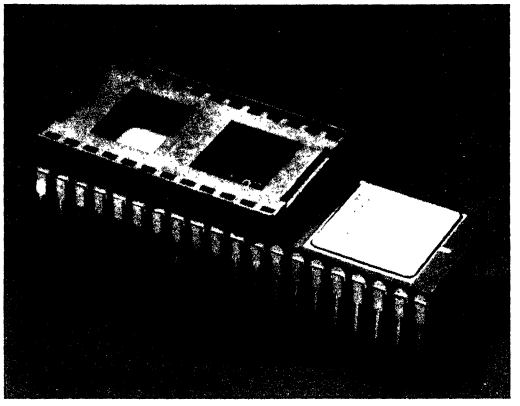
ORDERING INFORMATION

BACKPACK EMULATOR

Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R6500/1EB3	3K x 8	2732	0°C to 70°C 1 MHz
R6500/1EAB3	3K x 8	2732A (250 ns)	0°C to 70°C 2 MHz

SUPPORT PRODUCTS

Part Number	Description
RDC-3101	Low Cost Emulator (LCE)
RDC-3030	PROM Programmer Module
RDC-369	1- or 2-MHz R6500/1 Personality Module



R6500/1EB-R6500/1EAB Backpack Emulator

CONFIGURATION

The external memory must always occupy the upper 2K of available memory (addresses 800 through FFF) for implementation of interrupt vectors. See Memory Map. The Backpack Emulator provides a read block to the external memory where internal RAM or I/O are located in the same addresses as that occupied by external memory.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock. The R6500/1EB and R6500/1EAB divide the input clock by two regardless of the source.

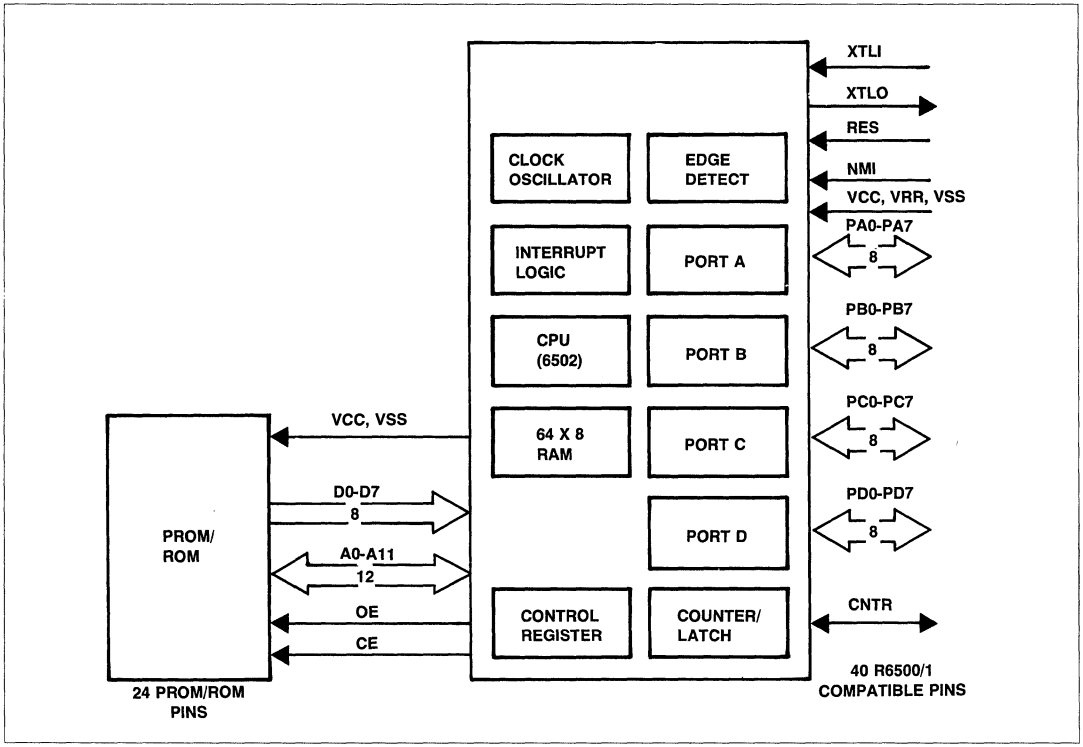
I/O PORT PULLUPS

The emulator devices have internal I/O port pullup resistors.

PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/1.

The Low Cost Emulator (LCE) with R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation. With the optional PROM Programmer, the LCE can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 2K ROM of the R6500/1.



R6500/1EB Interface Diagram

DETAILED MEMORY MAP

			HEX
PROM	IRQ VECTOR HIGH		FFF
	IRQ VECTOR LOW		FFE
	RES VECTOR HIGH		FFD
	RES VECTOR LOW		FFC
	NMI VECTOR HIGH		FFB
	NMI VECTOR LOW		FFA
	R6500/1 USER PROGRAM		FF9 400
PROM	R6500/1EB EXTENDED PROGRAM AREA (1)		3FF 400
NOT USED	UNASSIGNED		
I/O	CONTROL REGISTER		08F
	UNASSIGNED		08E 08B
	CLEAR PA1 NEG EDGE DETECTED	(2)	08A
	CLEAR PA0 POS EDGE DETECTED	(2)	089
	UPPER LATCH AND TRANSFER LATCH TO COUNTER	(3)	088
	LOWER COUNT	(3)	087
	UPPER COUNT		086
	LOWER LATCH		085
	UPPER LATCH		084
	PORT D		083
	PORT C		082
	PORT B		081
	PORT A		080
NOT USED	UNASSIGNED		03F
RAM	USER RAM		000

NOTES

(1) Additional 1024 bytes are decoded for external memory addressing by the Backpack Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1.

(2) I/O command only; i.e., no stored data.

(3) Clears Counter Overflow—Bit 7 in Control Register

(4) CAUTION: The device allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

RAM MAPPING

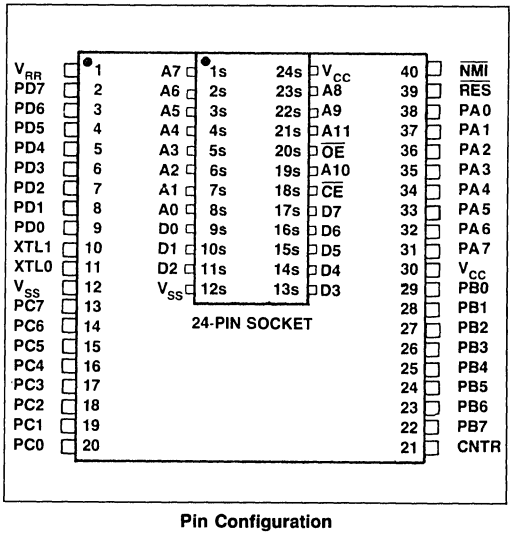
The Backpack Emulator allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F and 340-37F, as well as 000-03F. The production R6500/1, however, allows RAM mapping only at 000-03F. This means that a write to location 40, for example, will write to location 0 in the Backpack Emulator, and to invalid RAM in the R6500/1 production part.

I/O PORT INITIALIZATION

Ports A, B, C, and D and the CNTR line in the Backpack Emulator are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. The $\overline{RES}$ line to the device must, however, still be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range. See timing diagram.

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0-D7	9S-11S, 13S-17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0-A9	1S-8S, 23S, 24S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
A10	19S	Address Bus Line 10. This address line has the same characteristics and functions as Lines A0-A9.
$\overline{CE}$	18S	$\overline{CE}$ is active when the address is 400-FFF. This line can drive one TTL load.
$\overline{OE}$	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by the R/$\overline{W}$ signal from the CPU and then inverted by a standard TTL inverter, to form $\overline{OE}$.
V_{CC}	24S	Main Power Supply $5V. This pin is tied directly to pin 30 (V_{CC}).
A11	21S	Address Bus Line II. This pin is tied to A11. During backup power, power is supplied only to the RAM memory, and not to the PROMs.
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 12 (V_{SS}).

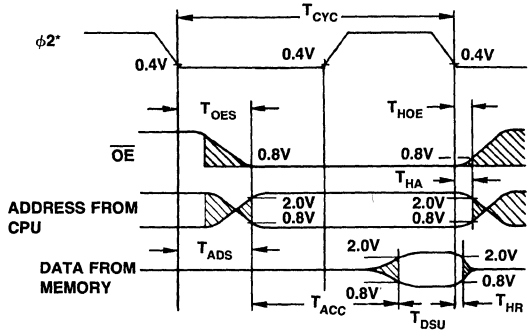


Pin Configuration

READ TIMING CHARACTERISTICS

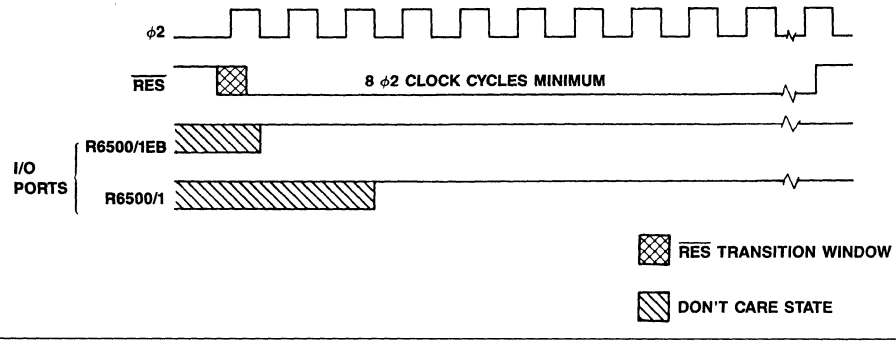
Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{OE}$ setup time from CPU	T_{OES}	—	300	—	150	ns
Address setup time from CPU	T_{ADS}	—	300	—	150	ns
Memory read access time	T_{ACC}	—	525	—	250	ns
Data stabilization time	T_{DSU}	150	—	100	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{OE}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

READ TIMING WAVEFORMS



*ϕ2 IS SHOWN FOR REFERENCE ONLY AND IS NOT AVAILABLE EXTERNAL TO THE DEVICE.

I/O PORT INITIALIZATION TIMING



MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input High Voltage D0–D7	V_{IH}	+2.4	—	—	V	
Input Low Voltage D0–D7	V_{IL}	—	—	+0.8	V	
Input Leakage Current (Three-State Off) D0–D7	I_{IN}	—	—	±10.0	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage (Except XTLO) D0–D7, A0–A11, $\overline{OE}$	V_{OH}	+2.4	—	—	V	I_{LOAD} = −100 μA V_{SS} = 4.75V
Output Low Voltage D0–D7, A0–A11, $\overline{OE}$	V_{OL}	—	—	+0.6	V	I_{LOAD} = 1.6 mA V_{SS} = 4.75V
I/O Port Pull-Up Resistance	R_L	3.0	6.0	11.5	Kohm	
Input Capacitance D0–D7	C_{IN}	—	—	15	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off) A0–A11	C_{OUT}	—	—	12	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Less EPROM)	P_D	—	800	1300	mW	T_A = 0°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

PACKAGE DIMENSIONS

40-PIN BACKPACK