Rockwell

R6518
One-Chip Microprocessor

INTRODUCTION

FEATURES

- Enhanced 6502 CPU
  - — Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - — Decimal and binary arithmetic modes
  - — 13 addressing modes
  - — True indexing
- 192-byte static RAM
- 16 TTL-compatible I/O lines
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - — Pulse width measurement
  - — Asymmetrical pulse generation
  - — Pulse generation
  - — Interval timer
  - — Event counter
  - — Retriggerable interval timer
- Serial port
  - — Full-duplex asynchronous operation mode
  - — Selectable 5- to 8-bit characters
  - — Wake-up feature
  - — Synchronous shift register mode
  - — Standard programmable bit rates, programmable up to 62.5K bits/sec @ 1 MHz
- Ten interrupts
  - — Four edge-sensitive lines; two positive, two negative
  - — Reset
  - — Non-maskable
  - — Two counter underflows
  - — Serial data received
  - — Serial data transmitted
- 16K bytes of external memory addressing
- Flexible clock circuitry
  - — 2 MHz or 1 MHz internal operation
  - — Internal clock with external 2 MHz to 4 MHz series resonant XTAL at two times internal frequency
  - — External clock input divided by one or two
- 1 μs minimum instruction execution time @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 12 mW stand-by power for 32 bytes of the 192-byte RAM
- 40-pin DIP
- 44-pin PLCC

SUMMARY

The Rockwell R6518 one-chip microprocessor is a complete 8-bit microcomputer on a single VLSI chip with the exception of external user-provided application ROM. The R6518 interfaces with up to 16K bytes of external memory via a multiplexed address/data bus.

The R6518 consists of an enhanced R6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 16 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and 16K of external address space.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make this device a leading candidate for microprocessor applications.

Rockwell supports development of R6500/* single-chip microcomputer applications with the Rockwell Design Center Low Cost Emulator (LCE) and R6500/* Personality Set. Program assembly can be performed on any user-provided computer using an assembler generating R6500/* machine code. The machine code can then be downloaded via an RS-232-C serial channel to the LCE for program debugging and in-circuit emulation. Refer to the RDC-3101/2 LCE and RDC-3XX R6500/* Personality Set data sheets, Order No.s RDC17 and RDC06, respectively, for detailed information.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order No. 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order No. 202).

CUSTOMER OPTIONS

The R6518 is available in 1 MHz (no suffix letter) or 2 MHz (A suffix) versions.

ORDERING INFORMATION

Part Number:
R6518

Temperature Range (T_L to T_H):
Blank = 0°C to +70°C
E = −40°C to +85°C

Package
C = 40-Pin Ceramic DIP
P = 40-Pin Plastic DIP
J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

Frequency
1 = 1 MHz
A = 2 MHz

INTERFACE

This section presents the interface requirements for the R6518 single-chip microprocessor. Figure 1 is the Interface Diagram, Figure 2 shows the pin configurations and Table 1 describes the function of each pin. A detailed block diagram of the device and its internal function is illustrated in Figure 3. Package dimensions are illustrated in the last section.

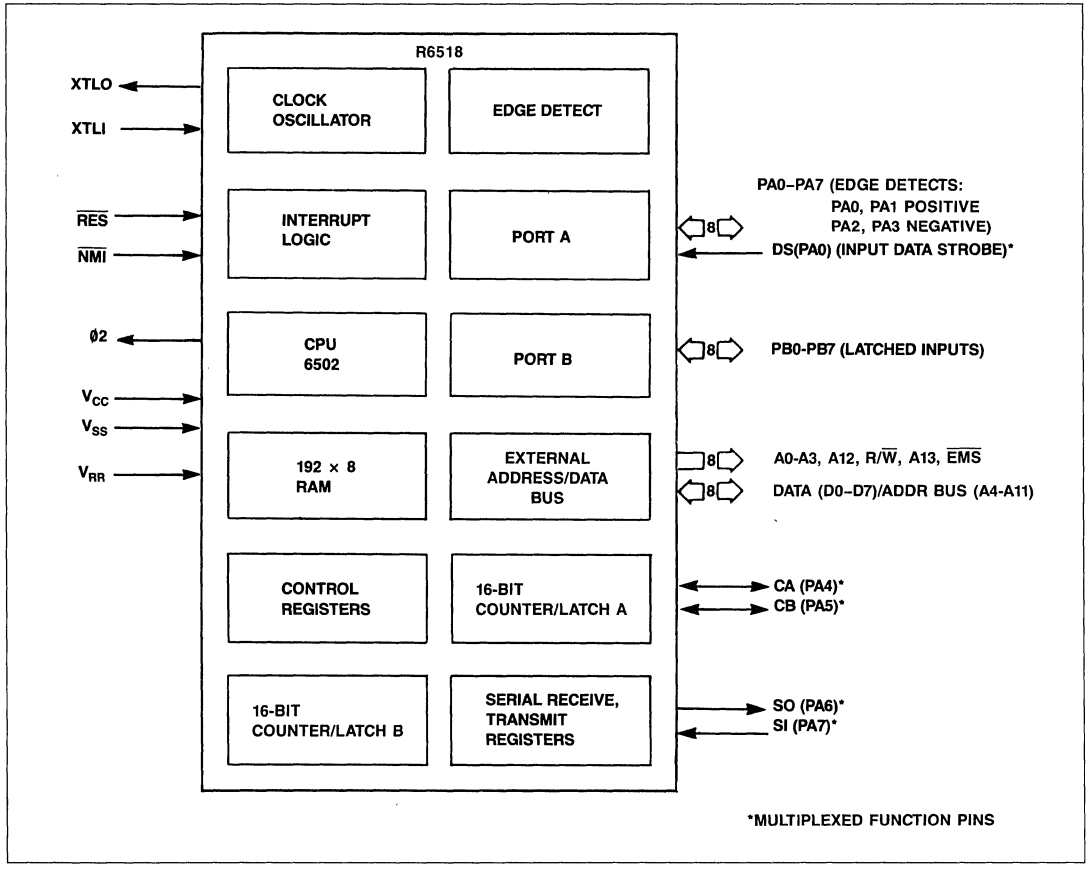
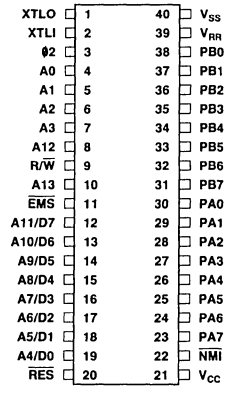
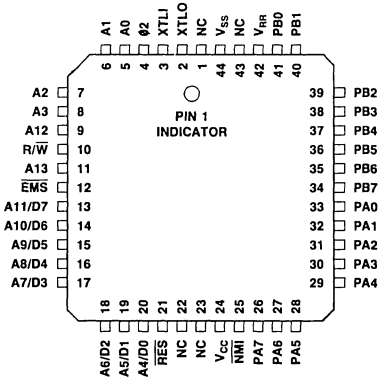


Figure 1. Interface Diagram



40-PIN DIP



44-PIN PLCC

Figure 2. R6518 Pin Assignments

Table 1. Pin Description

Signal Name	Pin Number DIP	Pin Number PLCC	Description
V_{CC}	21	24	Main power supply +5V
V_{RR}	39	42	Separate power pin for RAM. In the event that V_{CC} power is lost, this power retains 32 bytes of RAM Data.
V_{SS}	40	44	Signal and power ground (0V)
XTLI	2	3	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 clock if XTLO is floated.
XTLO	1	2	Crystal output from internal clock oscillator.
$\overline{RES}$	20	21	The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator is stabilized.
ϕ2	3	4	Clock signal output at internal frequency.
$\overline{NMI}$	22	25	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7	30-23 38-31	33-26 41-34	Two 8-bit ports used for either input/output. Each line of Ports A and B consists of an active transistor to V_{SS} and a passive pull-up to V_{CC}.
A0-A3, A12, R/$\overline{W}$ A13, & $\overline{EMS}$	4-11	5-12	The address and timing pins have an active transistor to V_{SS} and a passive pull-up to V_{CC}.
A4-A11/D0-D7	19-12	20-13	These multiplexed address/data pins have active pull-up and pull-down transistors.
NC	—	1,22 23,43	No connection. These pins should be left open.

SYSTEM ARCHITECTURE

This section provides a functional description of the R6518. Functionally it consists of a CPU, RAM memory, two 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

CPU LOGIC

The internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit index registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

ACCUMULATOR

The Accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the Accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

PROGRAM COUNTER

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

TIMING CONTROL

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

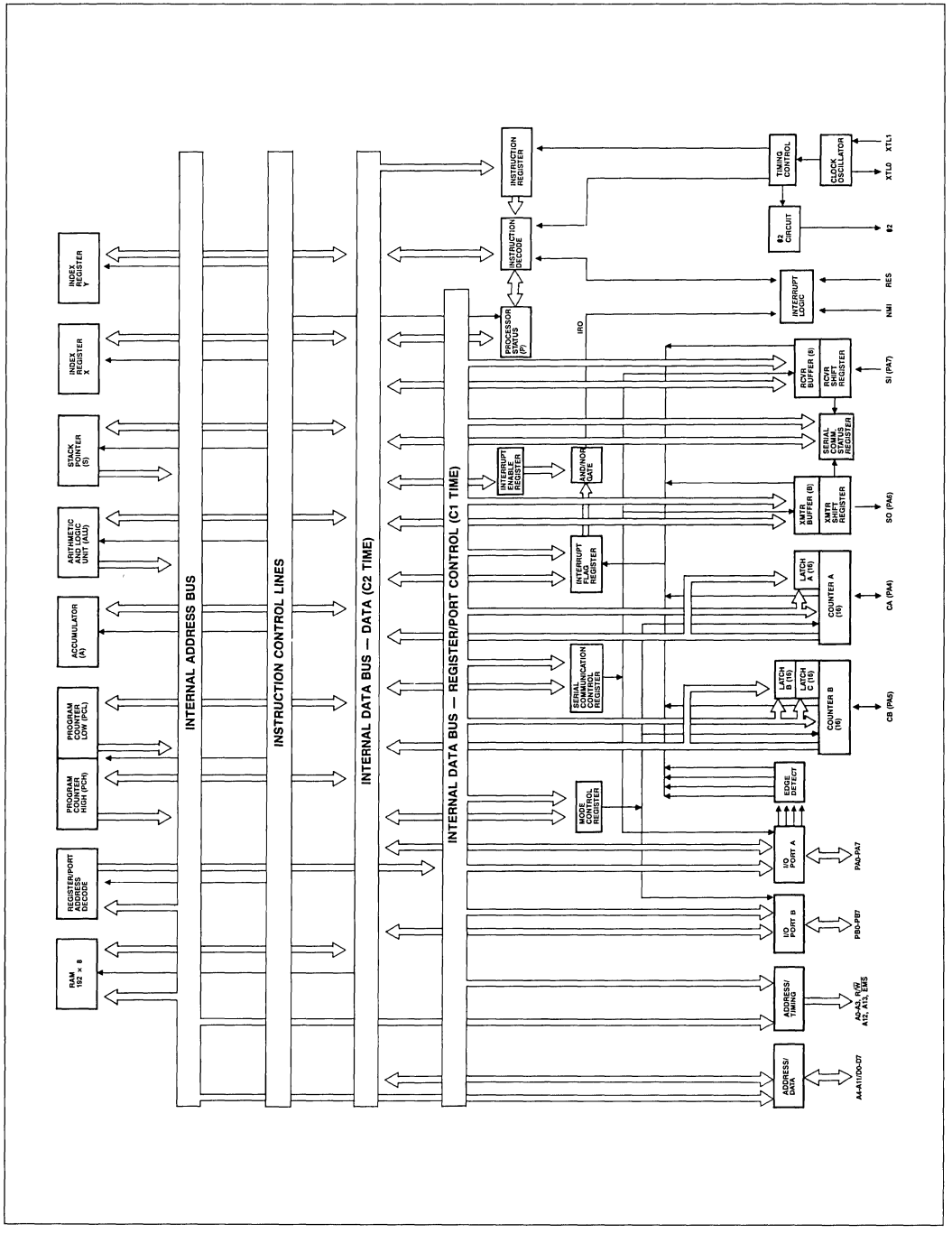


Figure 3. System Block Diagram

INTERRUPT LOGIC

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

The R6518 requires that 3-byte JMP instructions for $\overline{NMI}$, $\overline{RES}$ and $\overline{IRQ}$ be programmed in user-provided external ROM at hex locations 3FF7, 3FFA and 3FFD, respectively. These instructions must jump to the first instruction of the respective reset or interrupt handler routine. Terminate the interrupt handler routines as normal with an RTI. See Power-On Reset for details of $\overline{RES}$ internal initialization.

NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the device to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to either I/O port, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

SET MEMORY BIT (SMB m, ADDR.)

This instruction sets to "1" one of the 8 bits specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

RESET MEMORY BIT (RMB m, ADDR.)

This instruction is the same in operation and format as the SMB instruction except that a reset to "0" of the bit results.

BRANCH ON BIT SET RELATIVE (BBS m, ADDR, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

BRANCH ON BIT RESET RELATIVE (BBR m, ADDR, DEST)

This instruction is the same in operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

READ ONLY MEMORY (ROM)

This device has no internal application ROM. Up to 16K of external memory can be attached via the 16 address/data and timing pins.

RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R6518 provides a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 4 shows typical waveforms.

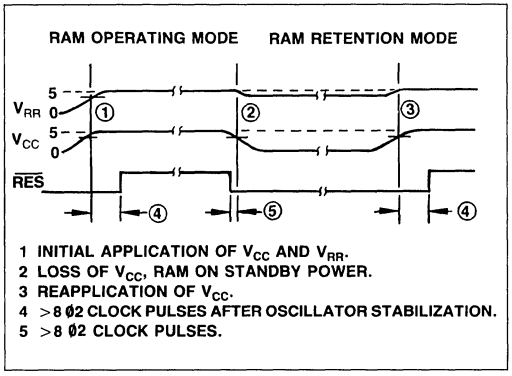


Figure 4. Data Retention Timing

CLOCK OSCILLATOR

A reference frequency can be generated with the on-chip oscillator using an external crystal. The oscillator reference frequency passes through an internal countdown network (divide by 2) to obtain the internal operating frequency (see Figure 5a). The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 5.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27\ \text{pF}$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C_L is in pF; and R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF}$$
(use standard value of 18 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 5b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

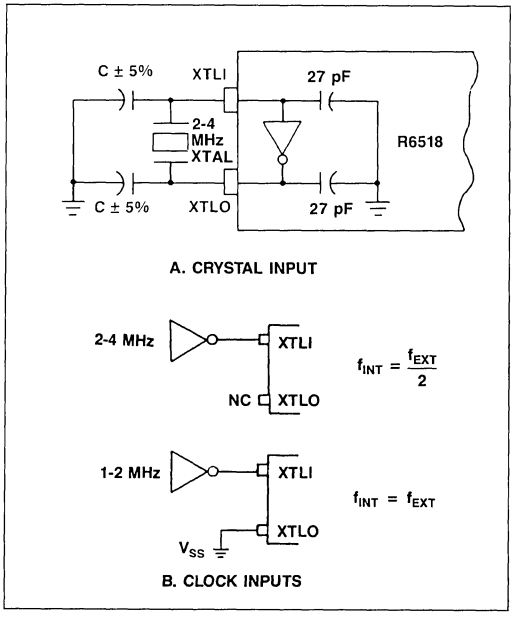


Figure 5. Clock Oscillator Input Options

MODE CONTROL REGISTER (MCR)

The Mode Control Register contains a control bit for Port B and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. MCR bits 7, 6, 5 must remain 1s in order for external memory referencing to be enabled. The Mode Control Register bit assignment is shown in Figure 6.

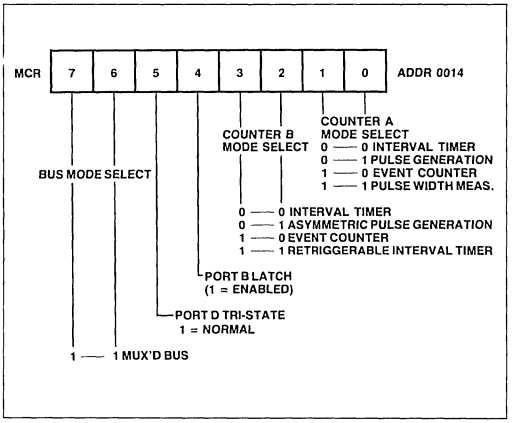


Figure 6. Mode Control Register

The use of Counter A Mode Select is shown in Section "Counter A".

The use of Counter B Mode Select is shown in Section "Counter B".

The use of Port B Latch Enable is shown in Section "Port B (PB)".

INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initialized by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 7 and the functions of each bit are explained in Table 2.

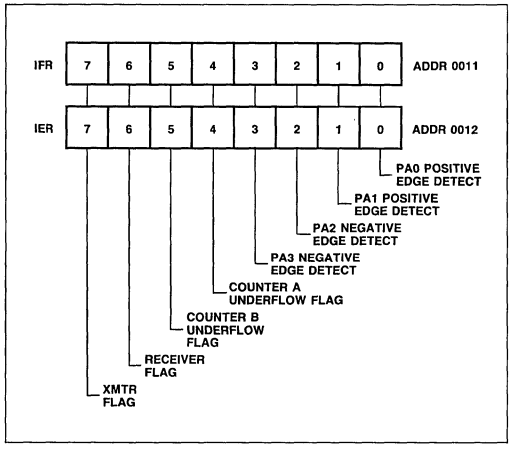


Figure 7. Interrupt Enable and Flag Registers

PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 8 contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

CARRY BIT (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

Table 2. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR0-3) are cleared or by $\overline{RES}$.
IRF 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR6 is set to a 1 while SCSR5 is a 0 or SCSR7 is set to a 1. Cleared when the Transmitter Status bits (SCSR6 & 7) are cleared or by $\overline{RES}$.

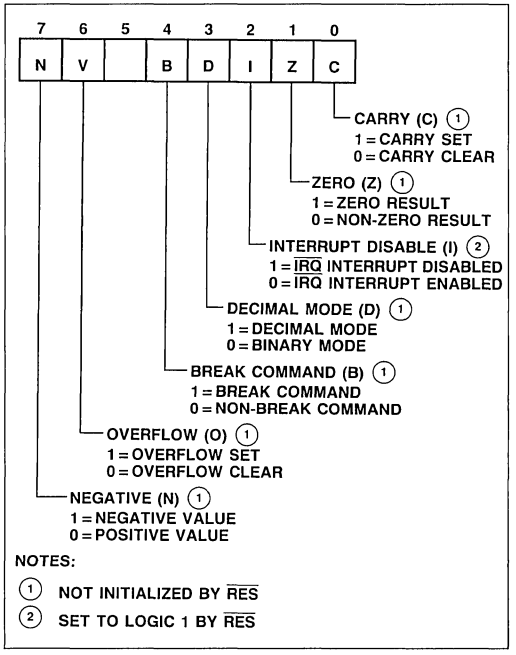


Figure 8. Processor Status Register

ZERO BIT (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6500 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

INTERRUPT DISABLE BIT (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request ($\overline{IRQ}$). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$), $\overline{IRQ}$, or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit is set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

DECIMAL MODE BIT (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

BREAK BIT (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

OVERFLOW BIT (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$).

This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

NEGATIVE BIT (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, AND TYA.

PARALLEL INPUT/OUTPUT PORTS

The R6518 has 16 I/O lines grouped into two 8-bit ports (PA, PB). Ports A and B may be used either for input or output individually or in groups of any combination.

Multifunction I/O's in Port A are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of 3K ≤ Rpu ≤ 12K ohm) are provided on all port pins.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 3. I/O Port Timing is shown on page 29.

Table 3. I/O Port Addresses

Port	Address
A	0000
B	0001

INPUTS

Inputs for Ports A and B are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces both I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Ready/Modify/Write instructions can be used to modify the operation of PA and PB. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

OUTPUTS

Outputs for Ports A and B are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the phase 2 (Ø2) clock rate. Edge detection timing is shown on page 29.

PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 5 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided through PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown on page 29.

Table 5. Port B Control & Usage

Pin Name	I/O Mode		Latch Mode	
	MCR4 = 0		MCR4 = 1 (2)	
	Signal		Signal	
	Name	Type (1)	Name	Type
PB0	PB0	I/O	PB0	INPUT
PB1	PB1	I/O	PB1	INPUT
PB2	PB2	I/O	PB2	INPUT
PB3	PB3	I/O	PB3	INPUT
PB4	PB4	I/O	PB4	INPUT
PB5	PB5	I/O	PB5	INPUT
PB6	PB6	I/O	PB6	INPUT
PB7	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down
(2) Input data is stored in port B latch by PA0 pulse

Table 4. Port A Control & Usage

	PA0 I/O		PORT B LATCH MODE			
	MCR4 = 0		MCR4 = 1			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
PA0 (2)	PA0	I/O	PORT B LATCH STROBE	INPUT (1)		
PA1 (2)	PA1-PA3 I/O					
	SIGNAL					
PA2 (3)	NAME	TYPE				
PA3 (3)	PA1 PA2 PA3	I/O I/O I/O				
PA4	PA4 I/O		COUNTER A I/O			
	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4) (5)		MCR0 = 1 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0 (4)		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1 (4)			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		
PA5	PA5 I/O		COUNTER B I/O			
	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)
PA6	PA6 I/O		SERIAL I/O XMTR OUTPUT			
	SCCR7 = 0		SCCR7 = 1			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	PA6	I/O	XMTR	OUTPUT		
PA7	PA7 I/O		SERIAL I/O RCVR INPUT			
	SCCR6 = 0		SCCR6 = 1			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	PA7	I/O	RCVR	INPUT (1)		

Notes:
(1) Hardware Buffer Float
(2) Positive Edge Detect
(3) Negative Edge Detect
(4) RCVR S/R Mode = 1 when SCCR6 • $\overline{SCCR5}$ • SCCR4 = 1
(5) For the following mode combinations PA4 is available as an input only pin:
$\overline{SCCR7}$•SCCR6•SCCR5.MCR1
+ $\overline{SCCR7}$•SCCR6•$\overline{SCCR4}$•MCR1
+ SCCR7•$\overline{SCCR6}$•$\overline{SCCR5}$
+ SCCR7•$\overline{SCCR5}$•$\overline{SCCR4}$•

SERIAL INPUT/OUTPUT CHANNEL

The device provides a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 9. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ Ø2 = 1 MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

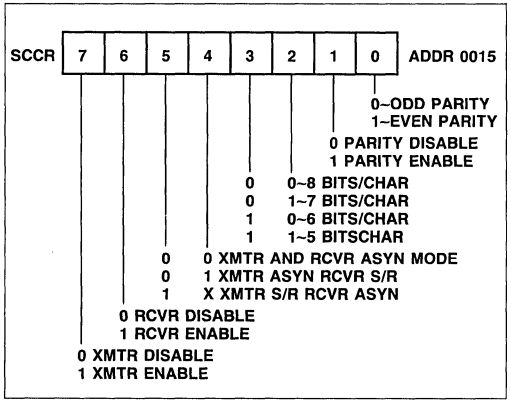


Figure 9. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Section "Counter A," Table 6 for hexadecimal values to represent the desired data rate.

TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5-, 6-, 7-, or 8-bits of data. The nine data modes are in Figure 10. When parity is disabled, the 5-, 6-, 7- or 8-bits of data are terminated with two stop bits.

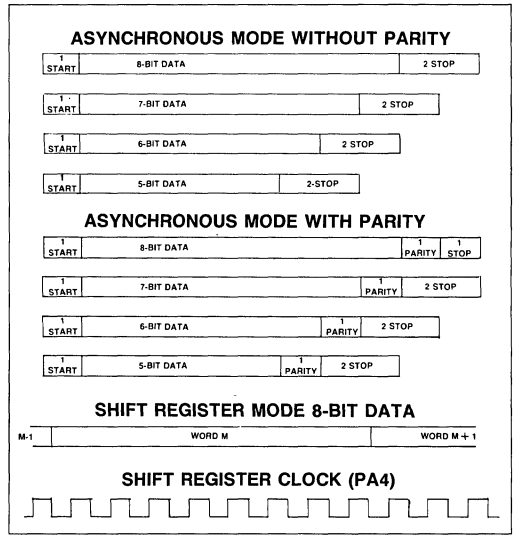


Figure 10. Transmitter Data Modes

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter under-runs in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6\ (\overline{SCSR5} + SCSR7)$$

RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR6 is set to a "1". In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to Figure 10 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the appropriate center of each incoming bit. Refer to Figure 11 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

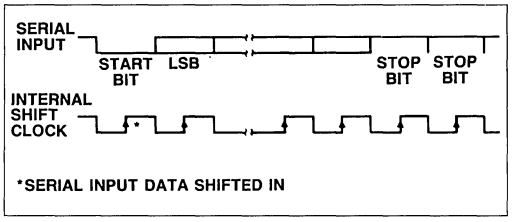


Figure 11. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 12 for S/R Mode Timing.

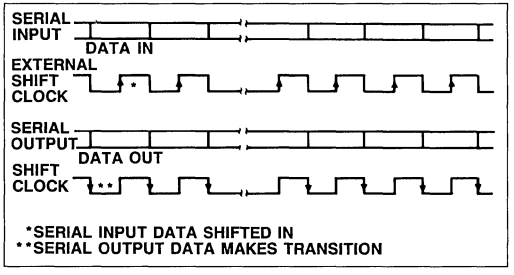


Figure 12. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 13. SCSR bit assignments and functions are:

SCSR0: ***Receiver Data Register Full***—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR6 = 0. The SCSR0 bit will not be set to a logic 1 if the received data contains an error condition, instead, a corresponding error bit will be set to a logic 1.

SCSR1: ***Over-Run Error***—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$.

SCSR2: ***Parity Error***—Set to a logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR3: ***Framing Error***—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$. (ASYN Mode only).

SCSR4: ***Wake-Up***—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1s. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR5: ***End of Transmission***—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Data Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR6: ***Transmitter Data Register Empty***—Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR7: ***Transmitter Under-Run***—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{RES}$.

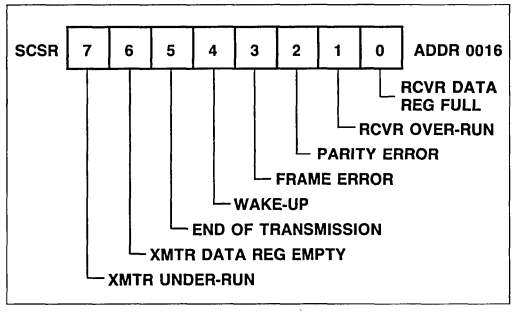


Figure 13. SCSR Bit Allocation

WAKE-UP FEATURE

In multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of ten consecutive 1s which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

COUNTER/TIMERS

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4).

COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (1FR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Select bits in the Mode Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

INTERVAL TIMER

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1 μs to 65.535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.7675 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer mode is shown in Figure 14.

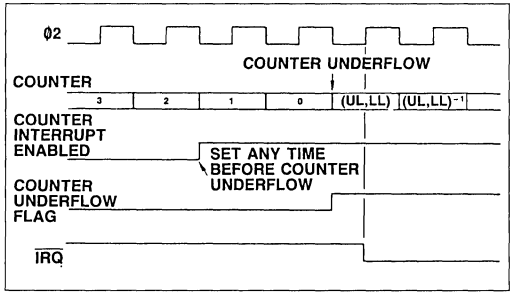


Figure 14. Interval Timer Timing Diagram

PULSE GENERATION MODE

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output wave form is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

EVENT COUNTER MODE

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the Ø2 clock rate (Figure 15).

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

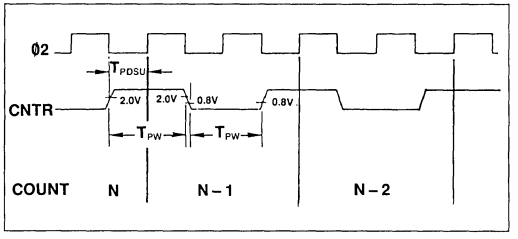


Figure 15. Event Counter Mode Timing

PULSE WIDTH MEASUREMENT MODE

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the Ø2 clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4 (Figure 16).

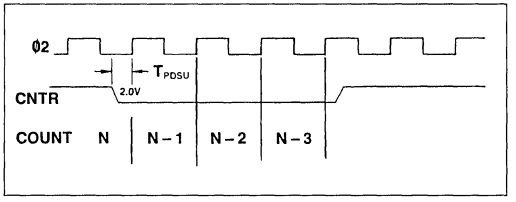


Figure 16. Pulse Width Measurement Timing

SERIAL I/O DATA RATE GENERATION

Counter A also provdes clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4).

Table 6 identifies the values to be loaded in Counter A for selecting standard data rates with a Ø2 clock rate of 1 MHz and 2 MHz. Although Table 6 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{Ø2}{16 \times bps} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent
Ø2 = the clock frequency (1 MHz or 2 MHz)
bps = the desired data rate.

NOTE

In Table 6 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6 for those baud rates which fall outside this limit.

Table 6. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed to Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either ∅2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer Mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

RETRIGGERABLE INTERVAL TIMER MODE

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 17 illustrates the operation of this timer mode.

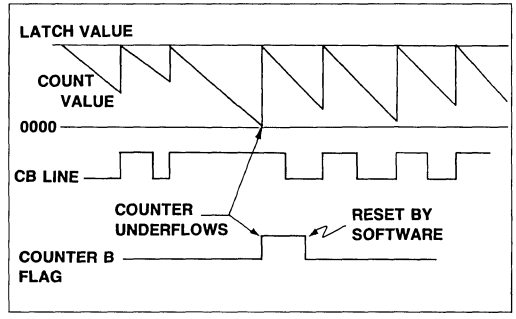


Figure 17. Counter B Retriggerable Interval Timer Mode

ASYMMETRICAL PULSE GENERATION MODE

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 18.
3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

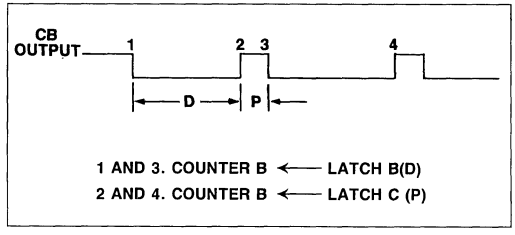


Figure 18. Counter B Pulse Generation

POWER-ON/INITIALIZATION CONSIDERATIONS

POWER-ON TIMING

After applications of V_{CC} and V_{RR} power to the device, $\overline{RES}$ must be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at Ø2 (pin 3). Figure 19 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

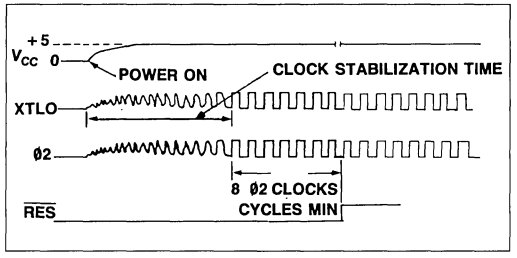


Figure 19. Power Turn-on Timing Detail

POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the device to set the Interrupt Mask Bit — bit 2 of the Processor Status Register. Both I/O ports (PA, PB) will be forced to the high (logic 1) state. An internal initialization sequence lasting 16 clock cycles is then performed which sets bits 5–7 of the Mode Control Register to logic 1, thus enabling external user memory (Multiplexed Bus Mode). The remaining bits of the Control Register will be cleared to logic 0 causing the Interval Timers counter mode (mode 00) to be selected and causing all interrupt enabled bits to be reset.

RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7.

Table 7. $\overline{RES}$ Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
Registers								
Processor Status	—	—	—	—	0	1	—	—
Mode Control (MCR)	1	1	1	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	0	0	0	0	0	0	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
Ports								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power-on situation) an initialization subroutine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrupts

A typical initialization subroutine could be as follows:

```
LDX     Load stack pointer starting address into X Register
TXS     Transfer X Register value to Stack Pointer
CLD     Clear Decimal Mode
SEC     Set Carry Flag
. . . .  Set-up Mode Control and
. . . .  special function
. . . .  registers as required
CLI     Clear Interrupts
```

ENHANCED R6502 INSTRUCTION SET

The following table contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Order No. 202. The four instructions notated with a * are added instructions to enhance the standard 6502 instruction set.

Instruction Set In Alphabetic Sequence

Mnemonic	Description	Mnemonic	Description
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or (Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTS	Return from Subroutine
CLV	Clear Overflow Flag		
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
		SEC	Set Carry Flag
DEC	Decrement Memory by One	SED	Set Decimal Mode
DEX	Decrement Index X by One	SEI	Set Interrupt Disable Status
DEY	Decrement Index Y by One	*SMB	Set Memory Bit
		STA	Store Accumulator in Memory
		STX	Store Index X in Memory
EOR	"Exclusive-Or" Memory with Accumulator	STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
		TXA	Transfer Index X to Accumulator
JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
JSR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator

INSTRUCTIONS

		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z. PAGE, Y			BIT ADDRESSING (OP BY BIT #)								PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7	N V · B D I Z C
ADC	A · M · C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																		N V · · · · Z C
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3																		N · · · · · Z ·
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3																					N · · · · · Z C
BBR[#(0-7)]	Branch on M_6 = 0 (5)(2)																																								0F	1F	2F	3F	4F	5F	6F	7F	· · · · · · · ·
BBS[#(0-7)]	Branch on M_6 = 1 (5)(2)																																								8F	9F	AF	BF	CF	DF	EF	FF	· · · · · · · ·
BCC	Branch on C = 0 (2)																															90	2	2																· · · · · · · ·
BCS	Branch on C = 1 (2)																															B0	2	2																· · · · · · · ·
BEQ	Branch on Z = 1 (2)																															F0	2	2																· · · · · · · ·
BIT	A∧M				2C	4	3	24	3	2																																							M M_6 · · · · Z ·
BMI	Branch on N = 1 (2)																															30	2	2																· · · · · · · ·
BNE	Branch on Z = 0 (2)																															D0	2	2																· · · · · · · ·
BPL	Branch on N = 0 (2)																															10	2	2																· · · · · · · ·
BRK	Break													00	7	1																																	· · · 1 · 1 · ·
BVC	Branch on V = 0 (2)																															50	2	2																· · · · · · · ·
BVS	Branch on V = 1 (2)																															70	2	2																· · · · · · · ·
CLC	0→C													18	2	1																																	· · · · · · · 0
CLD	0→D													D8	2	1																																	· · · · 0 · · ·
CLI	0→I													58	2	1																																	· · · · · 0 · ·
CLV	0→V													B8	2	1																																	· 0 · · · · · ·
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3																		N · · · · · Z C
CPX	X M	E0	2	2	EC	4	3	E4	3	2																																							N · · · · · Z C
CPY	Y M	C0	2	2	CC	4	3	C4	3	2																																							N · · · · · Z C
DEC	M 1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3																					N · · · · · Z ·
DEX	X 1→X													CA	2	1																																	N · · · · · Z ·
DEY	Y 1→Y													88	2	1																																	N · · · · · Z ·
EOR	A∀M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3																		N · · · · · Z ·
INC	M · 1→M				EE	6	3	E6															F6	6	2	FE	7	3																					N · · · · · Z ·
INX	X · 1→X													EB	2	1																																	N · · · · · Z ·
INY	Y · 1→Y													C8	2	1																																	N · · · · · Z ·
JMP	Jump to New Loc				4C	3	3																												6C	5	3												· · · · · · · ·
JSR	Jump Sub				20	6	3																																										· · · · · · · ·
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3																		N · · · · · Z ·
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2									N · · · · · Z ·
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																					N · · · · · Z ·
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																					0 · · · · · Z C
NOP	No Operation													EA	2	1																																	· · · · · · · ·
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3																		N · · · · · Z ·
PHA	A→Ms S 1→S													48	3	1																																	· · · · · · · ·
PHP	P→Ms S 1→S													08	3	1																																	· · · · · · · ·
PLA	S · 1→S Ms→A													68	4	1																																	N · · · · · Z ·
PLP	S · 1→S Ms→P													28	4	1																																	(Restored)
RMB[#(0-7)]	0→M_b (5)																																								07	17	27	37	47	57	67	77	· · · · · · · ·
ROL	←[7 0]←[C]←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																					N · · · · · Z C
ROR	[C]→[7 0]→				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																					N · · · · · Z C
RTI	Rtrn Int													40	6	1																																	(Restored)
RTS	Rtrn Sub													60	6	1																																	· · · · · · · ·
SBC	A · M · C→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3																		N V · · · · Z (3)
SEC	1→C													38	2	1																																	· · · · · · · 1
SED	1→D													F8	2	1																																	· · · · 1 · · ·
SEI	1→T													78	2	1																																	· · · · · 1 · ·
SMB[#(0-7)]	1→M_b (5)																																								87	97	A7	B7	C7	D7	E7	F7	· · · · · · · ·
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3																		· · · · · · · ·
STX	X→M				8E	4	3	86	3	2																												96	4	2									· · · · · · · ·
STY	Y→M				8C	4	3	84	3	2													94	4	2																								· · · · · · · ·
TAX	A→X													AA	2	1																																	N · · · · · Z ·
TAY	A→Y													A8	2	1																																	N · · · · · Z ·
TSX	S→X													BA	2	1																																	N · · · · · Z ·
TXA	X→A													8A	2	1																																	N · · · · · Z ·
TXS	X→S													9A	2	1																																	· · · · · · · ·
TYA	Y→A													98	2	1																																	N · · · · · Z ·

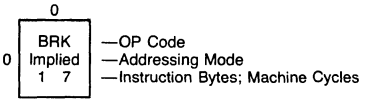
NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result.
5. Effects 8-bit data field of the specified zero page address.

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
· = Add
– = Subtract
∧ = And
V = Or
∀ = Exclusive Or
n = Number of cycles
\# = Number of Bytes

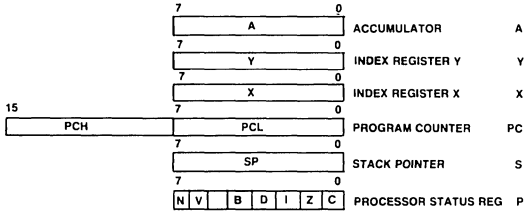
INSTRUCTION CODE MATRIX



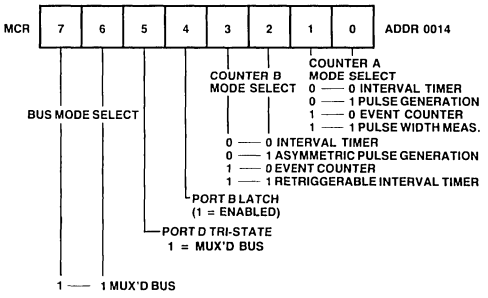
MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

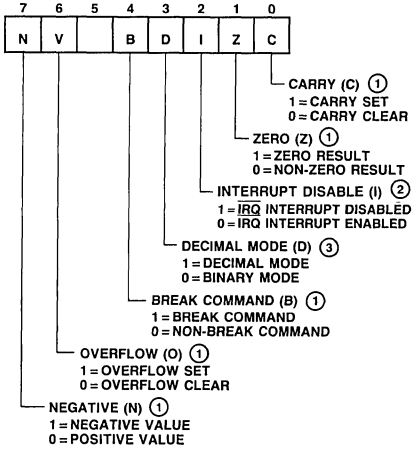
KEY REGISTER SUMMARY



CPU Registers



Mode Control Register



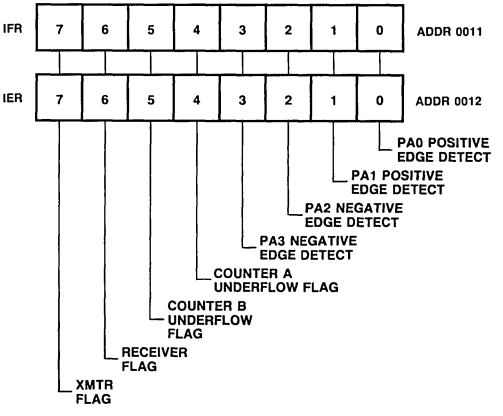
NOTES:

(1) NOT INITIALIZED BY $\overline{RES}$

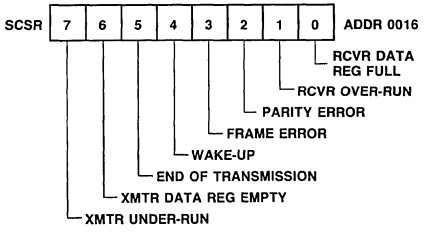
(3) SET TO LOGIC 1 BY $\overline{RES}$

(3) SET TO LOGIC 0 BY $\overline{RES}$

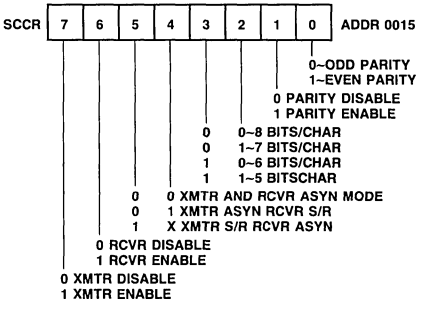
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Status Register



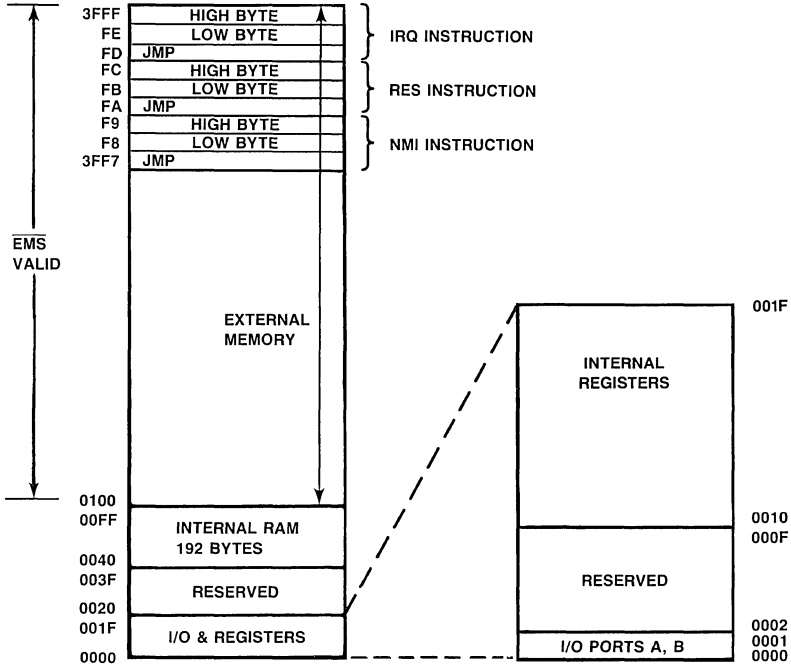
Serial Communications Control Register

ADDRESS ASSIGNMENTS AND MEMORY MAPS

I/O AND INTERNAL REGISTER ADDRESS

ADDRESS (HEX)	READ	WRITE
001F	—	—
1E	Lower Counter B	Upper Latch B, Cntr B ←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C ←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	—	—
1A	Lower Counter A	Upper Latch A, Cntr A ←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	—	—
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	—
0010	Read FF	Clear Int Flag (Bits 0–3 only, Write 0's only)
0F	—	—
0E	—	—
0D	—	—
0C	—	—
0B	—	—
0A	—	—
09	—	—
08	—	—
07	—	—
06	—	—
05	—	—
04	—	—
03	—	—
02	—	—
01	Port B	Port B
0000	Port A	Port A

MULTIPLEXED MODE MEMORY MAP



ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

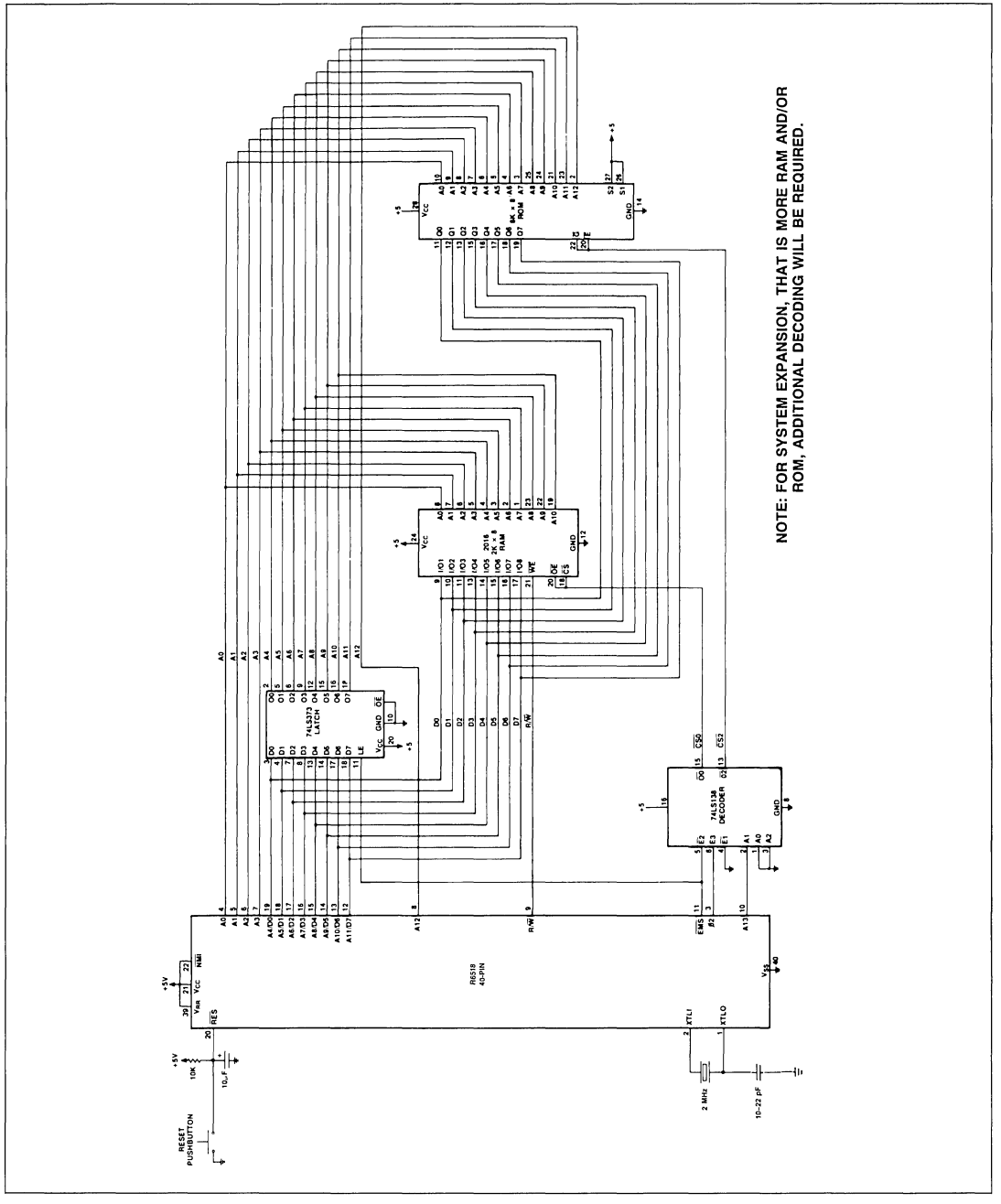
DC CHARACTERISTICS

(V_{CC} = 5V ±5%, V_{RR} = V_{CC}, V_{SS} = 0, T_A = 0 to 70°C except as noted)

Parameter	Symbol	Min	Typ.	Max.	Unit
Power Dissipation (Outputs High) Commercial @ 0°C	P_D	—		1000	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current ($\overline{RES}$, $\overline{NMI}$) V_{in} = 0 to 5.0 Vdc	I_{IN}			±10.0	μAdc
Input Low Current PA, PB, and Address/Data (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage (Except XTLO) (I_{LOAD} = 100 μAdc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{in} = 0V, T_A = 25°C, f = 1.0 MHz)	C_{in}				pF
PA, PB		—	—	10	
XTLI, XTLO		—	—	50	
I/O Port Pull-Up Resistance A0–A3, D0–D7; $\overline{EMS}$, R/$\overline{W}$ PA0–PA7, PB0–PB7	R_L	3.0	6.0	11.5	KΩ
Output Capacitance V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz	C_{OUT}	—	—	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

TYPICAL MEMORY HOOKUP



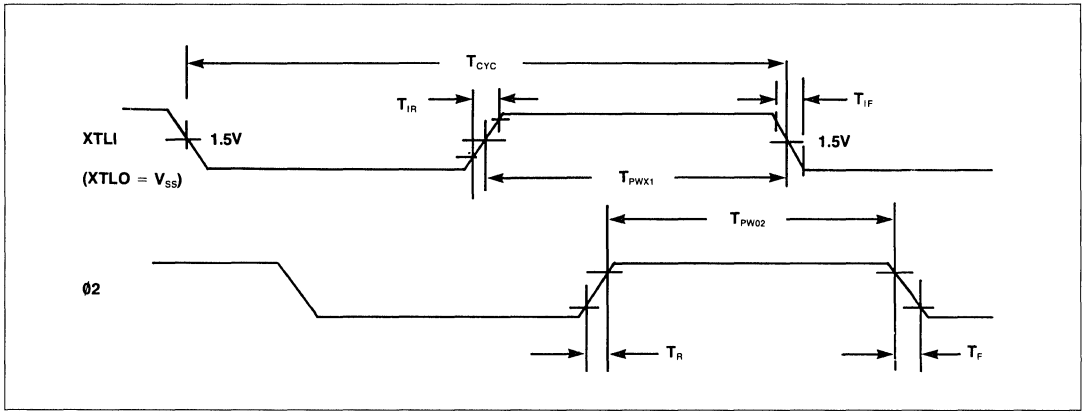
TIMING REQUIREMENTS AND CHARACTERISTICS

GENERAL NOTES

1. V_{CC} = 5V ±5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – $\overline{RES}$ sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130 pF maximum, except for Ports A and B which are 50 pF maximum.

CLOCK TIMING

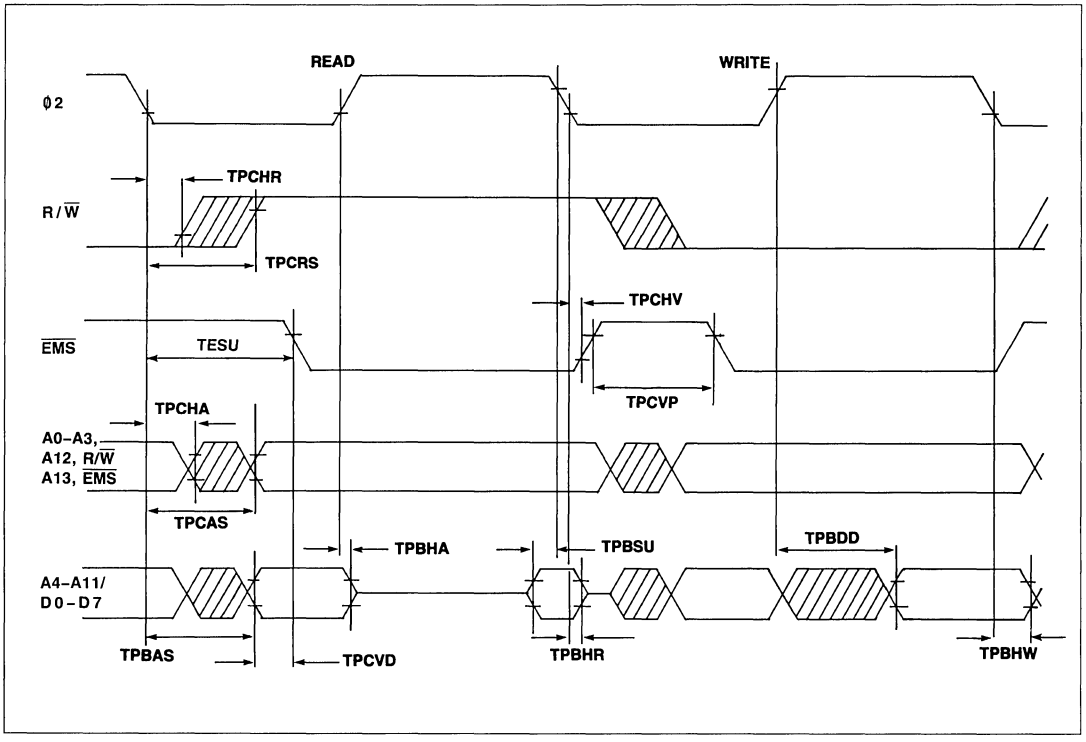
Symbol	Parameter	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
T_{CYC}	Cycle Time	1	10	0.5	10	μs
T_{PWX1}	XTLI Input Clock Pulse Width (XTLO = VSS)	500 ±25	—	250 ±10	—	ns
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1} +0 −25	T_{PWX1}	T_{PWX1} +0 −20	T_{PWX1}	ns
T_R, T_F	Output Clock Rise Fall Time	—	25	—	15	ns
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10	ns



ADDRESS/DATA TIMING

Symbol	Parameter	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
T_{PCRS}	R/W Setup Time	—	225	—	140	ns
T_{PCAS}	Address Setup Time	—	225	—	140	ns
T_{PBAS}	Address Setup Time	—	225	—	140	ns
T_{PBSU}	Data Setup Time	50	—	35	—	ns
T_{PBHR}	Data Read Hold Time	10	—	10	—	ns
T_{PBHW}	Data Write Hold Time	30	—	30	—	ns
T_{PBDD}	Data Output Delay	—	175	—	150	ns
T_{PCHA}	Address Hold Time	30	—	30	—	ns
T_{PBHA}	Address Hold Time	10	100	10	80	ns
T_{PCHR}	R/W Hold Time	30	—	30	—	ns
T_{PCHV}	$\overline{EMS}$ Hold Time	10	—	10	—	ns
T_{PCVD}(1)	Address to $\overline{EMS}$ Delay Time	30	—	30	—	ns
T_{PCVP}	$\overline{EMS}$ Stabilization Time	30	—	30	—	ns
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210	ns

Note 1: Values assume Address and $\overline{EMS}$ have the same capacitive load.

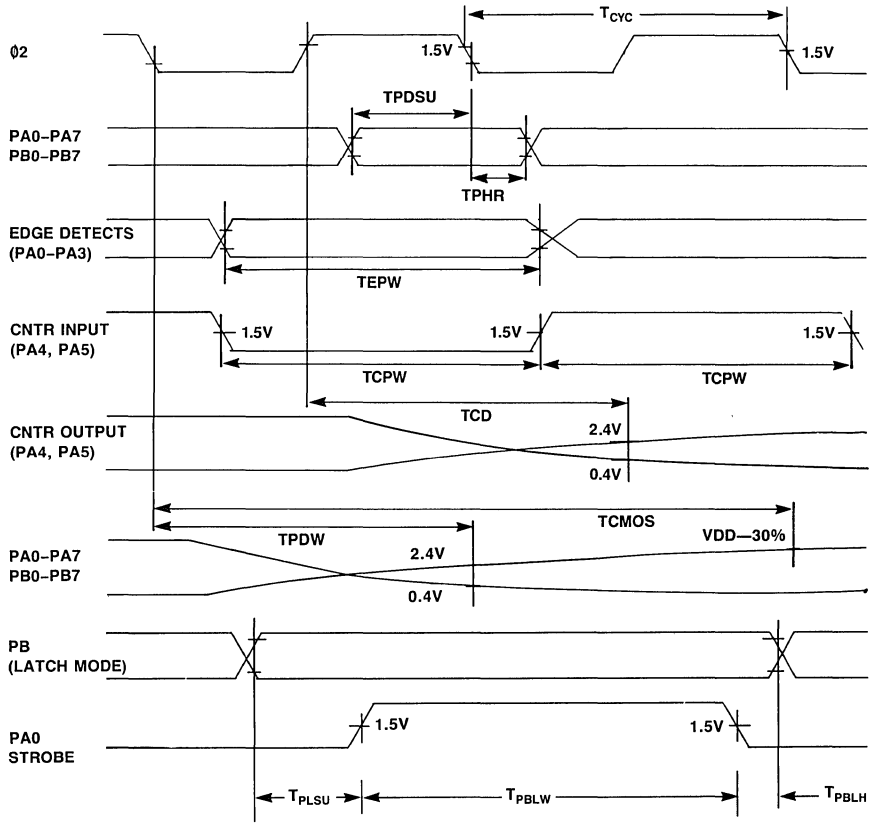


I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

Symbol	Parameter	1 MHz		2 MHz	
		Min	Max	Min	Max
	Internal Write to Peripheral Data Valid				
T_{PDW}(1)	PA, PB, TTL	—	500	—	500
T_{CMOS}(1)	PA, PB, CMOS	—	1000	—	1000
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB	200	—	200	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB	75	—	75	—
T_{EPW}	PA0–PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}(1)	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}(1)	PA6 XMTR TTL	—	500	—	500
T_{CMOS}(1)	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}(1)	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}(1)	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

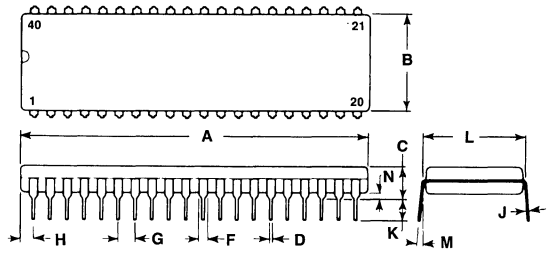
Notes: 1. Maximum load capacitance: 50 pF; passive pull-up required.
2. All times are in nanoseconds.

I/O, EDGE DETECT, COUNTER, AND SERIAL I/O TIMING



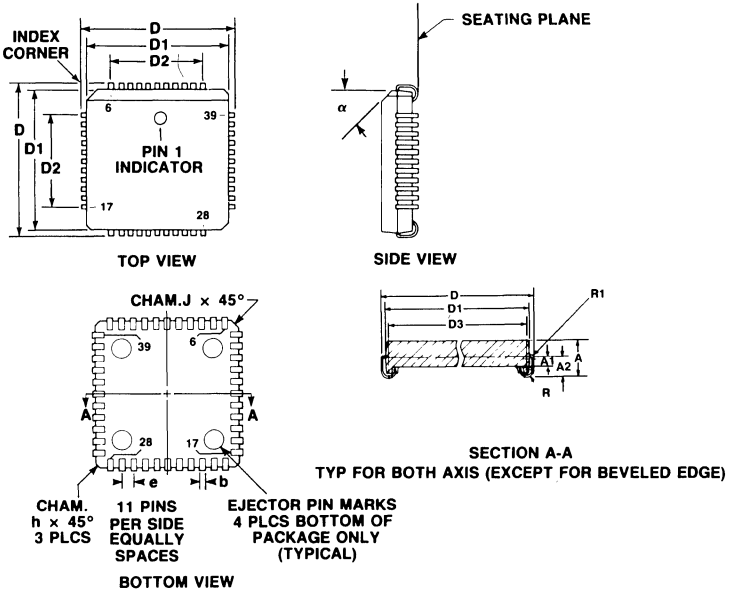
PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13 72	14.22	0.540	0.560
C	3.55	5.06	0 140	0 200
D	0.36	0.51	0.014	0 020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0 30	0.008	0 012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1 02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4 14	4.39	0.163	0 173
A1	1 37	1.47	0 054	0 058
A2	2.31	2 46	0 091	0 097
b	0 457 TYP		0 018 TYP	
D	17 45	17 60	0 687	0 693
D1	16 46	16.56	0.648	0 652
D2	12 62	12 78	0 497	0 503
D3	15.75 REF		0.620 REF	
e	1 27 BSC		0 050 BSC	
h	1 15 TYP		0 045 TYP	
J	0.25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0 89 TYP		0.035 TYP	
R1	0 25 TYP		0 010 TYP	