R6549
Color Video Display Generator (CVDG)

PRELIMINARY

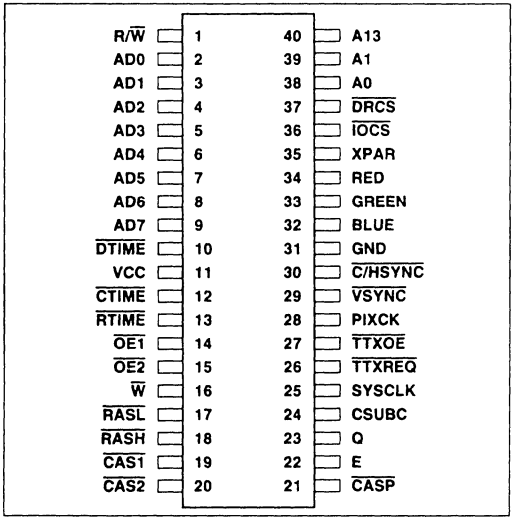
DESCRIPTION

The Rockwell R6549 Color Video Display Generator (CVDG) integrates video raster control; color lookup table (LUT) update and access; color generation and display refresh; teletext data DMA addressing, data routing and handshake; dynamic RAM (DRAM) control and refresh; and MPU/CVDG/DMA access to DRAM into a single device. Internal horizontal and vertical state machines generate video synchronization signals and control access of video color data from DRAM. A 16-entry color lookup table (LUT) supports 4-bit encoded color levels for red, green and blue (RGB) colors allowing 4096 color combinations to be generated. Each color code is converted to a 16-level analog signal by a dedicated DAC, combined with a blanking signal, and output in sync with a pixel clock.

Control registers allow MPU selection of CVDG operating mode and options while data registers allow MPU update of LUT data, current drawing pointer (CDP) graphics, Y scroll pointer and teletext pointer. The data registers can also be monitored by the MPU as can mode and raster scan status.

The R6549 is the first display generator to be designed exclusively in support of North American Presentation Level Protocol Syntax (NAPLPS) videotex (VTX) and teletext (TTX).

Replacing over 30 conventional MSI/LSI devices, the R6549 simplifies system design and layout, reduces printed circuit size, and minimizes required support circuits to speed system prototyping and greatly reduce both development and production costs.



R6549 CVDG Pin Assignments

FEATURES

- High performance video generator
  - 2:1 or 1:1 interlace
  - Analog red, green, blue (RGB) outputs
  - 16 levels per color plus blanking
  - 4096 color combinations
  - RS-170 sync and color subcarrier generation
  - 16 entry color look-up table (LUT)
  - RS-170 composite sync output with equalization and serration pulses
  - Internal/external video synchronization
  - Color subcarrier generation with line, field and pixel phase lock
  - Compatible with MC1377 color encoder
- Videotex (VTX)/Teletext (TTX) graphics
  - 256 x 210 x 4 bit-mapped video image buffer
  - Programmable border color
  - Transparent video overlay signal
  - Fast X CDP and Y CDP nibble or byte graphics I/O
  - NAPLPS X – Y origin with smooth Y vertical scroll
  - Fast horizontal drawing support with X auto increment byte write
- Dynamic RAM interface
  - Direct 48k-byte DRAM support, with auto inherent refresh for interfacing to six 16k x 4 DRAMS (4416-150 ns)
  - Supports three methods of DRAM access:
    - Video refresh 26.9k-byte DRAM—port or address mapped
    - Teletext/program 5.9k-byte DRAM—port or address mapped
    - Optional program 16k-byte DRAM extension—address mapped
  - Interleaving of MPU and CVDG DRAM access for uninterrupted read/write memory access without memory contention
  - On-chip refresh timing and control
- MPU Interface
  - Direct timing and cycle stealing for 1.4 MHz 68A09E MPU
  - Direct interface to R6512 CPU
- Teletext support
  - DMA interface and handshake to external NABTS teletext prefix processor
  - 5.72 Mbps effective data rate
  - 8k-byte teletext buffer DRAM interface

ORDERING INFORMATION

Part Number	Temperature Range
R6549 — Package: P = Plastic	0°C to 70°C

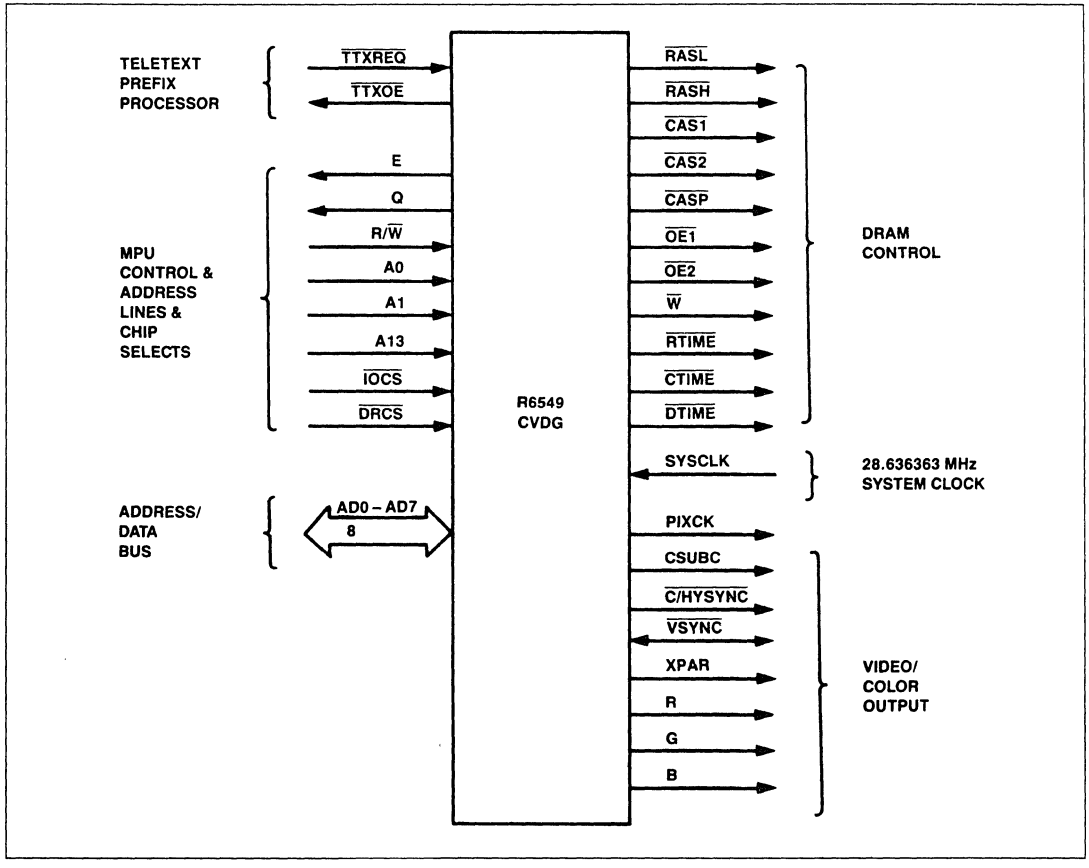


Figure 1. R6549 CVDG Interface Signals

PIN DESCRIPTION

Throughout this document signals are described logically using the terms active (or asserted) representing the true state, or inactive (or negated) representing the false state, regardless of whether the signal is active at a high or low voltage level.

The R6549 CVDG signals can be categorized into several different functional interfaces: MPU control and address bus, address/data (A/D) bus, DRAM control, color video output, teletext prefix processor and system clock input. Figure 1 identifies the signals within each group.

DMAC INTERFACE

$\overline{\text{TTXREQ}}$—Teletext DMA Request. An asynchronous falling edge-triggered request for direct memory access (DMA) transfer of data from a teletext prefix processor connected to the address/data (A/D) bus to DRAM. This TTL compatible input causes the CVDG to stop generating the E and Q clocks for one A/D bus cycle, output a 13-bit address (A0 – A12) to the DRAM during the processor portion of the A/D bus cycle, assert the $\overline{\text{TTXOE}}$ signal, and assert the $\overline{\text{W}}$ output to enable writing the data into DRAM.

$\overline{\text{TTXOE}}$—Teletext DMA Output Enable. An active LOW TTL compatible output pulse asserted within one A/D bus cycle after $\overline{\text{TTXREQ}}$ is asserted to acknowledge $\overline{\text{TTXREQ}}$ receipt and to enable data transfer from the teletext prefix processor onto the A/D bus (AD0 – AD7).

MPU CONTROL AND ADDRESS BUS

E—E Clock. A TTL compatible 1.43 MHz output clock that synchronizes data transfers over the MPU bus. This output drives the E clock input to the 6809E MPU. The E clock has special V_{OH} and V_{OL} output levels, V_{CC} – 0.5V and V_{SS} + 0.3V, respectively.

Q—Q Clock. A TTL compatible 1.43 MHz output clock that leads the E clock output for use by the 6809E.

R/$\overline{W}$—Read/Write. The TTL compatible Read/Write input controls the direction of data transfer between the MPU and the CVDG (HIGH = read from the CVDG; LOW = write to the CVDG). The R/$\overline{W}$ line should be connected to external data bus transceivers to also control the data direction between the MPU bus and the A/D bus.

A0, A1—MPU Address Line A0 and A1 Inputs. When $\overline{IOCS}$ is active, the encoded A0 and A1 inputs select the register in the CVDG to be accessed during a read or write operation (see Table 1). An exception is when A0 and A1 are both high during Mode 0, in which case DRAM is CDP accessed directly by the MPU at addresses generated by the CVDG.

When $\overline{DRCS}$ is active and program DRAM is selected (P = 1 in the DRAM Page Register), A0 is passed through the CVDG to drive the AD6 output during DRAM column address generation in the processor portion of the A/D bus cycle (see MPU DRAM Access Description).

A13—MPU Address Line A13 Input. When $\overline{DRCS}$ is active, A13 input HIGH causes program DRAM to be accessed ($\overline{CASP}$ asserted) during the processor portion of the A/D bus cycle independent of the P bit value in the DRAM Page Register. When program DRAM is selected in the DRAM Page Register (P = 1) or when A13 = 1, A13 is passed through the CVDG to drive the AD5 output during DRAM column address generation in the processor portion of the A/D bus cycle (see MPU DRAM Access Description).

$\overline{IOCS}$—I/O Chip Select. The active LOW, TTL compatible, $\overline{IOCS}$ input selects CVDG I/O port operation. The CVDG internal registers addressed by the A0 and A1 inputs are accessed as enabled by the mode selected in the Mode Register. Data direction is controlled by the R/$\overline{W}$ input as appropriate for each register and mode.

Table 1. CVDG Register Select Logic ($\overline{IOCS}$ = LOW)

A1	A0	Mode[1]	Read (R/$\overline{W}$ = H)	Write (R/$\overline{W}$ = L)
L	L	—	Status Register	Mode Register
L	H	0	X CDP Register	X CDP Register
H	L	0	Y CDP Register	Y CDP Register
H	H	0	DRAM[2]	DRAM[2]
H	H	1	—	LUT Address Register
H	H	2	LUT[3]	LUT Data Register
H	H	3	—	Switch Register
H	H	4	—	Y Scroll Register
H	L	5	TTX Pointer Register	TTX Pointer Register
H	H	6	—	DRAM Page Register

Notes:
1. The mode is selected in Mode Register.
2. DRAM is accessed directly by the MPU at DRAM addresses determined by the CVDG X CDP and Y CDP register contents.
3. The LUT is accessed as enabled and addressed in the LUT Address Register.

$\overline{DRCS}$—DRAM Chip Select. $\overline{DRCS}$ is a TTL compatible, active LOW, input that enables MPU access to the DRAM. $\overline{CTIME}$, $\overline{RTIME}$ and $\overline{DTIME}$ outputs are asserted by the CVDG at the proper times to enable external buffers which drive the MPU generated address onto the A/D bus and drive data between the MPU bus data lines and the A/D bus in the direction controlled by R/$\overline{W}$ (HIGH = read from DRAM; LOW = write to DRAM). Note that $\overline{DRCS}$ configurations are advanced and optional for many configurations.

ADDRESS/DATA BUS

AD0 – AD7—Address/Data Lines. Eight TTL compatible, bidirectional, multiplexed address/data lines (AD0 – AD7) interface the CVDG directly to the video/program DRAM, through external buffers to the MPU address bus (A1 – A12), and through external transceivers to the MPU data bus (D0 – D7). These lines transfer both address and data between the DRAM and the CVDG and between the MPU bus and the CVDG/DRAM during one 698 ns A/D bus cycle.

$\overline{RASL}$, $\overline{RASH}$—Row Address Strobe Low and High. TTL compatible outputs strobe the upper eight bits of the address on A/D bus lines AD0–AD7 into DRAM (as DRAM addresses A6–A13) on the falling edge. $\overline{RASL}$ strobes the address into the DRAM containing the lower four data bits (D0–D3) and $\overline{RASH}$ strobes the address into the DRAM containing the upper four data bits (D4–D7).

$\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$—Column Address Strobes 1, 2 and P. The TTL compatible CAS outputs strobe the six lower bits of the address on A/D bus lines (AD1–AD6) into DRAM (as DRAM addresses A0–A5) on the falling edge. $\overline{CAS1}$ and $\overline{CAS2}$ connect to the video DRAM containing the LUT addresses. Four 4-bit LUT addresses packed into two bytes are accessed during the video portion of each A/D bus cycle. $\overline{CAS1}$ strobes the DRAM containing the LUT addresses for the first two pixel positions while $\overline{CAS2}$ strobes the DRAM devices containing the LUT addresses for the second two pixel positions. $\overline{CASP}$ connects to the program DRAM containing the program instructions/data.

$\overline{OE1}$, $\overline{OE2}$—DRAM Output Enable. These active LOW, TTL compatible, outputs enable DRAM device data output lines during a read. $\overline{OE1}$ connects to the two video DRAM devices containing byte 1 (LUT addresses for pixels 1 and 2) and is asserted first during a video refresh cycle. $\overline{OE2}$ connects to the two DRAM devices containing byte 2 (LUT addresses for pixels 3 and 4) and is asserted following $\overline{OE1}$. $\overline{OE2}$ is also connected to the program DRAM devices and enables their data outputs during the processor portion of the A/D bus cycle.

$\overline{W}$—DRAM Write Enable. The TTL compatible, active LOW, $\overline{W}$ output strobes data from the A/D bus into DRAM during a write in the processor portion of the A/D bus cycle. $\overline{W}$ is held HIGH during a read from DRAM.

$\overline{RTIME}$—Row Address Time. The active LOW, TTL compatible, $\overline{RTIME}$ output enables DRAM row address lines from the MPU onto the A/D bus through external buffers when $\overline{DRCS}$ is active. (Required for $\overline{DRCS}$ configurations only.)

$\overline{CTIME}$—Column Address Time. The active LOW, TTL compatible, $\overline{CTIME}$ output enables DRAM column address lines from the MPU onto the A/D bus through external buffers when $\overline{DRCS}$ is active. (Required for $\overline{DRCS}$ configurations only.)

$\overline{\text{DTIME}}$—Data Time. The active LOW, TTL compatible, $\overline{\text{DTIME}}$ output enables data transfer between the MPU data bus and the A/D bus through external transceivers when $\overline{\text{DRCS}}$ or $\overline{\text{IOCS}}$ is active.

SYSTEM CLOCK

SYSCLK—System Clock. A clock input with a duty cycle of 40/60 to 50/50. The clock frequency should be 28.63636 MHz ±80 Hz for proper operation of the colorburst frequency. This input clock may be stopped in either state for up to 1 μs to allow for external digital phase lock techniques.

VIDEO/COLOR OUTPUTS

CSUBC—Color Subcarrier Clock Output. A TTL compatible 3.579545 MHz ± 10% color subcarrier clock. The clock rate complies with the North American Color Burst Clock Output Standard. The rate is the SYSCLK divided by eight and is phase keyed to the horizontal sync ($\overline{\text{HSYNC}}$) output on $\overline{\text{C/HSYNC}}$ (as either a component of $\overline{\text{CSYNC}}$ or pure $\overline{\text{HSYNC}}$). Vertical blanking interval (VBI) color gating by $\overline{\text{VSYNC}}$ must be done externally (since some modems require an uninterrupted 3.579 MHz clock).

When the color outputs are connected to an MC1377 color encoder, the CSUBC output can be connected to the MC1377 CLK input, typically through a 500 pF capacitor/150 μH inductor filter network.

$\overline{\text{C/HSYNC}}$—Composite/Horizontal Sync Output. Either a composite sync ($\overline{\text{CSYNC}}$) or a horizontal sync ($\overline{\text{HSYNC}}$) output at TTL levels, asserted "tips down", is selected by the External Sync (EXT) bit in the Switch Register.

In internal sync (EXT = 0), an RS-170 composite sync with full serration and equalization is output in either 2:1 or 1:1 interlace as selected by the 2:1 Interlace Select (S21) bit in the Switch Register (S21 = 1 for 2:1; S21 = 0 for 1:1).

In external sync (EXT = 1), a pure $\overline{\text{HSYNC}}$ is output in either normal or early timing as selected by the Normal Horizontal Sync (NHS) bit in the Switch Register. In normal timing (NHS = 1), a 15.7 kHz signal is output; in advance timing (NHS = 0), a 15.9 kHz stop clock signal is output.

When the color outputs are connected to an MC1377 color encoder, the $\overline{\text{C/HSYNC}}$ output can be connected directly to the MC1377 SYNC input pin.

$\overline{\text{VSYNC}}$—Vertical Sync Input/Output. A TTL compatible vertical sync ($\overline{\text{VSYNC}}$) input or output signal depending on the state of the External Sync (EXT) bit in the Switch Register (see Mode 3). $\overline{\text{VSYNC}}$ is an externally generated input at power up or when EXT = 1. $\overline{\text{VSYNC}}$ is an internally generated output when EXT = 0.

The $\overline{\text{VSYNC}}$ output can be used to disable the color subcarrier at the chroma modulator during VBI. Videotex decoders can also use $\overline{\text{VSYNC}}$ to interrupt the MPU at a 60 Hz rate for blink, task and timekeeping operations.

PIXCLK—Pixel Clock Output. A 5.7272 MHz pixel output clock running synchronously with the RGB color outputs.

R, G, B—Red, Green and Blue Color Outputs. Three separate color analog output voltages. Each output provides a 1.0 Vpp video signal at high impedance with a 1.8 Vdc offset. Each color level is controlled by a 4-bit color code accessed from the LUT for each pixel position. A digital-to-analog converter (DAC) converts the 4-bit code to one of 16 output voltage levels (black level = 1.875 Vdc; white level = 2.800 Vdc). The three outputs allow 4096 color level combinations. A composite blanking signal (1.800 Vdc) is included in each output.

The output signals include high frequency clock components which may require low pass filtering in some applications. The outputs can be connected to the R IN, G IN, and B IN inputs to a MC1377 color encoder through 15 μF (typical) AC coupling capacitors.

The color outputs, through external buffers, can also drive 75 ohm loads, e.g., the inputs to an RGB color monitor/TV.

XPAR—Transparent Output. A TTL compatible, active HIGH, output controlled by one bit in a 4-bit code (three bits are don't care) in the LUT. A LUT value of 1XXX in DRAM asserts XPAR (HIGH); LUT value of 0XXX in DRAM negates XPAR (LOW). This output can be used to indicate which video source to select. When XPAR output is HIGH, external video signals should be selected to display background video; when XPAR output is LOW, CVDG outputs should be selected to display graphics. The XPAR output is always HIGH during composite blanking to pass external vertical blanking interval (VBI) signals, external sync, color burst, etc.

POWER/GROUND

VCC—Primary Power. 5.0 Vdc.

VSS—Ground. Power and signal ground.

FUNCTIONAL DESCRIPTION

The R6549 CVDG operation is controlled by three free-running synchronous state machines with the following cycle rates:

Address/Data (A/D) Bus Cycle	698 ns/cycle (1.43 MHz)
Horizontal Raster Line Cycle	63.5 μs/cycle (15.74 kHz)*
Vertical Raster Frame Cycle	33.3 ms/cycle (30 Hz)

The CVDG also includes timing shift registers and sample flip-flops to generate internal and external timing signals; programmed logic arrays (PLAs) to perform I/O decoding, generate DRAM control signals and determine state machine outputs; registers to hold command/status and data; an internal 16-bit row/column bus in display X-Y coordinates; internal input and output 8-bit data busses; and input/output buffers to isolate internal circuits from external interfaces and to drive outputs. Figure 2 illustrates the main CVDG components.

*A 15.9 kHz stop-clock early sync is selectable.

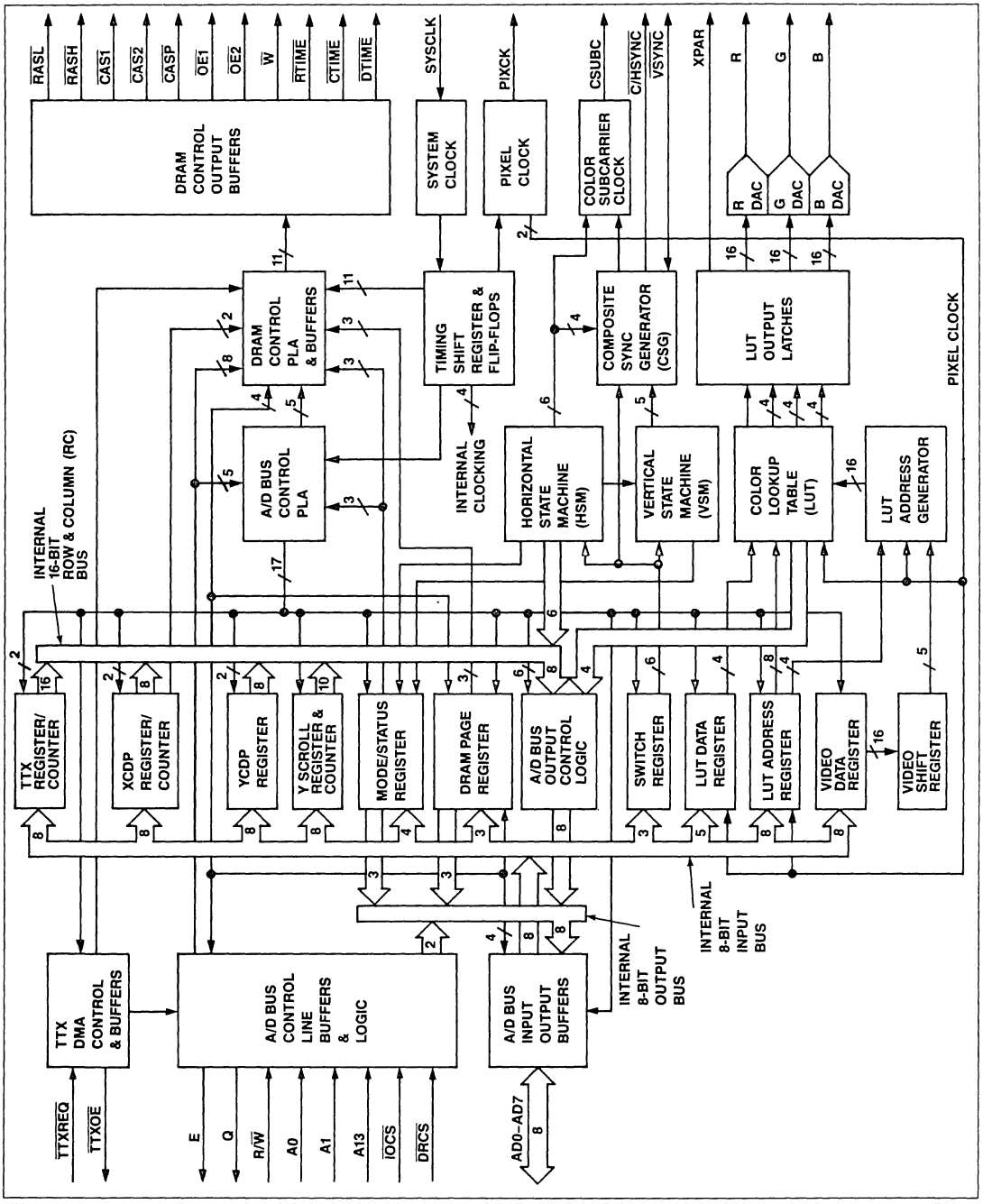


Figure 2. R6549 CVDG Block Diagram

SYSTEM TIMING

System Clock

Internal and output timing signals are derived from the 28.636363 MHz crystal frequency on the SYSCLK input pin. A two-phase non-overlapping 14.318181 MHz (SYSCLK/2) clock is generated to sequence high speed data transfer within the CVDG.

Timing Shift Register

The Timing Shift Register generates internal timing pulses as internal timing references at frequencies from 14.318 MHz down to 13.98 kHz. Flip-flops sample the various timing pulses to generate derivative timing reference signals for use by other CVDG circuits.

A two-phase non-overlapping 1.431818 MHz (SYSCLK/20) clock is generated for low speed sequencing within the CVDG and is also the external microprocessor bus and A/D bus timing reference. One phase of the 1.43 MHz clock drives the E clock output pin. A quadrature 1.431818 MHz clock leading the E clock is output on the Q output pin.

Pixel Clock

A 5.72 MHz pixel clock is output on the PIXCK output pin. Four pixel output clocks occur each 698 ns (one clock pulse coincident with each of the red, green and blue color level outputs and the transparent bit output for each pixel location).

VIDEO RASTER CONTROL

Horizontal Raster Line Cycle

An internal horizontal state machine (HSM) controls the horizontal raster line cycle. The HSM is incremented at the E clock rate, nominally every 698 ns. When normal horizontal sync timing is selected in the Switch Register (NHS = 1), 91 horizontal counts (HS0 – HS90), or states, comprise the 63.56 μs line raster. When early horizontal sync timing is selected (NHS = 0), typically to support external synchronization, 90 horizontal counts (HS0 – HS89) provide a 62.86 μs line raster. The first 64 counts clock the 256 displayed pixels (at four pixels per count). Figure 3 illustrates the horizontal and vertical raster count reference.

The HSM generates the horizontal raster timing pulses for internal logic and/or external output. These signals are the horizontal sync ($\overline{\text{HSYNC}}$), horizontal border and blanking, horizontal blanking, serration and equalization timing pulses.

The horizontal border and blanking pulse identifies the time that a border color is output (see LUT Data Register description) outside of the 256 pixel locations except during actual horizontal blanking. This signal is reported in bit 6 ($\overline{\text{HB}}$) of the Status Register.

An increment vertical count signal is also generated to increment the vertical state machine.

Vertical Raster Frame Cycle

An internal vertical state machine (VSM) controls the 33.3 ms vertical raster frame cycle. The VSM is incremented twice each horizontal raster line cycle. The VSM count (VS0 – VS523 or VS0 – VS524), or state, supports two frames per 30 ms vertical raster cycle. The upper count depends on the interlace mode (S21) switch position selected in the Switch Register. When 2:1 interlace mode is selected (S21 = 1), the upper VSM count supports a 262½ line frame. When 1:1 interlace is selected (S21 = 0), the upper VSM count supports a 262 line frame.

A VSM clear sign is normally generated when the VSM upper count is reached to restart the VSM at 0; however, when external sync is selected (EXT = 1) the VSM clear signal is generated from the external sync signal input on the $\overline{\text{VSYNC}}$ pin. Internal vertical state timing signals are generated for internal logic and/or external output. These signals include vertical sync ($\overline{\text{VSYNC}}$), vertical border and blanking, vertical blanking, and equalization enable pulses and the load Y scroll pointer time.

An internal vertical sync pulse, a vertical blanking pulse, and an equalization pulse are generated for combining with the $\overline{\text{HSYNC}}$ serration and equalization pulses when internal sync is selected (EXT = 0) to output composite sync on the $\overline{\text{C/HSYNC}}$ pin.

The vertical blanking pulse is also buffered and output on the $\overline{\text{VSYNC}}$ pin when internal sync is selected in the Switch Register (EXT = 0).

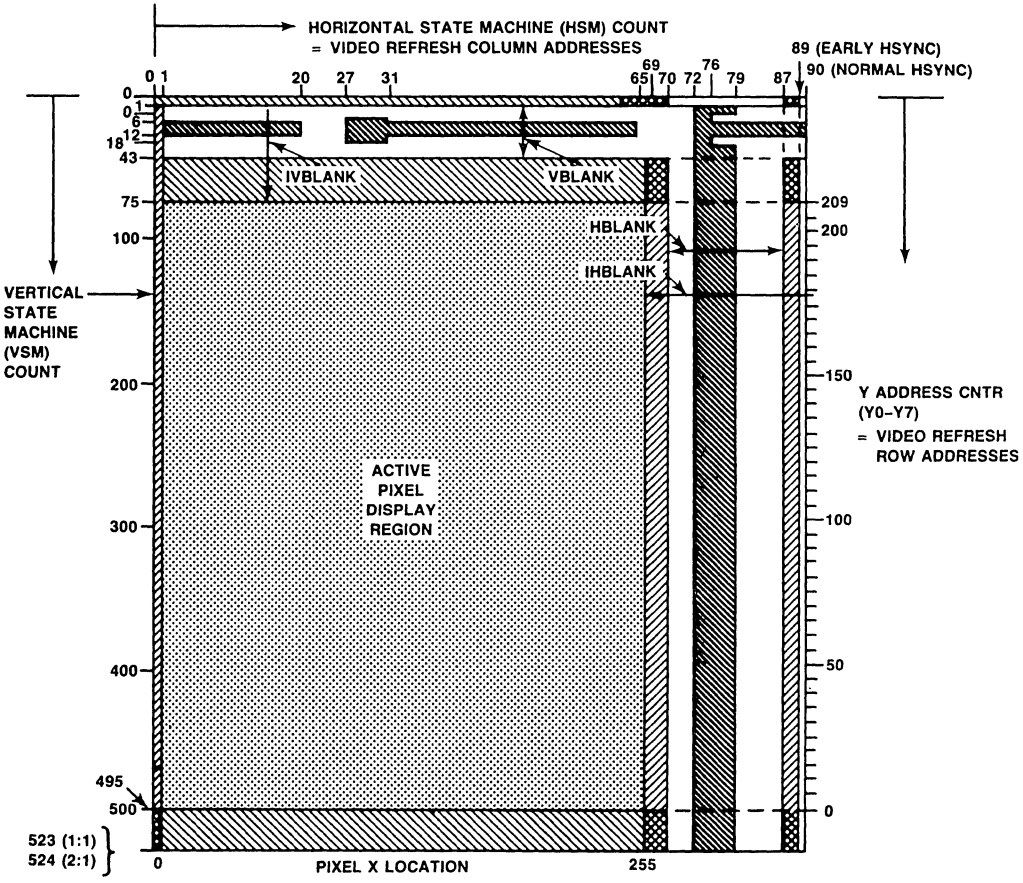
The internal vertical border and blanking pulse is generated and reported in bit 7 ($\overline{\text{VB}}$) of the Status Register. The pulse width is 3.302 ms for 2:1 interlace (S21 = 1) or 3.333 ms for 1:1 interlace (S21 = 0). This duration identifies the time the border color determined from the LUT Data Register is output, except during actual vertical blanking.

An internal load Y offset pointer signal is generated and routed to the Y Scroll Counter to cause the Y offset to load during the non-visible portion of the display raster.

Composite Sync and Color Subcarrier Clock Generation

$\overline{\text{HSYNC}}$ is output in one of two forms on the $\overline{\text{C/HSYNC}}$ pin depending upon the EXT bit state in the Switch Register. If internal sync is selected (EXT = 0), $\overline{\text{HSYNC}}$ is combined with horizontal blanking serration, equalization and vertical sync ($\overline{\text{VSYNC}}$) pulses to output as composite sync ($\overline{\text{CSYNC}}$). If external sync is selected (EXT = 1), the $\overline{\text{HSYNC}}$ signal is output on $\overline{\text{C/HSYNC}}$.

A 3.58 MHz color subcarrier clock (SYSCLK/8 and phase keyed to horizontal sync) is generated from composite sync and horizontal sync signals then is output on the CSUBC pin.



NOTES:
1. Vertical State Transition (HS28)
2. Vertical State Transition and $\overline{\text{HSYNC}}$ (HS73)
3. Symbol definitions:
   HBLANK = Horizontal Blanking
   IHBLANK = Horizontal Border and Blanking
   VBLANK = Vertical Blanking
   IVBLANK = Vertical Border and Blanking
   CBLANK = HBLANK + VBLANK = Composite Blanking
   ICBLANK = = IHBLANK + IVBLANK = Composite Borders and Blanking
4. Shading Legend:
   - Active Pixel Display Region
   - Right and Left Borders
   - Top and Bottom Borders
   - Blanking Region
   - Composite SYNC (CSYNC)

Figure 3. CVDG Video Raster Count Reference

ADDRESS/DATA BUS CONTROL

The Address/Data Bus state machine controls the operation of the 698 ns A/D bus cycle. The A/D bus cycle contains a 2-byte video data access cycle and a 1-byte I/O data access cycle (Figure 4). The addresses and data transferred on the A/D bus depend on the phase of the A/D bus cycle (i.e., the E clock level) and the type of operation in the I/O data access cycle. Table 2 identifies the source of the addresses for each type of DRAM access.

Video Data Access Cycle

The video data access cycle (also referred to as the video portion of the A/D bus cycle) occurs during the first half of the A/D bus cycle (when the E clock is LOW). Two bytes of video data (containing four LUT addresses corresponding to four pixel locations on the display) are read each cycle from DRAM at the DRAM address generated by the CVDG. The DRAM address is generated corresponding to the first of four pixel column locations in the horizontal raster and the pixel row location in the vertical raster. The video column (X) address of 0 to 64 is controlled by the horizontal state machine. The video row (Y) address of 209 to 0 is controlled by the Y Address Counter, which is in turn controlled by the vertical state machine and the Y Scroll Register. The two data bytes are loaded into the CVDG Video Data Register for subsequent serialization and LUT access (see the Pixel Color Generation description).

Up to 48k-bytes of Dynamic RAM (DRAM) can be connected to the A/D bus to store video data (LUT addresses) for video refresh, program instructions/data and received teletext data. The DRAM is segmented into six 8k-byte blocks with page selection of one block at a time during access (Figure 5). Four pages are required for video refresh (V00 – V11); three pages (V00, V01 and V10) hold video data exclusively, and one page (V11) holds video and program/teletext data. Two other pages hold program data. During the video data access cycle, and some modes of the I/O data access cycle, paging is handled automatically by the CVDG. The A13 and A0 input lines and the P, V1 and V0 bits in the CVDG DRAM Page Register select the page for MPU DRAM access during the I/O data access cycle (see MPU DRAM Access description).

I/O Data Access Cycle

The I/O data access cycle (also referred to as the processor portion of the A/D bus cycle) occurs during the second half of the A/D bus cycle (when E clock is HIGH). A/D bus address source and data source/destination depends upon CVDG chip select ($\overline{IOCS}$ and $\overline{DRCS}$) and Teletext Request ($\overline{TTXREQ}$) input levels, the selected CVDG mode, and the register select (A0 and A1) input levels. Refer to the description of each I/O access cycle function for details.

A/D Bus Control Line Buffers and Logic

The A/D Bus Control Line Buffers and Logic condition input and output A/D Bus control signals. Six input signals (R/$\overline{W}$, A0, A1, A13, $\overline{IOCS}$ and $\overline{DRCS}$) are buffered and routed to the DRAM Control PLA.

The E and Q output clocks are suppressed during a teletext DMA transfer. When $\overline{TTXREQ}$ input goes LOW, the Q and E clock outputs are held LOW to disable the clocks for one MPU bus cycle. In addition, the increment TTX address count goes HIGH to increment the modulo 32 TTX Counter. When $\overline{TTXREQ}$ goes HIGH at the completion of the DMA data transfer, the E and Q output clocks are enabled, the $\overline{TTXOE}$ output is negated (reset HIGH), and the increment TTX address count signal is reset.

Internal reset and initialization signals are generated when both $\overline{IOCS}$ and $\overline{DRCS}$ inputs are LOW for test purposes.

A/D Bus Control PLA

The A/D Bus Control PLA decodes CVDG and A/D Bus operation commands from buffered A/D bus control input signals and encoded mode bits in the Mode Register. Outputs from the PLA are buffered and routed to other circuits in the CVDG as internal enable signals.

A/D Bus Input/Output Buffers

The A/D Bus Input/Output Buffers isolate the internal CVDG data bus lines from the external A/D bus lines (AD0 – AD7). Input buffers continuously copy AD0 – AD7 onto the internal input data bus. Output buffers drive the states of the internal output data bus lines onto AD0 – AD7 when enabled by a CVDG output function and clocked by the 14.3 MHz internal clock. Two of these output buffers drive AD5 and AD6 during MPU DRAM access ($\overline{DRCS}$ = L) with the DRAM page signals, i.e., V0 and V1, respectively, or A13 and A0 inputs, respectively, depending on the state of the A13 input and the P bit in the DRAM Page Register.

A/D Bus Output Control Logic

The A/D Bus Output Control Logic drives data onto the internal output bus from the internal row and column bus lines, from the LUT, and from other internal CVDG circuits when enabled by outputs from the A/D Bus Control PLA.

DRAM Control PLA and Buffers

The DRAM Control PLA and Buffers generate and drive control and timing output signals to the DRAM; the row, column and data time output control signals for use by external line buffers and data line transceivers; and internal signals to control input/output data direction and to enable the internal row and column bus.

Timing pulses from the Timing Shift Registers; control signals from the Mode and Page registers, A/D Bus Control Buffers and Logic, and A/D Bus Control PLA; and control signals generated and derived from other sections of the CVDG are input to the PLA.

Output control states from the PLA are buffered and routed to external DRAM control signal pins ($\overline{RASL}$, $\overline{RASH}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$, $\overline{OE1}$, $\overline{OE2}$, and $\overline{W}$) and to external A/D bus control signal pins ($\overline{CTIME}$, $\overline{RTIME}$ and $\overline{DTIME}$). Other output signals are inverted and routed to internal logic.

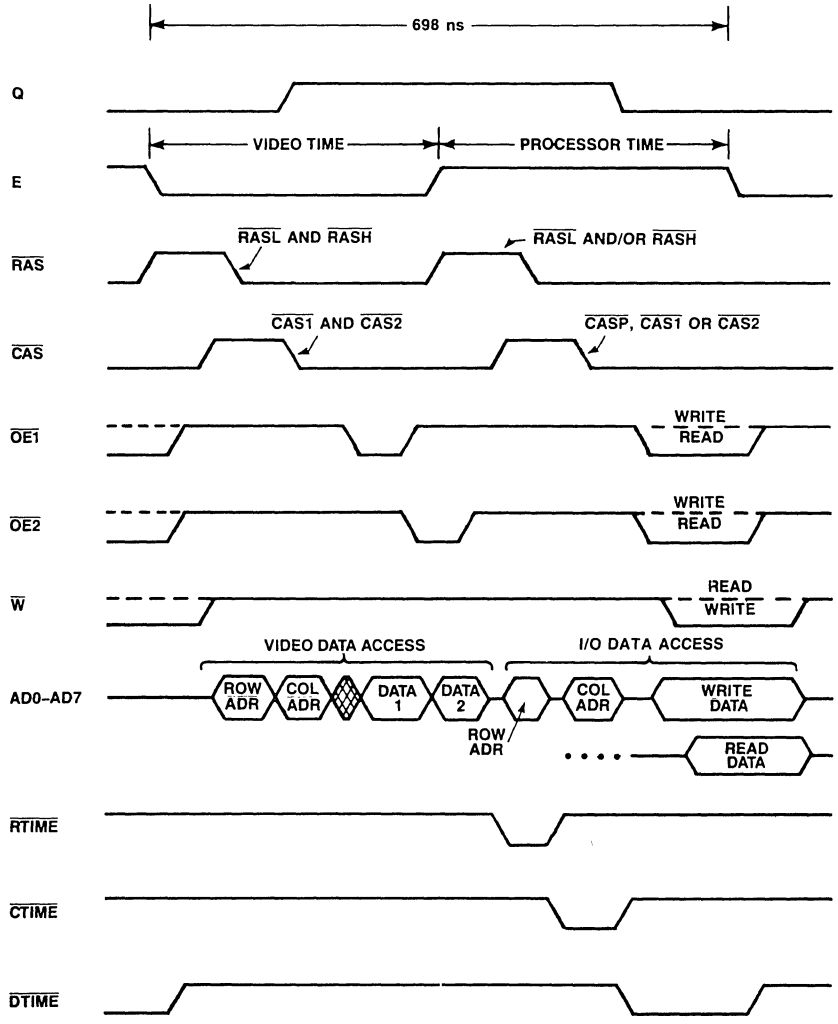


Figure 4. DRAM Address/Data (A/D) Bus Cycle

Table 2. Address/Data Bus Address Sources

DRAM Row/Column	—	CA5	CA4	CA3	CA2	CA1	CA0	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
CVDG Display Row/Column Bus	C7	C6	C5	C4	C3	C2	C1	C0	R7	R6	R5	R4	R3	R2	R1	R0
A/D Bus	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Video Cycle[1]	0	V7	V6	V5	V4	V3	V2	0	V1	V0	H6	H5	H4	H3	H2	H1
Processor Cycle CDP Graphics[2] ($\overline{IOCS}$ = L, Mode 0)	X1[3]	Y7	Y6	Y5	Y4	Y3	Y2	X0[4]	Y1	Y0	X7	X6	X5	X4	X3	X2
MPU Video DRAM Access[5] ($\overline{DRCS}$ = L, P = 0)	A0[6]	V1[7]	V0[2]	A12	A11	A10	A9	0	A8	A7	A6	A5	A4	A3	A2	A1
MPU Program DRAM Access[8] ($\overline{DRCS}$ = L, P = 1)	0	A0[9]	A13[9]	A12	A11	A10	A9	0	A8	A7	A6	A5	A4	A3	A2	A1
Teletext DMA Access[10] ($\overline{TTXREQ}$ = L)	T0	1[11]	1[11]	T12	T11	T10	T9	0	T8	T7	T6	T5	T4	T3	T2	T1

Notes:

1. Video Cycle:
   H1 – H6 = HSM Output = 0 to 64 (= 0 to 255 pixel LUT addresses @ 4 addresses per access);
   V0 – V7 = Y Scroll Counter Output = 209 to 0
2. CDP Graphics:
   X0 – X7 = X CDP Register/Counter contents = 0 to 255;
   Y0 – Y7 = Y CDP Register contents = 0 to 255 (0 to 209 for displayable data)
3. X1 controls the $\overline{CAS1}$ and $\overline{CAS2}$ outputs:
   0 = Assert $\overline{CAS1}$
   1 = Assert $\overline{CAS2}$
4. X0 controls the $\overline{RASL}$ and $\overline{RASH}$ outputs:
   0 = Assert $\overline{RASL}$
   1 = Assert $\overline{RASH}$
5. MPU Video DRAM Access: A0 – A12 = MPU Address = 0 to 4096.
6. A0 input controls the $\overline{CAS1}$ and $\overline{CAS2}$ outputs:
   L = Assert $\overline{CAS1}$
   H = Assert $\overline{CAS2}$
7. V0 and V1 bits in the DRAM Page Register control assertion of AD6 and AD5 outputs, respectively:
   0 = Negate output
   1 = Assert output
8. MPU Program DRAM Access: A0 – A13 = MPU Address = 0 to 8192
9. A0 and A13 inputs control the AD6 and AD5 outputs, respectively:
   L = Negate output
   H = Assert output
10. Teletext Access:
    T1 – T4 = Modulo 32 counter incremented by each DMA byte transfer
    T5 – T12 = Teletext Pointer Register contents incremented by T1 – T4 overflow
11. AD6 and AD5 asserted to select program DRAM.

DRAM Page Register				Addr (Hex)	Addr (Dec)	Memory Page	Memory Function
A13	P	V1	V0				
				1FFF	8191		
1	1	X	X			Program 1 (A13 = 1)	
				0	0		PROGRAM
				1FFF	8191		
0	1	X	X			Program 0 (A13 = 0)	
				0	0		
				1FFF	8191		PROGRAM/ TELETEXT
0	0	1	1			Video 3 (V11)	
				0900	2304		
				08FF	2303	0,209 | 1,209	Note 2
				0	0		
				1FFF	8191		
0	0	1	0			Video 2 (V10)	
				0	0		
				1FFF	8191		VIDEO[1] DATA
0	0	0	1			Video 1 (V01)	
				0	0		
				1FFF	8191		
0	0	0	0			Video 0 (V00)	
				0	0	254,0 | 255,0	Note 2

Notes:

1. 26,880 bytes of video memory are required to support video refresh, i.e., to supply 53,760 4-bit LUT addresses in support of the 210 x 256 pixel display area. With 32,768 bytes supplied in four 4416 DRAM devices, 5888 bytes are available for general program/TTX message use in the upper part of video memory page 3 (V11).
2. Nibbles shown correspond to beginning and ending data for 210 x 256 pixel display area in X(column), Y(row) coordinates.

Figure 5. DRAM Memory Map

PIXEL COLOR GENERATION

LUT Address Generation

The 16-bit Video Data Register latches the four LUT addresses contained in the two data bytes acquired during the video data access cycle. Two 4-bit color lookup table (LUT) addresses are packed into each byte. The Video Shift Register serializes the four LUT addresses and transfers them one byte at a time to the LUT Address Generator. The LUT Address Generator latches the 4-bit coded LUT addresses from the Video Shift Register, converts the coded address to 16 binary signals and latches the binary address (0 – 15) for routing to the LUT.

LUT Operation

The color look-up table (LUT) is a 16 × 13 bit memory holding 16 entries of R, G and B color codes and corresponding transparent state (see Table 3). Each entry holds three 4-bit encoded color levels (0000 = lowest voltage level, 1111 = highest voltage level) and a 1-bit transparent state (0 = off, 1 = on). For each pixel location the three color level codes (R, G and B) are sampled from the LUT, latched and routed through three separate digital-to-analog converters. The transparent bit corresponding to each pixel location is also accessed from the LUT, latched, buffered and output on the $\overline{\text{XPAR}}$ pin.

Digital-To-Analog Conversion (DACs)

The 4-bit color code for each color (R, G and B) at a pixel position is converted to a corresponding analog voltage through a 16-level digital-to-analog converter (DAC). Four lines from the four color code lines and their four complements are decoded to one of 16 levels, sampled and latched. The latched outputs are in turn connected to the color output pin (R, G and B) through a voltage divider ladder network.

Table 3. LUT Structure

LUT ADDR	LUT FORMAT																
	XPAR[1]				GREEN[2]				BLUE[2]				RED[2]				
(HEX)	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	
F																	
E																	
D																	
C	0				0	0	0	0	0	1	0	0	0	1	1	1	Example 1[3]
B																	
A		NO															
9	1	ACTUAL			1	0	0	0	1	1	0	0	1	1	1	1	Example 2[4]
8		DATA															
7																	
6																	
5																	
4																	
3																	
2																	
1																	
0																	

Notes:

1. XPAR is a single bit in the LUT; the format shown corresponds to the LUT Data Register format:
   0XXX = XPAR output LOW
   1XXX = XPAR output HIGH

2. Color Data Level:
   0000 = lowest output voltage = 1.875 Vdc
   1111 = highest output voltage = 2.800 Vdc

3. Example 1—LUT Address C Data:
   XPAR output = LOW
   G output = 1.875 + 0 (0.0617) = 1.875 Vdc
   B output = 1.875 + 4 (0.0617) = 2.122 Vdc
   R output = 1.875 + 7 (0.0617) = 2.307 Vdc

4. Example 2—LUT Address 9 Data:
   XPAR output = HIGH
   G output = 1.875 + 8 (0.0617) = 2.369 Vdc
   B output = 1.875 + 12 (0.0617) = 2.615 Vdc
   R output = 1.875 + 15 (0.0617) = 2.800 Vdc

I/O DATA ACCESS CYCLE FUNCTIONS

The I/O access cycle operates in one of five ways:

1. CVDG Mode/Status Register Access (enabled by $\overline{IOCS}$ LOW)
2. CVDG Graphics Access (enabled by $\overline{IOCS}$ LOW)
3. CVDG Parameter I/O Access (enabled by $\overline{IOCS}$ LOW)
4. MPU DRAM I/O Access (enabled by $\overline{DRCS}$ LOW)
5. Teletext Byte DMA (enabled by $\overline{TTXREQ}$ LOW)

The basic type of I/O access cycle is determined by the chip select ($\overline{IOCS}$ or $\overline{DRCS}$) and Teletext Request ($\overline{TTXREQ}$) inputs. When neither of the chip select inputs are LOW, nor has a TTX DMA transfer been initiated by $\overline{TTXREQ}$ LOW, the I/O access cycle is idle with no data transfer occurring during the processor portion of the A/D bus cycle.

When $\overline{IOCS}$ is LOW, the register address inputs (A0 and A1) and the mode selected in the CVDG Mode Register define the specific CVDG I/O operation, i.e., Mode/Status Register Access, CVDG Graphics Access (Mode 0), or one of the six CVDG Parameter Access modes (Modes 1-6). Table 4 shows the CVDG registers accessible during the I/O access cycle and the bit assignments. When A1 and A0 are both HIGH, the register bits are defined with reference to a pseudo Data Register (DR). The actual internal CVDG register accessed depends on the selected mode (see Table 4). The bits are defined in the following text.

CVDG Mode/Status Register Access

When $\overline{IOCS}$ is LOW and the register address is zero (A0 and A1 inputs are both LOW), the Mode Register (MR) or the Status Register (SR) is accessed depending upon the R/$\overline{W}$ input level. When R/$\overline{W}$ is LOW, the Mode Register is written; when R/$\overline{W}$ is HIGH, the Status Register is read.

Table 4. CVDG Register Summary

Internal CVDG Register	Mode	Register Select Lines A1	Register Select Lines A0	R/W[4]	Register Bit No. 7	6	5	4	3	2	1	0	Reset[3]
Mode Register	—	0	0	W	—	—	—	—	S	M2	M1	M0	0F
Status Register	—	0	0	R	$\overline{VB}$	$\overline{HB}$	M2	M1	M0	P	V1	V0	— —
X CDP Register	0	0	1	R/W	X7	X6	X5	X4	X3	X2	X1	X0	00
Y CDP Register	0	1	0	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	00
DRAM[1]	0	1	1	R/W	P3	P2	P1	P0	Q3	Q2	Q1	Q0	— —
LUT Address Register	1	1	1	W	XPE	RE	GE	BE	A3	A2	A1	A0	00
LUT[2]	2	1	1	R	—	—	—	—	D3	D2	D1	D0	— —
LUT Data Register	2	1	1	W	—	—	—	—	D3	D2	D1	D0	— —
Switch Register	3	1	1	W	NHS	S21	EXT	LS	TST	—	—	—	F8
Y Scroll Register	4	1	1	W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	00
TTX Pointer Register	5	1	0	R/W	A12	A11	A10	A9	A8	A7	A6	A5	00
DRAM Page Register	6	1	1	W	—	—	—	—	—	P	V1	V0	07

Notes:
1. The DRAM is directly accessed and not the CVDG.
2. Data is transferred from the LUT onto the A/D bus without going through the LUT Data Register.
3. Reset state upon power up.
4. R/W = Read/write (R = read only; W = write only; R/W = read or write).

Mode Register

The write-only Mode Register selects the CVDG mode for next read from, or write to, the CVDG. In addition, the Mode Register contains a submode flag applicable only to Mode 0. The Mode Register may be written at any time regardless of the current CVDG mode. The mode and submode bits are initialized to ones upon power up.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Mode	0	0	W	—	—	—	—	S	M2	M1	M0

MR7–MR4 Not used (no effect)

MR3 CDP Submode Flag (S) — (Mode 0 only—see Mode 0 description)

0 Enable CDP Nibble Submode. Allows read/write of a single 4-bit pixel nibble in a byte.

1 Enable CDP Byte Submode. Allows read/write of two 4-bit pixel nibbles in a byte with automatic increment of the X CDP for faster storage of LUT addresses in DRAM.

MR2–MR0 CVDG Mode (M2–M0)

(M2)	(M1)	(M0)	
0	0	0	Mode 0 — Port CDP Graphics
0	0	1	Mode 1 — LUT Address
0	1	0	Mode 2 — LUT Data
0	1	1	Mode 3 — Switch Register
1	0	0	Mode 4 — Y Scroll Offset Register
1	0	1	Mode 5 — Teletext DMA Pointer
1	1	0	Mode 6 — Set DRAM Page
1	1	1	Not used — no effect

Note that the mode must be written into the Mode Register before the desired mode can be executed.

Status Register

The read-only Status Register reports the selected CVDG mode, the selected DRAM page and the status of the horizontal and vertical raster blanking signals. The Status Register may be read at anytime regardless of the CVDG mode.

The horizontal blanking ($\overline{HB}$) and vertical blanking ($\overline{VB}$) signals report the state of the video raster at the time of access. The states of these two signals can be used for 15 kHz poll-driven timing, vertical blanking interval (VBI) identification, LUT loading, etc. These blanking times reflect the non-pixel display time including the time actual horizontal and vertical blanking signals are generated (for inclusion in composite sync output).

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Status	0	0	R	$\overline{VB}$	$\overline{HB}$	M2	M1	M0	P	V1	V0

SR7 Vertical Blanking ($\overline{VB}$)

0 Vertical blanking is asserted.

1 Vertical blanking is not asserted.

SR6 Horizontal Blanking ($\overline{HB}$)

0 Horizontal blanking is asserted.

1 Horizontal blanking is not asserted.

SR5–SR3 Mode Selected (M2–M0)

Reports the current CVDG mode as selected in bits 2–0 of the Mode Register.

SR5 (M2)	SR4 (M1)	SR3 (M0)	
0	0	0	Mode 0 — Port CDP Graphics
0	0	1	Mode 1 — LUT Address
0	1	0	Mode 2 — LUT Data
0	1	1	Mode 3 — Switch Register
1	0	0	Mode 4 — Y Scroll Offset Register
1	0	1	Mode 5 — Teletext DMA Pointer
1	1	0	Mode 6 — DRAM Page
1	1	1	Not used — no effect

SR2–SR0 DRAM Page Selected (P, V1, V0)

Reports the current DRAM Page selected in bits 2–0 of the Page Register (see Mode 6 — Write DRAM Page). P is the program RAM page indicator. V0 and V1 are the video page indicators.

SR2 (P)	SR1 (V1)	SR0 (V0)	Selected DRAM Page
0	0	0	Video Page 0: 8k-byte video RAM
0	0	1	Video Page 1: 8k-byte video RAM
0	1	0	Video Page 2: 8k-byte video RAM
0	1	1	Video Page 3: 2.3k-byte video RAM; 5.9k-byte program RAM
1	0	0	Program Page: 16k-byte optional program RAM accessed via $\overline{DRCS}$ (additionally paged by A13 and A0 inputs)

Mode 0 — Port CDP Graphics

When $\overline{IOCS}$ is LOW and Mode 0 is selected in the Mode Register, the Port Current Drawing Pointer (CDP) Mode is active. In this mode display column and row addresses can be written to the CVDG Current Drawing Pointer (CDP) X and Y registers, respectively, and pixel data accessed in DRAM. This mode is primarily used to update LUT addresses (i.e., the CDPs) in the video pages of DRAM. These LUT addresses are the video data read from the DRAM by the CVDG during the video portion of the A/D bus cycle.

This mode can be used to write or read data in any of the four 8k-byte video pages of DRAM defined by the V0 and V1 bits in the CVDG DRAM Page Register. The first three pages (V00, V01 and V10) are used exclusively for video data. 2304 bytes (addresses 0–8FF) of the fourth page (V11) are used for video data while the rest of the DRAM can be used for program or teletext message storage.

In mode 0, the MPU writes the address of the data in display coordinates into the CVDG X CDP and Y CDP registers. The X CDP contains the pixel position in the horizontal axis (i.e., the display column number) and varies from 0 to 255 (hex FF). Each pixel data nibble corresponds to a location (0 to 15) in the color look-up table (LUT) from which the corresponding R, G and B color levels and transparent bit data are retrieved for color generation. The Y CDP contains the pixel position in the vertical axis (i.e., the display row number) and varies from 0 to 255 (hex FF). Only values of 0 to 209 are used by the CVDG during the video portion of the A/D bus cycle to access video data. Y addresses 210–255 identify DRAM address on video DRAM page V11 that can contain non-displayable data, i.e., program or teletext data.

The registers accessible (besides in Mode and Status registers) in this mode are:

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
X CDP	0	1	R/W	X7	X6	X5	X4	X3	X2	X1	X0
Y CDP	1	0	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
DRAM*	1	1	R/W	P3	P2	P1	P0	Q3	Q2	Q1	Q0
*Not CVDG Access											

The X CDP Register is accessed at register address 1 (A1 = 0 and A0 = 1) and the Y CDP Register is accessed at register address 2 (A1 = 1 and A0 = 0). When register address 3 (A1 = 1 and A0 = 1) is detected, the CVDG generates DRAM row and column addresses corresponding to the display coordinates loaded in the X CDP and Y CDP registers. Data is then written from the A/D bus to the DRAM (R/$\overline{W}$ = low) or read from the DRAM to the A/D bus (R/$\overline{W}$ = high).

There are two submodes in Mode 0 that allow accessing of DRAM data at either the nibble (4-bit) or byte (8-bit) level. The submode is selected by the S bit (bit 3) in the Mode Register:

S = 0 CDP Nibble Submode
S = 1 CDP Byte Submode

CDP Nibble Submode

The CDP Nibble Submode (S = 0) reads or writes DRAM data one nibble at a time. Eight bits of data corresponding to two 4-bit LUT addresses (P3–P0 and Q3–Q0) are on the A/D data bus, but only one nibble is read or written during each access.

When writing the data, the Q nibble should contain the same pixel data as the P nibble. Only one of the nibble values is strobed into DRAM according to the X0 value in the X CDP Register which enables the $\overline{RASL}$ or $\overline{RASH}$ signal to DRAM during the write. If X0 = 0, the Q nibble (data bits 3–0) is written into the DRAM (row address strobed by $\overline{RASL}$); if X0 = 1, the P nibble (data bits 7–4) is written into the DRAM (row address strobed by $\overline{RASH}$).

When reading the data, only one nibble is read depending on the state of X0 in the X CDP. If X0 = 0, the Q nibble is read (row address strobed by $\overline{RASL}$); if X0 = 1, the P nibble is read (row address strobed by $\overline{RASH}$).

Reading or writing the data in this submode has no effect on the X CDP or Y CDP register values.

CDP Byte Access Submode

The CDP Byte Submode (S = 1) reads or writes two 4-bit LUT addresses at a time (in one byte) with an automatic increment of the X CDP value in the X CDP Register during write. Each write of the DRAM data writes the eight data bits on AD0–AD7 into DRAM and increments the X CDP by two upon the completion of the write cycle. (The new X CDP count can be read from the X CDP Register at any time.) As writing of the data continues, the X CDP value eventually wraps around to zero and continues incrementing. The Y CDP Register value must be incremented by writing a new Y CDP value. The automatic increment of X CDP value allows fast horizontal drawing for filling of polygon and rectangle type shapes (i.e., no intervening X CDP update is required). Note that the filled boundaries must be addressed by the horizontal line software since the X0 value has no effect in this submode.

This feature is useful for fast non-modulo 210 Y scrolling with quick reads/writes interleaved by old/new Y address updates. Note that when S = 1 in the Mode Register, the X0 value has no effect (the P nibble corresponds to X0 = 1 and the Q nibble corresponds to X0 = 0).

Reading of the DRAM data in this submode does not effect the X CDP count.

CVDG PARAMETER I/O ACCESS

Six CVDG Parameter Access modes allow the MPU to load control parameters into CVDG internal registers. Two of the modes also allow the MPU to read the parameter values from registers. The exact mode and access is controlled by the selected mode in the Mode Register and the register select input lines (A1 and A0).

Mode 1 — LUT Address

In Mode 1, data written to register address 3 (A1 = 1 and A0 = 1) is loaded into the LUT Address Register. Four bits control LUT write and read and the other four bits contain the actual LUT address. Bits 7–4 (XPE, RE, GE and BE) enable writing into, or reading from, corresponding sections of the LUT (i.e., XPAR, R, G and B) during Mode 2 access. Bits 3–0 in the register contain the LUT address (0–15) accessed during Mode 2.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
LUT Address	1	1	W	XPE	RE	GE	BE	A3	A2	A1	A0

DR7 Transparent Enable (XPE)

0 Disable XPAR write or read
1 Enable XPAR write or read

DR6 Red Enable (RE)

0 Disable R write or read
1 Enable R write or read

DR5 Green Enable (GE)

0 Disable G write or read
1 Enable G write or read

DR4 Blue Enable (BE)

0 Disable B write or read
1 Enable B write or read

DR3-DR0 LUT Address (A3-A0)

DR3 (A3)	DR2 (A2)	DR1 (A1)	DR0 (A0)	
0	0	0	0	LUT address 0
0	0	0	1	LUT address 1
	.	.	.	
1	1	1	1	LUT address 15

The LUT address in the LUT Address Register, rather than the LUT addresses read from DRAM, is also used to lookup the color level code in the LUT during the active display time (border and/or pixel) in two circumstances:

1. Outside the 256 x 210 graphics area, i.e., to generate the border color. Note that programs loading the LUT during the vertical blanking interval (VBI) must restore the address of the border color in the LUT into the LUT Address Register prior to unblanking.
2. Within the 256 x 210 graphics area when the LS bit = 0 in the Switch Register.

Mode 2 — LUT Data

In Mode 2, LUT data (i.e., color levels and transparent state) written to, or read from, register address 3 (A1 = 1, A0 = 1) is loaded into, or read from the LUT at the LUT address contained in the LUT Address Register. Only the section (R, G, B and/or XPAR codes) of the LUT entry enabled by bits 7-4 in the LUT Address Register are accessed. Normally only one enable bit at a time is set to a 1. During a write, data will be written into each LUT section enabled. During a read, ambiguous data will be accessed if more than one enable bit is set.

The transparent state (XPAR) is only one bit (D3). The other three data bits (D2-D0) are don't care.

During a write, the data on the A/D bus is written into the CVDG LUT Data Register. The LUT Address Generator latches the 4-bit LUT address from the LUT Data Register rather than from the Video Shift Register. The LUT Address Generator then generates the 16-bit binary address for routing to the LUT. The LUT is loaded in a similar manner as described for pixel color generation.

During a read, data is transferred from the LUT directly to the A/D bus without going through the LUT Data Register. XPAR is not availabe for readback.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
LUT Data*	1	1	R/W	—	—	—	—	D3	D2	D1	D0

*During a read, data is transferred directly from LUT to A/D bus without going through LUT Data Register.

DR7-DR4 Not used (no effect)

DR3-DR0 Color Level Code or Transparent Bit State

D3	D2	D1	D0	R, G or B Color Output Level
0	0	0	0	Color output level 0
0	0	0	1	Color output level 1
		.		.
1	1	1		Color output level 15
D3	**D2**	**D1**	**D0**	**XPAR Output Level**
0	X	X	X	XPAR output LOW
1	X	X	X	XPAR output HIGH (X = no effect)

Mode 3 — Switch Register

In Mode 3, switch position data (represented by bit states) written to register address 3 (A1 = 1, A0 = 1) is loaded into the CVDG Switch Register. Three bits control video raster operation, one bit controls the LUT address access source, and one bit enables the CVDG test mode. All five bits are set to a 1 by power up.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Switch	1	1	W	NHS	S21	EXT	LS	TST	—	—	—

DR7 Normal Horizontal Sync (NHS) Select

0 Early 15.9 kHz ($\overline{\text{HSYNC}}$) Output
1 Normal 15.7 kHz $\overline{\text{HSYNC}}$ Output

DR6 2:1 Interlace Select (S21)

0 1:1 interlace
1 2:1 interlace

DR5 External Sync Select (EXT)

0 Internal sync output on $\overline{\text{VSYNC}}$ ($\overline{\text{C/HSYNC}}$ output enabled.
1 External sync input on $\overline{\text{VSYNC}}$ ($\overline{\text{C/HSYNC}}$ output disabled)

DR4 LUT Address Select (LS)

0 Select the LUT Address Register as the LUT address source
1 Select Video Shift Register data as LUT address source

DR3 Test Mode Select (TST)

0 Normal mode; Vertical state machine (VSM) and Y address counter (YAC) run at normal rate
1 Test mode; VSM and YAC run at 1.413 MHz (used for factory test only)

Mode 4 — Y Scroll Register

In Mode 4, a Y scroll offset value written to register address 3 (A1 = 1, A0 = 1) is loaded into the Y Scroll Register. The Y scroll offset may vary from 0 to 209 (decimal). The value written defines the first horizontal row to be displayed at the top of the 256 x 210 graphics image area.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Y Scroll	1	1	W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

DR7–DR0 Y Scroll Offset

0000000 Offset = 0
0000001 Offset = 1
. .
. .
. .
11010001 Offset = 209 (maximum allowed)

Mode 5 — Teletext DMA Pointer

In Mode 5, an 8-bit Teletext pointer written to register address 2 (A1 = 1, A0 = 0) is loaded into the TTX Pointer Register and Counter. The pointer, consisting of address bits A12–A5 specifies the starting address on a 32-byte boundary for the DMA transfer of teletext data into video page 3 of DRAM. During a teletext DMA data transfer, the Modulo 32 Teletext Counter is incremented by one upon each DMA byte transfer. The TTX Pointer Register is incremented by one every 32 bytes. The value of the Teletext Pointer can be read at any time in Mode 5.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
Teletext Pointer	1	0	R/W	A12	A11	A10	A9	A8	A7	A6	A5

The status of the P, V1 and V0 in the Mode/Status Register are unchanged during a Teletext DMA data transfer.

Mode 6 — Set DRAM Page

In Mode 6, data written to register address 3 (A1 = 1, A0 = 1) is loaded into the DRAM Page Register. The data contains a 3-bit DRAM page select code and five unused bits (don't care). These DRAM page select bits specify the 8k-byte DRAM page accessed during a MPU DRAM access ($\overline{DRCS}$ = low) when A13 input is LOW. The DRAM page bits can be read from the Status Register at any time.

				Bit Position							
Register	A1	A0	R/W	7	6	5	4	3	2	1	0
DRAM Page	1	1	W	—	—	—	—	—	P	V1	V0

DR7–DR3 Not Used (no effect)

DR2–DR0 Selected DRAM Page

DR2 (P)	DR1 (V1)	DR0 (V0)	
0	0	0	Video Page 0: 8k-byte video RAM
0	0	1	Video Page 1: 8k-byte video RAM
0	1	0	Video Page 2: 8k-byte video RAM
0	1	1	Video Page 3: 2.3k-byte video RAM; 5.9k-byte program RAM
1	0	0	Program Page 0: 16k-byte optional program RAM accessed via $\overline{DRCS}$ (additionally paged by A13 and A0 inputs)

MPU DRAM I/O ACCESS

When $\overline{DRCS}$ is LOW, the MPU directly accesses the DRAM in an address map manner. The MPU generates the DRAM row and column addresses (except for two column address lines which are driven by the CVDG). The CVDG drives the AD5 and AD6 lines during DRAM column address time and also outputs control signals ($\overline{RTIME}$, $\overline{CTIME}$ and $\overline{DTIME}$) to enable external A/D bus buffers. MPU address line A1–A8 are enabled onto A/D bus lines AD0–AD7, respectively, by $\overline{RTIME}$ to drive the DRAM row address. MPU address line A9–A12 are enabled onto A/D bus lines AD1–AD4, respectively, by $\overline{CTIME}$ to drive the DRAM column address. The CVDG drives AD5 and AD6 with one of two sets of signals during $\overline{CTIME}$. External bidirectional data line buffers are enabled by $\overline{DTIME}$ in the direction controlled by the MPU R/$\overline{W}$ output to transfer data between the MPU data bus lines D0–D7 and A/D bus lines AD0–AD7.

A13 input high causes program DRAM to be accessed during the processor portion of the A/D bus independent of the P bit value in the DRAM Page Register. $\overline{CASP}$ is asserted in response to the A13 HIGH to strobe the column address lines into program DRAM.

When A13 input is LOW, the section of DRAM accessed depends on the P bit value in the DRAM Page Register and the A0 input. If P = 0, video DRAM is accessed; $\overline{CAS1}$ is generated when A0 is LOW and $\overline{CAS2}$ is generated when A0 is HIGH. If P = 1, program DRAM is accessed since $\overline{CASP}$ is generated instead of $\overline{CAS1}$ or $\overline{CAS2}$ to strobe the DRAM column address.

The AD5 and AD6 outputs are driven by the CVDG during DRAM column address generation in the processor portion of the A/D bus cycle as controlled by the P bit in the DRAM Page Register. If video DRAM is selected (P = 0), the V0 and V1 bits in the DRAM Page Register are output on AD5 and AD6, respectively. If program DRAM is selected (P = 1), the A0 and A13 inputs are output on AD5 and AD6, respectively.

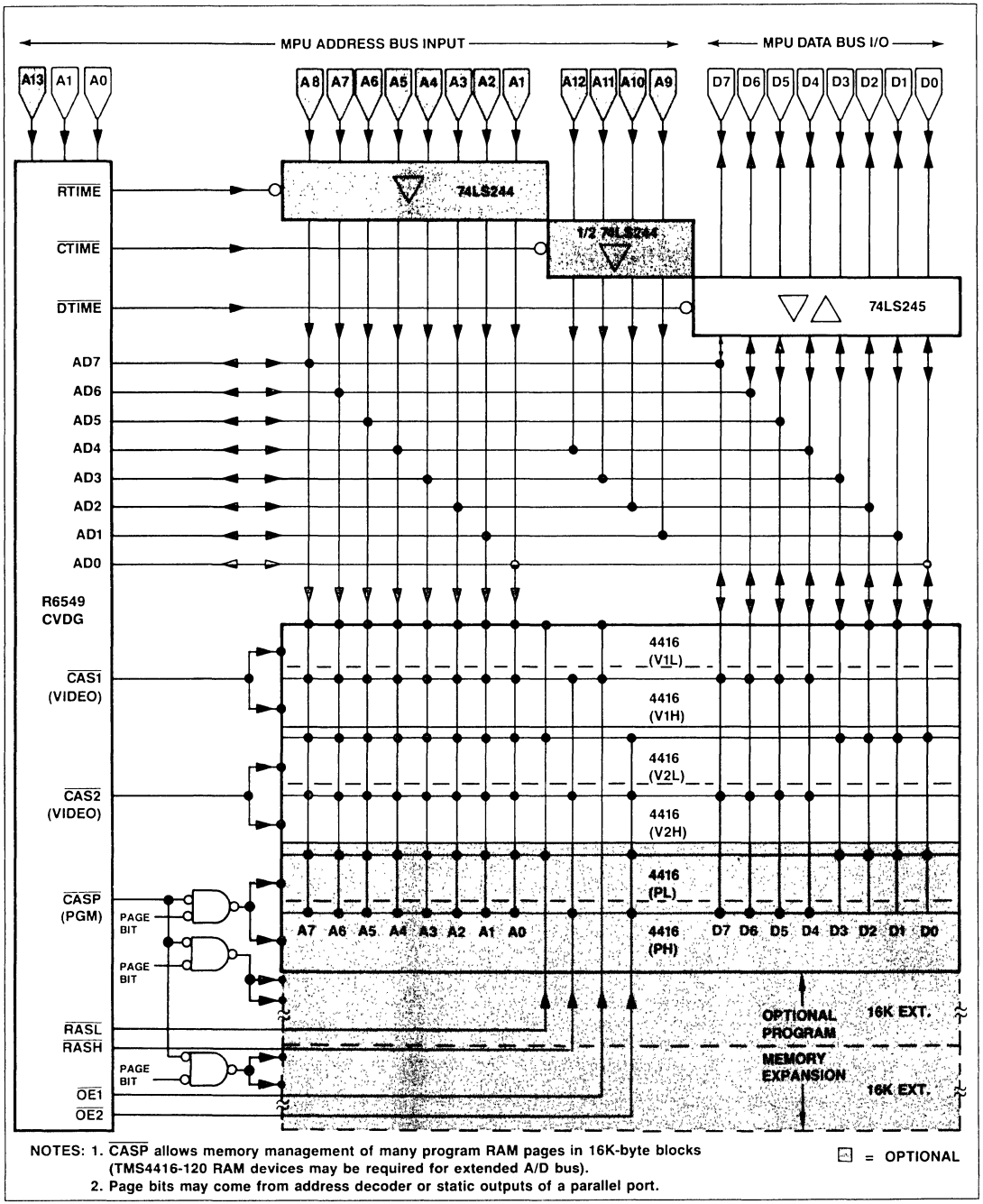
Note that the DRAM requires assertion of all three control signals for a valid access (i.e., $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$ for a read and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ for a write). The CVDG sometimes outputs one or two of these signals but not all three control signals in "no access" situations.

TELETEXT DMA I/O ACCESS

Teletext data can be DMA transferred from a teletext prefix processor connected to the A/D bus to DRAM locations addressed by the CVDG. A 13-bit TTX Latch/Counter determines the DRAM address. The upper 8-bits of the TTX Counter is a latch. The value of the latch is defined by the TTX Pointer Register which can be loaded in Mode 5 by writing to register address 2 (A1 = 1 and A0 = 0). The TTX Pointer Register value therefore defines the TTX DMA starting address on a 32-byte boundary. The lower 5-bits of the TTX Latch/Counter is a modulo 32 counter. This counter increments by one after each TTX byte transfer. When the counter overflows (i.e., from 31 to 0) the upper count is incremented by one to increment the total address. The address is reset to zero during horizontal blanking. The upper count may be read from the TTX Pointer Register at any time in Mode 5.

TTX DMA transfer is initiated by asserting $\overline{\text{TTXREQ}}$ to the CVDG. The CVDG asserts TTX Output Enable ($\overline{\text{TTXOE}}$) to acknowledge $\overline{\text{TTXREQ}}$ receipt, suspends outputting the E and Q clocks for one cycle, outputs the 13-bit DRAM address and asserts DRAM Write Enable ($\overline{\text{W}}$) to enable writing into DRAM.

Note that DMA must be used only when the horizontal sync is genlocked to the external teletext raster.



NOTES: 1. $\overline{\text{CASP}}$ allows memory management of many program RAM pages in 16K-byte blocks (TMS4416-120 RAM devices may be required for extended A/D bus).
2. Page bits may come from address decoder or static outputs of a parallel port.

[ ] = OPTIONAL

Figure 6. CVDG Connection to A/D Bus and DRAM

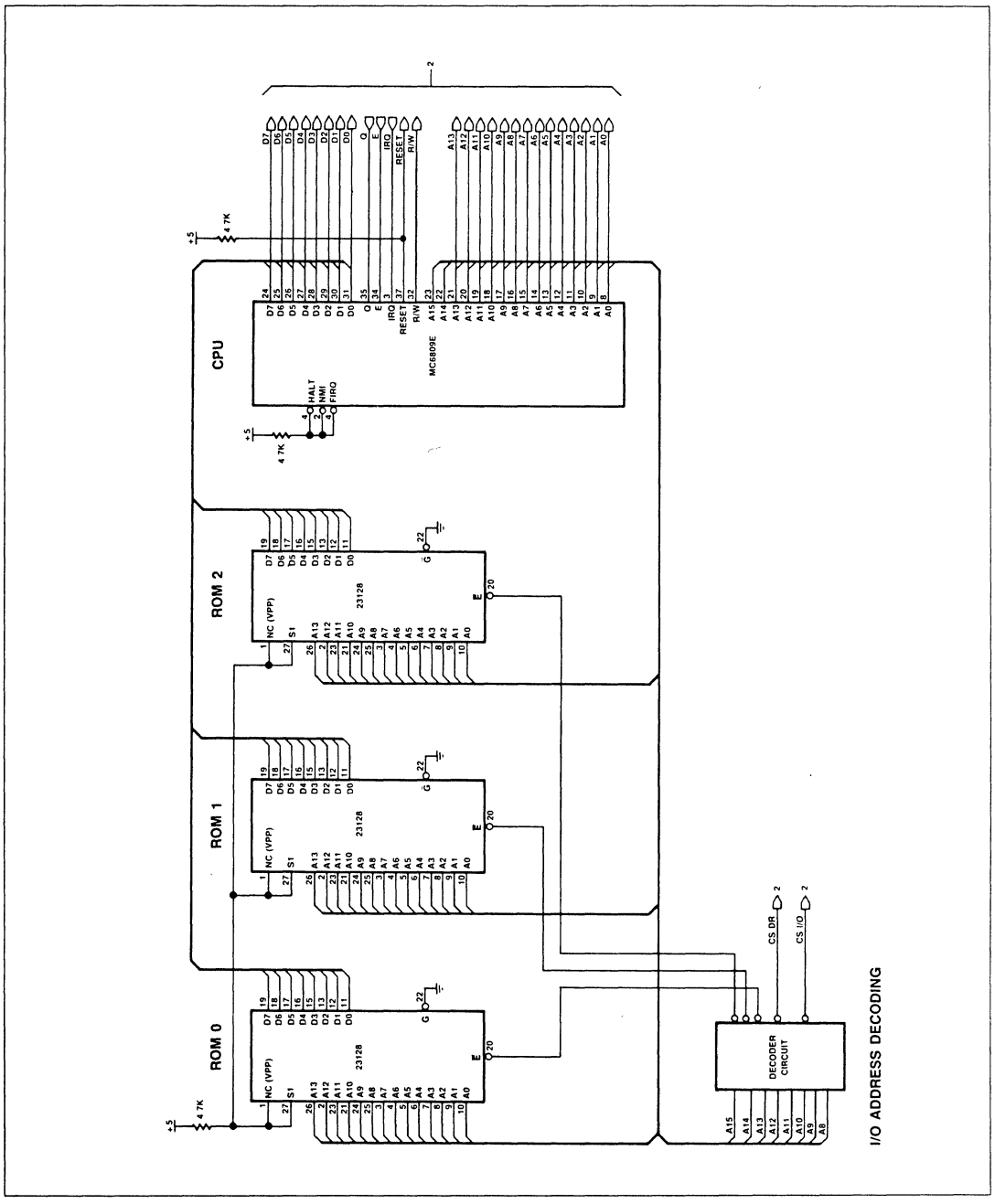


Figure 7. CVDG Application Schematic (Typical) (Sheet 1 of 2)

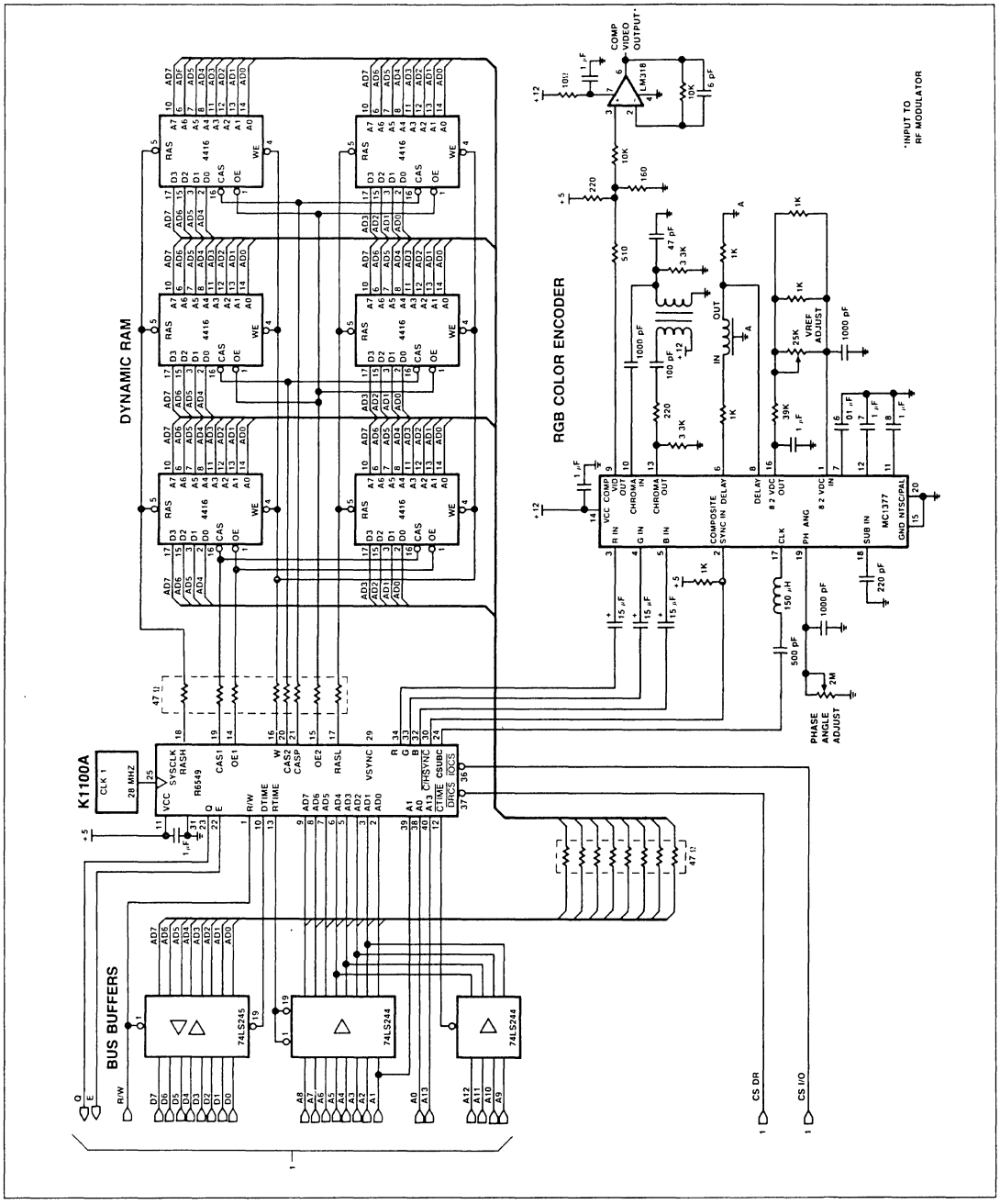


Figure 7. CVDG Application Schematic (Typical) (Sheet 2 of 2)

AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0)

MPU CLOCK AND CONTROL LINE TIMING

Ref. Fig. 8 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{ECYC}	E Cycle Time	700	698		ns	1
2	t_r, t_f	E and Q Rise and Fall		25		ns	
3	t_{ELEH}	E Low to E High		350		ns	
4	t_{EHEL}	E High to E Low		350		ns	
5	t_{ELQH}	E Low to Q Rising		175		ns	
6	t_{QHEH}	Q High to E Rising		175		ns	
7	t_{EHQL}	E High to Q Falling		175		ns	
8	t_{QLEL}	Q Low to E Falling		175		ns	
9	t_{SLEH}	Chip Select Low to E Rising (Setup)		70		ns	
10	t_{SHEH}	Chip Select High to E Rising (Hold)		0		ns	
11	t_{EHQV}	E High to Data Valid (Read)			240	ns	
12	t_{ELQZ}	E Low to Output High Z (Read)		10		ns	
13	t_{DVEL}	Data Valid to E Falling (Write)	100			ns	
14	t_{ELDZ}	E Falling to Data Invalid (Write)		30		ns	

Note:
1. Based on 28.636363 MHz SYSCLK input.

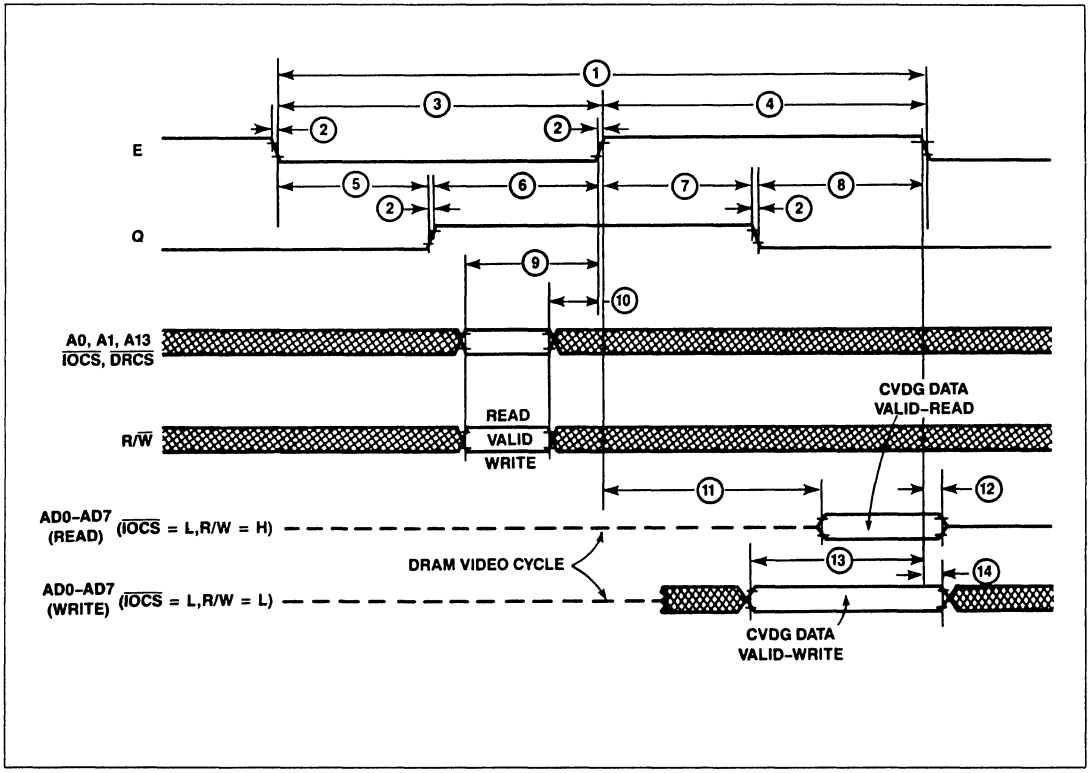


Figure 8. CVDG-MPU A/D Bus Timing Waveforms

DRAM TIMING — VIDEO ACCESS CYCLE

Ref. Fig. 9 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{RLRTL}	$\overline{RAS}$ Low to $\overline{RTIME}$ Low (Delay)		315		ns	
2	t_{RTLRTH}	$\overline{RTIME}$ Low to $\overline{RTIME}$ High		70		ns	
3	t_{RLCTL}	$\overline{RAS}$ Low to $\overline{CTIME}$ Low (Delay)		35		ns	
4	t_{CTLCTH}	$\overline{CTIME}$ Low to $\overline{CTIME}$ High		87		ns	
5	t_{RLDTL}	$\overline{RAS}$ Low to $\overline{DTIME}$ Low (Delay)		122		ns	
6	t_{DTLDTH}	$\overline{DTIME}$ Low to $\overline{DTIME}$ High		157		ns	
7	t_{RC}	RAM Read/Write Cycle		350		ns	
8	t_{RP}	$\overline{RAS}$ High Width		105		ns	
9	t_{RAS}	$\overline{RAS}$ Low Width		245		ns	
10	t_{RCD}	$\overline{RAS}$ Low to $\overline{CAS}$ Low (Delay)		70		ns	
11	t_{CAS}	$\overline{CAS}$ Low Width		245		ns	
12	t_{CSH}	$\overline{RAS}$ Low to $\overline{CAS}$ Rising (Delay)		315		ns	
13	t_{RSH}	$\overline{CAS}$ Low to $\overline{RAS}$ Rising (Delay)		175		ns	
14	t_{CPN}	$\overline{CAS}$ High Width		105		ns	
15	t_{CRP}	$\overline{CAS}$ High to $\overline{RAS}$ Falling (Delay)		35		ns	
16	t_t	$\overline{RAS}$ and $\overline{CAS}$ Transition Times		5		ns	
17	t_{RCS}	Read Command Setup		105		ns	
18	t_{ASR}	Row Address Setup		35		ns	
19	t_{RAH}	Row Address Hold		35		ns	
20	t_{ASC}	Column Address Setup		35		ns	
21	t_{CAH}	Column Address Hold		70		ns	
22	t_{AR}	$\overline{RAS}$ Low to Column Hold		140		ns	
23	t_{RAC}	$\overline{RAS}$ Low to Data Valid (Setup)			150	ns	
24	t_{CAC}	$\overline{CAS}$ Low to Data Valid (Setup)			80	ns	
25	t_{RLG1L}	$\overline{RAS}$ Low to $\overline{OE1}$ Low (Delay)		140		ns	
26	t_{GLGHr}	$\overline{OE}$ Low to $\overline{OE}$ High		70		ns	
27	t_{OEA}	$\overline{OE}$ Low to Data Valid (Setup)	0		40	ns	
28	t_{OEZ}	$\overline{OE}$ High to Output High Z (Hold)	0		35	ns	
29	t_{RLG2L}	$\overline{RAS}$ Low to $\overline{OE2}$ Low (Delay)		210		ns	

DRAM TIMING — MPU DRAM ACCESS CYCLE

Ref. Fig. 9 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
30	t_{RRH}	Read Command Hold After $\overline{RAS}$ High		280		ns	
31	t_{RCH}	Read Command Hold After $\overline{CAS}$ High		210		ns	
33	t_{GLGH}	$\overline{OE1}$, $\overline{OE2}$ Low to $\overline{OE1}$, $\overline{OE2}$ High		140		ns	
36	t_{DS}	Data Setup		12		ns	
37	t_{WP}	$\overline{W}$ Low to $\overline{W}$ High		140		ns	
38	t_{DH}	Data Hold After $\overline{W}$ Low		70		ns	
39	t_{DHC}	Data Hold After $\overline{CAS}$ Low		175		ns	
40	t_{DHR}	Data Hold After $\overline{RAS}$ Low		245		ns	
41	t_{WCR}	Write Command Hold After $\overline{RAS}$ Low		315		ns	
42	t_{WCH}	Write Command Hold After $\overline{CASP}$ Low		245		ns	
43	t_{RWL}	Write Command Setup before $\overline{RAS}$ Rising		70		ns	
44	t_{CWL}	Write Command Setup before $\overline{CAS}$ Rising		140		ns	

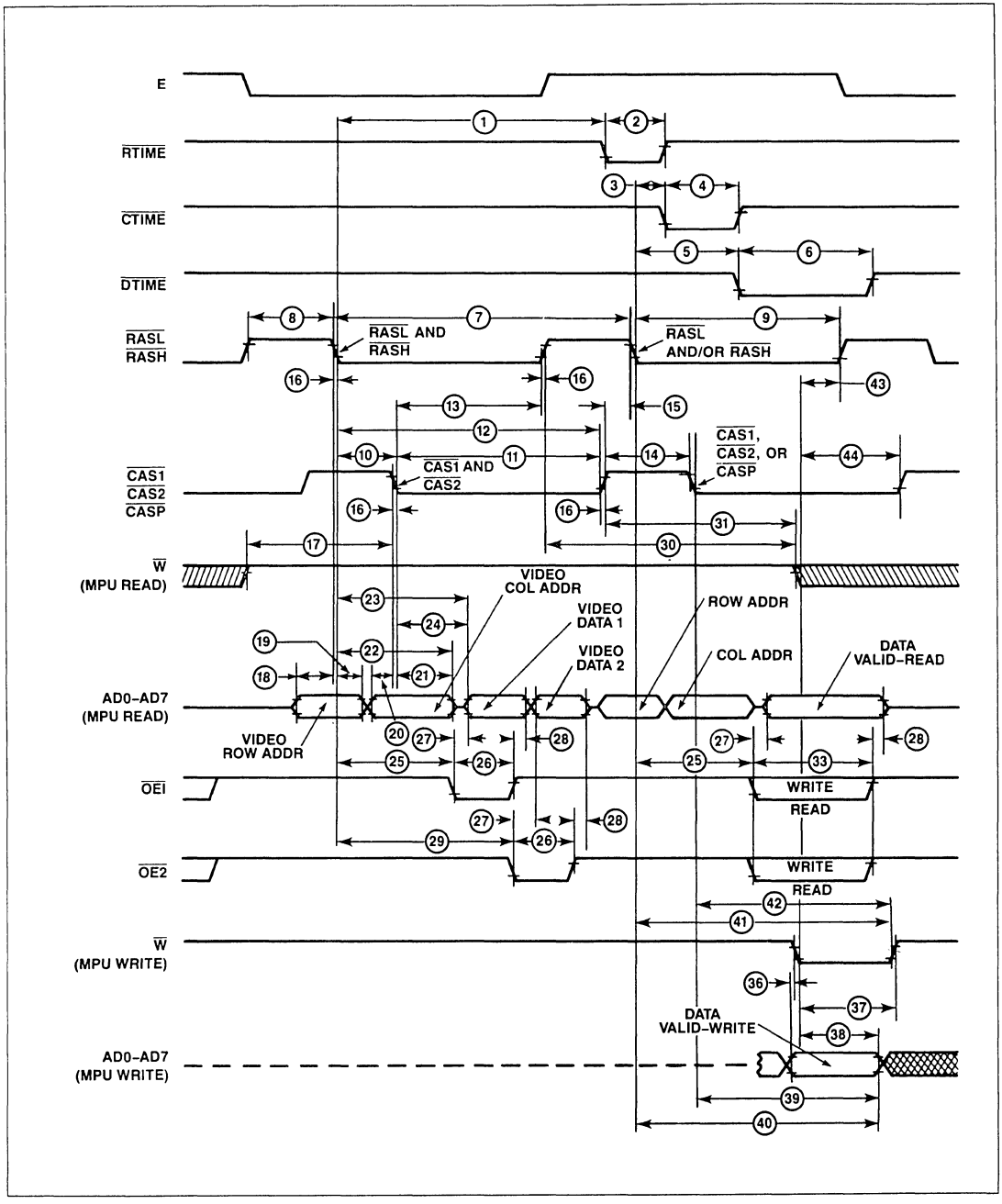


Figure 9. CVDG-DRAM A/D Bus Timing Waveforms

TELETEXT DMA CYCLE TIMING

Ref. Fig. 10 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{RLEL}	$\overline{TTXREQ}$ Low to E Low (Setup)		80		ns	
2	t_{ELRH}	E Low to $\overline{TTXREQ}$ High (Hold)		10		ns	
3	t_{ELGL}	E Low to $\overline{TTXOE}$ Low		595		ns	
4	t_{GLGH}	$\overline{TTXOE}$ Low to $\overline{TTXOE}$ High		140		ns	

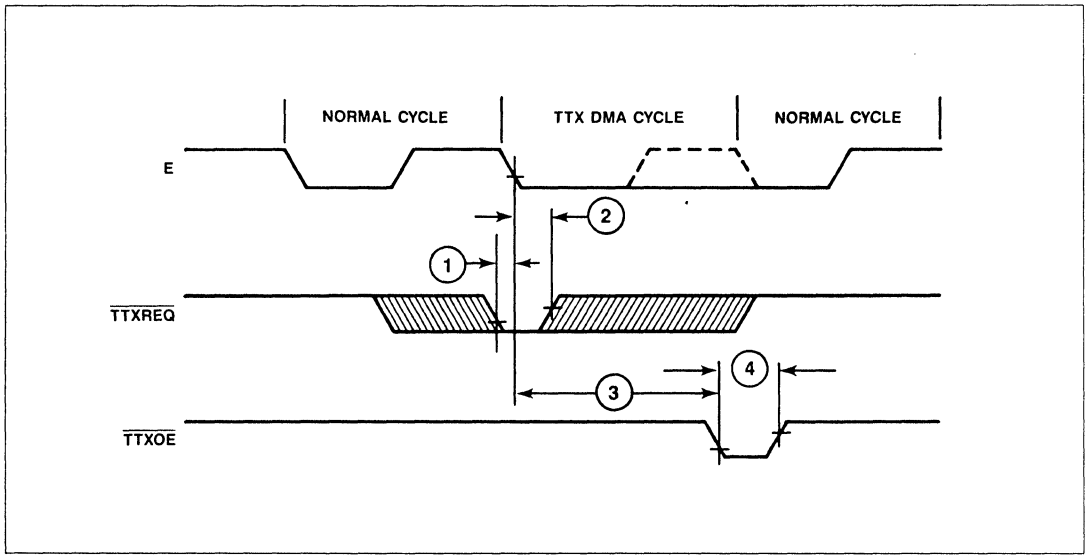


Figure 10. Teletext Prefix Processor — CVDG Timing Waveforms

HORIZONTAL VIDEO TIMING

Ref. Fig. 11 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1		H Sync to Setup	9.3	9.4	9.5	μs	1
2		H Front Porch	1.4	1.5	1.6	μs	1
3		H Sync to XPAR	—	10.16	—	μs	2
4		XPAR Front Porch	—	2.79	—	μs	2
5		H Sync to Border 1	—	8.38	—	μs	2
6		H Sync to Graphics	—	12.57	—	μs	2
7		H Sync to Border 2	—	57.27	—	μs	2
8		Border Front Porch	—	2.79	—	μs	2
9		H Sync Tip	—	4.81	—	μs	2
10		H Period (Normal)	—	63.556	—	μs	2
11		H Period (Early)	—	62.857	—	μs	2

Notes: 1. RS-170A Specification (shown for reference only).
2. ±0.1μs; based on 28.636363 MHz SYSCLK input.

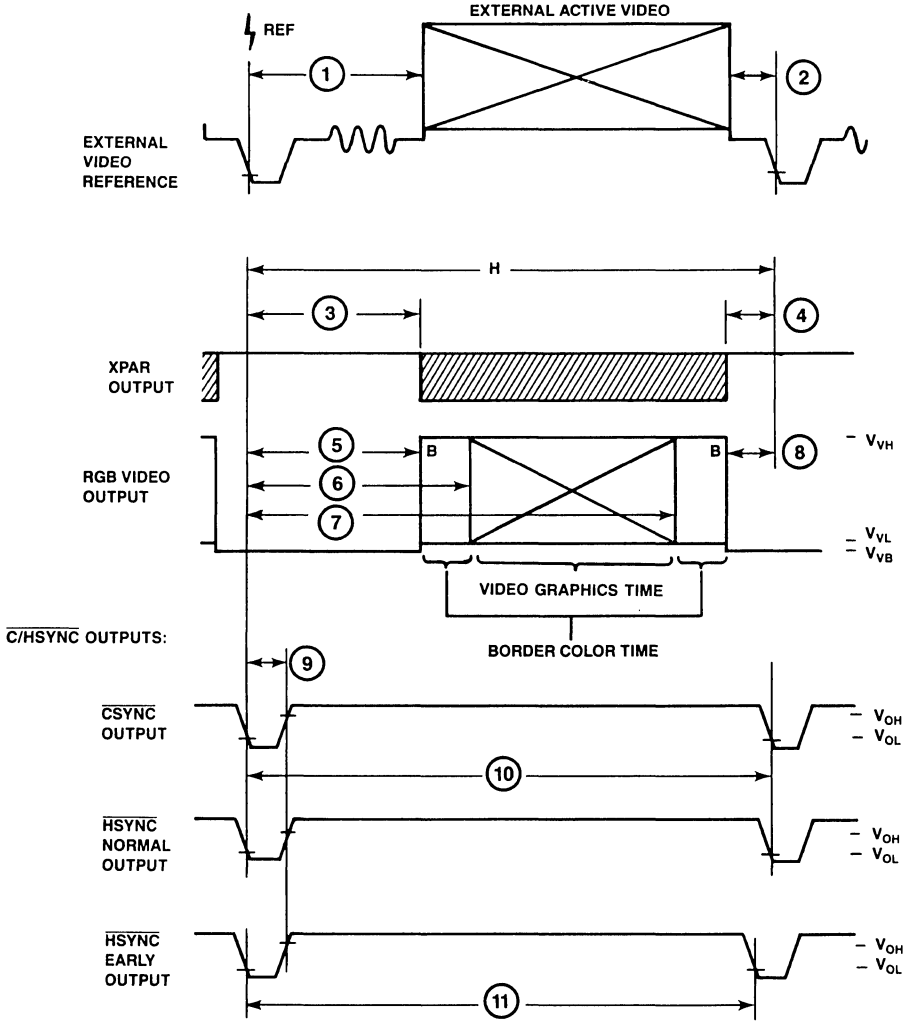
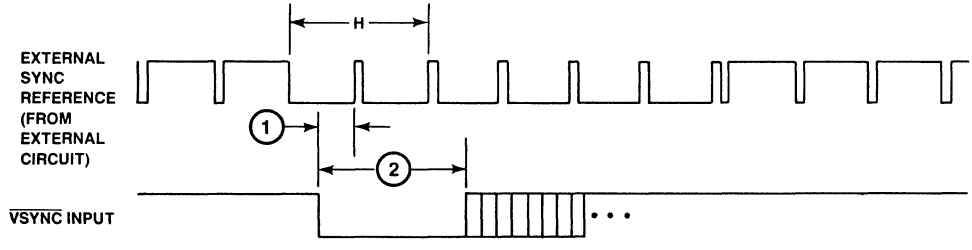


Figure 11. Horizontal Video Output Timing Waveforms

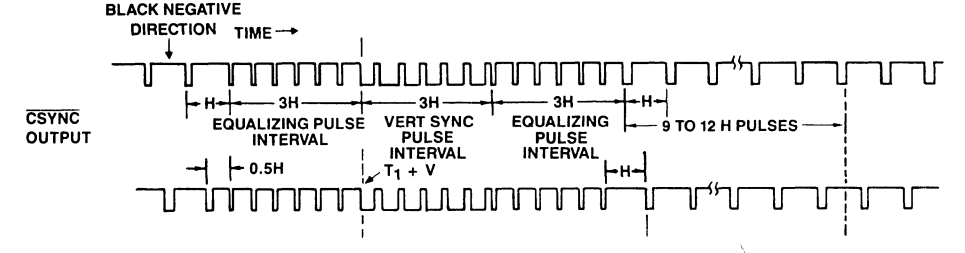
Vertical Cycle Timing

Ref. Fig. 12 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	V_{SU}	$\overline{VSYNC}$ Low Input to First Serration Setup	20	—	—	ns	3
2	V_H	$\overline{VSYNC}$ Low Input Pulse Duration	63.5	—	—	μs	3
—		$\overline{VSYNC}$ Low Output Pulse Duration (Burst Blank)	19	—	—	H	1
—		V Blank Duration	52	—	—	H	1
—		V Unblank to Graphics Duration (Top Border)	21	—	—	H	1
—		Graphics to V Blank Duration (Bottom Border)	31	—	—	H	1, 2

Notes: 1. H = $\overline{HSYNC}$ pulse width (63.5 μs)
2. 2:1 interlace mode.
3. Shown for reference only—not an R6549 requirement.



a. Vertical Synchronization



b. RS-170A Composite Sync VBI Timing Specifications

Figure 12. Vertical Cycle Waveforms—2:1 Interlace

TELETEXT DMA CYCLE TIMING

Ref. Fig. 13 No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	t_{ELPL}	E Low to PIXCK High		0		ns	
2	t_{PHPL}	PIXCK High to PIXCK Low		70		ns	
3	t_{PLPH}	PIXCK Low to PIXCK High		105		ns	
4	t_{PCYC}	PIXCK Cycle		175		ns	

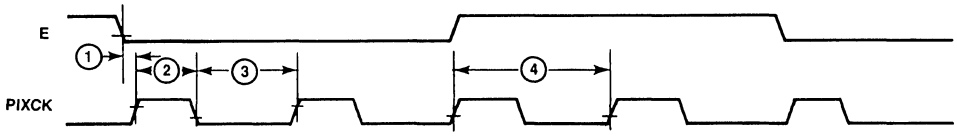


Figure 13. Video Output Waveforms

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage					V	
SYSCLK	V_{IHC}	V_{CC} - 0.75	—	V_{CC}		
$\overline{IOCS}$, $\overline{DRCS}$, $\overline{TTXREQ}$, A0, A1, A13, R/$\overline{W}$, $\overline{VSYNC}$, AD0-AD7	V_{IH}	V_{SS} + 2.0	—	V_{CC}		
Input Low Voltage					V	
SYSCLK	V_{ILC}	V_{SS} - 0.3	—	V_{SS} + 0.4		
$\overline{IOCS}$, $\overline{DRCS}$, $\overline{TTXREQ}$, A0, A1, A13, R/$\overline{W}$ $\overline{VSYNC}$, AD0-AD7	V_{IL}	V_{SS} - 0.3	—	V_{SS} + 0.8		
Input Leakage Current	I_{IL}	—	—	±10	μA	V_{IN} = 0V to 5.25V V_{CC} = 0
Output High Voltage	V_{OH}				V	V_{CC} = 4.75V
E		V_{CC} - 0.75	—	—		I_{OH} = -0.14 mA Note 1
Q, $\overline{RTIME}$, $\overline{CTIME}$, $\overline{DTIME}$, $\overline{RASL}$, $\overline{RASH}$, $\overline{W}$ $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$, $\overline{OE1}$, $\overline{OE2}$, $\overline{TTXOE}$, C/$\overline{HSYNC}$, $\overline{VSYNC}$, CSUBC, PIXCK, XPAR		V_{SS} + 2.4	—	—		I_{OH} = -80 μA Note 2
AD0-AD7		V_{SS} + 2.4	—	—		I_{OH} = -170 μA Note 3
Output Low Voltage	V_{OL}				V	V_{CC} = 4.75V
E		—	—	V_{SS} + 0.4		I_{OL} = 1.7 mA Note 1
Q, $\overline{RTIME}$, $\overline{CTIME}$, $\overline{DTIME}$, $\overline{RASL}$, $\overline{RASH}$, $\overline{W}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CASP}$, $\overline{OE1}$, $\overline{OE2}$, $\overline{TTXOE}$, C/$\overline{HSYNC}$, $\overline{VSYNC}$, CSUBC, PIXCK, XPAR		—	—	V_{SS} + 0.4		I_{OL} = 1.6 mA Note 2
AD0-AD7		—	—	V_{SS} + 0.4		I_{OL} = 3.0 mA Note 3
Output Leakage Current (Off-State) AD0-AD7	I_{OFF}	—	—	±20	μA	V_{IN} = 0 to 5.25V
Output High Voltage R, G, B	V_{VH}	—	+2.800	—	V	C_L = 30 pF R_L = 10K Ohms t_r/t_f = 50 ns
Output Low Voltage R, G, B	V_{VL}	—	+1.875	—	V	
Output Blanking Voltage R, G, B	V_{VB}	—	+1.800	—	V	
Input Capacitance[4]	C_{IN}				pF	V_{CC} = 5.0V, chip
SYSCLK		—	—	10		deselected, pin
$\overline{IOCS}$, $\overline{DRCS}$, $\overline{TTXREQ}$, A0, A1, A13, R/$\overline{W}$, $\overline{VSYNC}$, AD0-AD7		—	—	5		Under test at 0V, T_A = 25°C, f = 0.986 MHz (SYSCLK = 28.6363 MHz)

Notes:
1. Output Load: 1 TTL gate; C_L = 140 pF
2. Output Load: 1 TTL gate; C_L = 100 pF
3. Output Load: 6 DRAM, 2 LS244 buffers and 1 LS245 transceiver; C_L = 180 pF
4. This parameter is periodically sampled and is not 100% tested.

ABSOLUTE MAXIMUM RATINGS*

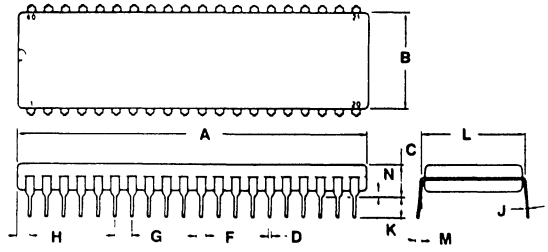
Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltages	V_{IN}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE DIMENSIONS

2

40-PIN PLASTIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040