Rockwell

R65C10
One-Chip Microcomputer

SECTION I
INTRODUCTION

SUMMARY

The Rockwell R65C10 microcomputer is a complete 8-bit computer fabricated on a single chip using an N-well silicon gate CMOS process. The R65C10 complements an industry standard line of R6500 and R65C00 microprocessors, R6500/* and R65C00/* microcomputers and compatible peripheral devices. The R65C10 has a wide range of microcomputer applications where high 8-bit performance, minimal chip count and low power consumption is required.

The R65C10 consists of a 6502 Central Processing Unit (CPU), 2048 bytes of mask programmable Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and interface circuitry for peripheral devices. The parallel interface consists of four 8-bit ports including two edge detect lines. A 16-bit counter/timer with four selectable modes is also included.

The innovative architecture and the demonstrated high performance of the R65C02 CPU, as well as instruction simplicity, result in system cost-effectiveness and a wide range of computational power. These features make the R65C10 a leading candidate for low-power single-chip microcomputer applications.

Hardware enhancements of the R65C10 include a software-controlled system and/or counter/timer clock prescaler, and an ultra-low-power Stop mode.

This description assumes that the reader is familiar with the R6502 CPU programming capabilities as described in the R6500 Programming Manual (Order No. 202).

ORDERING INFORMATION

R65C10

- Temperature Range
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Operating Frequency (Internal Ø2 clock)
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package
  - C = 40-pin CERDIP
  - P = 40-pin Plastic DIP
  - J = 44-pin Plastic Leaded Chip Carrier (PLCC)

FEATURES

- Single-chip microcomputer
- R6502 CPU instruction compatible
- 8-bit parallel processing
- Decimal or binary arithmetic
- Variable length stack
- True indexing capability
- 13 addressing modes
- Internal 1 MHz to 4 MHz clock with crystal or clock input
  - — Internal divide-by-2 network
  - — 2 MHz to 8 MHz crystal input
  - — 20 kHz to 8 MHz clock input
- Software-controllable prescaler
  - — Selectable system clock and timer clock prescaler or timer clock only prescaler
  - — Divide by 8, 32, 64, or 128 options
- Low-power oscillator Stop mode (cleared by $\overline{RES}$)
- 15 mW to 60 mW operating power (1 MHz to 4 MHz)
- 2K × 8 ROM on-chip
- 64 × 8 RAM on-chip
- 32 bidirectional TTL compatible I/O lines
  - — 1 positive edge-sensitive I/O line
  - — 1 negative edge-sensitive I/O line
- 1 bidirectional TTL compatible counter I/O line
- 16-bit buffered timer/counter with four modes
  - — Interval timer
  - — Pulse generator
  - — Event counter
  - — Pulse width measurement
- Three maskable interrupt requests (IRQ)
  - — 1 counter overflow
  - — 2 I/O edge detect
- $\overline{NMI}$ and $\overline{RES}$ inputs
- Available in 40-pin DIP and 44-pin PLCC packages
- +5V ±10% power

SECTION 2
INTERFACE DESCRIPTION

This section describes the interface requirements for the R65C10 single-chip microcomputer. An interface diagram for the R65C10 is shown in Figure 2-1. The R65C10 pin assignments are identified in Figure 2-2. The function of each pin of the R65C10 is explained in Table 2-1.

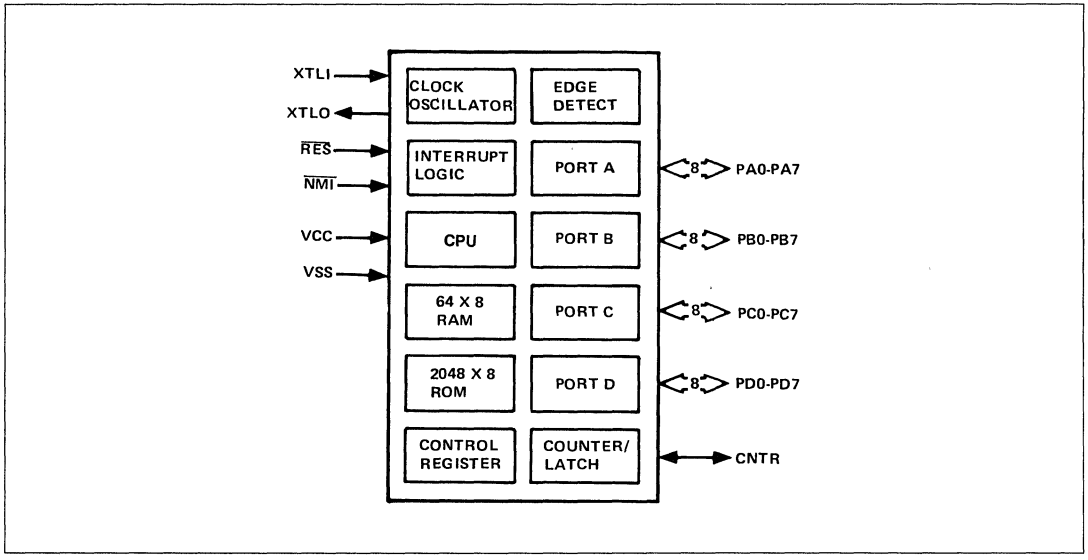


Figure 2-1. R65C10 Interface Diagram

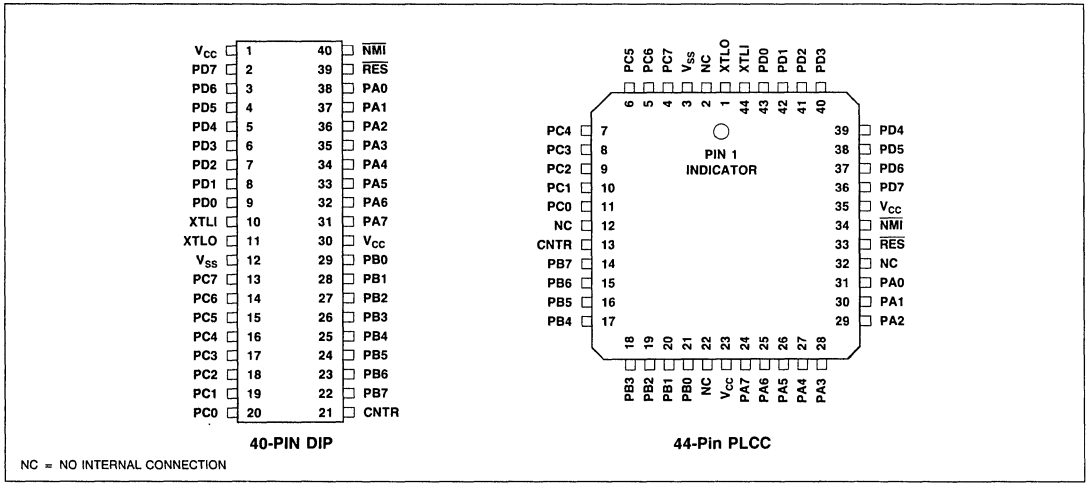


Figure 2-2. R65C10 Pin Assignments

Table 2-1. R65C10 Pin Description

Signal Name	I/O	Description
V_{CC}		**POWER**. +5 Vdc; must be connected to both pins.
V_{SS}		**GROUND**. Signal return and power ground (0V).
XTLI	I	**CRYSTAL INPUT**. The crystal or external clock input to the internal clock oscillator. The oscillator generates the internal master clock at the frequency of the input crystal/clock divided either by 1 or by 2 depending upon mask option. The system and counter/timer clocks are derived from the master clock under control of the Prescaler Control Register.
XTLO	O	**CRYSTAL OUTPUT**. The crystal output from the internal clock oscillator. XTLO should be left open when a clock is input at XTLI.
$\overline{RES}$	I	**RESET**. The active low $\overline{RES}$ input initializes the R65C10. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
$\overline{NMI}$	I	**NON-MASKABLE INTERRUPT**. A negative-going edge on the $\overline{NMI}$ input interrupts the CPU.
PA0–PA7	I/O	**PORT A**. General purpose I/O Port A.
PB0–PB7	I/O	**PORT B**. General purpose I/O Port B.
PC0–PC7	I/O	**PORT C**. General purpose I/O Port C.
PD0–PD7	I/O	**PORT D**. General purpose I/O Port D.
		Four 8-bit ports used for either input or output. Each line consists of an active transistor to V_{SS} and an optional active pull-up to V_{CC} (see Section 4.3). The two lower bits of the Port A (PA0 and PA1) also serve as edge-detect inputs with maskable interrupts. PA0 detects a positive-going edge and PA1 detects a negative-going edge.
CNTR	I/O	**COUNTER**. This line is either an input to, or an output from, the counter. CNTR is an input in the event counter and pulse width measurement modes, and is an output in the pulse generator modes. It consists of an active transistor to V_{SS} and an optional active pull-up to V_{CC}.

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R65C10. A block diagram of the R65C10 is presented in Figure 3-1.

3.1 INDEX REGISTERS

There are two 8-bit index registers: X and Y. Either index register can be used as a base to modify the program counter contents and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

3.2 STACK POINTER

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the CPU to perform stack manipulation in response to program instructions, the $\overline{\text{NMI}}$ interrupt input or the internally generated IRQ interrupt. The Stack Pointer must be initialized by the user program. The JSR, BRK, RTI, and RTS instructions use the stack and the Stack Pointer. The stack is located in RAM from address 0 to address $3F (0 to 63 decimal).

3.3 ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data is placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic 0; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.4 ACCUMULATOR

The Accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the Accumulator usually contains one of the two data words used in these operations.

3.5 PROGRAM COUNTER

The 12-bit Program Counter provides the addresses that step the processor through sequential instructions in a program. Each time the processor fetches an instruction from the program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the eight low-order lines of the internal address bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the four high-order lines of the internal address bus. The Program Counter is incremented each time an instruction or data is fetched from program memory.

3.6 INSTRUCTION REGISTER AND INSTRUCTION DECODE

Instructions are fetched from ROM or RAM and gated onto the internal data bus. These instructions are latched into the Instruction Register, then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.7 PROCESSOR STATUS REGISTER (PSR)

The 8-bit Processor Status Register, shown in Figure 3-2, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user program and the CPU. The R65C10 instruction set contains a number of conditional branch instructions which allow testing of these flags. Each of the seven processor status flags is described in the following paragraphs.

CARRY (C) BIT

The Carry (C) bit can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred, or cleared to logic 0 of no carry occurred, as the result of arithmetic operations.

The Carry bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

ZERO (Z) BIT

The Zero (Z) bit is set to logic 1 by the CPU during any data movement or by any calculation which sets all eight bits of the result to zero. This bit is cleared to logic 0 when the resultant eight bits of a data movement or calculation operation are not all zero. The R65C10 instruction set contains no instruction to specifically set or clear the Zero bit. The Zero bit is, however, affected by the following instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

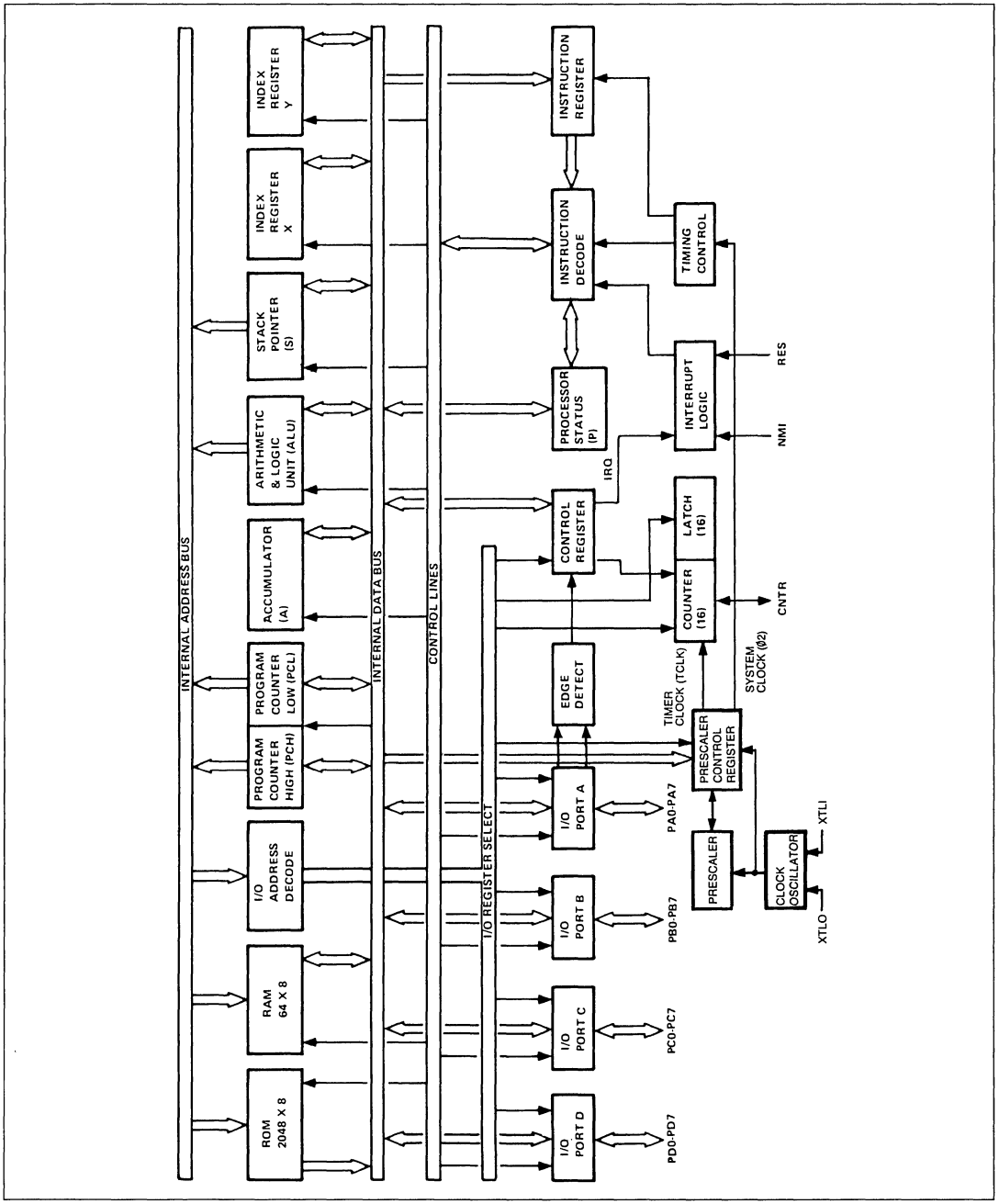
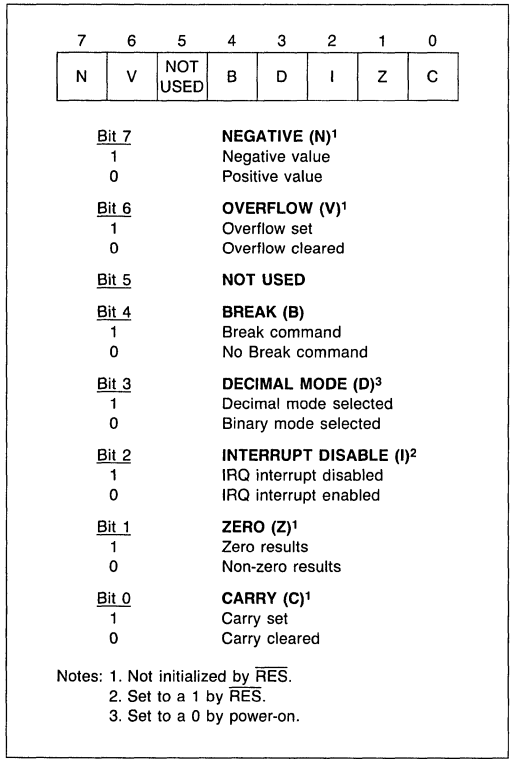


Figure 3-1. R65C10 Block Diagram



7	6	5	4	3	2	1	0
N	V	NOT USED	B	D	I	Z	C

Bit 7 — **NEGATIVE (N)[1]**
1 Negative value
0 Positive value

Bit 6 — **OVERFLOW (V)[1]**
1 Overflow set
0 Overflow cleared

Bit 5 — **NOT USED**

Bit 4 — **BREAK (B)**
1 Break command
0 No Break command

Bit 3 — **DECIMAL MODE (D)[3]**
1 Decimal mode selected
0 Binary mode selected

Bit 2 — **INTERRUPT DISABLE (I)[2]**
1 IRQ interrupt disabled
0 IRQ interrupt enabled

Bit 1 — **ZERO (Z)[1]**
1 Zero results
0 Non-zero results

Bit 0 — **CARRY (C)[1]**
1 Carry set
0 Carry cleared

Notes: 1. Not initialized by $\overline{RES}$.
2. Set to a 1 by $\overline{RES}$.
3. Set to a 0 by power-on.

Figure 3-2. Processor Status Register

INTERRUPT DISABLE (I) BIT

The Interrupt Disable (I) bit controls the servicing of the internal interrupt request (IRQ). If the I bit is reset to logic 0, the IRQ will be serviced. If the bit is set to logic 1, the IRQ will be ignored. The CPU will set the Interrupt Disable bit to logic 1 if NMI, an enabled IRQ interrupt or the $\overline{RES}$ signal is detected.

The I bit is restored by the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (provided the Interrupt Disable bit was cleared prior to the interrupt). The Interrupt Disable bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

DECIMAL MODE (D) BIT

The Decimal Mode (D) bit controls the arithmetic mode of the CPU. When this bit is set to a logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by two instructions. The Set Decimal Mode (SED) instruction sets the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the Decimal Mode Bit. The Decimal Mode Bit is cleared upon power application and by $\overline{RES}$ thus establishing binary mode.

BREAK (B) BIT

The Break (B) bit indicates the condition which caused the IRQ service routine to be entered. If the IRQ service routine was entered because the CPU executed a BRK command, the B bit will be set to logic 1. If the IRQ routine was entered as the result of an IRQ occurring, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

OVERFLOW (V) BIT

The Overflow (V) bit indicates that the result of a signed, binary addition or subtraction operation is a value that cannot be contained in seven bits ($-128 \leq n \leq +127$). The indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the V bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the V bit is cleared to logic 0. The V bit may also be cleared under program control by the Clear Overflow (CLV) instruction.

The Overflow bit may also be used with the BIT instruction. The BIT instruction, which may be used to sample interface devices, allows the Overflow bit to reflect the condition of Bit 6 in the sampled field. During a BIT instruction, the Overflow bit is set equal to the content of Bit 6 of the data tested with the BIT instruction. When used in this mode, the Overflow bit has nothing to do with signed arithmetic, but is just another sense bit for the CPU. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI, and SBC.

NEGATIVE (N) BIT

The Negative (N) bit copies the arithmetic sign bit value resulting from a data movement or an arithmetic operation. If the sign bit is set, the resulting value of the data movement or arithmetic operation is negative and the N bit is a logic 1; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive and the N bit is a logic 0. There are no instructions that set or clear the N bit since the N bit represents only the status of a result. The instructions that affect the state of the bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

3.8 I/O ADDRESS DECODE

The internal memory, control registers, I/O ports, and Counter/Latch are memory mapped into the 4096-byte address space. The I/O Address Decode logic decodes the address from the internal address bus and routes enable signals to the appropriate functions. The memory map of the R65C10 is shown in Figure 3-3.

Parameter	Address Hex	Address Dec
IRQ Vector High	FFF	4095
IRQ Vector Low	FFE	4094
RES Vector High	FFD	4093
RES Vector Low	FFC	4092
NMI Vector High	FFB	4091
NMI Vector Low	FFA	4090
R65C10 User Program	FF9 : 800	4089 : 2048
Unassigned	7FF : 094	2047 : 148
Port D Direction Register (Write Only)[3]	093	147
Port C Direction Register (Write Only)[3]	092	146
Port B Direction Register (Write Only)[3]	091	145
Port A Direction Register (Write Only)[3]	090	144
Control Register (CR)	08F	143
Prescaler Control Register (PCR)	08E	142
Stop Mode (Write Only)[3]	08D	141
Unassigned	08C 08B	140 139
Clear PA1 Neg Edge Detected (Write Only)[1]	08A	138
Clear PA0 Pos Edge Detected (Write Only)[1]	089	137
Upper Latch and Transfer Latch to Counter, Clear Counter Overflow (Write Only)[2]	088	136
Lower Count, Clear Counter Overflow (Read Only)[2]	087	135
Upper Count (Read Only)	086	134
Lower Latch (Write Only)	085	133
Upper Latch (Write Only)	084	132
Port D (PD)	083	131
Port C (PC)	082	130
Port B (PB)	081	129
Port A (PA)	080	128
Unassigned	07F : 040	127 : 64
User RAM	03F : 000	63 : 0

Notes: 1. I/O command only; i.e., no stored data.
2. Clears Counter Overflow — Bit 7 in Control Register.
3. Mask option.

Figure 3-3. R65C10 Memory Map

3.9 2K x 8 ROM

The internal 2,048 x 8-bit Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed during fabrication.

The ROM is mapped from $800 to $FFF.

3.10 64 x 8 RAM

The internal 64 x 8-bit Random Access Memory (RAM) contains the user program stack and is used for scratchpad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. In the event that execution stops, RAM data is retained until execution resumes.

The R65C10 RAM is assigned page zero memory address 0 to $03F.

3.11 CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the R65C10. The reference frequency is provided by an external source and can be from a crystal or clock input. The external frequency may vary from 2 MHz to 8 MHz for a parallel resonant crystal input or from 20 kHz to 8 MHz for a clock input. The external clock rate is divided by 2 or 1 to generate an internal master clock (MCLK) as shown in Figure 3-4. Selection of the input crystal/clock divide-by-2 or divide-by-1 is a mask option. The divide-by-2 option can be used with either a crystal or clock input. The divide-by-1 option can be used only with a clock input. The divide-by-2 option causes the R65C10 to operate at the same internal frequency as the R6500/1 or R6500/1E when connected to the same input clock frequency. MCLK may be prescaled by four different values under program control (discussed below).

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-5A.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 22) = 2C_L \quad \text{or} \quad C = 2C_L - 22$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

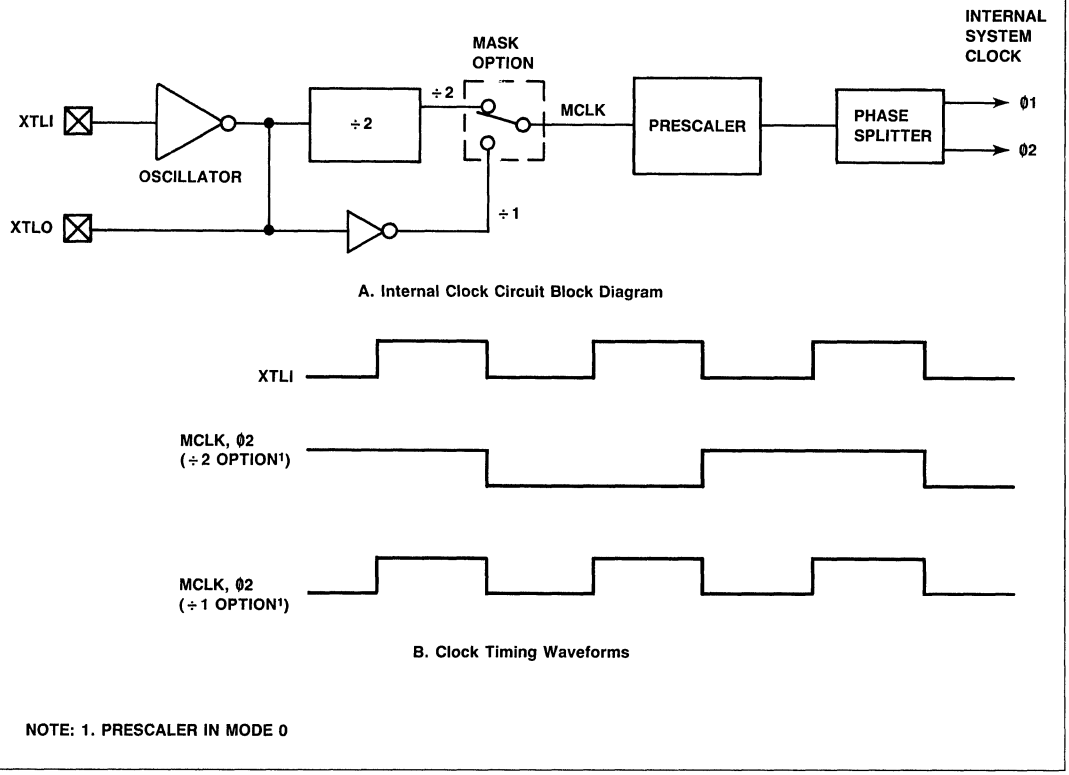


Figure 3-4. Internal System Clock Timing

For example, if C_L = 30 pF for a 4 MHz parallel resonant crystal, then

$C = (2 \times 30) - 22 = 38$ pF (Use standard value of 39 pF.)

(Note: C = Total shunt capacitance including that due to board layout.)

The series resistance of the crystal must be less than

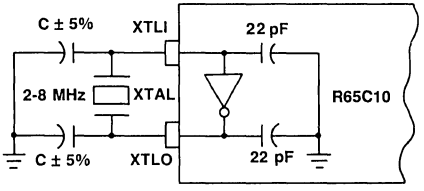
$$R_{smax} = \frac{2 \times 10^6}{(4 \times 30)^2} = 139 \text{ ohms}$$

The R65C10 internal oscillator and clock can be stopped under program control (Stop mode) and restarted by a $\overline{RES}$ input. The Stop mode is described in Section 4.

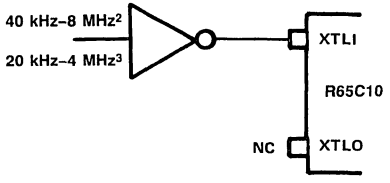
3.12 PRESCALER CONTROL

Clock prescaler mode and value selection is controlled by the Prescaler Control Register (PCR) at the address $08E (see Figure 3-6). The prescaler mode (PM) is determined by the value written to bits 0 and 1. The prescaler value (PV) is determined by the value written to bits 2 and 3. The system clock (Ø2) and timer clock (TCLK) rates are determined by the combination of selected prescaler mode and value. When prescaler mode 0 is selected, Ø2 and TCLK both run at the internal master clock (MCLK) rate regardless of the selected prescaler value. Ø2 runs at MCLK in prescaler modes 0 and 1 and at MCLK ÷ PV in prescaler mode 3. TCLK runs at MCLK in prescaler mode 0 and at MCLK ÷ PV in prescaler modes 1 and 3. Prescaler mode 2 is illegal and will cause indeterminate operation if selected.

The selected prescaler value is invoked in the cycle following the write or interrupt occurrence. Waveforms for five of these operations are illustrated in Figure 3-7.



A. Crystal Input



B. Clock Input

Notes:
1. Clock input divide-by-2 option must be selected.
2. Clock input divide-by-2 selected.
3. Clock input divide-by-1 selected.

Figure 3-5. Clock Oscillator Input Options

	7	6	5	4	3	2	1	0
ADDR $08E	NOT USED				V1	V0	M1	M0

Bits 3-2 Prescaler Value (PV) Select[1]

V1	V0	Prescale Value
0	0	Divide by 8
0	1	Divide by 32
1	0	Divide by 64
1	1	Divide by 128

Bits 1-0 Prescaler Mode (PM) Select[1]

M1	M0	Mode	System Clock (Ø2) Rate	Timer Clock (TCLK) Rate
0	0	0	MCLK	MCLK
0	1	1	MCLK	MCLK ÷ PV
1	0	2	N/A	N/A (Illegal Mode)
1	1	3	MCLK ÷ PV	MCLK ÷ PV

Note: 1. All bits are reset to 0 by $\overline{RES}$.

Figure 3-6. Prescaler Control Register

3.13 CONTROL REGISTER (CR)

The Control Register (CR), shown in Figure 3-8, is located at address $8F. The CR contains five control bits and three status bits. The control bits must be written to the Control Register. The status bits can be read, along with the previously written control bits, by reading the register. All control and status bits in the Control Register are cleared to 0 by the assertion of $\overline{RES}$. The signals controlled by and reported in the CR are described in the following paragraphs.

Bits 0 to 4 in the Control Register are control bits (Figure 3-8). The control signals are set by writing a 1 into the respective bit position, and cleared either by writing a 0 into the respective bit position or by assertion of $\overline{RES}$.

Bits 5 to 7 in the Control Register are status bits (Figure 3-8). The status bits are read-only information. Each status bit is set to a 1 by monitoring circuitry, and is cleared to a 0 either by writing to specific address or by assertion of $\overline{RES}$.

COUNTER MODE CONTROL 0 AND 1

Counter Mode Control signals CMC0 and CMC1 (bits 0 and 1) control the Counter operating modes. The modes of operation and the corresponding configuration of CMC0 and CMC1 are shown in Figure 3-8. These modes are selected by writing the appropriate bit values into the Counter Mode Control bits.

The Counter is reset to the Interval Timer mode (Mode 0) by assertion of $\overline{RES}$ (which causes 0s to be loaded into all bits of the Control Register).

PA1 INTERRUPT ENABLE BIT (A1IE)

If the PA1 Interrupt Enable bit (bit 2) is set to a 1, IRQ will occur when the PA1 Negative Edge Detected bit (bit 5) is set to a 1.

PA0 INTERRUPT ENABLE BIT (A0IE)

If the PA0 Interrupt Enable bit (bit 3) is set to a 1, IRQ will occur when the PA0 Positive Edge Detected bit (bit 6) is set to a 1.

COUNTER INTERRUPT ENABLE BIT (CIE)

If the Counter Interrupt Enable Bit (bit 4) is set to a 1, IRQ will occur when Counter Overflow (bit 7) is set to a 1.

PA1 NEGATIVE EDGE DETECTED BIT (A1ED)

The PA1 Negative Edge Detected bit (bit 5) is set to a 1 whenever a negative (falling) edge is detected on PA1. This bit is cleared to a 0 by writing to address $08A or by assertion of $\overline{RES}$.

The edge detecting circuitry is active regardless of whether PA1 is an input or is an output. When PA1 is used as an output, A1ED will be set when the negative edge is detected during a high-to-low transition. When PA1 is used as an input and the negative

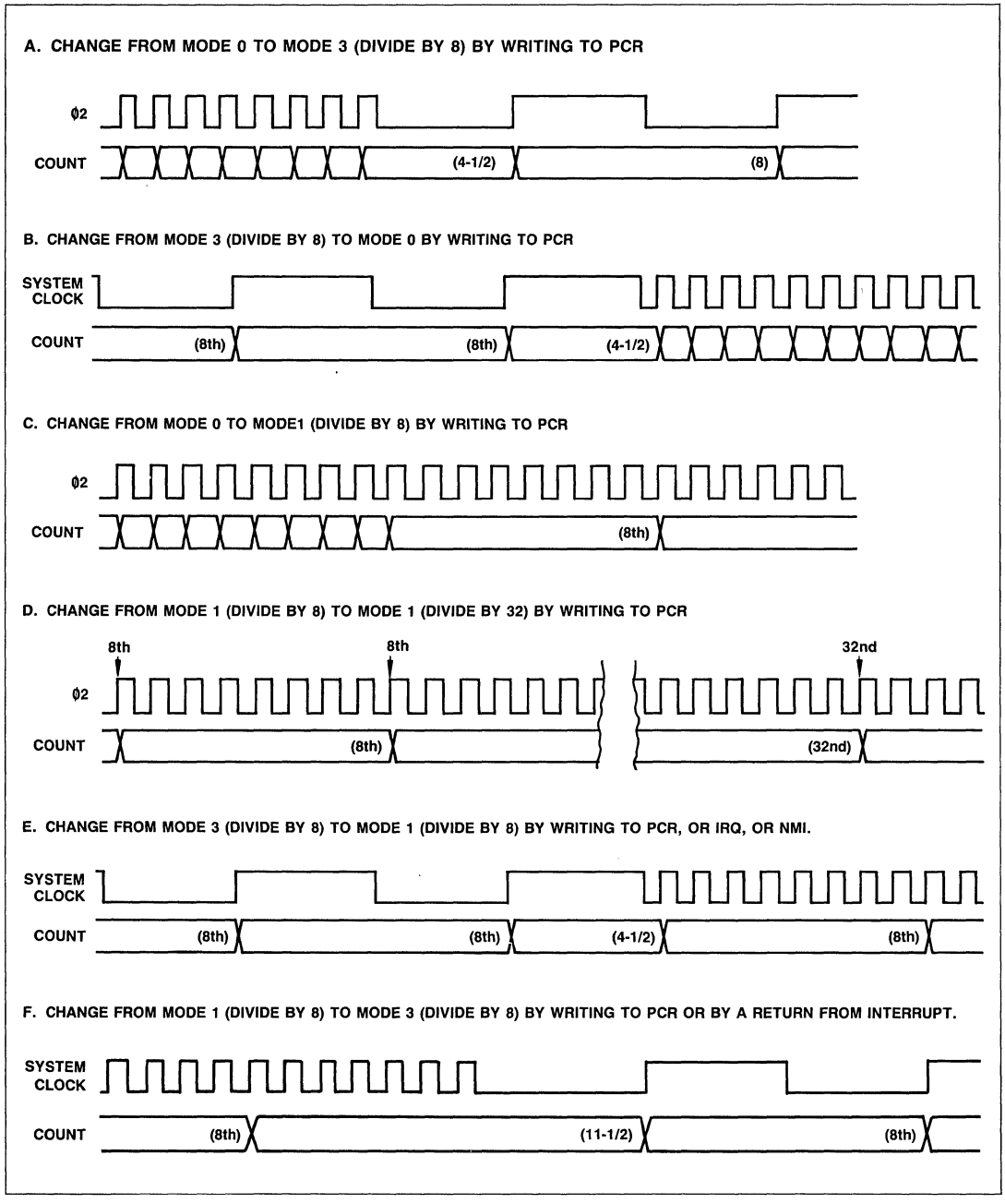


Figure 3-7. Prescaler Waveform Examples

	7	6	5	4	3	2	1	0
ADDR	INTERRUPT STATUS			INTERRUPT ENABLE			TIMER MODE	
$08F	TIMER	PA0	PA1	TIMER	PA0	PA1	CONTROL	

Bit 7 **COUNTER OVERFLOW (CTRO)[1]**
1 Counter overflow occurred
0 No counter overflow

Bit 6 **PA0 POSITIVE EDGE DETECT (A0ED)[1]**
1 PA0 positive edge detected
0 PA0 positive edge not detected

Bit 5 **PA1 NEGATIVE EDGE DETECT (A1ED)[1]**
1 PA1 negative edge detected
0 PA1 negative edge not detected

Bit 4 **COUNTER INTERRUPT ENABLE (CIE)[2]**
1 Enable counter interrupt
0 Disable counter interrupt

Bit 3 **PA0 INTERRUPT ENABLE (A0IE)[2]**
1 Enable PA0 interrupt
0 Disable PA0 interrupt

Bit 2 **PA1 INTERRUPT ENABLE (A1IE)[2]**
1 Enable PA1 interrupt
0 Disable PA1 interrupt

Bit 10 **COUNTER MODE CONTROL (CMC1 & CMC2)[2]**
0 0 Interval Timer
0 1 Pulse Generator
1 0 Event Counter
1 1 Pulse Width Measurement

Notes: 1. Read only.
2. Read/write.

Figure 3-8. Control Register

edge detecting circuitry is used, A1ED should be cleared by the user program upon initialization and upon completion of the PA1 Negative Edge Detected IRQ processing.

PA0 POSITIVE EDGE DETECTED BIT (A0ED)

The PA0 Positive Edge Detected bit (bit 6) is set to a 1 whenever a positive (rising) edge is detected on PA0. This bit is cleared to a 0 by writing to address $089 or by assertion of $\overline{RES}$.

The edge detecting circuitry is active regardless of whether PA0 is an input or is an output. When PA0 is used as an output, A0ED will be set when the positive edge is detected during a low-to-high transition. When PA0 is used as an input and the positive edge detecting circuitry is used, A0ED should be cleared by the user program upon initialization and upon completion of PA0 Positive Edge Detected IRQ processing.

COUNTER OVERFLOW BIT (CTRO)

The Counter Overflow bit (bit 7) is set to a 1 whenever the Counter overflow occurs in any of the four counter operating modes. Overflow occurs when the Counter is decremented one count from 0. This bit is cleared to a 0 by reading from address $087, writing to address $088, or by assertion of $\overline{RES}$.

The CTRO bit should be cleared by the user program upon initialization and upon completion of Counter Overflow IRQ interrupt processing.

When a Counter Overflow occurs, the Upper Count (UC) in address $086, and the Lower Count (LC) in address $087, are loaded with to the values contained in the Upper Latch (UL) in address $084, and in the Lower Latch (LL) in address $085, respectively.

3.14 PARALLEL INPUT/OUTPUT PORTS

The R65C10 provides four memory-mapped 8-bit Input/Output (I/O) ports: PA, PB, PC and PD. All 32 I/O lines of the four ports are completely bidirectional. All lines may be used either for input or output in any combination, i.e., there are no line grouping or port association restrictions. A mask option is available to select I/O port operation with or without direction registers. Table 3-1 lists the I/O port and edge detected bit reset addresses.

Table 3-1. I/O Port Addresses

Port/Function	Address
Port A Direction Register (Write Only)	$090
Port B Direction Register (Write Only)	$091
Port C Direction Register (Write Only)	$092
Port D Direction Register (Write Only)	$093
Port A Data Register (Read/Write)	$080
Port B Data Register (Read/Write)	$081
Port C Data Register (Read/Write)	$082
Port D Data Register (Read/Write)	$083
Clear PA0 Positive Edge Detected Bit (Write Only)	$089
Clear PA1 Negative Edge Detected Bit (Write Only)	$08A

I/O PORT OPERATION WITHOUT DIRECTION REGISTERS

If direction registers are *not* selected, the direction of the 32 I/O lines is controlled by writing to the four 8-bit port data registers located in page zero at addresses $80–$83 (see Figure 3-3). This arrangement provides quick programming access using simple 2-byte zero page address instructions. I/O handling is simplified since programming of direction registers is not required.

Inputs

Inputs are enabled by writing a 1 into all I/O port register bit positions that correspond to input lines. A low ($\leq$0.8 Vdc) input level causes a 0 to be read when a read instruction is issued to the port register. A high ($\geq$2.0 Vdc) input level causes a 1 to be read. Assertion of $\overline{RES}$ forces all bits in the I/O port registers to 1s, thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port register.

Outputs

Outputs are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions.

A 1 will force a high (≥2.4 Vdc) output while a 0 will force a low (≤0.4 Vdc) output.

I/O PORT OPERATION WITH DIRECTION REGISTERS

If direction registers are selected, the direction of all 32 I/O lines is controlled by individual bits in four write-only I/O port direction registers. The direction registers for ports A, B, C and D are located at addresses $90, $91, $92 and $93, respectively. Setting a bit in a direction register to a 1 causes the corresponding I/O line to operate as an output; resetting the bit to a 0 causes the I/O line to be an input. Assertion of $\overline{RES}$ clears all direction register bits to 0s causing all I/O lines to initially be inputs.

Inputs

If an I/O line is an input, the state of the corresponding bit in the I/O port data register shows the input logic level: 1 = high; 0 = low.

Outputs

If an I/O line is an output, the state of the corresponding bit written to the port data register determines the output logic level: 1 = high; 0 = low.

EDGE DETECTION CAPABILITY

The Port A PA0 and PA1 circuitry has edge detection capability. Edges detected on these lines are reported in the Control Register and will cause an IRQ if enabled in the Control Register (see Section 3.14). The edge detect timing waveforms are illustrated in Figure 3-9.

PA0 Positive Edge Detection

In addition to its normal I/O function, an asynchronous positive (rising) edge signal can be detected on PA0. This occurrence will be reported in the PA0 Positive Edge Detected bit in the Control Register (CR6). CR6 is cleared by writing to address $089 or by assertion of $\overline{RES}$.

PA1 Negative Edge Detection

In addition to its normal I/O function, an asynchronous negative (falling) edge signal can be detected on PA1. This occurrence wil be reported in the PA1 Negative Edge Detected bit in the Control Register (CR5). CR5 is cleared by writing to address $08A or by assertion of $\overline{RES}$.

3.15 COUNTER/LATCH

GENERAL

The Counter/Latch consists of a 16-bit Counter, and a 16-bit Latch. The Counter resides in two 8-bit registers: address $086 contains the Upper Count value (bits 8–15 of the Counter) and address $087 contains the Lower Count value (bits 0–7 of the Counter). The Counter contains the count of either unscaled or prescaled Ø2 clock periods, or external events, depending on Counter mode selected in the Control Register and, for clock driven Counter modes, the Prescaler mode and value selected in the Prescaler Control Register. Table 3-2 lists the addresses associated with Counter/Latch operation.

Table 3-2. Counter/Latch Addresses

Function	Address
Write Upper Latch (Write Only)	$084
Write Lower Latch (Write Only)	$085
Read Upper Count (Read Only)	$086
Read Lower Count, Clear Timer Overflow (Read Only)	$087
Write Upper Latch and Transfer Latch to Counter, Clear Counter Overflow (Write Only)	$088

The Latch contains the Counter initialization value. The Latch resides in two 8-bit registers: address $084 contains the Upper Latch value (bits 8–15 of the Latch) and address $085 contains the Lower Latch value (bits 0–7 of the Latch). The 16-bit Latch can hold values from 0 to 65,535.

The latch registers can be loaded at any time by writing to the Upper Latch address ($084) and the Lower Latch address ($085). In each case, the contents of the Accumulator are copied into the applicable Latch register. The Upper Latch and Lower Latch

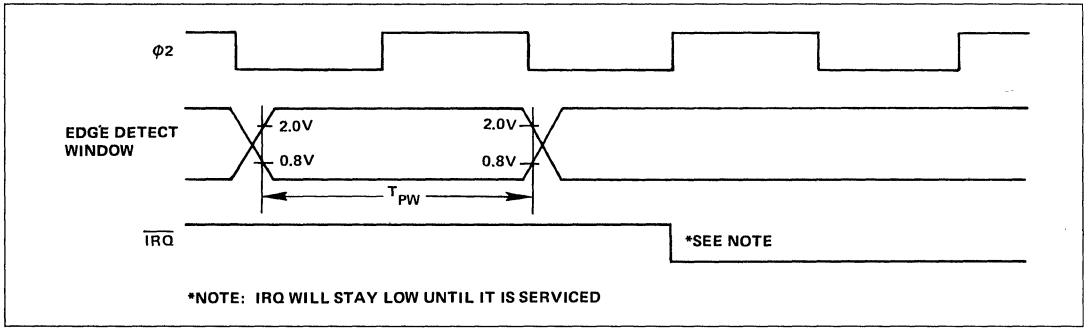


Figure 3-9. PA0 and PA1 Edge Detection Timing Waveforms

can be loaded independently; it is not required to load both registers at the same time, or sequentially. The Upper Latch can also be loaded by writing to address $088.

The Counter will also be initialized to the Latch value whenever the Counter overflows. When the Counter decrements from 0, the next Counter value will be the Latch value, not $FFFF.

Whenever the Counter overflows, the Counter Overflow status bit in the Control Register (CR7) is set to a 1. This bit is cleared whenever the lower eight bits of the Counter are read from address $087 or by writing to address $088.

COUNTER/TIMER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register (see Table 3-3).

The Interval Timer, Pulse Generator, and Pulse Width Measurement modes are internally clocked modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

Interval Timer (Mode 0)

In the Interval Timer mode, the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0, the next Counter value is the Latch value, not $FFFF.

2. When a write operation is performed to the Upper Latch and the Transfer Latch to Counter address ($088), the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented at the timer clock (TCLK) rate. The 16-bit Counter can hold from 1 to 65,535 counts. For a 4 MHz internal Ø2 clock and no prescaler selected, the timer range is 0.25 μs to 16.384 ms. For a 4 MHz internal Ø2 clock and divide-by-128 prescaler selected, the timer range is 32 μs to 2.097 seconds.

When the Counter decrements from 0, the Counter Overflow bit in the Control Register (CR7) is set to a 1 at the next counter clock pulse. If the Counter Interrupt Enable bit (CR4) is also set, IRQ will occur. The Counter Overflow bit in the Control Register can be examined in the IRQ interrupt routine to determine that the IRQ was caused by the Counter overflow.

While the timer is operating in the Interval Timer mode, the Counter-Out/Event-In (CNTR) line is held in the high impedance state (output disabled).

A timing diagram of the Interval Timer mode is shown in Figure 3-10.

Pulse Generator Mode (Mode 1)

In the Pulse Generator mode, the CNTR line operates as a Counter-Out. When a write is performed to address $088 the CNTR output is initialized high. The Counter is decremented at the TCLK rate. The CNTR line toggles from low to high or from high to low whenever a Counter overflow occurs.

Either a symmetric or an asymmetric output waveform can be output on the CNTR line in this mode. The CNTR output is initialized to the high impedance state (output disabled) by assertion of $\overline{RES}$ since the Interval Timer mode is established by $\overline{RES}$.

Event Counter Mode (Mode 2)

In this mode, the CNTR line is used as an Event-In input, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the system (Ø2) clock rate.

The Counter can count up to 65,535 occurrences before overflowing. As in the other modes, the Counter Overflow bit (CR7) is set to a 1 if the overflow occurs.

Figure 3-11 is a timing diagram of the Event Counter mode.

Pulse Width Measurement Mode (Mode 3)

This mode allows the accurate measurement of a low pulse duration on the CNTR line. In this mode, CNTR is used in the Event-In capacity. The Counter decrements at the TCLK rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state.

If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device (if present) will cause the CNTR input to be in the high ($\geq$2.0 volt) state.

A timing diagram for the Pulse Width Measurement mode is shown in Figure 3-12.

3.16 INTERRUPT LOGIC

Interrupt logic controls the sequencing of $\overline{RES}$ and the two interrupts: $\overline{NMI}$, and IRQ.

$\overline{RES}$ Sequencing

$\overline{RES}$ going from low-to-high causes the R65C/1 to set the Interrupt Disable bit in the Processor Status Register (bit 2) and to initiate RES vector fetch at address $FFC and $FFD to begin user program execution. All of the I/O ports (PA, PB, PC, and PD) and CNTR are forced to the high (logic 1) state. All bits of the Control Register are cleared to logic 0, causing the Interval Timer Counter Mode (Mode 0) to be selected and causing all interrupt enable bits to be reset. All Prescaler Control Register bits are also reset to 0 causing Prescaler Mode 0 to be selected.

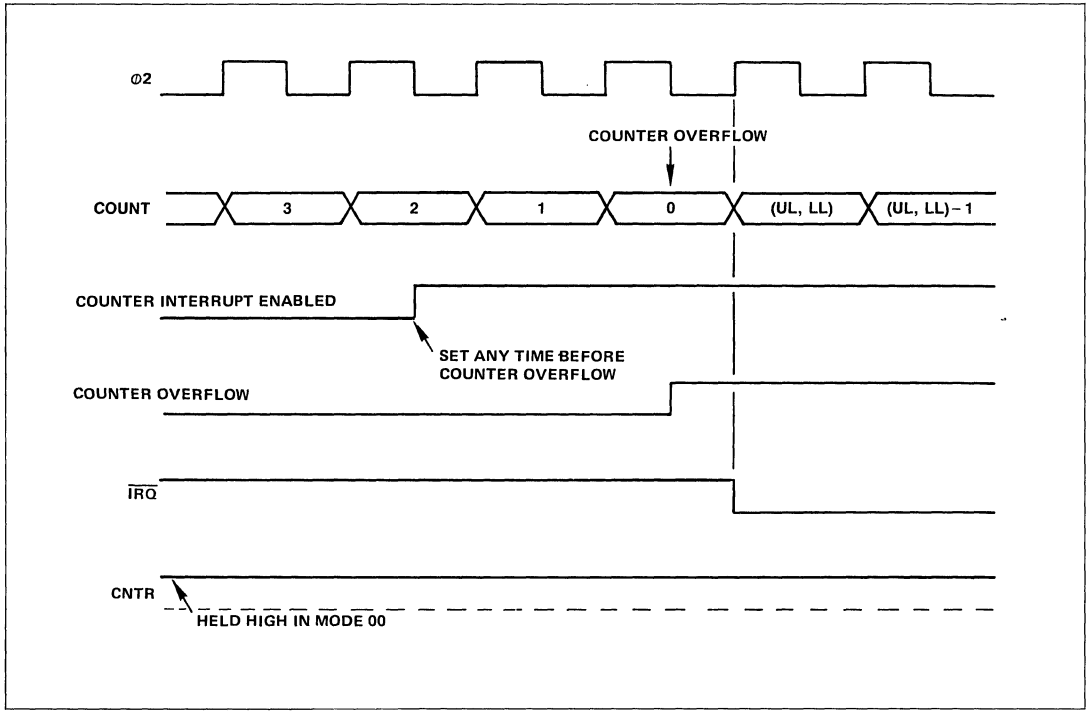


Figure 3-10. Interval Timer (Mode 0) Timing Waveforms

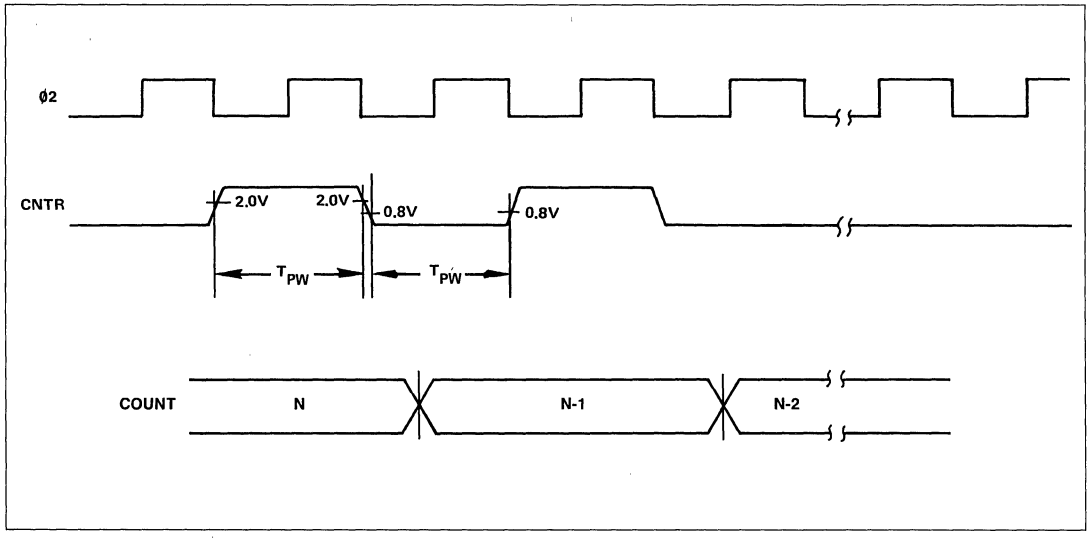


Figure 3-11. Event Counter (Mode 2) Timing Waveforms

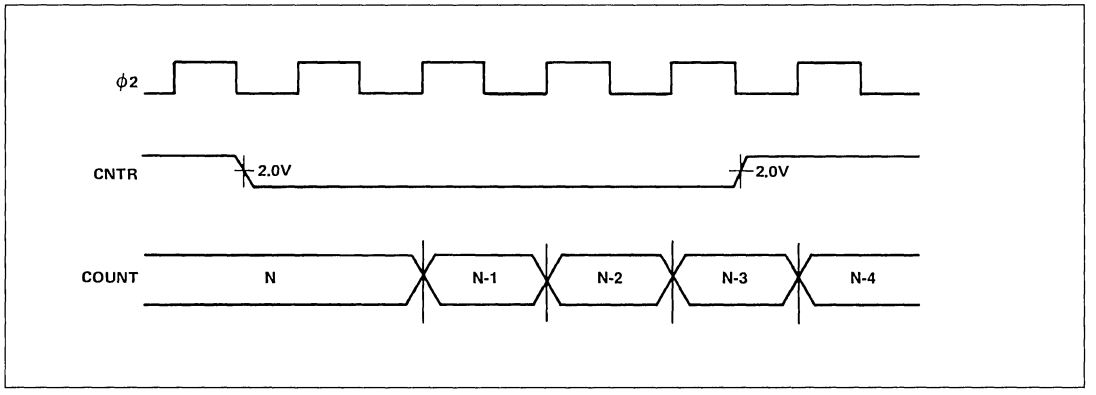


Figure 3-12. Pulse Width Measurement (Mode 3) Timing Waveforms

$\overline{\text{NMI}}$ Sequencing

At the first operation code fetch following the high-to-low transition of the $\overline{\text{NMI}}$ input, the interrupt logic forces execution of the Break (BRK) instruction and subsequent execution from the address vector stored at $FFA and $FFB. Simultaneous with the execution of the BRK instruction, the Interrupt Disable bit in the Processor Status Register is set to disable an IRQ and bit 1 in the Prescaler Control Register is cleared to select unscaled system clock. Bit 0 of the Prescaler Control Register is unaffected.

IRQ Sequencing

The internal IRQ can be generated by any or all of three possible conditions: Counter Overflow, a positive edge detected on PA0, or a negative edge detected on PA1. The IRQ in response to these conditions can be enabled or disabled by setting or resetting the appropriate interrupt enable bits in the Control Register.

The first IRQ condition is Counter Overflow. IRQ will occur whenever both the Counter Interrupt Enable (CR4) and the Counter Overflow (CR7) are logic 1.

The second IRQ condition is detection of a positive edge on PA0. IRQ will occur whenever both the PA0 Interrupt Enable (CR3) and the PA0 Positive Edge Detected (CR6) are logic 1.

The third IRQ condition is detection of a negative edge on PA1. IRQ will occur whenever both the PA1 Interrupt Enable (CR2) and the PA1 Negative Edge Detected (CR5) are logic 1.

Multiple simultaneous interrupts will cause the IRQ to remain active until all interrupting conditions have been serviced and cleared.

The IRQ interrupt occurs when bit 2 of the Process Status Register is clear (enabling an IRQ), an IRQ enable bit (bit 2, 3 or 4) in the Control Register is set, and the corresponding interrupt bit (bit 5, 6 or 7) in the Control Register is set. Upon IRQ interruption, the BRK instruction is forced and subsequent program execution begins from the address vector stored at $FFE and $FFF. Bit 2 of the Processor Status Register is set. Bit 1 in the Prescaler Control Register is cleared to select unscaled system ϕ2 clock. Bit 0 of the Prescaler Control Register is unaffected.

SECTION 4
POWER ON/OFF INITIALIZATION AND OTHER CONSIDERATIONS

This section describes power turn-on, stop mode and mask option considerations for the R65C10.

4.1 POWER-ON TIMING

After application of V_{CC} power to the R65C10, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal clock oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the crystal or clock input circuit. The clock oscillator output can be monitored on XTLO (Pin 11).

The power turn-on waveforms are illustrated in Figure 4-1.

4.2 STOP MODE

The Stop mode is an ultra-low-power mode in which the internal oscillator and clock is stopped. This mode is entered by writing to address $08D and is exited only when $\overline{RES}$ is asserted.

While in this mode, the R65C10 is dormant; however, the contents of RAM are preserved. Maximum power dissipation while in the Stop mode is under 4 mW. The oscillator stops with XTLO low.

A mask option is provided to inhibit Stop mode entry. This option is recommended if Stop mode is not used during operation.

4.3 MASK OPTIONS

Mask options are user selectable options permanently implemented when the R65C10 device is manufactured in response to a customer order. The options are to be specified on the R65C10 sheet in the R6500/* ROM Code Order Forms (Literature Order No. 2134). The options deal with three basic circuits:

- Input crystal/clock frequency divisor
- I/O port direction registers and internal pull-up resistors
- Stop mode enable/disable

Input Crystal/Clock Frequency Divisor

The input clock/crystal frequency divisor can be selected to be either 1 or 2 (see Section 3.11).

Direction Registers/Pull-up Resistors

Direction registers can be selected for controlling port input/output operation (see Section 3.14).

If direction registers are not used, then internal pull-up resistors can be optionally selected. In this case, pull-up resistors can be optionally included for 8-bit port groups only, i.e., not for individual I/O lines within an 8-bit port group. In addition, an internal pull-up for the CNTR line is selectable.

If direction registers are included, then internal pull-ups are not allowed.

Stop Mode Entry Enable

An option also exists to enable Stop mode use by writting to address 08D. (see Section 4.2).

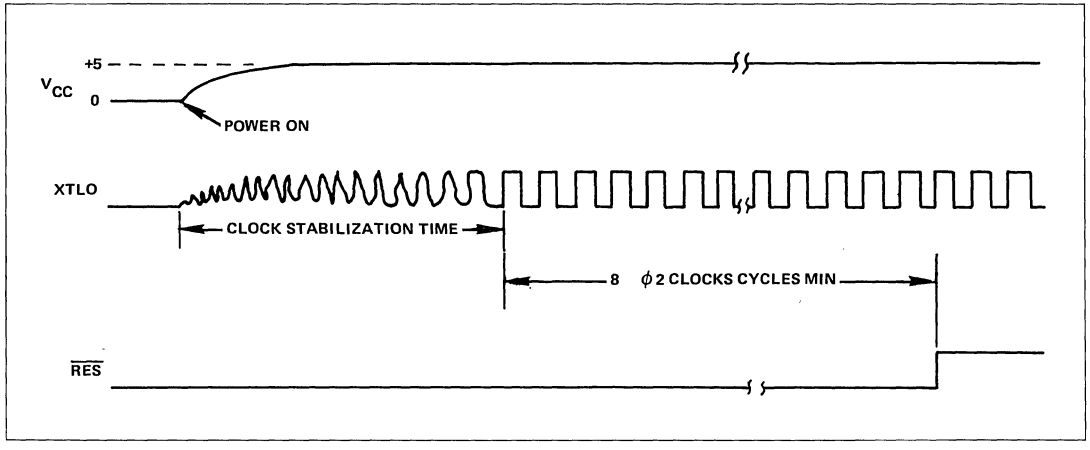


Figure 4-1. Power Turn-On Timing Detail

SECTION 5
SYSTEM SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses exceeding those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5.0 Vdc ±10%
Operating Temperature (Ambient) Commercial Industrial	T_A	T_L to T_H 0°C to +70°C −40°C to +85°C

3

ELECTRICAL CHARACTERISTICS

(Over operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input High Voltage All except $\overline{NMI}$ and $\overline{RES}$ $\overline{NMI}$, $\overline{RES}$	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} V_{CC}	V	V_{CC} = 5.5V
Input Low Voltage	V_{IL}	—	—	+0.8	V	V_{CC} = 4.5V
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±2.5	μA	V_{IN} = 0 to 5.0V
Output High Voltage	V_{OH}	+2.4	—	—	V	V_{CC} = 4.5V I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	V_{CC} = 5.5V I_{LOAD} = 1.6 mA
Output High Current (Sourcing)	I_{OH}	−100	—	—	μA	V_{OUT} = 2.4V
Output Low Current (Sinking)	I_{OL}	1.6	—	—	mA	V_{OUT} = 0.4V
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PD0–PD7, CNTR	R_L	2.0	3.2	6.0	Kohm	
Input Capacitance XTLI, XTLO PA0–PA7, PB0–PB7, PC0–PC7, PD0–PD7, CNTR	C_{IN}	 — —	 — —	 25 7	pF	T_A = 25°C V_{IN} = 0V f = 2 MHz–4 MHz
Output Capacitance	C_{OUT}	—	—	50	pF	1 TTL load
Input Frequency (f) Crystal Clock Clock	f	 2.0 0.04 0.02	 — — —	 8.0 8.0 4.0	 MHz MHz MHz	 ÷2 selected ÷2 selected ÷1 selected
Power Dissipation Operating Stop Mode	P_D	 — —	 12 1.4	 14 1.6	 mW/MHz mW	V_{CC} = 5.5V Outputs High Frequency = unscaled ϕ2 clock No external clock input

Notes:
1. T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

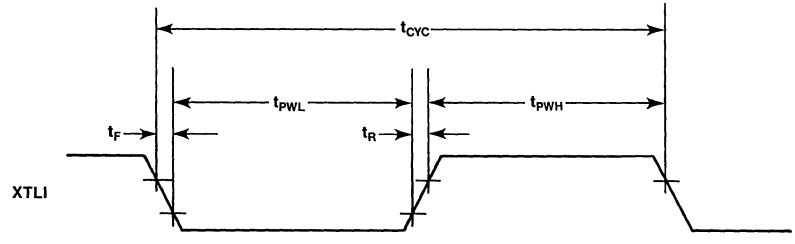
SWITCHING CHARACTERISTICS

(Over operating conditions unless otherwise noted)

Parameter	Mode	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
XTLI Input Clock											
Cycle Time	÷2	t_{CYC}	0.500	25.0	0.250	25.0	0.166	25.0	0.125	25.0	μs
Pulse Width, Low	÷2	t_{PWL}	100		55		45		40		ns
Pulse Width, High	÷2	t_{PWH}	100		55		45		40		ns
Rise and Fall Time	÷2	t_R, t_F		60		25		20		15	ns
XTLI Input Clock											
Cycle Time	÷1	t_{CYC}	1.000	50.0	0.500	50.0	0.333	50.0	0.250	50.0	μs
Pulse Width, Low	÷1	t_{PWL}	450		225		145		110		ns
Pulse Width, High	÷1	t_{PWH}	450		225		145		110		ns
Rise and Fall Time	÷1	t_R, t_F		20		15		12		10	ns
Count and Edge Detect Pulse Width			1		1		1		1		Ø2 Period*

*Function of Prescaler

SWITCHING WAVEFORMS



APPENDIX A
R65C10 INSTRUCTION SET

This appendix summarizes the R65C10 instruction set. The basic instructions are listed alphabetically by standard mnemonic in Table A-1. The instruction operation codes (OP Codes) for all valid addressing modes are listed in Table A-2. Also listed in Table A-2 are the number of bytes and number of CPU cycles required in each addressing mode. The effect of instruction execution on the Processor Status Register is also shown.

A matrix of instructions and addressing modes arranged by operation code is shown in Table A-3. For detailed information about CPU instruction execution, consult the R6500 Programming Manual (Order No. 202).

Table A-4 summarizes the differences in operation between the R65C10 CPU and the R6502 CPU.

Table A-1. R65C10 Instruction Set Alphabetic Sequence

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	JMP	Jump to New Location
AND	"AND" Memory with Accumulator	JSR	Jump to New Location Saving Return Address
ASL	Shift Left One Bit (Memory or Accumulator)		
		LDA	Load Accumulator with Memory
		LDX	LOAD Index X with Memory
BCC	Branch on Carry Clear	LDY	Load Index Y with Memory
BCS	Branch on Carry Set	LSR	Shift One Bit Right (Memory or Accumulator)
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	NOP	No Operation
BMI	Branch on Result Minus	ORA	"OR" Memory with Accumulator
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	PHA	Push Accumulator on Stack
BRK	Force Break	PHP	Push Processor Status on Stack
BVC	Branch on Overflow Clear	PLA	Pull Accumulator from Stack
BVS	Branch on Overflow Set	PLP	Pull Processor Status from Stack
CLC	Clear Carry Flag	ROL	Rotate One Bit Left (Memory or Accumulator)
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit	RTI	Return from Interrupt
CLV	Clear Overflow Flag	RTS	Return from Subroutine
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X	SBC	Subtract Memory from Accumulator with borrow
CPY	Compare Memory and Index Y	SEC	Set Carry Flag
		SED	Set Decimal Mode
		SEI	Set Interrupt Disable Status
DEC	Decrement Memory by One	STA	Store Accumulator in Memory
DEX	Decrement Index X by One	STX	Store Index X in Memory
DEY	Decrement Index Y by One	STY	Store Index Y in Memory
EOR	"Exclusive-Or" Memory with Accumulator	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
INC	Increment Memory by One	TXA	Transfer Index X to Accumulator
INX	Increment Index X by One	TXS	Transfer Index X to Stack Register
INY	Increment Index Y by One	TYA	Transfer Index Y to Accumulator

Table A.2. R65C10 Instruction Set by Address Modes

		ADDRESSING MODES																																		PROCESSOR STATUS CODES	
		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y			Z PAGE. X			ABS X			ABS. Y			RELATIVE			INDIRECT			Z PAGE. Y			7 6 5 4 3 2 1 0	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N V * B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3								N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3								N • • • • • Z •	AND
ASL	C ← [7 6 5 4 3 2 1 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3											N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2						• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2						• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2						• • • • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																														M_7 M_6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2						• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2						• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2						• • • • • • • •	BPL
BRK	BREAK													00	7	1																								• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2						• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2						• • • • • • • •	BVS
CLC	0 → C													18	2	1																								• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																								• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																								• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																								• 0 • • • • • •	CLV
CMP	A − M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3								N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																														N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																														N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3											N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																								N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																								N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3								N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3											N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																								N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																								N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																		• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3								N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							96	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3											N • • • • • Z •	LDY
LSR	0 → [7 6 5 4 3 2 1 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3											0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																								• • • • • • • •	NOP
ORA	A ∨ M → A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3								N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																								• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																								• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																								N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																								(RESTORED)	PLP
ROL	[7 6 5 4 3 2 1 0] ← [C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3											N • • • • • Z C	ROL
ROR	[C] → [7 6 5 4 3 2 1 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3											N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																								(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																								• • • • • • • •	RTS
SBC	A − M − $\overline{C}$ • A (4) (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3								N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																								• • • • • • • 1	SEC
SED	1 → D													F8	2	1																								• • • • 1 • • •	SED
SEI	1 → I													78	2	1																								• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3								• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																												96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2															• • • • • • • •	STY
TAX	A → X													AA	2	1																								N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																								N • • • • • Z •	TAY
TSX	S → X													BA	2	1																								N • • • • • Z •	TSX
TXA	X → A													8A	2	1																								N • • • • • Z •	TXA
TXS	X → S													9A	2	1																								• • • • • • • •	TXS
TYA	Y → A													98	2	1																								N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) ADD 1 TO N IF IN DECIMAL MODE

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER
+ ADD
− SUBTRACT
∧ AND
∨ OR
¥ EXCLUSIVE OR
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
n NO CYCLES
NO BYTES

Table A-3. R65C10 Instruction Set Operation Code Matrix

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	
1	BPL Relative 2 2[b]	ORA (IND), Y 2 5[a]				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4[a]				ORA ABS, X 3 4[a]	ASL ABS, X 3 7	
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	
3	BMI Relative 2 2[b]	AND (IND), Y 2 5[a]				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4[a]				AND ABS, X 3 4[a]	ROL ABS, X 3 7	
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	
5	BVC Relative 2 2[b]	EOR (IND), Y 2 5[a]				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4[a]				EOR ABS, X 3 4[a]	LSR ABS, X 3 7	
6	RTS Implied 1 6	ADC (IND, X) 2 6[c]				ADC ZP 2 3[c]	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2[c]	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4[c]	ROR ABS 3 6	
7	BVS Relative 2 2[b]	ADC (IND), Y 2 5[a,c]				ADC ZP, X 2 4[c]	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4[a,c]				ADC ABS, X 3 4[a,c]	ROR ABS, X 3 7	
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	
9	BCC Relative 2 2[b]	STA (IND), Y 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	
B	BCS Relative 2 2[b]	LDA (IND), Y 2 5[a]			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4[a]	TSX Implied 1 2		LDY ABS, X 3 4[a]	LDA ABS, X 3 4[a]	LDX ABS, Y 3 4[a]	
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	
D	BNE Relative 2 2[b]	CMP (IND), Y 2 5[a]				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4[a]				CMP ABS, X 3 4[a]	DEC ABS, X 3 7	
E	CPX IMM 2 2	SBC (IND, X) 2 6[c]			CPX ZP 2 3	SBC ZP 2 3[c]	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2[c]	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4[c]	INC ABS 3 6	
F	BEQ Relative 2 2[b]	SBC (IND), Y 2 5[a,c]				SBC ZP, X 2 4[c]	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4[a,c]				SBC ABS, X 3 4[a,c]	INC ABS, X 3 7	

NOTES:

[a]Add 1 to N if page boundary is crossed.

[b]Add 1 to N if branch occurs to same page; add 2 to N if branch occurs to different page.

[c]Add 1 to N if in decimal mode.

0	
0	BRK Implied 1 7

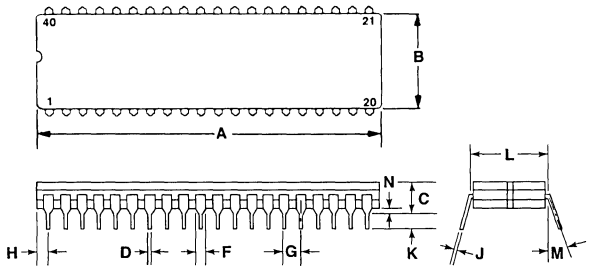
— OP Code
— Addressing Mode
— No. of Instruction Bytes (#); No. of Machine Cycles (n)

Table A-4. R65C10 Instruction Enhancements

Function	NMOS R6502 Microprocessor	CMOS R65C10 Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D = 0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

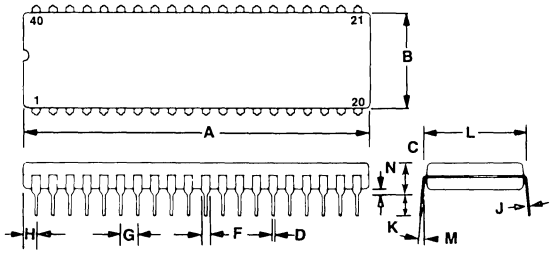
PACKAGE DIMENSIONS

40-PIN CERDIP



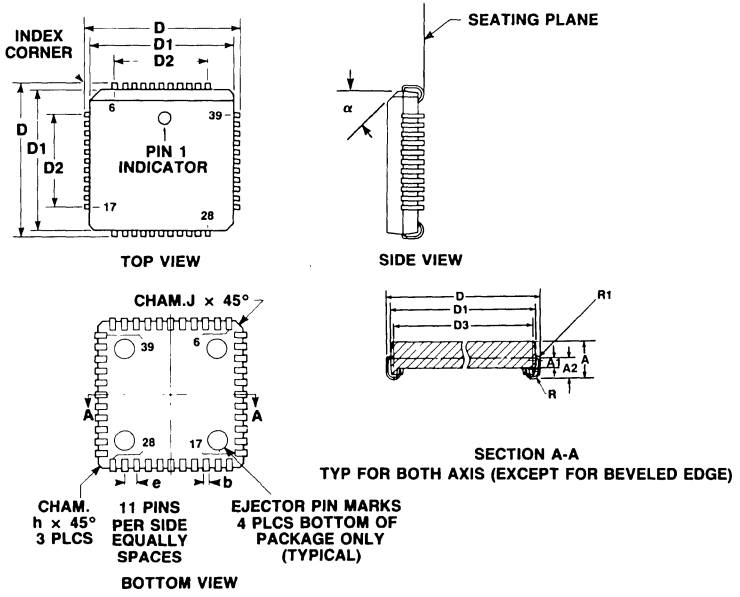
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51 56	52 58	2.030	2.070
B	12.95	13.46	0.510	0.530
C	4 06	5 08	0 160	0.200
D	0 41	0.51	0.016	0 020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
H	1.78	2 29	0.070	0.090
J	0.20	0.30	0.008	0 012
K	3.05	4.06	0.120	0.160
L	15 24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.38	0.89	0.015	0.035

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5 08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0 20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2 46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0 648	0.652
D2	12.62	12 78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0 010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	

3