Rockwell

R65C24
Peripheral Interface Adapter/Timer (PIAT)

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DESCRIPTION

The R65C24 Peripheral Interface Adapter/Timer (PIAT) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C24 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

The PIAT also contains one 16-bit Counter/Timer comprised of a 16-bit counter, two 8-bit latches associated with the counter, and an 8-bit snapshot latch for the upper half of the counter. A counter mode control register, under software direction, selects any one of eight counter modes of operation, and the status register contains an underflow flag to report counter time-out. A maskable interrupt request allows immediate CPU notification upon counter time-out.

FEATURES

- Low power CMOS N-well silicon gate technology
- Two 8-bit bidirectional I/O ports with individual data direction control
- Programmable 16-bit Counter/Timer with eight modes of operation
- Three 8-bit latches associated with the Counter/Timer
- Selectable divide-by-sixteen prescaler for all modes
- Automatic "Handshake" control of data transfers
- Three interrupts with program control
  - — Port A
  - — Port B
  - — Counter/Timer
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- Wide variety of packages
  - — 40-pin plastic and ceramic DIP
  - — 44-pin plastic leaded chip carrier (PLCC)
- Single +5 Vdc power requirement
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors

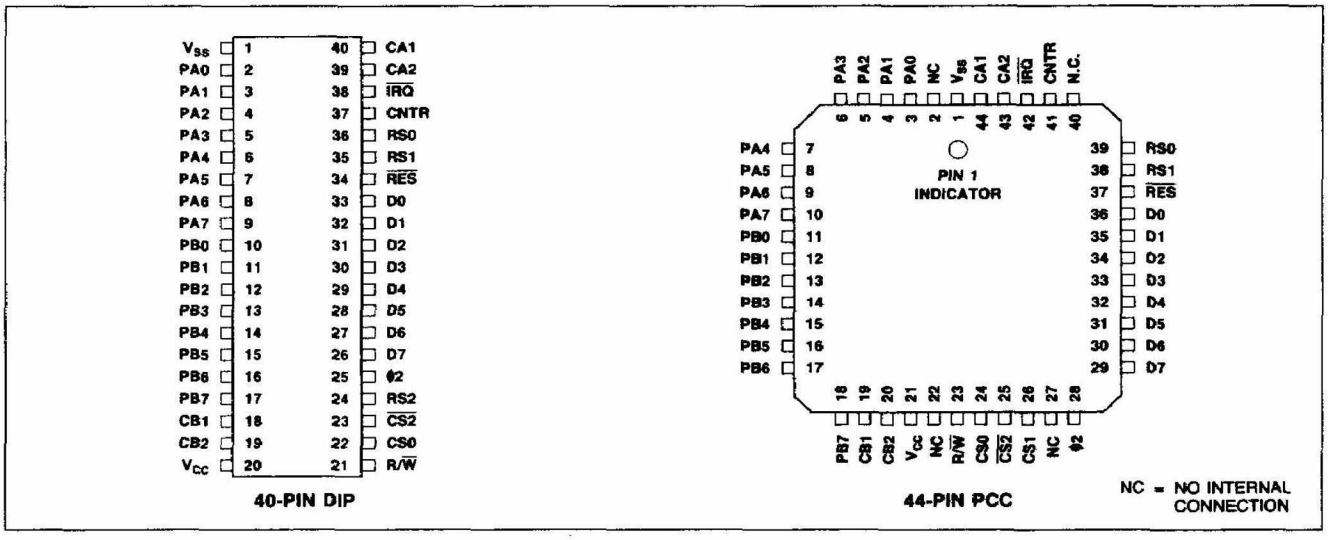


Figure 1. R65C24 Pin Assignments

ORDERING INFORMATION

Part Number:
R65C24

- Temperature Range:
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range:
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package:
  - C = 40-Pin Ceramic DIP
  - P = 40-Pin Plastic DIP
  - J = 44-Pin Plastic Leaded Chip Carrier (PLCC)

INTERFACE SIGNALS

The PIAT interfaces to the R6500, R6500/* or the R65C00 microprocessor family with a reset line, a ϕ2 clock line, a read/write line, an interrupt request line, three register select lines, two chip select lines, and an 8-bit bidirectional data bus.

The PIAT interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data ports. A Counter/Timer input/output line (CNTR) also interfaces to a peripheral device.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 2 shows the interface relationship of these signal as they pertain to the CPU and the peripheral devices.

CHIP SELECT (CS0, $\overline{CS2}$)

The PIAT is selected when CS0 is high and $\overline{CS2}$ is low. These two chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIAT is selected, data will be transferred between the data lines and PIAT registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, RS1 and RS2 lines and the contents of Control Registers A and B.

NOTE:

An R65C24 PIAT may be installed in a circuit in place of an R65C21 PIA subject to chip select considerations. Since the R65C21 has a CS1 input and the R54C24 does not have a CS1 input, the PIAT will be selected in the same addresses as the PIA and maybe more depending upon external address decoding circuitry.

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R65C24 PIAT. A low signal on the ($\overline{RES}$) input causes all internal registers to be cleared.

CLOCK SIGNAL (ϕ2)

The Phase 2 Clock Signal (ϕ2) is the system clock that triggers all data transfers between the CPU and the PIAT. ϕ2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIAT.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIAT and the data lines associated with the CPU and the peripheral devices. A high on the R/$\overline{W}$ line permits the peripheral devices to transfer data to the CPU from the PIAT. A low on the R/$\overline{W}$ line allows data to be transfered from the CPU to the peripheral devices from the PIAT.

REGISTER SELECT (RS0, RS1, RS2)

Two of the Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB), select various R65C24 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and, therefore, are shown separately in Table 1.

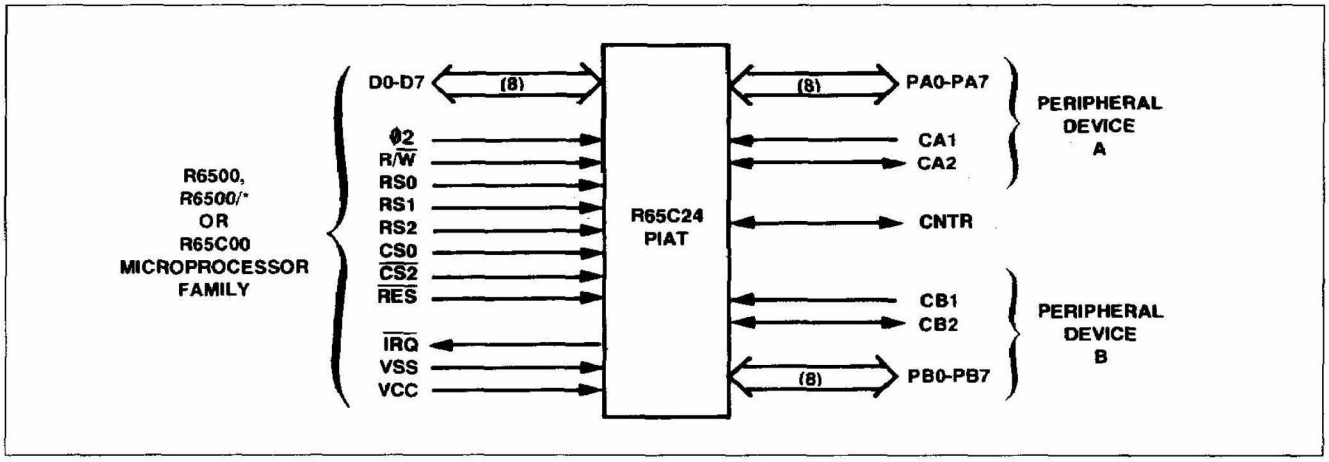


Figure 2. Interface Signals Relationship

Table 1. Peripheral Register Addressing

Register Address (Hex)	Register Select Lines			Data Direction Register Control		Register Operation	
	RS2	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$ = H	R/$\overline{W}$ = L
4	H	L	L	1	—	Read PIBA	Write ORA
4	H	L	L	0	—	Read DDRA	Write DDRA
5	H	L	H	—	—	Read CRA	Write CRA
6	H	H	L	—	1	Read PIBB	Write ORB
6	H	H	L	—	0	Read DDRB	Write DDRB
7	H	H	H	—	—	Read CRB	Write CRB

Register Select line RS2 determines whether the addressed registers are part of the Counter/Timer or the peripheral Port A and Port B sections of the PIAT. When RS2 is high, the Port A/Port B registers shown in Table 1 are selected. When the RS2 is low, the Counter/Timer registers are selected and operated upon as shown in Table 2.

Table 2. Counter/Timer Register Addressing

Register Address (Hex)	Register Select Lines			Counter/Timer Operation	
	RS2	RS1	RS0	(R/$\overline{W}$ = H)	(R/$\overline{W}$ = L)
0	L	L	L	Read Snapshot Latch (SL) SL → D0-D7 0 → UF	Write Upper Latch (UL) D0-D7 → UL 0 → UF Load and Enable Counter UL → UC, LL → LC
1	L	L	H	Read Upper Counter (UC) UC → D0-D7	Write Upper Latch (UL) D0-D7 → UL
2	L	H	L	Read Lower Counter (LC) LC → D0-D7 UC → SL	Write Lower Latch (LL) D0-D7 → LL UC → SL
3	L	H	H	Read Status Register (SR) SR → D0-D7 0 → UF,	Write Counter Control Mode Register (CMCR) D0-D7 → CMCR

INTERRUPT REQUEST LINE ($\overline{IRQ}$)

Three internal active low Interrupt Request lines ($\overline{IRQA}$, $\overline{IRQB}$, and $\overline{IRQT}$) act to interrupt the microprocessor through the external $\overline{IRQ}$ output. $\overline{IRQ}$ is an open drain output and is capable of sinking 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these internal lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port. The T corresponds to the Counter/Timer generated interrupt request.

$\overline{IRQA}$ and $\overline{IRQB}$ Lines — These two internal Interrupt Request lines are associated with the Port A and Port B sections of the PIAT and are controlled by Control Registers CRA and CRB, and the Peripheral Control lines CA1, CA2, CB1, and CB2.

These Interrupt Request lines have three interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 3.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$ (Table 3). Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled by CRB bit 0. Likewise, bit 6 (IRQB2) in CRB is set by an active transition on CB2, and $\overline{IRQB}$ from this flag is controlled by CRB bit 3. Also, both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation.

$\overline{IRQT}$ Line — The internal $\overline{IRQT}$ line is associated with the Counter/Timer and is controlled by the $\overline{IRQT}$ Enable bit in the Counter Mode Control Register and the Underflow Flag in the Status Register. A thorough discussion of the functions and operation of the $\overline{IRQT}$ line is given in the Counter/Timer Operation section of this product description.

Table 3. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{IRQA}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{IRQA}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{IRQB}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{IRQB}$ goes low (Active)

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 5 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a 0 in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative (high to low) transition of the CA1 signal, or by setting a 1 if it is to be set on a positive (low to high) transition.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a single pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0, respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

FUNCTIONAL DESCRIPTION

The R65C24 PIAT is organized into three independent sections referred to as the A Side, the B Side, and a Counter/Timer. The A Side and B Side each consist of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB), and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIAT registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. The Counter/Timer consists of a 16-bit counter; i.e., an 8-bit Upper Counter (UC) and 8-bit Lower Counter (LC), an 8-bit Upper Latch (UL), an 8-bit Lower Latch (LL), an 8-bit Snapshot Latch (SL), and a Status Register (SR). A Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation. Figure 3 is a block diagram of the R65C24 PIAT.

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIAT, the data which appears on the data bus during the Ø2 clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIAT after the trailing edge of the Ø2 clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 4 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a 0 in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a 1 causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a 1, a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a 0, a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1 and RS2) selects the various internal registers as shown in Table 1.

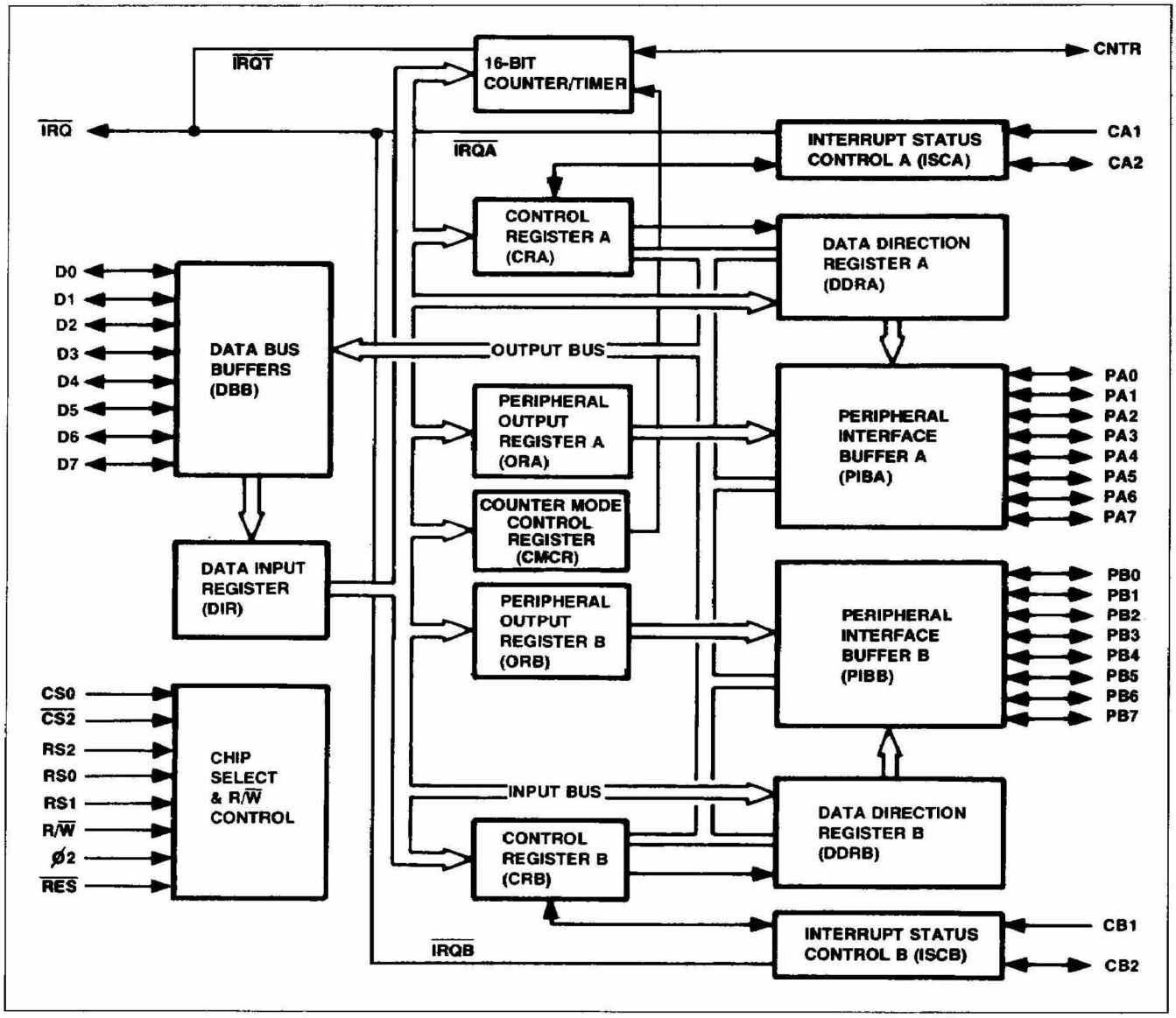


Figure 3. R65C24 PIAT Block Diagram

Table 4. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low ($\leq$0.4 Vdc); writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to Vcc for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or any output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than +2.4 Vdc.

Unlike the PA0-PA7 lines (which have pull-up devices), the PB0 through PB7 lines have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 Vdc for a "high" state or are above 0.8 Vdc for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 mA at 1.5 Vdc to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the miroprocessor and the PIAT. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

COUNTER/TIMER

The Counter/Timer includes a 16-bit counter and three 8-bit data latches. It also includes an 8-bit Counter Mode Control Register (CMCR) to select the Counter/Timer operating mode and options and an 8-bit Status Register to report time-out conditions as well as peripheral data port interrupt conditions. Figure 4 illustrates the Timer/Counter.

Counter/Latches — The Upper Counter (UC) and Lower Counter (LC) form a 16-bit down-counter that counts either Ø2 clock pulses from the processor bus or external events from input line CNTR, depending on the mode selected. The Upper Latch (UL) and Lower Latch (LL) hold the initial higher- and lower-order count values to be loaded into the counter. The Snapshot Latch (SL) is loaded with the value of the UC when the LC is read or the LL is written into by the PIAT. After a read of the LC, the Snapshot Latch is read to provide the current 16-bit value of the counter. The Underflow Flag (UF) in the Status Register (SR) is set to a 1 whenever the counter (UC, LC) decrements past $0000. A Prescaler can be program activated to divide-by-sixteen rather than divide-by-one for any of the Counter/Timer modes.

Counter Mode Control Register — The Counter Mode Control Register (CMCR) allows program selection of any of eight Counter/Timer modes of operation, for the enabling or disabling of the Prescaler, and the enabling or disabling of the $\overline{IRQT}$ interrupt line. Bits 2, 1 and 0 of the CMCR select one of the following Counter/Timer operating modes:

- Disable Counter/Timer
- One-Shot Interval Timer
- Free-Run Interval Timer
- Pulse Width Measurement
- Event Counter
- One-Shot Pulse Width Generation
- Free-Run Pulse Generation
- Retriggerable Interval Timer

Bit 7 of the CMCR controls the $\overline{IRQT}$ line. When bit 7 is set to a 1, $\overline{IRQT}$ is enabled and an Underflow Flag (UF bit in the Status Register set to a 1) will cause $\overline{IRQ}$ to be asserted. When bit 7 is set to a 0, the $\overline{IRQT}$ is disabled.

Bit 4 of the CMCR enables or disables the Prescaler. A 1 in bit 4 causes the Prescaler to be enabled so that the Counter/Timer is operating in a divide-by-sixteen mode. When this bit is a 0 the Prescaler is disabled so that the Counter/Timer is operating in a normal (divide-by-one) mode.

Status Register — Bit 7 of the Status Register (SR) reports the Counter Underflow Status. This underflow (UF) bit is set to 1 when the counter decrements past $0000. When this bit is set, the $\overline{IRQ}$ output will be asserted if the Interrupt Enable bit in the CMCR is set to a 1. The status of the Port A Interrupt Flag (IRQA) and Port B Interrupt Flag (IRQB) are reported in bits 6 and 5, respectively, in addition to being reported in the ISCA and ISCB registers.

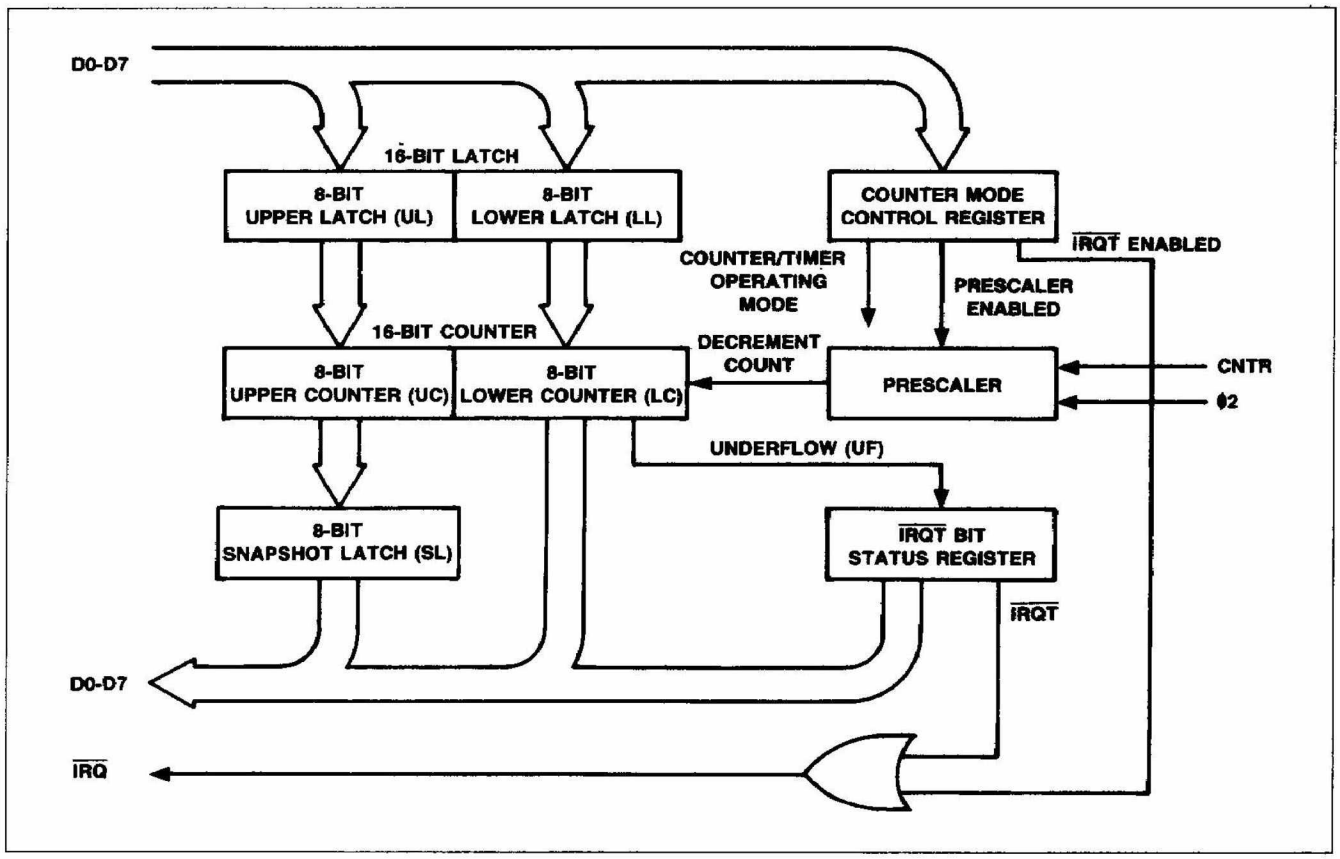


Figure 4. Counter/Timer

CA2 INPUT MODE (BIT 5 = 0) **CONTROL REGISTER A (CRA)**

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			$\overline{\text{IRQA}}$/IRQA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	ORA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$/IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQA1 FLAG
1 A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
0 No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.

Bit 2 OUTPUT REGISTER A SELECT
1 Select Output Register A.
0 Select Data Direction Register A.

Bit 1 IRQA1 POSITIVE TRANSITION
1 Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
0 Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.

Bit 0 $\overline{\text{IRQA}}$ ENABLE FOR IRQA1
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQA2 FLAG
1 A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
0 No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.

Bit 5 CA2 MODE SELECT
0 Select CA2 Input Mode.

Bit 4 IRQA2 POSITIVE TRANSITION
1 Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
0 Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.

Bit 3 $\overline{\text{IRQA}}$ ENABLE FOR IRQA2
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero.

Bit 5 CA2 MODE SELECT
1 Select CA2 Output Mode.

Bit 4 CA2 OUTPUT CONTROL
1 CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
0 CA2 goes low on the first negative (high-to-low) Ø2 clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.

Bit 3 CA2 READ STROBE RESTORE CONTROL (BIT 4 = 0)
1 CA2 returns high on the next Ø2 clock negative transition following a read of Output Register A.
0 CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 5. Summary of Control Lines Operation (1 of 2)

CB2 INPUT MODE (BIT 5 = 0) **CONTROL REGISTER B (CRB)**

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			$\overline{\text{IRQB}}$/IRQB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	ORB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$/IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQB1 FLAG
1 A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.

Bit 2 OUTPUT REGISTER B SELECT
1 Select Output Register B.
0 Select Data Direction Register B.

Bit 1 IRQB1 POSITIVE TRANSITION
1 Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1.
0 Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1.

Bit 0 $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQB2 FLAG
1 A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.

Bit 5 CB2 MODE SELECT
0 Select CB2 Input Mode.

Bit 4 IRQB2 POSITIVE TRANSITION
1 Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
0 Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.

Bit 3 $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero.

Bit 5 CB2 MODE SELECT
1 Select CB2 Output Mode.

Bit 4 CB2 OUTPUT CONTROL
1 CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
0 CB2 goes low on the first negative (high-to-low) Ø2 clock transition following a write to Output Register B. CB2 returns high as specified by bit 3.

Bit 3 CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1 CB2 returns high on the next Ø2 clock negative transition following a write to Output Register B.
0 CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 5. Summary of Control Lines Operation (2 of 2)

COUNTER/TIMER REGISTERS

COUNTER MODE CONTROL REGISTER (CMCR)

The 8-bit Counter Mode Control Register (CMCR) selects the Counter/Timer mode of operation and enables or disables both the internal $\overline{IRQT}$ and the Prescaler. The format of the CMCR is:

7	6	5	4	3	2 1 0
$\overline{IRQT}$ Enabled	0	0	Prescaler Enabled	0	Counter/Timer Mode

Bit 7 — **$\overline{IRQT}$ Enabled**
- 0 $\overline{IRQT}$ Disabled
- 1 $\overline{IRQT}$ Enabled

Bits 6-5 — **Not used, don't care value during write.**

Bit 4 — **Prescaler Enabled**
- 0 Prescaler Disabled ($\div 1$)
- 1 Prescaler Enabled ($\div 16$)

Bit 3 — **Not used, don't care value during write.**

Bits 2-0

2	1	0	Counter/Timer Mode
0	0	0	Mode 0—Disable Counter/Timer
0	0	1	Mode 1—One-Shot Interval Timer
0	1	0	Mode 2—Free-Run Interval Timer
0	1	1	Mode 3—Pulse Width Measurement
1	0	0	Mode 4—Event Counter
1	0	1	Mode 5—One-Shot Pulse Width Generation
1	1	0	Mode 6—Free-Run Pulse Generation
1	1	1	Mode 7—Retriggerable Interval Timer

The CMCR can be written into at any time without disabling or stopping the Counter/Timer. This allows the Counter/Timer mode of operation to be changed while it is still in operation. However, selecting Mode 0 disables the Counter/Timer and stops its operation. The Prescaler and the $\overline{IRQT}$ interrupt can also be enabled or disabled at any time. The CMCR is written to when the register address is 3 and R/$\overline{W}$ is low.

STATUS REGISTER (SR)

The 8-bit Status Register (SR) reports the status of three interrupt conditions: Counter underflow ($\overline{IRQT}$), Port A interrupt ($\overline{IRQA}$) and Port B interrupt ($\overline{IRQB}$). The format of the Status Register is:

7	6	5	4	3	2	1	0
UF ($\overline{IRQT}$) Interrupt Flag	IRQA Interrupt Flag	IRQB Interrupt Flag	1	1	1	1	1

Bit 7 **Counter Underflow (UF) Interrupt Flag**
- 0 Counter underflow has not occurred.
- 1 Counter underflow has occurred.

Bit 6 **IRQA Interrupt Flag**
- 0 Port A interrupt has not occurred.
- 1 Port A interrupt has occurred.

Bit 5 **IRQB Interrupt Flag**
- 0 Port B interrupt has not occurred.
- 1 Port B interrupt has occurred.

Bit 4-0 **Not used, always read as shown in register figure.**

The Counter Underflow (UF) Interrupt, bit 7, is updated in the same clock cycle that an underflow condition occurs on the Counter/Timer. The IRQA and IRQB interrupt flags (bits 6 and 5) are updated at the rising edge of the next Ø2 clock immediately following the setting of corresponding interrupt bits in the CRA register. The IRQA Interrupt Flag is set whenever the IRQA1 or IRQA2 bit is set. The IRQB Interrupt Flag is set whenever the IRQB1 or IRQB2 bit is set. The Counter Underflow bit is cleared whenever the Snapshot Latch is read, the Upper Latch (UL) is written to at register address 0, Mode 0 is selected in the CMCR, or a $\overline{RES}$ occurs. The Status Register is read when the register address is 3 and R/$\overline{W}$ is high.

LOWER LATCH (LL)

The Lower Latch (LL) holds the least significant 8-bits of the 16-bit latch value. The LL is written from the data bus (D0–D7) when the register address is 2 and R/$\overline{W}$ is low. When the LL is loaded, the contents of the UC are copied into the Snapshot Latch (SL) without affecting the counting operation of the UC.

UPPER LATCH (UL)

The Upper Latch (UL) holds the most significant 8-bits of the 16-bit latch value. The UL is written from the data bus (D0–D7) when R/$\overline{W}$ is low and the register address is either 0 or 1. The difference in the two register address functions are:

Register Address 0

1. The UL is loaded from D0–D7.
2. The contents of the latches (UL and LL) are transferred to the counters (UC and LC, respectively).
3. The UF bit is cleared in the SR.
4. The Counter is enabled, i.e., the count in UC and LC is decremented by one upon detection of a rising edge on either Ø2 or CNTR (depending upon mode selection) as scaled by the Prescaler.

Register Address 1

1. The UL is loaded from D0–D7.
2. All other elements of the Counter/Timer are unaffected.

LOWER COUNTER (LC)

The Lower Counter (LC) holds the least significant 8-bits of the 16-bit counter.

When the LC decrements below $00, 1 is borrowed from the UC to load $FF into the LC.

The LC is read to the data bus (D0-D7) when the register address is 2 and R/$\overline{W}$ is high. When LC is read, the 8-bit contents of the UC is transferred to the Snapshot Latch without affecting the operation of the counter (i.e., the count-down continues without interruption).

UPPER COUNTER

The Upper Counter (UC) holds the most significant 8-bits of the 16-bit counter. The UC is read to the data bus (D0-D7) when the register address is 1 and R/$\overline{W}$ is high. When the UC is read, there is no other effect on the Counter/Timer operation. Counter underflow occurs when the LC borrows a 1 from an UC value of $00.

Note:

When reading the UC directly, the value read can be one count too high if the LC value is just above $00 at the start of the read since an underflow in the LC will result in decrementing the UC by one count. The Snapshot Latch should be read to obtain the UC value corresponding to the LC value.

SNAPSHOT LATCH (SL)

The Snapshot Latch holds the value of the UC corresponding to the LC value. The SL is loaded with the value of the UC when the LL is written to, or when the LC is read. The SL is read to the data bus (D0-D7) when the register address is 0 and R/$\overline{W}$ is high, without affecting the counting operation. When the SL is read, the UF in the SR is cleared. Since the SL is loaded with the value of the UC whenever the LC is read, an accurate count of the total 16-bit counter can be made without the need for further calculations to account for delays between the reading of the LC and the UC.

COUNTER/TIMER OPERATION

The Counter/Timer has eight modes of operation. The Counter/Timer is always either disabled (mode 0) or operating in one of the other seven modes as selected in the Counter Mode Control Register (CMCR).

To operate the Counter/Timer, first issue Mode 0 to stop any counting in progress due to a previously selected mode, to clear the counter underflow bit in the SR and to disable the $\overline{IRQT}$ interrupt. The order of mode selection and latch loading depends upon the desired mode. Generally, if a timer mode based on the Ø2 clock rate is to be selected, first select the mode then write the timer initialization value to the latch. Write the LL first then the UL value (to register address 0). When the UL is written, the UL and LL values are loaded into the UC and LC, respectively, and the counter is enabled. The counter then decrements one count for every positive edge (low to high) transition detected on the Ø2 or CNTR input (depending on the selected mode) as scaled by the Prescaler. In most modes, each time the counter underflows below $0000, the underflow bit is set in the SR, the counter reloads to the latch value and the down-counting continues. If the UF bit is set when the $\overline{IRQT}$ is enabled in the CMCR, the $\overline{IRQ}$ output will be asserted to the processor.

MODE 0—DISABLE COUNTER/TIMER

The Counter/Timer is disabled (all counting stops), the $\overline{IRQT}$ interrupt (bit 7 in the CMCR) is disabled, and the counter underflow (bit 7 in the SR) is cleared. Mode 0 may be selected at any time by selecting Mode 0 in the CMCR or upon $\overline{RES}$ which initializes the CMCR to $00. Selecting Mode 0 in the CMCR does not affect any data in the LL or UL, any count in the LC or UC, or any data in the SL.

MODE 1—ONE SHOT INTERVAL TIMER

The counter counts down once from the latch value at the Ø2 clock rate (as scaled by the Prescaler) and sets the UF bit in the SR upon underflow. The counter starts when data is written to the UL at register address 0, which causes the UL and LL values to be loaded into the UC and LC, respectively. When the counter decrements below $0000, the UF bit in the SR is set. The set UF bit causes $\overline{IRQ}$ to be asserted if the $\overline{IRQT}$ Enable bit is set in the CMCR. Upon decrementing below $0000, the UC and LC are automatically reset to a value of $FFFF and the counter continues down-counting. However, the UF bit in the SR will not be set again (due to the counter again decrementing through $0000) until the UL is again written at register address 0. The CNTR line is not used in this mode. Figure 6 shows the timing relationship for Mode 1 operation.

Typical Application: Can be used for an accurate time delay such as would be required to control the duration of time to have a thermal printer element activated.

MODE 2—FREE-RUN INTERVAL TIMER

The counter repetitively counts down at the Ø2 clock rate, as scaled by the Prescaler, and sets the UF bit in the SR each time the counter underflows. The counter is initialized to the UL and LL values and starts down counting at the clock rate when the UL value is written to register address 0. Each time the counter decrements below $0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the count-down cycle continues. If the $\overline{IRQT}$ Enable bit is set in the CMCR, $\overline{IRQ}$ will be asserted upon each time-out. The CNTR line is not used in this mode. Figure 7 shows the timing relationship for Mode 2 operation.

Typical Application: Can be used for a timed interrupt structure when a hardware location needs updating at specific intervals, such as would be required to update a multiplexed display.

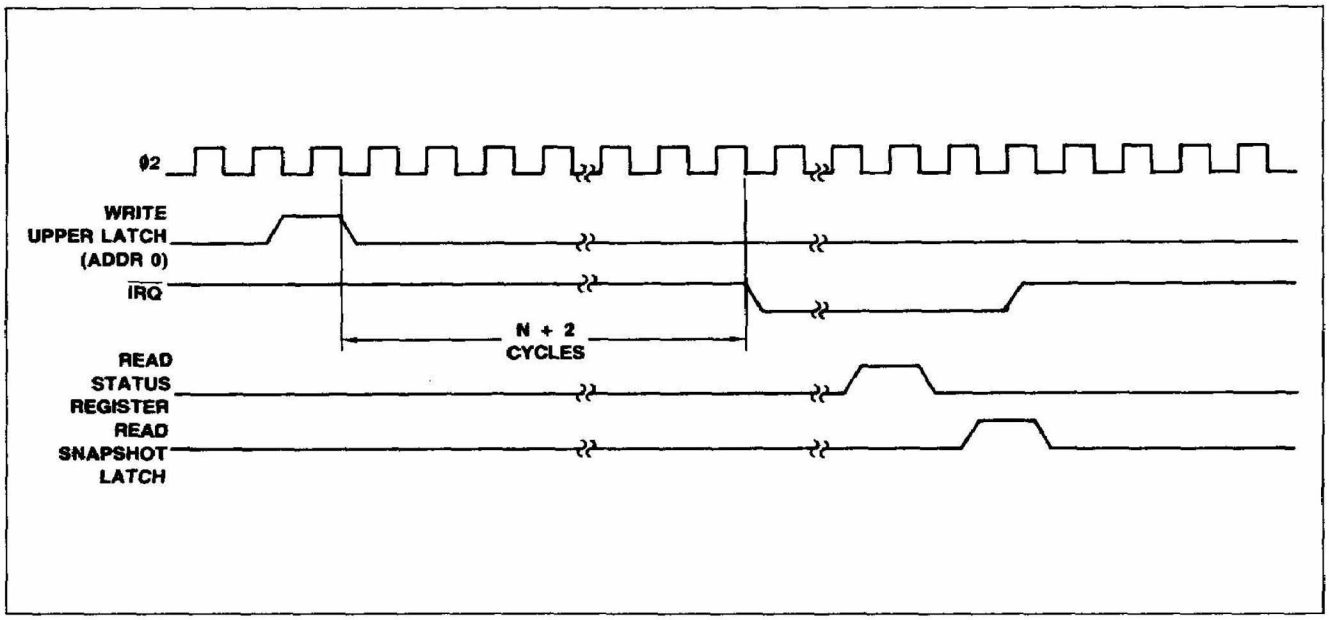


Figure 6. Mode 1—One-Shot Interval Timer Timing

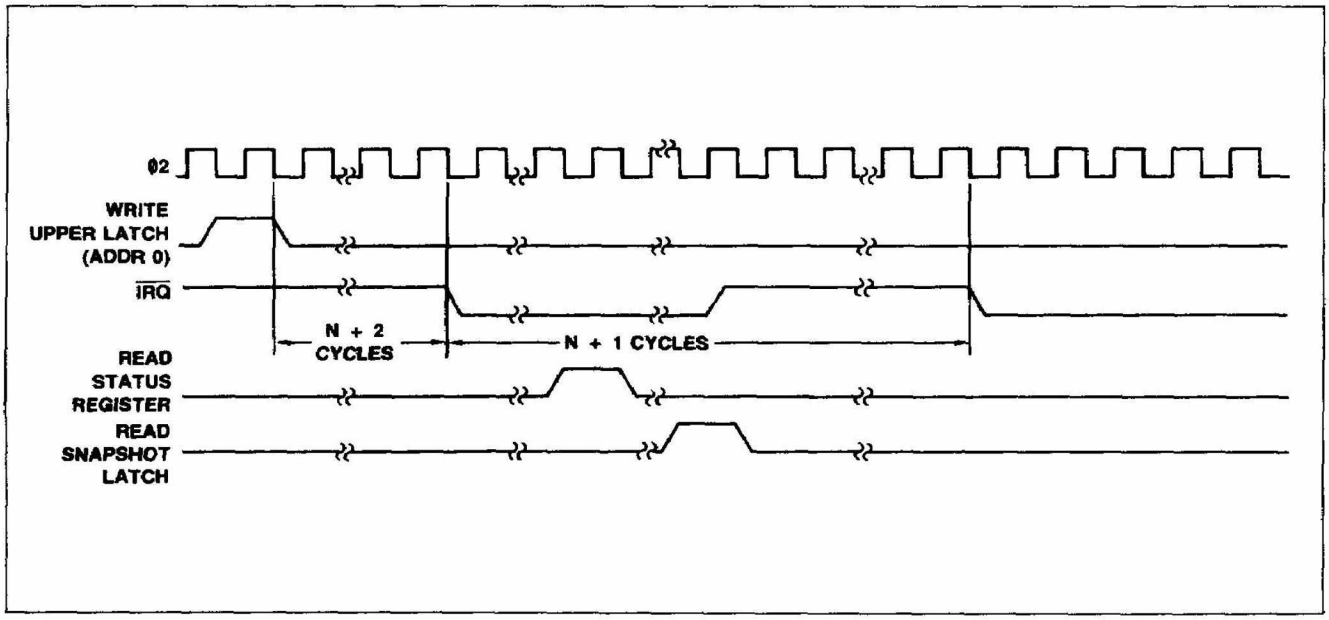


Figure 7. Mode 2—Free-Run Interval Timer Timing

MODE 3—PULSE WIDTH MEASUREMENT

The counter counts down from the latch value at the ϕ2 clock rate (scaled by the Prescaler) from the time the CNTR input goes low until CNTR goes high to provide a measurement of the CNTR low pulse duration. The counter is loaded with the value of the UL and LL upon writing UL to register address 0. The counter starts decrementing at the scaled ϕ2 clock rate when the CNTR line goes low and stops decrementing when the CNTR line returns high. If the counter decrements below $0000 before the CNTR line goes high, the UF bit in the SR is set, the counter is reloaded with the UL and LL value, and the cycle continues down until CNTR goes high. Once the CNTR line has cycled from high to low and back to high, the Counter/Timer will ignore any additional high to low transitions on the CNTR line. To reinitiate Mode 3, it is necessary to reload the UL by writing to register address 0. Figure 8 shows the timing relationships for a Mode 3 operation.

Typical Application: Can be used to measure the duration of an event from an external device. Allows an accurate measurement of the duration of a logical low pulse on the CNTR line.

MODE 4—EVENT COUNTER

CNTR is an input and the Counter/Timer counts the number of positive transitions on CNTR. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter then decrements one count on the falling edge of the CNTR input after a falling edge (high-to-low transition) is detected on the ϕ2 clock. The maximum rate at which this falling edge can be detected is one-half the ϕ2 clock rate. When the counter decrements below $0000, the UF bit in the SR is set, the counter is reloaded with the UL and LL value and the operation repeats. Figure 9 shows the timing relationship of a Mode 4 operation.

Typical Application: Can be used with a timed software loop to count external events (i.e., a frequency counter).

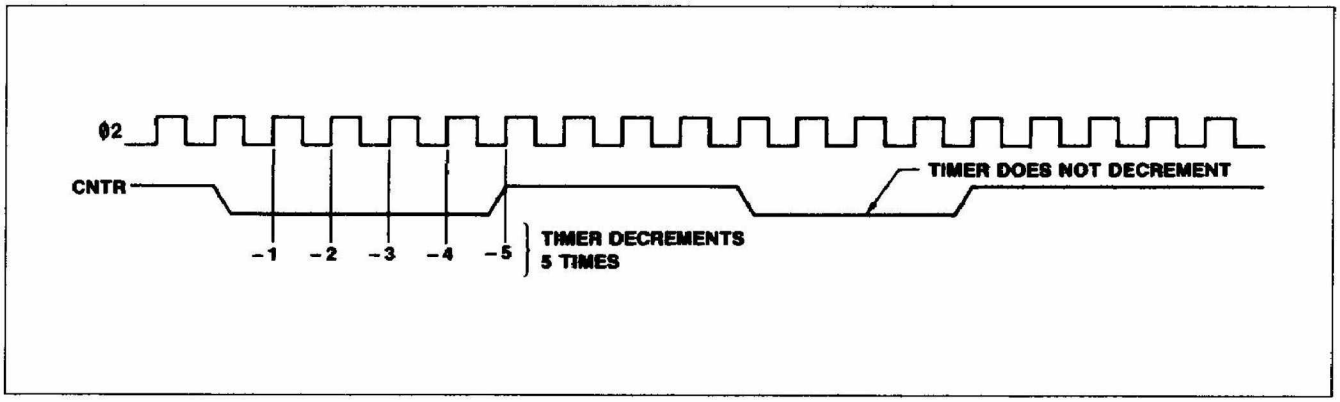


Figure 8. Mode 3—Pulse Width Measurement Timing

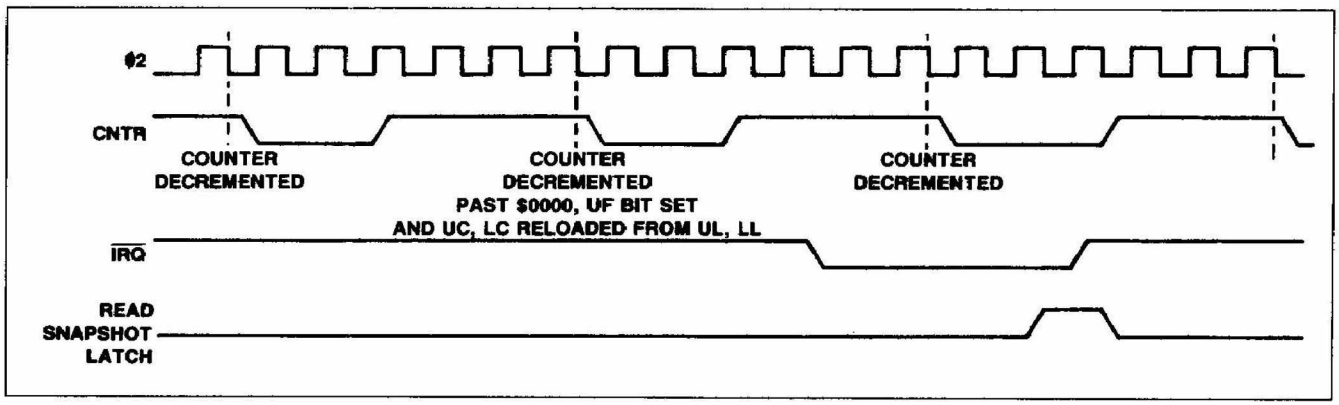


Figure 9. Mode 4—Event Counter Timing

MODE 5—ONE-SHOT PULSE WIDTH GENERATION

CNTR is an output which can be pulsed low for a programmed time interval. When this mode is selected in the CMCR, the CNTR output goes high if the UF bit is set. It goes low if the UF bit is cleared. The CNTR line then goes low when data is written to the UL at register address 0, which also starts the counter. The counter decrements from the UL and LL value at the Ø2 clock rate as scaled by the Prescaler. When the counter decrements below $0000, the CNTR output goes high, the UF bit is set in the SR, the counter is reloaded with $FFFF and the count-down continues. Figure 10 shows the timing relationship of Mode 5 operation.

Note that clearing the UF bit after it is set upon the first timeout causes CNTR to go low, in which case CNTR will again go high upon the next counter timeout.

Typical Application: Can be used to hold-off (delay) an external hardware event on an asynchronous basis such as disallowing a motor startup until certain parameters are met.

MODE 6—FREE-RUN PULSE GENERATION

CNTR is an output and the Counter/Timer can be programmed to generate a symmetrical waveform, an asymmetrical waveform, or a string of varying width pulses on CNTR. The CNTR line is forced low when data is written to the UL at register address 0 which also starts the counter. The counter decrements at the Ø2 clock rate as scaled by the Prescaler. When the counter decrements below $0000, CNTR toggles from low to high (or high to low depending upon its initial state), the counter is reloaded with the UL and LL value and the counter continues down-counting. The UF bit in the SR is set the first time the counter decrements past $0000 and is cleared only if a new write to UL at register address 0 occurs. Figure 11 shows the timing relationship of a Mode 6 operation.

This mode can be used to generate an asymmetrical waveform by toggling the UL and LL with the CNTR high and low times. Immediately after starting the counter with the first CNTR low time, load the LL and UL (by writing to register address 1, which does not restart the counter) with the CNTR high time. When the first counter underflow occurs, the counter loads the new latch value (i.e., the CNTR high time) into the counter and continues counting. During the $\overline{IRQ}$ interrupt processing resulting from the first counter time-out, load the LL and UL (at register address 1) with the original CNTR low time. Continue to alternate loading of the high and low time latch values during the interrupt processing for the duration of the mode.

Typical Application: Can be used to supply external circuitry with a software variable clock based upon the system Ø2 clock (e.g., a tone generator for audio feedback).

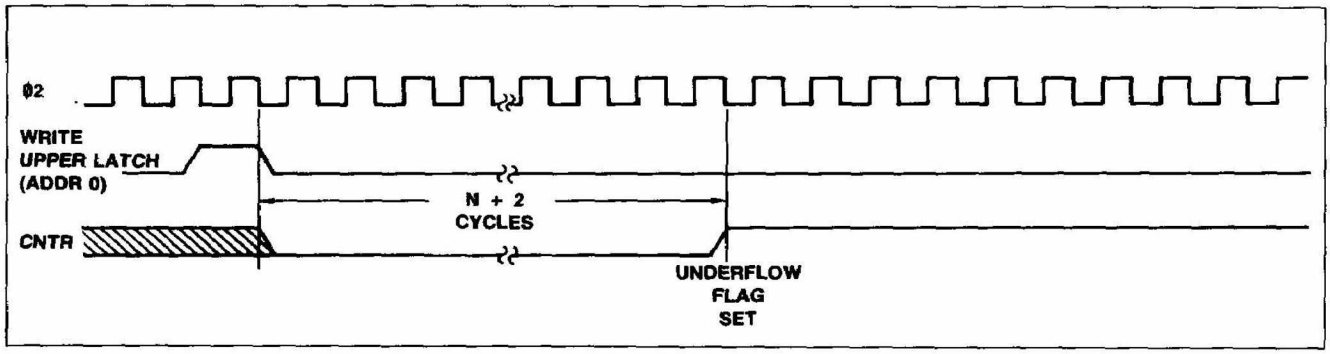


Figure 10. Mode 5—One-Shot Pulse Width Generation Timing

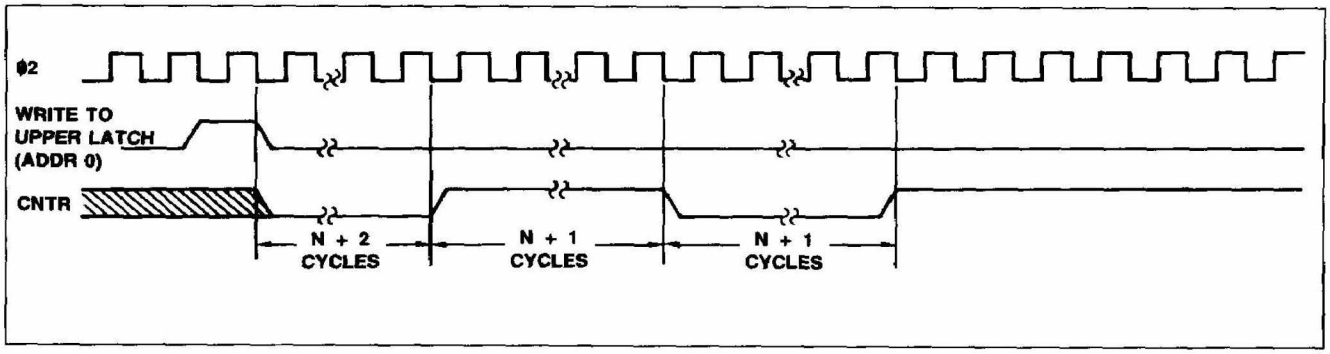


Figure 11. Mode 6—Free-Run Pulse Generation Timing

MODE 7—RETRIGGERABLE INTERVAL TIMER

The Counter/Timer operates as a timer which is retriggered, i.e., reinitialized to its starting value, upon detection of a negative transition on the CNTR input. The counter is initially loaded with the UL and LL value when the UL is written to register address 0. The counter starts decrementing at the Ø2 clock rate (as scaled by the Prescaler) when a falling edge (high to low transition) is detected on CNTR. The counter is reinitialized to the UL and LL value whenever a falling edge is subsequently detected on CNTR. If the counter decrements past $0000 before the falling edge is detected, the UF bit is set in the SR, the counter is initialized to the UL and LL value and the count-down continues.

Typical Application: Can be used to monitor signals that should be periodic and can interrupt the processor if the signal being monitored does not occur within a specified time frame; such as a synchronous motor that has fallen out of synchronization.

PRESCALER

The Counter/Timer operates in either the divide by one or divide by sixteen mode. In the divide by one mode, the counter holds from 1 to 65,535 counts. The counter capacity is therefore 1 μs to 65,535 μs at 1 MHz Ø2 clock rate or 0.25 μs to 16,383 μs at a 4 MHz Ø2 clock rate. Timer intervals greater than the maximum counter value can be easily measured by counting underflow flags or $\overline{IRQ}$ interrupt requests.

The divide by sixteen prescaler can be enabled to extend the timing interval by 16. This provides timing from 1048.56 ms (1 MHz) to 260.21 ms (4 MHz). The prescaler clocks the Counter/Timer at the Ø2 clock rate divided by sixteen, except for Mode 4. In Mode 4, sixteen positive CNTR edges must occur to decrement the Counter/Timer by one count.

INITIALIZING THE COUNTER/TIMER

The following program segment is one suggested technique for initializing the Counter/Timer:

```
;Data Definition
   SL    = $XXX0    ;Snapshot Latch
   UC    = $XXX1    ;Upper Counter
   LC    = $XXX2    ;Lower Counter
   SR    = $XXX3    ;Status Register
   ULEC  = $XXX0    ;Upper Latch and Enable Counter
   UL    = $XXX1    ;Upper Latch
   LL    = $XXX2    ;Lower Latch
   CMCR  = $XXX3    ;Counter Mode Control Register

;Program
   LDA   #$mode0    ;disable Counter/Timer
   STA   CMCR       ;write to mode register
   LDA   #$mode     ;select mode and Prescaler and
                      IRQT enable/disable
   STA   CMCR       ;write to mode register
   LDA   #$lovalue  ;lower latch value
   STA   LL         ;write to lower latch
   LDA   #$hivalue  ;upper latch value
   STA   ULEC       ;write to upper latch
                    ;clear underflow flag, and enable
                      counter
```

The following instructions change the mode while the Counter/Timer is in operation:

```
   LDA   #$mode     ;select desired mode, except
                      mode 0
   STA   CMCR       ;write to mode register
```

The change of mode operation will take effect immediately. Thus, the Free-Run Internal Timer mode (Mode 2) could be systematically stopped by changing to the One-Shot Interval Timer mode (Mode 1). The Counter/Timer will then halt operation when the underflow condition occurs. This technique can also be used to enable or disable $\overline{IRQ}$ during program execution.

READING THE COUNTER/TIMER

To service an interrupt request, the following sequence can be used:

```
   BIT   $status    ;get underflow flag
   BNE   error      ;check if flag is set
   LDA   $LC        ;get low counter value for overflow
   LDX   $SL        ;get high counter value for overflow
                    ;underflow flag is cleared
```

By reading the LC and SL, it is possible to determine the amount of time between the interrupt request and servicing the interrupt.

To read a timer value at any time, the suggested technique is as follows:

```
   LDA   $LC        ;get low counter value
                    ;upper counter transferred to
                      snapshot
         .          ;any miscellaneous code to store
         .            value if desired
         .
   LDA   $SL        ;get high counter value
```

READ/WRITE TIMING CHARACTERISTICS OF PIAT

Figure 13 is a timing diagram for the R65C24 PIAT during a Read operation (input mode). Figure 14 is a timing diagram for the PIAT during a Write operation (output mode).

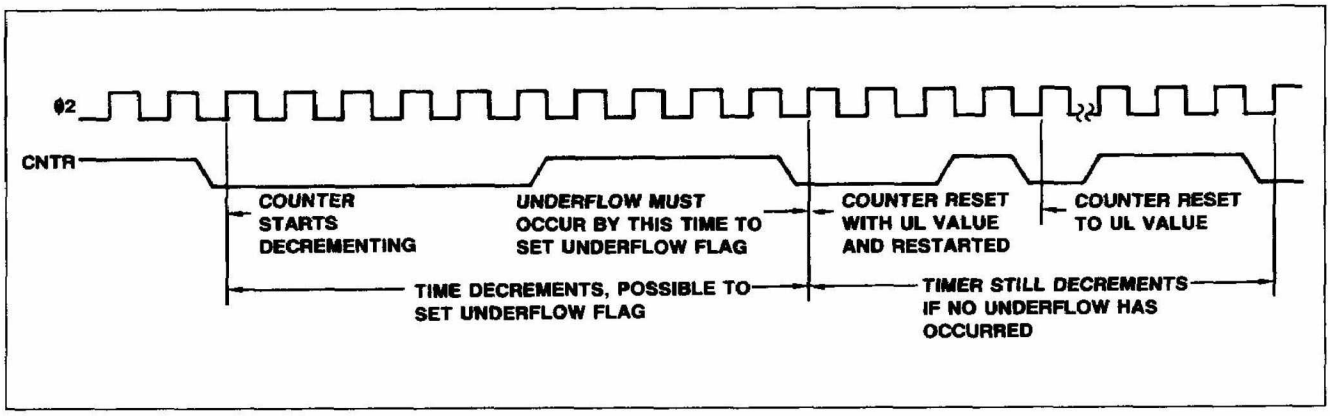


Figure 12. Mode 7—Retriggerable Interval Timer Timing

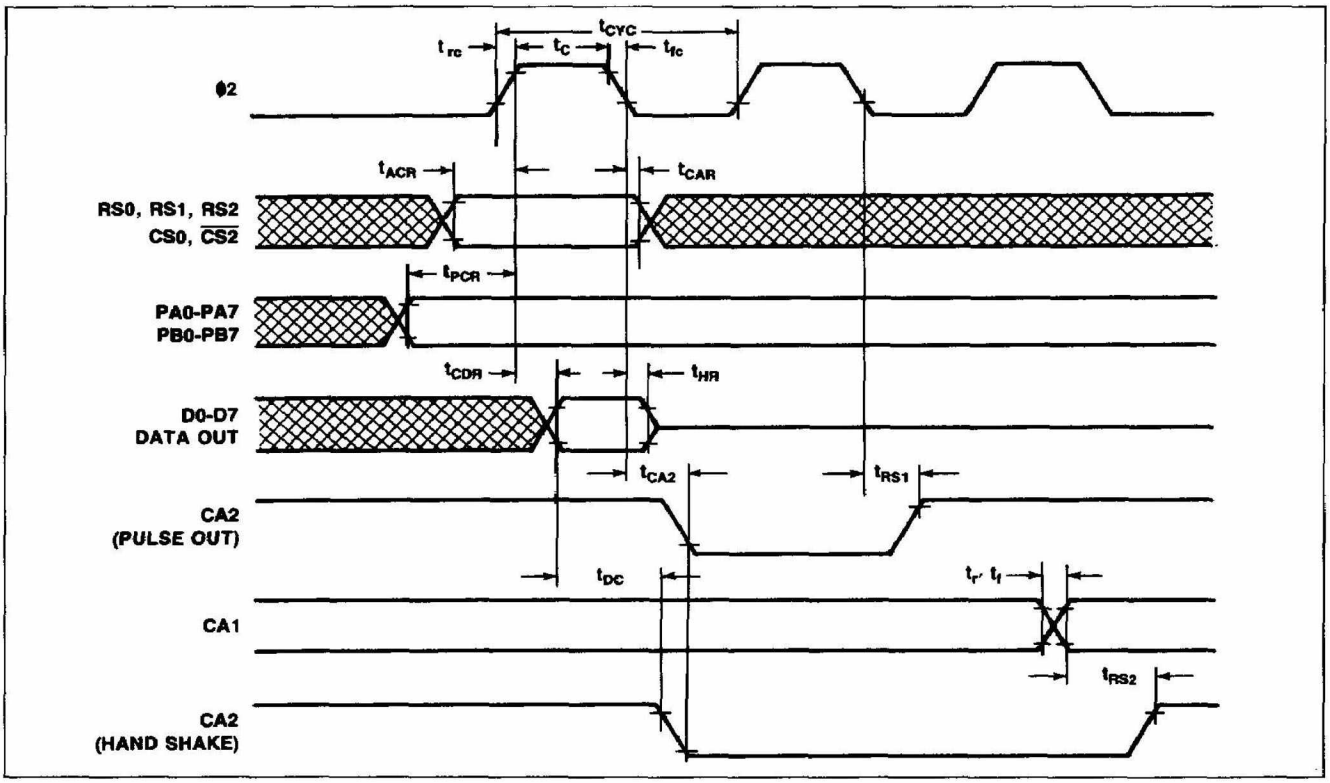


Figure 13. Read Timing Diagram

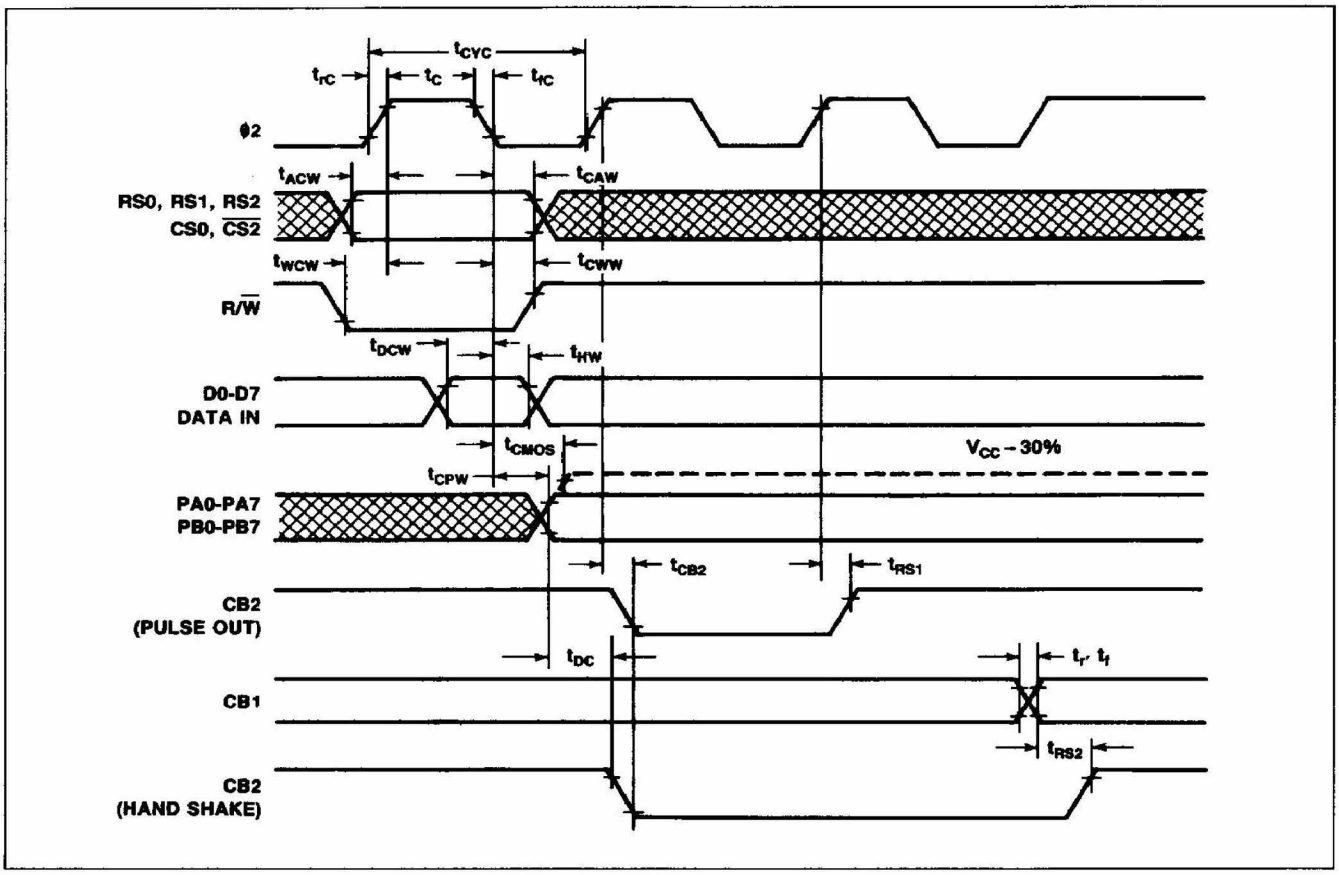


Figure 14. Write Timing Diagram

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4 Vdc when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

BUS TIMING

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Ø2 Cycle	t_{CYC}	1.0	—	0.5	—	0.33	—	0.25	—	μs
Ø2 Pulse Width	t_C	450	—	220	—	160	—	110	—	ns
Ø2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	—	12	—	10	ns
Read										
Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	335	—	145	—	105	—	85	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns
Write										
Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0.5	μs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	110	—	75	—	ns
Ø2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Ø2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Ø2 Low to CNTR Low/High Delay	t_{CNTR}	—	1.0	—	0.5	—	0.5	—	0.5	μs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1.0	—	1.0	—	1.0	μs
Ø2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0.5	—	0.5	μs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1.5	0	0.75	0	0.5	0	0.37	μs
Ø2 High to CB2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.5	—	0.5	μs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	μs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1.0	—	1.0	—	1.0	μs

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 Vdc and a high voltage of 2.0 Vdc.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	T_L to T_H 0°C to 70°C −40°C to +85°C

ELECTRICAL CHARACTERISTICS

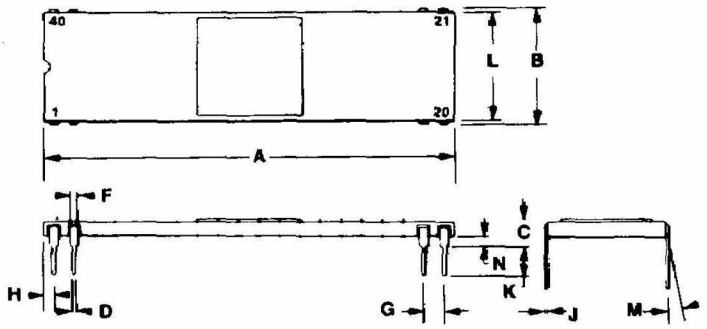
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[2]	Test Conditions
Input High Voltage All except R/W, CS2 R/W, CS2	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current R/W, RES, RS0, RS1, CS0, CS2, CA1, CB1, Ø2 RS2	I_{IN}	—	 ±1 ±1	 ±2.5 ±10	µA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7, PB0–PB7, CB2	I_{TSI}	—	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2	I_{IH}	−200	−400	—	µA	V_{IH} = 2.0V
Input Low Current PA0–PA7, CA2	I_{IL}	—	−2	−3.2	mA	V_{IL} = 0.8V
Output High Voltage Logic PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —	V	V_{CC} = 4.75V I_{LOAD}[2] = −200µA I_{LOAD}[2] = −3.2mA
Output Low Voltage PA0–PA7, CA2, PB0–PB7, CB2 D0–D7, IRQ, CNTR	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 −200 −3.2	 −1500 −6	 — —	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0–PA7, PB0–PB7, CB2, CA2 D0–D7, IRQ, CNTR	I_{OL}	 3.2 1.6	 — —	 — —	 mA mA	V_{OL} = 0.4V
Output Leakage Current (Off State) IRQ	I_{OFF}	—	1	±10	µA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D	—	7	10	mW/MHz	
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2 R/W, RES, RS0, RS1, RS2, CS0, CS2, CNTR, CA1, CB1, Ø2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

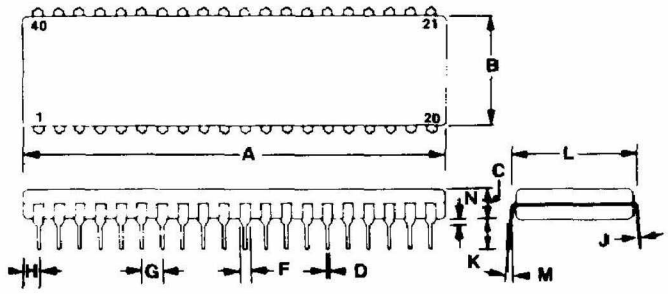
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



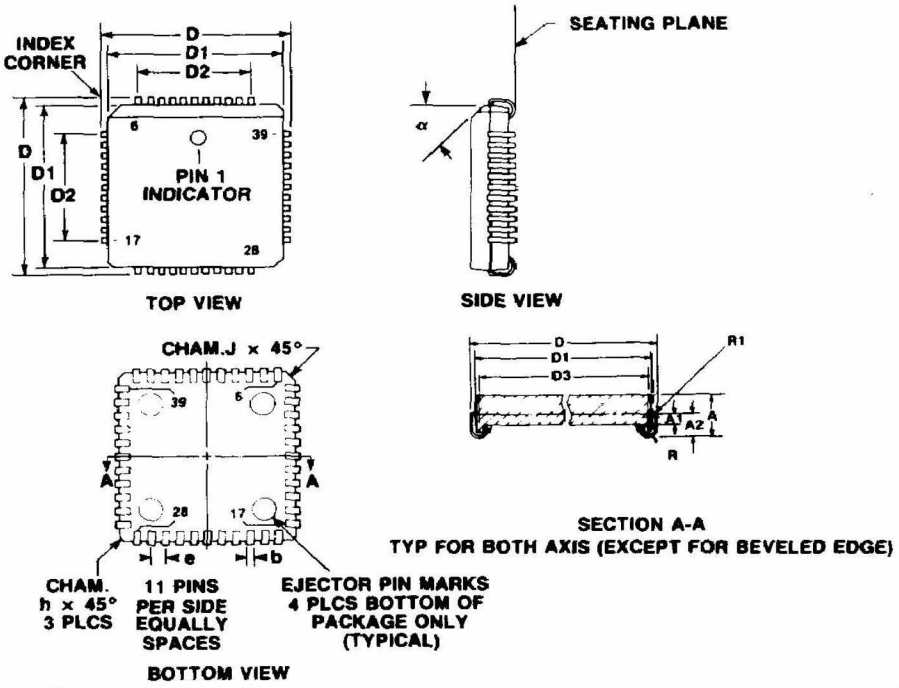
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	15.11	15.88	0.595	0.625
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.27	0.030	0.050
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	