Rockwell

R65F11 and R65F12 FORTH Based Microcomputers

SECTION 1 INTRODUCTION

1.1 FEATURES

- FORTH kernel in ROM
- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 192-byte static RAM
- 16 bidirectional, TTL-compatible I/O lines (two ports, R65F11) or 40 bidirectional, TTL-compatible I/O lines (five ports, R65F12)
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse width measurement
  - —Asymmetrical pulse generation
  - —Pulse generation
  - —Interval timer
  - —Event counter
  - —Retriggerable interval timer
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Synchronous shift register mode
  - —Standard programmable bit rates, programmable up to 62.5K bits/sec
- Ten interrupts
  - —Four edge-sensitive lines; two positive, two negative
  - —Reset
  - —Non-maskable
  - —Two counter
  - —Serial data received
  - —Serial data transmitted
- Expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two times internal frequency
  - —External clock input divided by one or two
- 1 μs minimum instruction execution time @ 2 MHz
- NMOS silicon gate, depletion load technology
- Single +5V power supply
- 12 mW standby power for 32 bytes of the 192-byte RAM
- 40-pin DIP (R65F11)
- 64-pin QUIP (R65F12) has three additional 8-bit I/O ports to provide a total of 40 I/O lines.

1.2 SUMMARY

The Rockwell R65F11 and R65F12 are complete, high-performance 8-bit NMOS single chip microcomputers, and are compatible with all members of the R6500 family.

The kernel of the high level Rockwell Single Chip RSC-FORTH language is contained in the preprogrammed ROM of the R65F11 and R65F12. RSC-FORTH is based on the popular fig-FORTH model with extensions. All of the run time functions of RSC-FORTH are contained in the ROM, including 16- and 32-bit mathematical, logical and stack manipulation, plus memory and input/output operators. The RSC-FORTH Operating System allows an external user program written in RSC-FORTH or Assembly Language to be executed from external EPROM, or development of such a program under the control of the R65FR1 RSC-FORTH Development ROM. Other development ROM's can also be accommodated.

The R65F11 and R65F12 consist of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 16 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of

computational power. These features in combination with the FORTH high level operating system make the R65F11 and R65F12 ideal for microcomputer applications.

For systems requiring additional I/O ports, the 64-pin QUIP version, the R65F12, provides three additional 8-bit ports.

A complete RSC-FORTH development system can be created with three MOS parts: the R65F11, one RAM chip and the R65FR1 Development ROM.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilites of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 ORDERING INFORMATION

Part No.	Description
R65F11P	40-Pin FORTH Based Microcomputer at 1 MHz
R65F11AP	40-Pin FORTH Based Microcomputer at 2 MHz
R65F12Q	64-Pin FORTH Based Microcomputer at 1 MHz
R65F12AQ	64-Pin FORTH Based Microcomputer at 2 MHz
R65FR1P	FORTH Development ROM for R65F11 or R65F12
R65FR2P	FORTH Development ROM for expanded capacity
R65FK2P	FORTH Kernel ROM for expanded capacity development
R65FR3P	FORTH Development ROM for R6501Q
R65FK3P	FORTH Kernel ROM for R6501Q
Order No.	**Description**
2148	FORTH Based Microcomputer User's Manual*

Note:
*Included with R65FR1.

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the R65F11 and R65F12 single chip microcomputers. Figure 2-1 is the Interface Diagram for the R65F11 and R65F12, Figure 2-2 shows the pin out configuration and Table 2-1 describes the function of each pin of the R65F11 and R65F12. Figure 3-1 is a detailed block diagram.

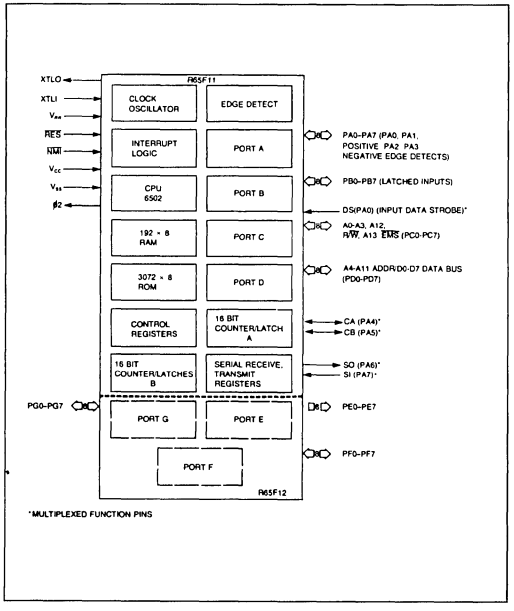
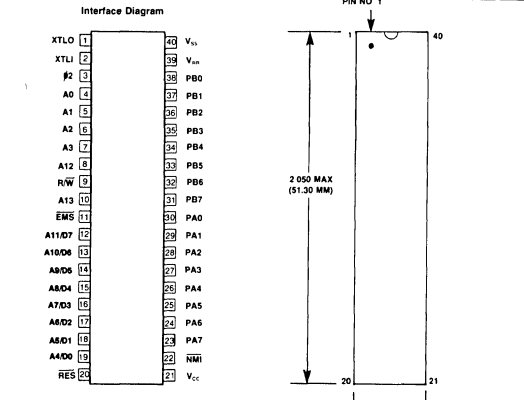


Figure 2-1. R65F11 and R65F12 Interface Diagram

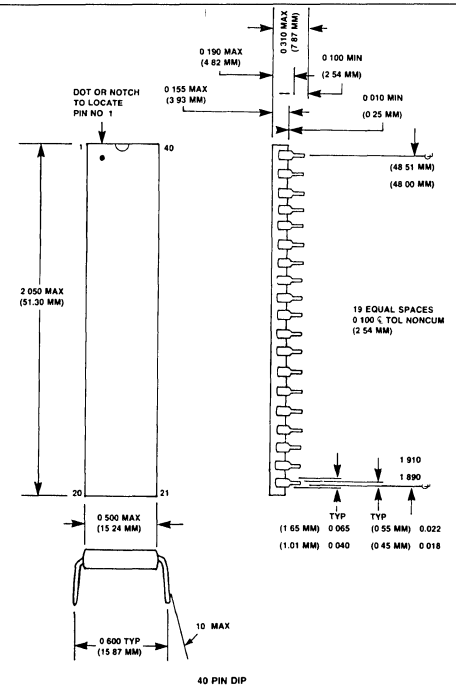
Table 2-1. R65F11 and R65F12 Pin Descriptions

Signal Name	Pin No. R65F11	Pin No. R65F12	Description
V_{CC}	21	50	Main power supply +5V
V_{RR}	39	12	Separate power pin for RAM. In the event that V_{CC} power is lost, this power retains RAM data.
V_{SS}	40	11	Signal and power ground (0V)
XTLI	2	10	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to V_{SS}, or X2 or X4 clock if XTLO is floated.
XTLO	1	9	Crystal output from internal clock oscillator.
$\overline{RES}$	20	41	The Reset input is used to initialize the R65F11. This signal must not transition from low to high for at least eight cycles after V_{CC} reaches operating range and the internal oscillator has stabilized.
$\phi 2$	3	13	Clock signal output at internal frequency.
$\overline{NMI}$	22	51	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7	30-23 38-31	64-57 8-1	Two 8-bit ports used for either input/output. Each line of Ports A and B consist of an active transistor to V_{SS} and a passive pull-up to V_{CC}.
PC0-PC7 A0-A3 A12, R/$\overline{W}$ A13, $\overline{EMS}$	4-11	25-32	Port C has an active pull-up transistor. Port D has active pull-up and pull-down transistors. Ports C and D lines form the external multiplexed address and data bus to allow external memory addressing.
PD0-PD7 A4-A11 D0-D7	19-12	40-33	
PE0-PE7 PF0-PF7 PG0-PG4 PG5-PG7		49-42 24-17 52-56, 14-16	On the R65F12, Port E may be used for output only. Ports F and G are similar to Ports A and B in construction and may be used for inputs or outputs.

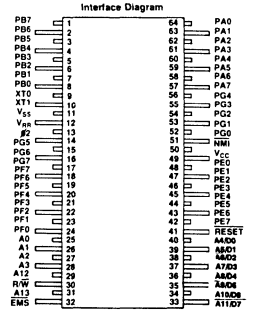
3



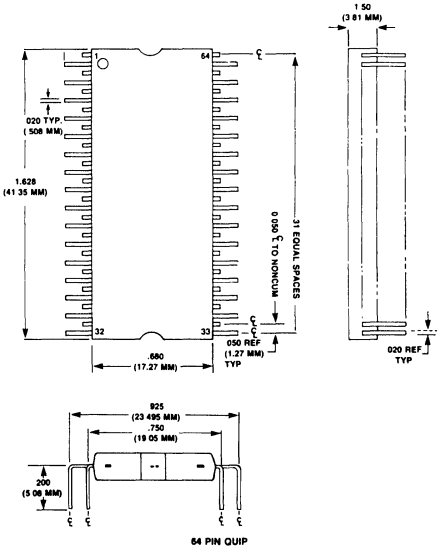
R65F11 Pin Out Designation



R65F11 Dimensional Outline



R65F12 Pin Out Designation



R65F12 Dimensional Outline

Figure 2-2. Pin Out Configuration

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the R65F11 and R65F12. Functionally the R65F11 consists of a CPU, RAM memory, two 8-bit parallel I/O ports (five in the 64-pin R65F12), a serial I/O port, dual counter/latch circuits, a mode control register, an interrupt flag/enable dual register circuit, and an internal Operating System. The kernel of FORTH in ROM complements the system hardware. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The R65F11 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, and ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal $\overline{IRQ}$ interrupt, or the external interrupt line $\overline{NMI}$. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 00FF-0040. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 00FF.

3.1.4 Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. See Appendix B for details.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Arithmetic And Logic Unit (ALU)

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.7 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

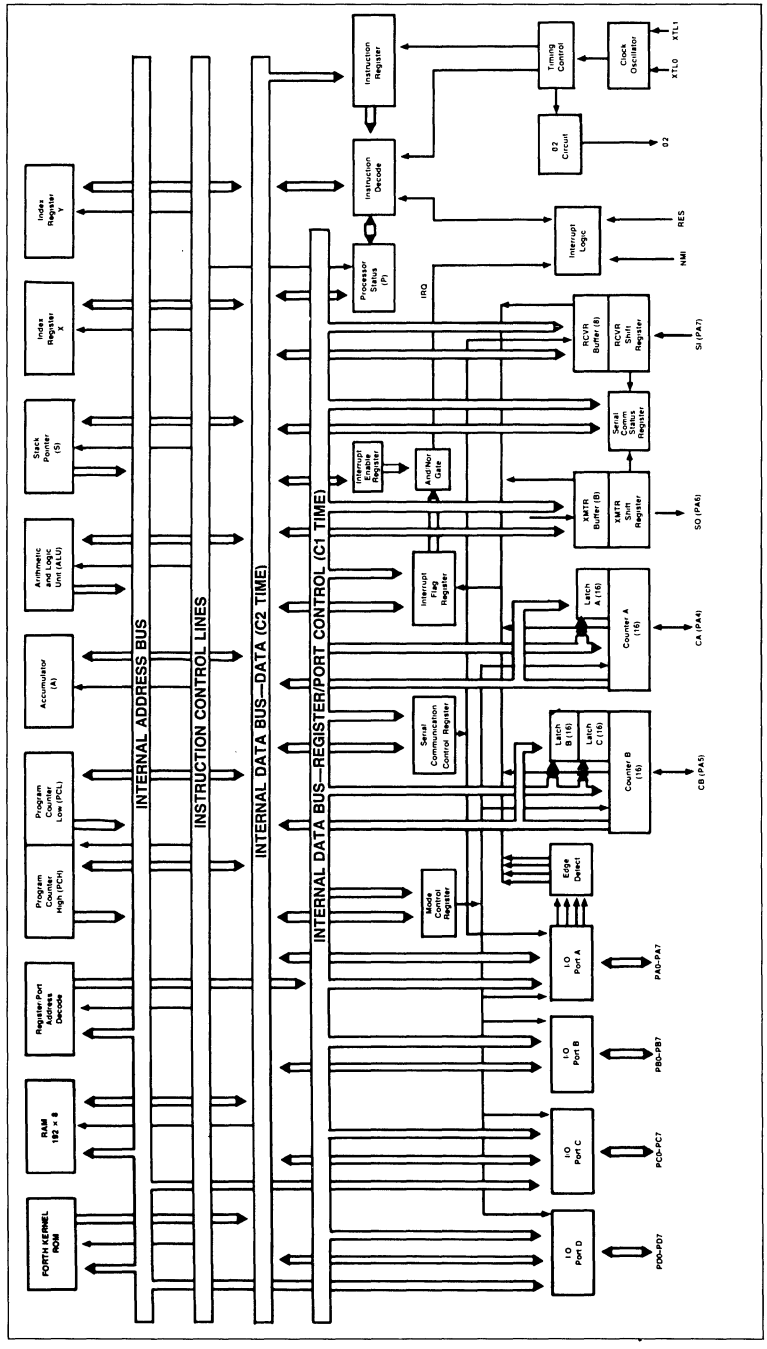


Figure 3-1. Detailed Block Diagram

3.1.8 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

3.1.9 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

3.2 CPU INSTRUCTION SET

The machine code instruction set of the R65F11 and R65F12 microcomputers are based on the popular R6500 microprocessor set. They contain all the instructions in the standard R6502 set, with the addition of the four new bit instructions added to the R6511 processor family. Refer to Appendix A for the Op Code mnemonics addressing matrix for details on these instructions.

3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of preprogrammed memory with an address space from F400 to FFFF. It contains the run time kernel of the high level language Rockwell Single Chip FORTH. There are 133 included functions stored in the ROM. Codes are in the format of a two byte code field, which identifies the interpreter assigned to execute that word, followed by a variable length Parameter Field, which contains the instructions and data used by that interpreter according to the programmed intention of that definition. See Appendix D for a complete list of the names of all included words. All words needed for support of the run time operation of dedicated applications programs are included. The RSC-FORTH Operating System is also part of the ROM code and is entered upon Reset. This Operating System allow the R65F11 and R65F12 to auto start a user program written in either RSC-FORTH or Assembly Language or enter a Development ROM if one is present. If no auto start program is found, an attempt will be made to boot an operating program from floppy disk.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R65F11 and R65F12 provide a separate power pin (V_{RR}) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of V_{CC} power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the V_{RR} pin. If the RAM data retention is not required then V_{RR} must be connected to V_{CC}. During operation V_{RR} must be at the V_{CC} level.

For the RAM to retain data upon loss of V_{CC}, V_{RR} must be supplied within operating range and $\overline{RES}$ must be driven low at least eight Ø2 clock pulses before V_{CC} falls out of operating range. $\overline{RES}$ must then be held low while V_{CC} is out of operating range and until at least eight Ø2 clock cycles after V_{CC} is again within operating range and the internal Ø2 oscillator is stabilized. V_{RR} must remain within V_{CC} operating range during normal operation. When V_{CC} is out of operating range, V_{RR} must remain within the V_{RR} retention range in order to retain data. Figure 3-2 shows typical waveforms.

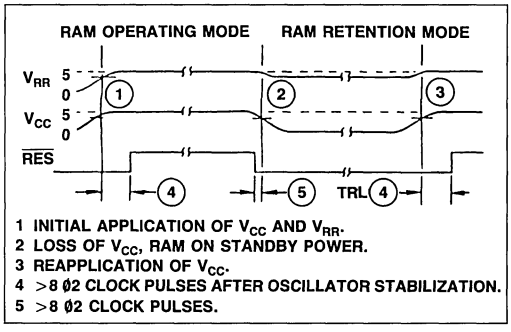


Figure 3-2. Data Retention Timing

3.5 CLOCK OSCILLATOR

A reference frequency can be generated with the on-chip oscillator using an external crystal. The oscillator reference frequency passes through an internal countdown network (divide by 2) to obtain the internal operating frequency.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-3a.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \quad \text{or} \quad C = 2C_L - 27 \text{ pF}$$

$$R_s \leq R_{smax} = \frac{2 \times 10^6}{(FC_L)^2} \quad F \text{ in MHz; } C_L \text{ in pF}$$

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a Crystal Manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 22 pF for a 4 MHz parallel resonant crystal, then

$$C = (2 \times 22) - 27 = 17 \text{ pF}$$
(use standard value, 18 pF)

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to V_{SS}, the internal coundown network is bypassed casuing the chip to operate at the freqency of the external source.

The R65F11 and R65F12 operate in the CLOCK MASTER mode. In this mode a frequence source (crystal or external source) must be applied to the XTLI and XTLO pins.

Ø2 is a buffered output signal which closely approximates the internal timing. When a common external source is used to drive multiple devices the internal timing between devices as well as their Ø2 outputs will be skewed in time. If skewing represents a system problem it can be avoided by the Master/Slave connection and options shown in Figure 3-4.

The R65F11 and R65F12 is operated in the CLOCK MASTER MODE. A second processor could be operated in the CLOCK SLAVE MODE. Mask options in the SLAVE unit convert the Ø2 signal into a clock input pin which is tightly coupled to the internal timing generator. As a result, the internal timing of the MASTER and SLAVE units are synchronized with minimum skew. If the Ø2 signal to the SLAVE unit is inverted, the MASTER and SLAVE UNITS WILL OPERATE OUT OF PHASE. This approach allows the two devices to share external memory using cycle stealing techniques.

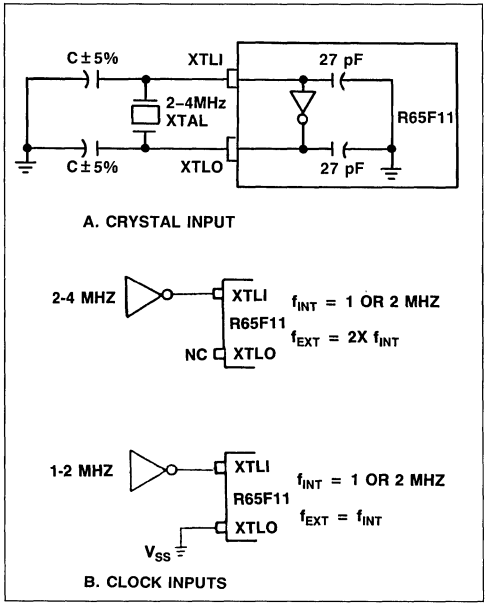


Figure 3-3. Clock Oscillator Input Options

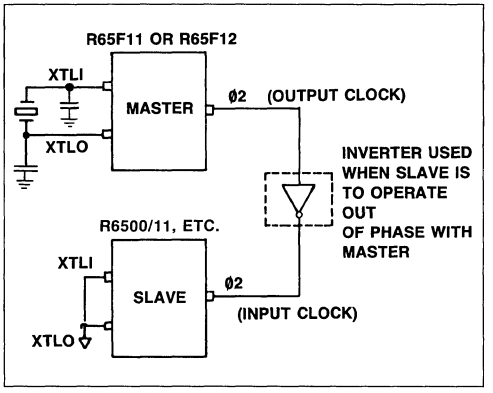


Figure 3-4. Master/Slave Connections

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R65F11 and R65F12 in any application. The Model Control Register bit assignment is shown in Figure 3-5. MCR Bits 7, 6, 5 must remain 1's in order for external memory referencing to be enabled.

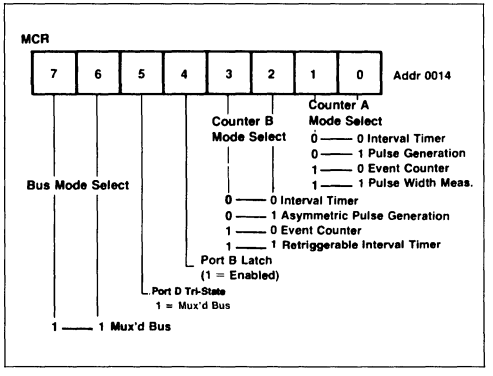


Figure 3-5. Mode Control Register

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared in low level code by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-6 and the functions of each bit are explained in Table 3-1.

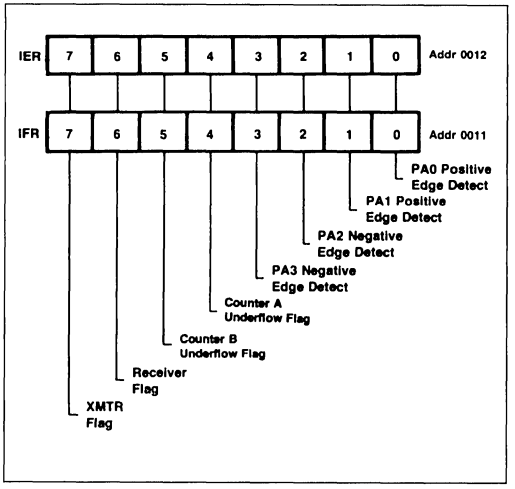


Figure 3-6. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Flag Register Bit Codes

Bit Code	Function
IFR 0:	PA0 Positive Edge Detect Flag—Set to a "1" when a positive going edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by $\overline{RES}$.
IFR 1:	PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by $\overline{RES}$.
IFR 2:	PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by $\overline{RES}$.
IFR 3:	PA3 Negative Edge Detect Flag—Set to 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or by $\overline{RES}$.
IFR 4:	Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.
IFR 5:	Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.
IFR 6:	Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by $\overline{RES}$.
IFR 7:	Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1. Cleared when the Transmitter Status bits (SCSR 6 & 7) are cleared or by $\overline{RES}$.

3.8 OPERATING SYSTEM

The system startup function, COLD, is executed upon Reset. COLD, a high level FORTH word, forms the basis of the RSC Operating System. Upon reset this function initializes the R65F11 or R65F12 registers to establish the external 16K byte memory map and disable all interrupt sources. It also sets up the serial channel for 1200 baud (assuming a 1 MHz internal clock) asynchronous transmission (seven bits, parity disabled). The internal FORTH structure "W" is prepared for use and the low level input/output vectors are forced to point to the system serial channel routines. The FORTH User Area Pointer, UP, is assigned the value 0300 Hex.

A test is made of the variable CLD/WRM in memory location 030E. If this contains a value other than A55A Hex a cold reset is assumed. In this case, the low level IRQ vector, IRQVEC; the low level NMI Vector, NMIVEC, and the high level interrupt vector, INTVEC, are all forced to point to the system reset routine. This prevents an unintentionally generated interrupt from crashing the system. System variables TIB, RO, SO, UC/L, UPAD, UR/W and BASE are also initialized to their default values.

Whether a warm or cold reset, the memory map is then searched at every 1K byte boundary starting at location 0400 Hex. The first two bytes at each boundary are checked against an A55A Hex bit pattern. This pattern indicates that an auto start program is installed. The next two bytes are assumed to point to the Parameter Field of the high level RSC-FORTH word to be executed upon reset. This may be the main function of a user defined program or the start up routine of a Development ROM. Figure 3-7 details proper alignment.

If no auto start ROM is found, the Operating System turns control over to a program that issues a "NO ROM" message to the systems terminal via the serial channel and attempts to boot a program from disk. A floppy disk controller, compatible with the WD1793 type, is assumed to be present at address 0100 Hex. The first half of Track 0 Sector 1 is loaded from a double density boot diskette into RAM starting at address 005F. When successfully loaded execution will be turned over to this boot program.

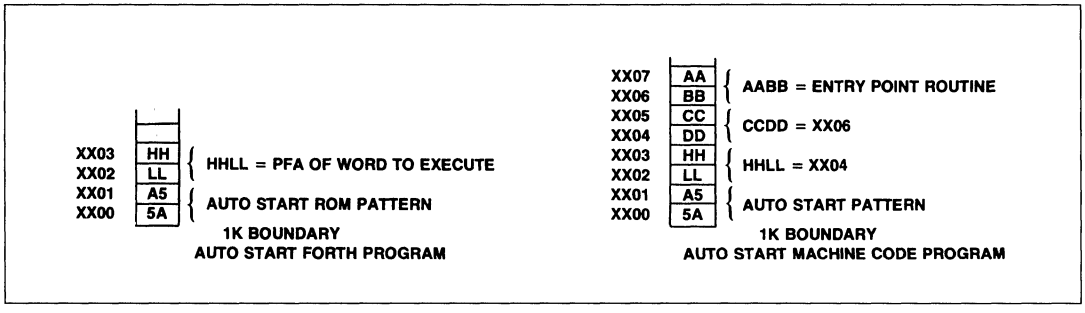


Figure 3-7. Auto Start ROM

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

The R65F11 has 16 I/O lines grouped into two 8-bit ports (PA, PB) and 16 lines programmed as an Address/Data bus (PC & PD). Ports A and B may be used either for input or output individually or in groups of any combination. The R65F12 has 24 additional port lines grouped into three 8-bit ports (PE, PF, PG).

Multifunction I/O's such as Port A are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FET's with an impedance range of 3K ≤ Rpu ≤ 12K ohm) are provided on all port pins.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1.

Table 4-1. I/O Port Addresses

Port	Address
A	0000
B	0001
E	0004
F	0005
G	0006

Appendix F.4 shows the I/O Port Timing.

4.1 INPUTS

Inputs for Ports A and B are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA and PB. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A and B are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as a standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-3 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the ∅2 clock rate. Edge detection timing is shown in Appendix F.4.

4.4 PORT B (PB)

Port B can be programmed as an 8 bit, bit independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-2 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided thru PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix F.4.

Table 4-2. Port B Control & Usage

Pin No. R65F11	Pin No. R65F12	I/O Mode MCR4 = 0 Signal Name	I/O Mode MCR4 = 0 Signal Type (1)	Latch Mode MCR4 = 1 (2) Signal Name	Latch Mode MCR4 = 1 (2) Signal Type
38	8	PB0	I/O	PB0	INPUT
37	7	PB1	I/O	PB1	INPUT
36	6	PB2	I/O	PB2	INPUT
35	5	PB3	I/O	PB3	INPUT
34	4	PB4	I/O	PB4	INPUT
33	3	PB5	I/O	PB5	INPUT
32	2	PB6	I/O	PB6	INPUT
31	1	PB7	I/O	PB7	INPUT

(1) Resistive pull-up, active buffer pull down
(2) Input data is stored in port B latch by PA0 pulse

Table 4-3. Port A Control and Usage

R65F11/R65F12 PORT[5]	PA0 I/O		PORT B LATCH MODE	
	MCR4 = 0		MCR4 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
PA0[2]	PA0	I/O	PORT B LATCH STROBE	INPUT[1]

	PA1-PA3 I/O	
	SIGNAL	
	NAME	TYPE
PA1[2] PA2[3] PA3[3]	PA1 PA2 PA3	I/O I/O I/O

	PA4 I/O		COUNTER A I/O			
PA4	MCR0 = 0 MCR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0[4] [6]		MCR0 = 1 MSR1 = 0 SCCR7 = 0 RCVR S/R MODE = 0[4]		SCCR7 = 0 SCCR6 = 0 MCR1 = 1	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA4	I/O	CNTA	OUTPUT	CNTA	INPUT (1)
	SERIAL I/O SHIFT REGISTER CLOCK					
	SCCR7 = 1 SCCR5 = 1		RCVR S/R MODE = 1[4]			
	SIGNAL		SIGNAL			
	NAME	TYPE	NAME	TYPE		
	XMTR CLOCK	OUTPUT	RCVR CLOCK	INPUT (1)		

	PA5 I/O		COUNTER B I/O			
PA5	MCR3 = 0 MCR2 = 0		MCR3 = 0 MCR2 = 1		MCR3 = 1 MCR2 = X	
	SIGNAL		SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE	NAME	TYPE
	PA5	I/O	CNTB	OUTPUT	CNTB	INPUT (1)

	PA6 I/O		SERIAL I/O XMTR OUTPUT	
PA6	SCCR7 = 0		SCCR7 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA6	I/O	XMTR	OUTPUT

	PA7 I/O		SERIAL I/O RCVR INPUT	
PA7	SCCR6 = 0		SCCR6 = 1	
	SIGNAL		SIGNAL	
	NAME	TYPE	NAME	TYPE
	PA7	I/O	RCVR	INPUT (1)

(1) HARDWARE BUFFER FLOAT
(2) POSITIVE EDGE DETECT
(3) NEGATIVE EDGE DETECT
(4) RCVR S/R MODE = 1 WHEN SCCR6 • SCCR5 • SCCR4 = 1
(5) APPLIES TO EITHER R65F11 OR R65F12 PORT (SEE PIN DIAGRAM)
(6) FOR THE FOLLOWING MODE COMBINATIONS PA4 IS AVAILABLE AS AN INPUT ONLY PIN:
$\overline{SCCR7} \cdot \overline{SCCR6} \cdot SCCR5 \cdot \overline{MCR1} + \overline{SCCR7} \cdot SCCR6 \cdot \overline{SCCR4} \cdot MCR1 + SCCR7 \cdot \overline{SCCR6} \cdot \overline{SCCR5} + SCCR7 \cdot \overline{SCCR5} \cdot \overline{SCCR4}$

4.5 PORT C (PC)

Port C is preprogrammed as part of the Address/Data bus. PC0-PC7 function as A0-A3, A12, R/W, A13, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0100 and 3FFF. (See Memory Map, Appendix C). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port D. See Appendix F.3 for Port C timing.

4.6 PORT D (PD)

Port D is also preprogrammed as part of the Address/Data bus. Data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix C) for Multiplexed memory assignments. See Appendix F.3 for Port D timing.

4.7 PORT E (PE), PORT F (PF), PORT G (PG)

Ports E, F and G are available on the R65F12 only. Port E can only be used as outputs. Port F and Port G can be used for inputs or outputs and are similar to Port A and Port B in operation.

Table 4-4. Port C Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode MCR7 = 1 MCR6 = 1 Signal Name	Signal Type (1)
PC0	A0	OUTPUT
PC1	A1	OUTPUT
PC2	A2	OUTPUT
PC3	A3	OUTPUT
PC4	A12	OUTPUT
PC5	R/W	OUTPUT
PC6	A13	OUTPUT
PC7	EMS	OUTPUT

Table 4-5. Port D Control and Usage

R65F11/ R65F12 Port	Multiplexed Mode MCR7 = 1 MCR6 = 1 MCR5 = 1 Signal Phase 1 Name	Signal Phase 1 Type (2)	Signal Phase 2 Name	Signal Phase 2 Type (3)
PD0	A4	OUTPUT	DATA0	I/O
PD1	A5	OUTPUT	DATA1	I/O
PD2	A6	OUTPUT	DATA2	I/O
PD3	A7	OUTPUT	DATA3	I/O
PD4	A8	OUTPUT	DATA4	I/O
PD5	A9	OUTPUT	DATA5	I/O
PD6	A10	OUTPUT	DATA6	I/O
PD7	A11	OUTPUT	DATA7	I/O

(1) Active Buffer Pull-up and Pull-Down
(2) Tri-State Buffer is in Active Mode
(3) Tri-State Buffer is in Active Mode only during the Phase 2 Portion of a Write Cycle

SECTION 5
SERIAL INPUT/OUTPUT CHANNEL

The R65F11 and R65F12 Microcomputers provide a full duplex Serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (@ Ø2 = 1 MHZ). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.

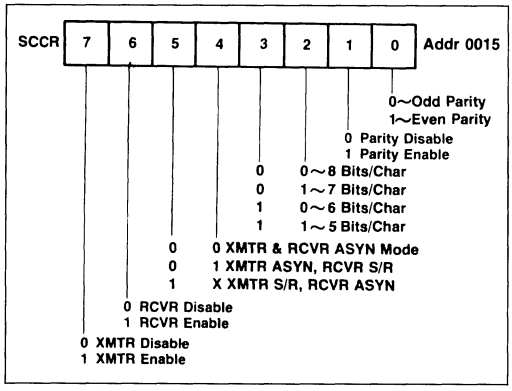


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Communications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one or two stop bits, and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown below. When parity is disabled, the 5, 6, 7 or 8 bits of data are terminated with two stop bits.

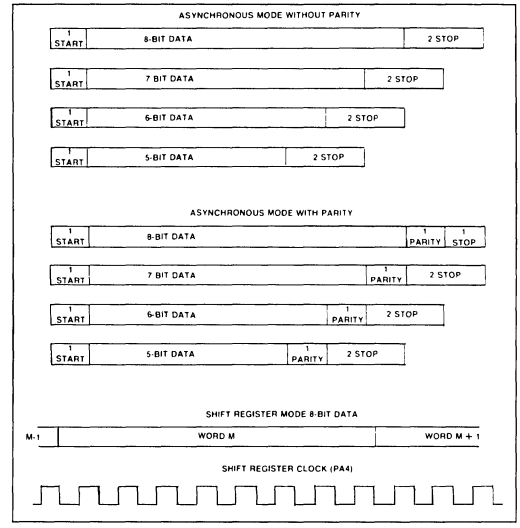


Figure 5-2. Bit Allocations

In the S/R mode, eight data bits are always shifted out. Bits/character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCCR5, SCCR6 and SCCR7.

$$IFR7 = SCSR6\ (\overline{SCCR5} + SCCR7)$$

5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1." In the ASYN mode, data format must have a start bit, appropriate number of data bits, a parity bit (if enabled) and one stop bit. Refer to Figure 5-2 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and a strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for ASYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits, and any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.

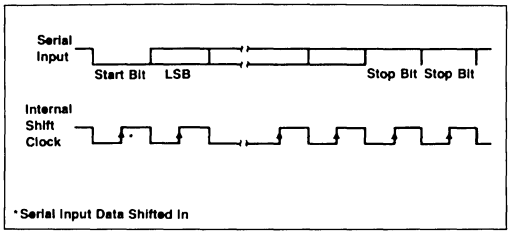


Figure 5-3. ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.

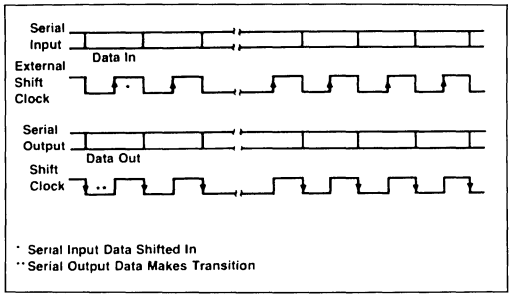


Figure 5-4. S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

5.3 SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full*—Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$ and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition, however, a corresponding error bit will be set to a logic 1 instead.

SCSR 1: *Over-Run Error*—Set to a logic 1 when a new character is transferred from the Receiver Shift Register, with the last character still in the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by $\overline{RES}$.

SCSR 2: *Parity Error*—Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by $\overline{RES}$.

SCSR 3: *Framing Error*—Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by $\overline{RES}$. (ASYN Mode only).

SCSR 4: *Wake-Up*—Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by $\overline{RES}$ or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission*—Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by $\overline{RES}$ or upon writing a new data word into the Transmitter Data Register. When the End-of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty*—Set to a logic 1 when the contents of the Transmitter Data Register is transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by $\overline{RES}$.

SCSR 7: *Transmitter Under-Run*—Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register, or by $\overline{RES}$.

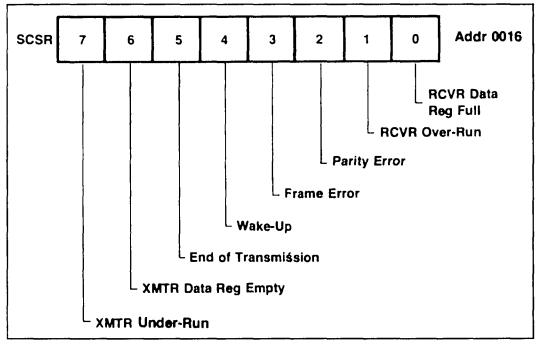


Figure 5-5. SCSR Bit Allocations

5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full Flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of ten consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.

SECTION 6
COUNTER/TIMERS

The R65F11 and R65F12 Microcomputers contain two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

Counter A	Counter B
• Pulse width measurement	• Retriggerable Interval Counter
• Pulse Generation	• Asymmetrical Pulse Generation
• Interval Timer	• Interval Timer
• Event Counter	• Event Counter

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4.2).

6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either Ø2 clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the Lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter A Underflow Flag (IFR 4) will be set to "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

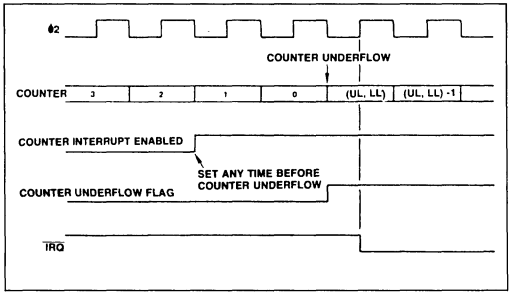


Figure 6-1. Interval Timer Timing Diagram

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register. See Table 6-1.

Table 6-1. Counter A Control Bits

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are Ø2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:-

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the Ø2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65 535 ms at the 1 MHz Ø2 clock rate or 0.5 μs to 32.767 ms at the 2 MHz Ø2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs, or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode the CA is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

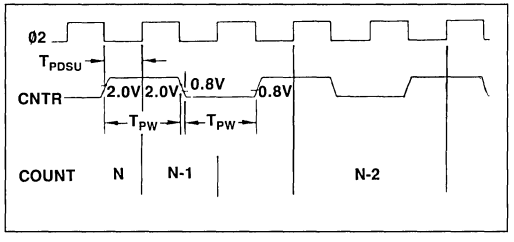


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the ϕ2 clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6-3.

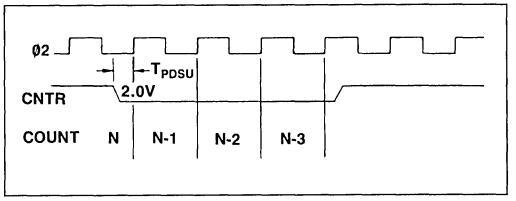


Figure 6-3. Pulse Width Measurement

6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-2 identifies the values to be loaded in Counter A for selecting standard data rates with a ϕ2 clock rate of 1 MHz and 2 MHz. Although Table 6-2 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi 2}{16 \times bps} - 1$$

where

N = decimal value to be loaded into Counter A using its hexadecimal equivalent.
ϕ2 = the clock frequency (1 MHz or 2 MHz)
bps = the desired data rate.

NOTE

In Table 6-2 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-2 for those baud rates which fall outside this limit.

Table 6-2. Counter A Values for Baud Rate Selection

Standard Baud Rate	Hexadecimal Value		Actual Baud Rate At		Clock Rate Needed To Get Standard Baud Rate	
	1 MHz	2 MHz	1 MHz	2 MHz	1 MHz	2 MHz
50	04E1	09C3	50.00	50.00	1.0000	2.0000
75	0340	0682	75.03	74.99	1.0000	2.0000
110	0237	046F	110.04	110.04	1.0000	2.0000
150	01A0	0340	149.88	150.06	1.0000	2.0000
300	00CF	01A0	300.48	299.76	1.0000	2.0000
600	0067	00CF	600.96	600.96	1.0000	2.0000
1200	0033	0067	1201.92	1201.92	1.0000	2.0000
2400	0019	0033	2403.85	2403.85	1.0000	2.0000
3600	0010	0021	3676.47	3676.47	0.9792	1.9584
4800	000C	0019	4807.69	4807.69	1.0000	2.0000
7200	0008	0010	6944.44	7352.94	1.0368	1.9584
9600	0006	000C	8928.57	9615.38	1.0752	2.0000

6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either Ø2 clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D for the Upper Counter B and at location 001E or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address: 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by $\overline{RES}$.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation Mode.

6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.

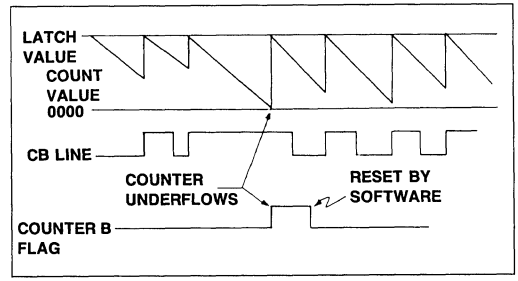


Figure 6-4. Counter B. Retriggerable Interval Timer Mode

6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value which corresponds to the desired pulse width (referred to as P in the following descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C, and the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.
2. The lower 8 bits of D are loaded into LLB by writing to address 001C, and the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the contents of the 16-bit Latch B to be downloaded into the Counter B and causes the CB output to go low as shown in Figure 6-5.
3. When the Counter B underflow occurs the contents of the Latch C is loaded into the Counter B, and the CB output toggles to a high level and stays high until another underflow occurs. Latch B is then down-loaded and the CB output toggles to a low level repeating the whole process.

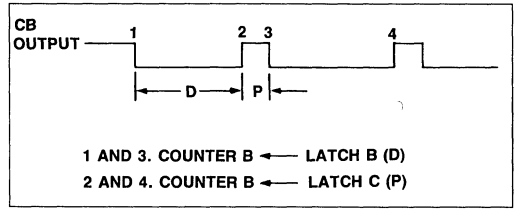


Figure 6-5. Counter B Pulse Generation

SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER-ON-RESET

The occurrence of $\overline{RES}$ going from low to high will cause the R65F11 or R65F12 to reset and enter the RSC-FORTH Operating System. As was described in Section 3.8, upon reset certain system variables will be initialized. See Appendix C.4 for a list of these variables names, locations and contents. The external memory map will be searched for an auto start ROM.

A bit pattern of A55A at a 1K byte page boundary indicates that an auto start program follows. The next two bytes are assumed to be a pointer to the high level RSC-FORTH word that is the entry point to that program. Auto start programs is written in assembly language, rather than RSC-FORTH, a series of indirect pointers as shown in 3-7 can be used to initiate program execution.

7.2 POWER ON TIMING

After application of V_{CC} and V_{RR} power to the R65F11 or R65F12, $\overline{RES}$ must be held low for at least eight $\phi 2$ clock cycles after V_{CC} reaches operating range and the internal oscillator has stabilized. This stabilization time is dependent upon the input V_{CC} voltage and performance of the internal oscillator. The clock can be monitored at $\phi 2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.

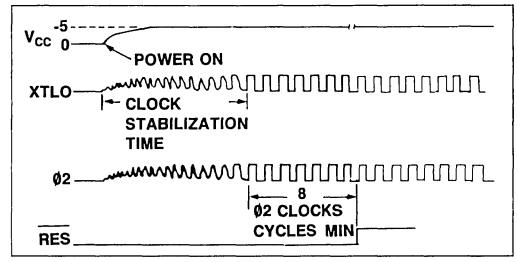


Figure 7-1. Power Turn-On Timing Detail

7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high the R65F11 or R65F12 is put in a reset state. The registers and I/O ports are configured as shown in Table 7-1 when the external ROM is autostarted.

Table 7-1. RES Initialization of I/O Ports and Registers

	7	6	5	4	3	2	1	0
REGISTERS								
Mode Control (MCR)	1	1	1	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	0	0	0	0	0
Ser. Com. Control (SCCR)	1	1	0	0	0	1	0	0
Ser. Com. Status (SCSR)	0	1	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1

APPENDIX A
R65F11 AND R65F12 INSTRUCTION SET

This appendix contains a summary of the R6500 instruction set. For detailed information, consult the R6500 Microcomputer System Programming Manual, Document 29650 N30. The four instructions notated with a * are added instructions for the R65F11 and R65F12 which are not part of the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

Mnemonic	Instruction	Mnemonic	Instruction
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator		
BMI	Branch on Result Minus	PHA	Push Accumulator on Stack
BNE	Branch on Result not Zero	PHP	Push Processor Status on Stack
BPL	Branch on Result Plus	PLA	Pull Accumulator from Stack
BRK	Force Break	PLP	Pull Processor Status from Stack
BVC	Branch on Overflow Clear		
BVS	Branch on Overflow Set	*RMB	Reset Memory Bit
		ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit		
CLV	Clear Overflow Flag	RTI	Return from Interrupt
CMP	Compare Memory and Accumulator	RTS	Return from Subroutine
CPX	Compare Memory and Index X		
CPY	Compare Memory and Index Y	SBC	Subtract Memory from Accumulator with Borrow
DEC	Decrement Memory by One	SEC	Set Carry Flag
DEX	Decrement Index X by One	SED	Set Decimal Mode
DEY	Decrement Index Y by One	SEI	Set Interrupt Disable Status
		*SMB	Set Memory Bit
EOR	"Exclusive-Or" Memory with Accumulator	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
		STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One	TAX	Transfer Accumulator to Index X
INY	Increment Index Y by One	TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R65F11 AND R65F12 INSTRUCTION SET SUMMARY TABLE

R65F11 AND R65F12 ADDRESS MODES

MNEMONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM. OP	n	#	IMPLIED OP	n	#
ADC	A · M · C→A (4)(1)	69	2	2	6D	4	3	65	3	2						
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2						
ASL	C← [7 0] ←0				0E	6	3	06	5	2	0A	2	1			
BBR[#(0-7)]	Branch on M_b = 0 (5)(2)															
BBS[#(0-7)]	Branch on M_b = 1 (5)(2)															
BCC	Branch on C = 0 (2)															
BCS	Branch on C = 1 (2)															
BEQ	Branch on Z = 1 (2)															
BIT	A ∧ M				2C	4	3	24	3	2						
BMI	Branch on N = 1 (2)															
BNE	Branch on Z = 0 (2)															
BPL	Branch on N = 0 (2)															
BRK	Break													00	7	1
BVC	Branch on V = 0 (2)															
BVS	Branch on V = 1 (2)															
CLC	0→C													18	2	1
CLD	0→D													D8	2	1
CLI	0→I													58	2	1
CLV	0→V													B8	2	1
CMP	A M (1)	C9	2	2	CD	4	3	C5	3	2						
CPX	X M	E0	2	2	EC	4	3	E4	3	2						
CPY	Y M	C0	2	2	CC	4	3	C4	3	2						
DEC	M 1→M				CE	6	3	C6	5	2						
DEX	X 1→X													CA	2	1
DEY	Y 1→Y													88	2	1
EOR	A⊻M→A (1)	49	2	2	4D	4	3	45	3	2						
INC	M · 1→M				EE	6	3	E6								
INX	X · 1→X													E8	2	1
INY	Y · 1→Y													C8	2	1
JMP	Jump to New Loc				4C	3	3									
JSR	Jump Sub				20	6	3									
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2						
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2						
LDY	M→Y (1)	A0	2	2	AC	4	3	A4	3	2						
LSR	0→ [7 0] →C				4E	6	3	46	5	2	4A	2	1			
NOP	No Operation													EA	2	1
ORA	AVM→A (1)	09	2	2	0D	4	3	05	3	2						
PHA	A→Ms S 1→S													48	3	1
PHP	P→Ms S 1→S													08	3	1
PLA	S · 1→S Ms→A													68	4	1
PLP	S · 1→S Ms→P													28	4	1
RMB[#(0-7)]	0→M_b (5)															
ROL	←[7 0]←[C]←				2E	6	3	26	5	2	2A	2	1			
ROR	→[C]→[7 0]→				6E	6	3	66	5	2	6A	2	1			
RTI	Rtrn Int													40	6	1
RTS	Rtrn Sub													60	6	1
SBC	A M C→A (1) (4)	E9	2	[illegible]	ED	4	3	E5	3	2						
SEC	1→C													38	2	1
SED	1→D													F8	2	1
SEI	1→T													78	2	1
SMB[#(0-7)]	1→M_b (5)															
STA	A→M				8D	4	3	85	3	2						
STX	X→M				8E	4	3	86	3	2						
STY	Y→M				8C	4	3	84	3	2						
TAX	A→X													AA	2	1
TAY	A→Y													A8	2	1
TSX	S→X													BA	2	1
TXA	X→A													8A	2	1
TXS	X→S													9A	2	1
TYA	Y→A													98	2	1

MNEMONIC	(IND, X) OP	n	#	(IND), Y OP	n	#	Z. PAGE, X OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#	RELATIVE OP	n	#	INDIRECT OP	n	#	Z. PAGE, Y OP	n	#
ADC	61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3									
AND	21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3									
ASL							16	6	2	1E	7	3												
BBR[#(0-7)]																								
BBS[#(0-7)]																								
BCC																90	2	2						
BCS																B0	2	2						
BEQ																F0	2	2						
BIT																								
BMI																30	2	2						
BNE																D0	2	2						
BPL																10	2	2						
BRK																								
BVC																50	2	2						
BVS																70	2	2						
CLC																								
CLD																								
CLI																								
CLV																								
CMP	C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3									
CPX																								
CPY																								
DEC							D6	6	2	DE	7	3												
DEX																								
DEY																								
EOR	41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3									
INC							F6	6	2	FE	7	3												
INX																								
INY																								
JMP																			6C	5	3			
JSR																								
LDA	A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3									
LDX													BE	4	3							B6	4	2
LDY							B4	4	2	BC	4	3												
LSR							56	6	2	5E	7	3												
NOP																								
ORA	01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3									
PHA																								
PHP																								
PLA																								
PLP																								
RMB[#(0-7)]																								
ROL							36	6	2	3E	7	3												
ROR							76	6	2	7E	7	3												
RTI																								
RTS																								
SBC	E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3									
SEC																								
SED																								
SEI																								
SMB[#(0-7)]																								
STA	81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3									
STX																						96	4	2
STY							94	4	2															
TAX																								
TAY																								
TSX																								
TXA																								
TXS																								
TYA																								

MNEMONIC	BIT ADDRESSING (OP BY BIT #) 0	1	2	3	4	5	6	7	PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0 / N V · B D I Z C
ADC									N V · · · · Z C
AND									N · · · · · Z ·
ASL									N · · · · · Z C
BBR[#(0-7)]	0F	1F	2F	3F	4F	5F	6F	7F	· · · · · · · ·
BBS[#(0-7)]	8F	9F	AF	BF	CF	DF	EF	FF	· · · · · · · ·
BCC									· · · · · · · ·
BCS									· · · · · · · ·
BEQ									· · · · · · · ·
BIT									M_7 M_6 · · · · Z ·
BMI									· · · · · · · ·
BNE									· · · · · · · ·
BPL									· · · · · · · ·
BRK									· · · 1 · 1 · ·
BVC									· · · · · · · ·
BVS									· · · · · · · ·
CLC									· · · · · · · 0
CLD									· · · · 0 · · ·
CLI									· · · · · 0 · ·
CLV									· 0 · · · · · ·
CMP									N · · · · · Z C
CPX									N · · · · · Z C
CPY									N · · · · · Z C
DEC									N · · · · · Z ·
DEX									N · · · · · Z ·
DEY									N · · · · · Z ·
EOR									N · · · · · Z ·
INC									N · · · · · Z ·
INX									N · · · · · Z ·
INY									N · · · · · Z ·
JMP									· · · · · · · ·
JSR									· · · · · · · ·
LDA									N · · · · · Z ·
LDX									N · · · · · Z ·
LDY									N · · · · · Z ·
LSR									0 · · · · · Z C
NOP									· · · · · · · ·
ORA									N · · · · · Z ·
PHA									· · · · · · · ·
PHP									· · · · · · · ·
PLA									N · · · · · Z ·
PLP									(Restored)
RMB[#(0-7)]	07	17	27	37	47	57	67	77	· · · · · · · ·
ROL									N · · · · · Z C
ROR									N · · · · · Z C
RTI									(Restored)
RTS									· · · · · · · ·
SBC									N V · · · · Z (3)
SEC									· · · · · · · 1
SED									· · · · 1 · · ·
SEI									· · · · · 1 · ·
SMB[#(0-7)]	87	97	A7	B7	C7	D7	E7	F7	· · · · · · · ·
STA									· · · · · · · ·
STX									· · · · · · · ·
STY									· · · · · · · ·
TAX									N · · · · · Z ·
TAY									N · · · · · Z ·
TSX									N · · · · · Z ·
TXA									N · · · · · Z ·
TXS									· · · · · · · ·
TYA									N · · · · · Z ·

NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result
5. Effects 8-bit data field of the specified zero page address

LEGEND

X = Index X
Y = Index Y
A = Accumulator
M = Memory per effective address
M_s = Memory per stack pointer
M_b = Selecter zero page memory bit
M_7 = Memory Bit 7
M_6 = Memory Bit 6
· = Add
− = Subtract
∧ = And
V = Or
⊻ = Exclusive Or
n = Number of cycles
# = Number of Bytes

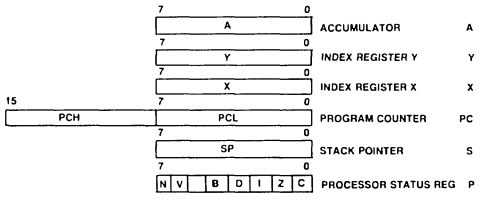
A.3 INSTRUCTION CODE MATRIX

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY. ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

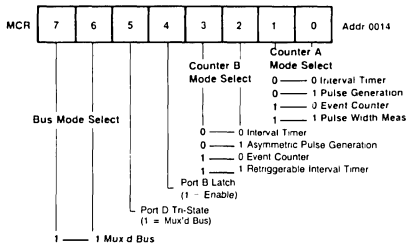
0	0
BRK Implied 1 7	—OP Code —Addressing Mode —Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

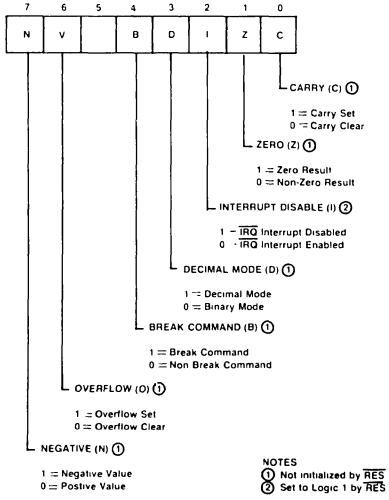
APPENDIX B
KEY REGISTER SUMMARY



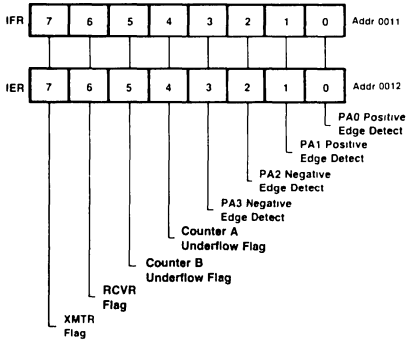
CPU Registers



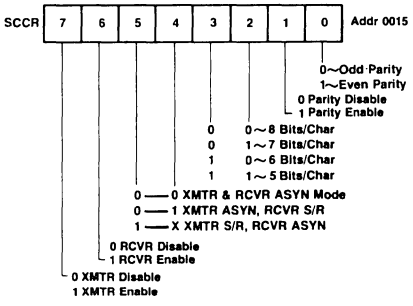
Mode Control Register



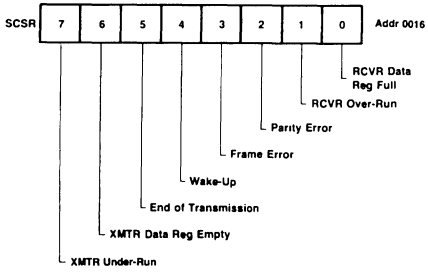
Processor Status Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

APPENDIX C
ADDRESS ASSIGNMENTS/MEMORY MAPS/PIN FUNCTIONS

C.1 I/O AND INTERNAL REGISTER ADDRESSES

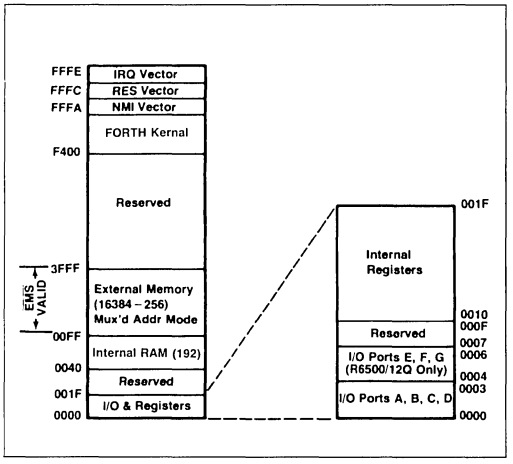
ADDRESS (HEX)	READ	WRITE
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B.
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Counter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G*	Port G*
05	Port F*	Port F*
04	Port E*	Port E*
03	— —	— —
02	— —	— —
01	Port B	Port B
0000	Port A	Port A

NOTE: *R65F12 Only

C.2 MULTIPLE FUNCTION PIN ASSIGNMENTS— PORT C AND PORT D

PIN NUMBER		I/O PORT FUNCTION	MULTIPLEXED PORT
R65F11	R65F12	REPLACED	FUNCTION
4	25	PC0	A0
5	26	PC1	A1
6	27	PC2	A2
7	28	PC3	A3
8	29	PC4	A12
9	30	PC5	R/W
10	31	PC6	A13
11	32	PC7	EMS
19	40	PD0	A4/D0
18	39	PD1	A5/D1
17	38	PD2	A6/D2
16	37	PD3	A7/D3
15	36	PD4	A8/D4
14	35	PD5	A9/D5
13	34	PD6	A10/D6
12	33	PD7	A11/D7

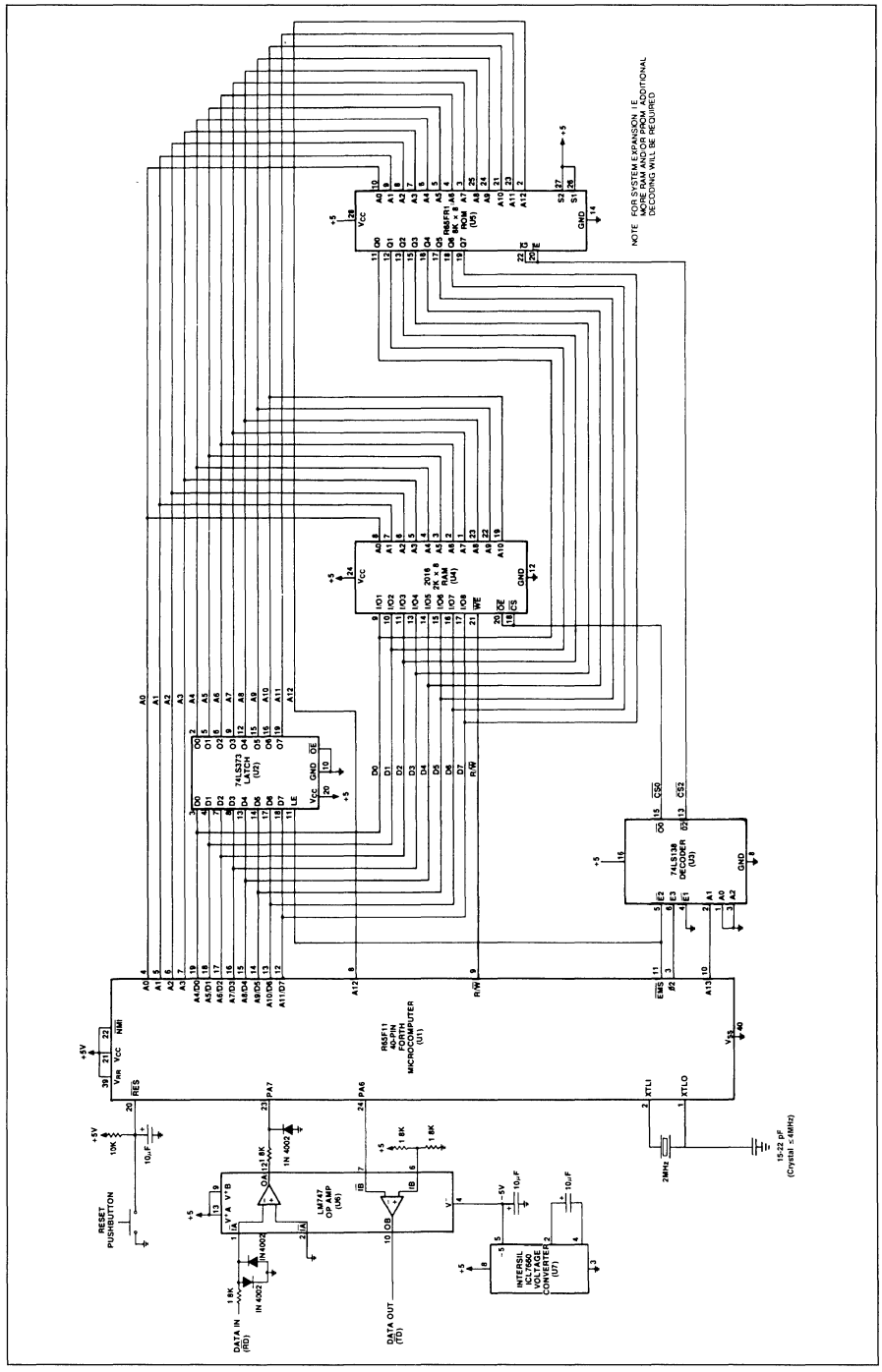
C.3 MULTIPLEXED MODE MEMORY MAP



C.4 SYSTEM VARIABLES IN RAM

ADDRESS	NAME	COLD START VALUE	WARM START VALUE
0040	IRQVEC	(COLD)	—
0042	NMIVEC	(COLD)	—
0044	UKEY	(INK)	(INK)
0046	UEMIT	(OUT)	(OUT)
0048	UP	0300	0300
004A	INTFLG	00	00
004B	(W-1)	6C	6C
004C	W	—	—
004E	IP	—	—
0050	(N-1)	—	—
0051	N	—	—
0059	XSAVE	—	—
005B	INTVEC	(COLD)	—
005D	TOS	—	—
0300	TIB	0380	0380
0302	R0	00FF	00FF
0304	S0	00C2	00C2
0306	UC/L	0050	—
0308	UPAD	037E	—
030A	UR/W	(DISK)	—
030C	BASE	0010	—
030E	CLD/WRM	—	—
0310	IN	—	—
0312	DPL	—	—
0314	HLD	—	—
0316	DISKNO	—	—
0318	CURCYL	—	—
031C	B/SIDE	—	—

APPENDIX D
TYPICAL MINIMUM HOOKUP



APPENDIX E
ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} & V_{RR}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{RR} = V_{CC}; V_{SS} = 0V; T_A = 0° to 70°, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0		V_{CC}	V	
RAM Standby Current (Retention Mode)	I_{RR}	—	4	—	mA	T_A = 25°C
Input High Voltage All Except XTLI XTLI	V_{IH}	 +2.0 +4.0	 — —	 V_{CC} V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current PA, PB, PC, PD, PF[3], PG[3]	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage (Except XTLO)	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA
I/O Port Pull-Up Resistance PA0–PA7, PB0–PB7, PC0–PC7, PF0–PF7[3], PG0–PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output Leakage Current (Three-State Off)	I_{OUT}	—	—	±10	μA	
Darlington Current Drive PE[3]	I_{OH}	−1.0	—	—	mA	V_{OUT} = 1.5V
Input Capacitance XTLI, XTLO All Others	C_{IN}	 — —	 — —	 50 10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—		1000	mW	T_A = 25°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R65F12 only.

APPENDIX F
TIMING REQUIREMENTS AND CHARACTERISTICS

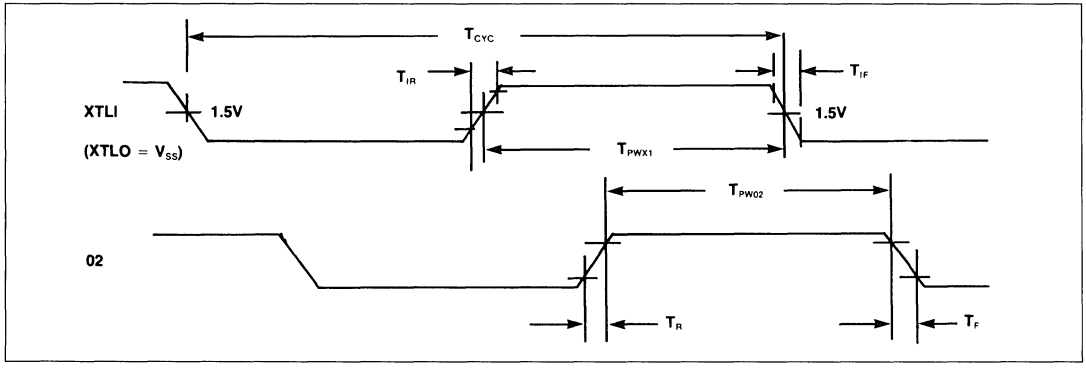
F.1 GENERAL NOTES

1. V_{CC} = 5V ± 5%, 0°C ≤ TA ≤ 70°C
2. A valid V_{CC} – RES sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

   PA, PB, PE, PF, PG — 50pf maximum

F.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
T_{PWX1}	XTLI Input Clock Pulse Width XTLO = VSS	500 ± 25	—	250 ± 10	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	T_{PWX1}	T_{PWX1} ± 25	T_{PWX1}	T_{PWX1} ± 20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



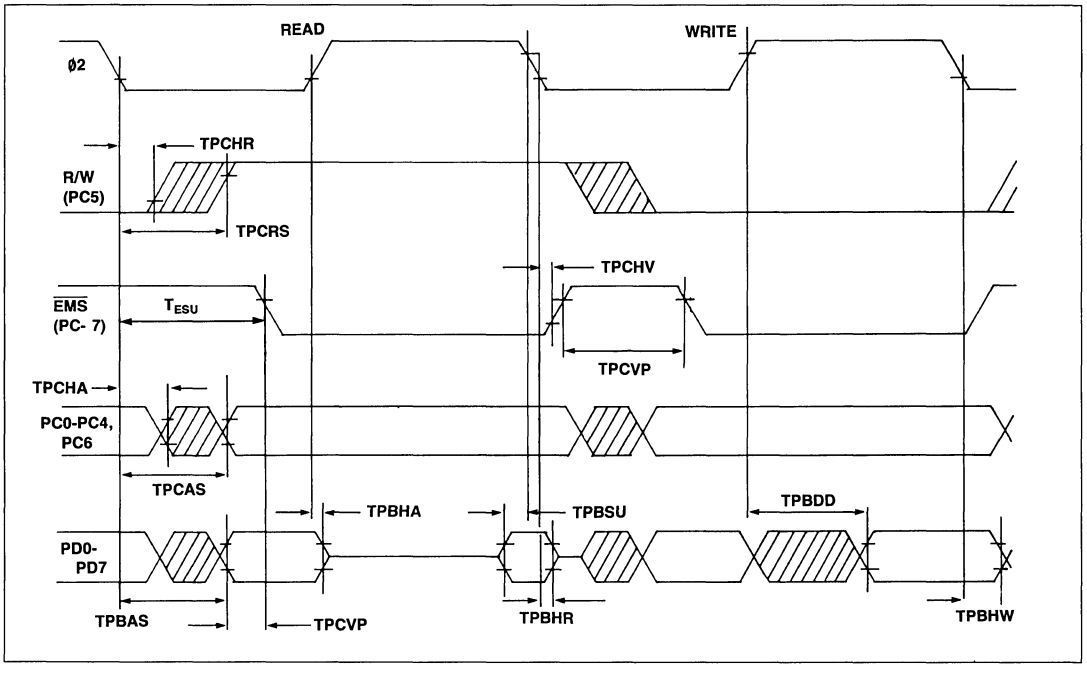
F.3 MULTIPLEXED MODE TIMING—PC AND PD

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC4, PC6) Address Setup Time	—	225	—	140
T_{PBAS}	(PD) Address Setup Time	—	225	—	140
T_{PBSU}	(PD) Data Setup Time	50	—	35	—
T_{PBHR}	(PD) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PD) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PD) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC4, PC6) Address Hold Time	30	—	30	—
T_{PBHA}	(PD) Address Hold Time	10	100	10	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC7) EMS Hold Time	10	—	10	—
T_{PCVD} (1)	(PC7) Address to EMS Delay Time	30	—	30	—
T_{PCVP}	(PC7) EMS Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Set Up Time	—	350	—	210

NOTE 1: Values assume PC0-PC4, PC6 and PC7 have the same capacitive load.

F.3.1 Multiplex Mode Timing Diagram

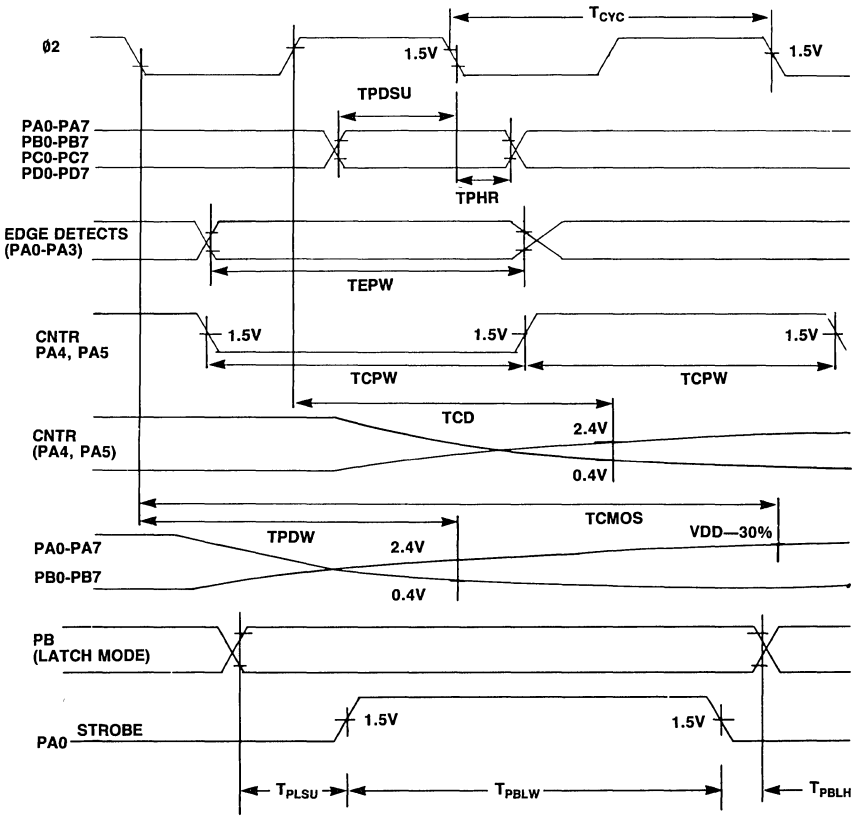


F.4 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}[1]	PA, PB TTL	—	500	—	500
T_{CMOS}[1]	PA, PB CMOS	—	1000	—	1000
	Peripheral Data Setup Time				
T_{PDSU}	PA, PB	200	—	200	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PB	75	—	75	—
T_{EPW}	PA0-PA3 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counters A and B				
T_{CPW}	PA4, PA5 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}[1]	PA4, PA5 Output Delay	—	500	—	500
	Port B Latch Mode				
T_{PBLW}	PA0 Strobe Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{PLSU}	PB Data Setup Time	175	—	150	—
T_{PBLH}	PB Data Hold Time	30	—	30	—
	Serial I/O				
T_{PDW}[1]	PA6 XMTR TTL	—	500	—	500
T_{CMOS}[1]	PA6 XMTR CMOS	—	1000	—	1000
T_{CPW}	PA4 RCVR S/R Clock Width	4 T_{CYC}	—	4 T_{CYC}	—
T_{PDW}[1]	PA4 XMTR Clock—S/R Mode (TTL)	—	500	—	500
T_{CMOS}[1]	PA4 XMTR Clock—S/R Mode (CMOS)	—	1000	—	1000

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required.

F.4.1 I/O Edge Detect, Counter, and Serial I/O Timing



APPENDIX G
INCLUDED FORTH FUNCTIONS IN ROM

BANKEXECUTE	BANKEEC!	BANKC@	BANKC!
EEC!	•	.R	D.
?	#S	#	SIGN
D.R	<#	SPACES	SEEK
#>	DWRITE	DREAD	SELECT
INIT	M/MOD	*/	*/MOD
DISK	/	/MOD	*
MOD	M*	MAX	MIN
M/	ABS	D+-	+-
DABS	COLD	(NUMBER)	HOLD
S->D	ERASE	FILL	QUERY
BLANKS	(.")	-TRAILING	TYPE
EXPECT	DECIMAL	HEX	-DUP
COUNT	PICK	ROT	>
SPACE	U<	=	-
<	1-	2+	1+
2-	C/L	HLD	DPL
PAD	CLD/WRM	BASE	UR/W
IN	UC/L	R0	S0
UPAD	BL	4	3
TIB	1	0	C!
2	C@	@	TOGGLE
!	BOUNDS	2DUP	DUP
+!	2DROP	DROP	OVER
SWAP	NEGATE	D+	+
DNEGATE	0=	R	R>
0<	LEAVE	;S	RP@
>R	SP!	SP@	XOR
RP!	AND	U/	U*
OR	CR	?TERMINAL	KEY
CMOVE	ENCLOSE	(FIND)	DIGIT
EMIT	(+LOOP)	(LOOP)	0BRANCH
(DO)	EXECUTE	CLIT	LIT
BRANCH			