Rockwell

R68560, R68561 Multi-Protocol Communications Controller (MPCC)

DESCRIPTION

The R68560, R68561 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 68008/68000 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, two channel DMA interface and three separate interrupt vector numbers optimize MPCC performance to take full advantage of the 68008/68000 processing capabilities and asynchronous bus structure.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 22 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC68440/MC68450 DMA Controllers. Three prioritized interrupt vector numbers separately support receiver, transmitter and modem interface operation.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

The 48-pin R68561 supports word-length (16-bit) operation when connected to the 68000 16-bit asynchronous bus, as well as byte-length (8-bit) operation when connected to the 68008 8-bit bus. The 40-pin R68560 supports byte-length operation on the 68008 bus.

FEATURES

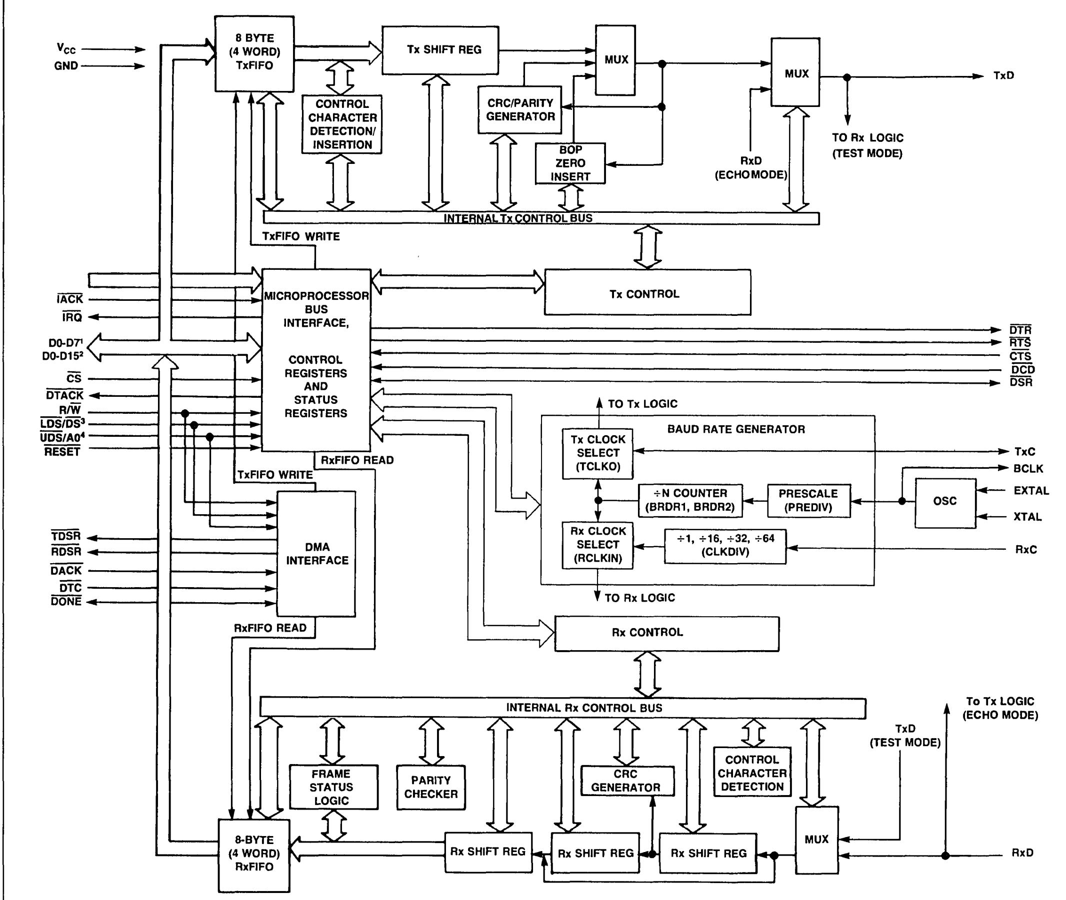
- Full duplex synchronous/asynchronous receiver and transmitter
- Implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, X3.28k, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit oriented protocols (BOP), such as SDLC, HDLC, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and baud rate generator with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 68008/68000 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer; polled, interrupt and two-channel DMA transfer compatible with MC68440/MC68450
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R6856 _ _	4 MHz	0°C to 70°C

Package: C = Ceramic
P = Plastic

Number of pins: 0 = 40
1 = 48



NOTES:
1. R68560 ONLY.
2. R68561 ONLY.
3. UDS ON R68561 A0 ON R68560
4. LDS ON R68561 DS ON R68560

Figure 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the document, signals are presented using the terms active and inactive or asserted and negated independently of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. For example, R/W̄ indicates write is active low and read is active high.

Note: The R68561 interface is described for word mode operation only and the R68560 interface is described for byte mode operation only.

A1–A4—Address Lines. A1–A4 are active high inputs used in conjunction with the CS̄ input to access the internal registers. The address map for these registers is shown in Table 1.

D0–D15—Data Lines. The bidirectional data lines transfer data between the MPCC and the MPU, memory or other peripheral device. D0–D15 are used when connected to the 16-bit 68000 bus and operating in the MPCC word mode. D0–D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the MPCC byte mode. The data bus is three-stated when CS̄ is inactive. (See exceptions in DMA mode.)

CS—Chip Select. CS low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the CS input is inactive in non-DMA mode. CS must be decoded from the address bus and gated with address strobe (AS).

R/W—Read/Write. R/W controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

DTACK—Data Transfer Acknowledge. DTACK is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, DTACK is asserted by the MPCC after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. DTACK is driven high after assertion prior to being tri-stated. A holding resistor is required to maintain DTACK high between bus cycles.

DS—Data Strobe (R68560). During a write (R/W low), the DS positive transition latches data on data bus lines D0–D7 into the MPCC. During a read (R/W high), DS low enables data from the MPCC to data bus lines D0–D7.

LDS—Lower Data Strobe (R68561). During a write (R/W low), the positive transition latches data on the data bus lines D0–D7 (and on D8–D15 if UDS is low) into the MPCC. During a read (R/W high), LDS low enables data from the MPCC to D0–D7 (and to D8–D15 if UDS is low).

A0—Address Line A0 (R68560). When interfacing to an 8-bit data bus system such as the 68008, address line A0 is used to access an internal register. A0 = 0 defines an even register and A0 = 1 defines an odd register. See Table 1b.

UDS—Upper Data Strobe (R68561). When interfacing to a 16-bit data bus system such as the 68000, a low on control bus signal UDS enables access to the upper data byte on D8–D15. A high on UDS disables access to D8–D15. Data is latched and enabled in conjunction with LDS.

IRQ—Interrupt Request. The active low IRQ output requests interrupt service by the MPU. IRQ is driven high after assertion prior to being tri-stated.

IACK—Interrupt Acknowledge. The active low IACK input indicates that the current bus cycle is an interrupt acknowledge cycle. When IACK is asserted the MPCC places an interrupt vector on the lower byte (D0–D7) of the data bus.

TDSR—Transmitter Data Service Request. When Transmitter DMA mode is active, the low TDSR output requests DMA service.

RDSR—Receiver Data Service Request. When receiver DMA mode is active, the low RDSR output requests DMA service.

DACK—DMA Acknowledge. The DACK low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

DTC—Data Transfer Complete. On a 68000 bus, the DTC low input indicates that a DMA data transfer was completed with no bus conflicts. DTC in response to a RDSR indicates that the data has been successfully stored in memory. DTC in response to a TDSR indicates that the data is present on the data bus for strobing into the MPCC. If not used, this input should be connected to ground.

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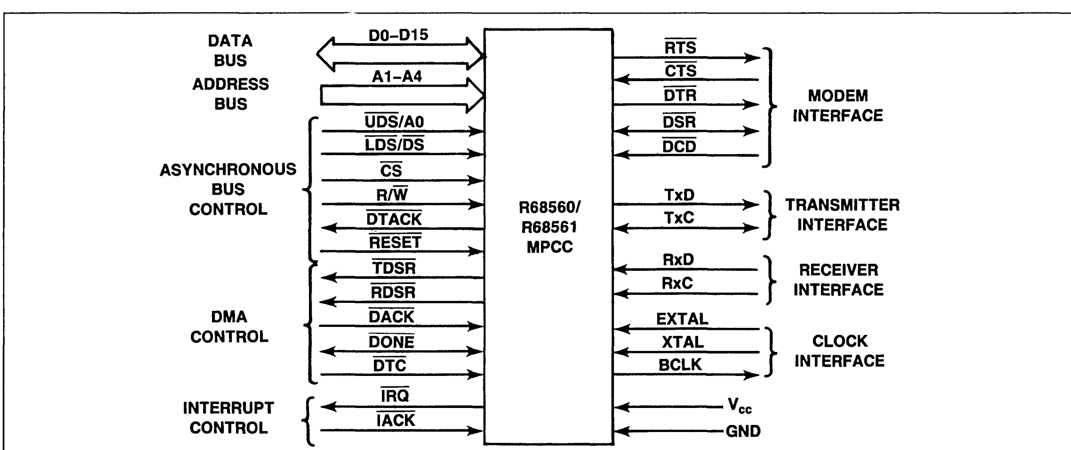


Figure 2. MPCC Input and Output Signals

DONE—Done. DONE is a bidirectional active low signal. The DONE signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or asserted by the MPCC when the status byte following the last character of a frame (block) is being transferred in response to a RDSR. The DONE signal asserted by the DMAC in response to a TDSR will be stored to track with the data byte (lower byte for word transfer) through the TxFIFO.

RESET—Reset. RESET is an active low, high impedance input that initializes all MPCC functions. RESET must be asserted for at least 500 ns to initialize the MPCC.

DTR—Data Terminal Ready. The DTR active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

RTS—Request to Send. The RTS active low output is general purpose in nature, and is controlled by the RTSLVL bit in the SICR.

CTS—Clear to Send. The CTS active low input positive transition and level are reported in the CTST and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

DSR—Data Set Ready. The DSR active low input negative transition and level are reported in the DSRT and DSRLVL bits in the SISR, respectively. DSR is also an output for RSYN.

DCD—Data Carrier Detect. The DCD active low input positive transition and level are reported in the DCDT and DCDLVL bits in the the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the negative going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator.

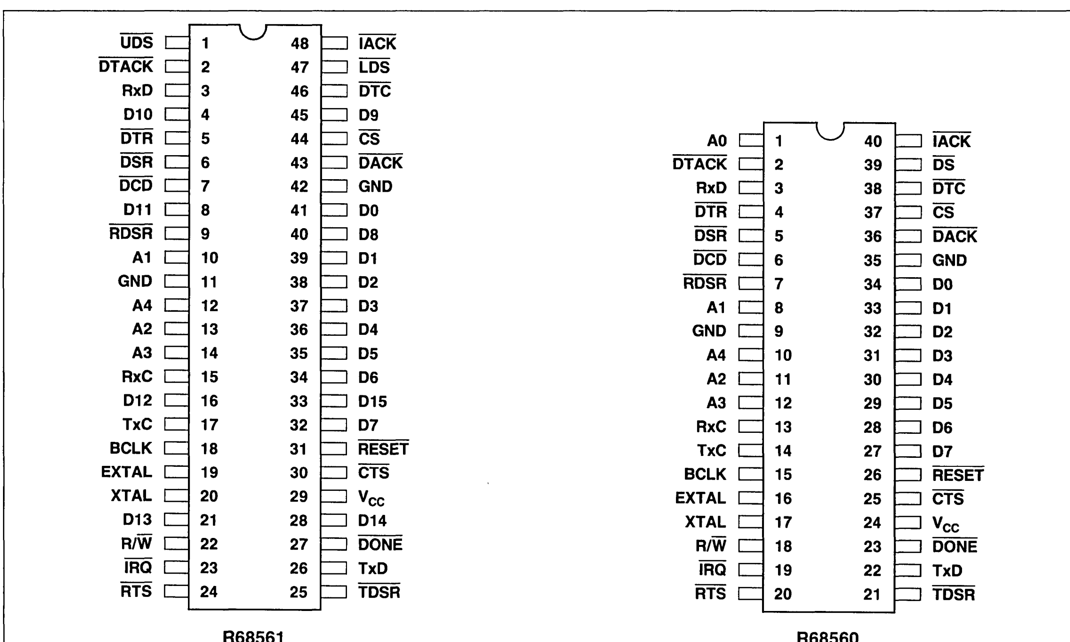
RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information.

EXTAL—Crystal/External Clock Input.
XTAL Crystal Return. EXTAL and XTAL connect a 20 kHz to 8.064 MHz parallel resonant external crystal to the MPCC internal oscillator (see CLOCK OSCILLATOR). The pin EXTAL may also be used as a TTL level input to supply DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

V_{CC}—Power. 5V ±5%.

GND—Ground. Ground (V_{SS}).



Pin Configuration

MPCC REGISTERS

Twenty-two registers control and monitor the MPCC operation. The registers and their addresses are identified in Table 1a (R68561 operation in word mode) and in Table 1b (R68560 operation in byte mode). When the R68561 is operated in the word mode, two registers are read or written at a time starting at an even boundary. When the R68560 is operated in the byte mode, each register is explicitly addressed based on A0.

Table 2 summarizes the MPCC register bit assignments and their access. A read from an unassigned location results in a read from a "null register." A null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.

Table 1a. R68561 Accessible Registers (Word Mode)

Register(s)		R/W	Addr (Hex.)	Address Lines A4	A3	A2	A1
15 —— (Odd Registers) —— 8	7 —— (Even Registers) —— 0						
Receiver Control Register (RCR)	Receiver Status Register (RSR)	R/W	00	0	0	0	0
Receiver Data Register (RDR)—16 bits[1]		R	02	0	0	0	1
Receiver Interrupt Enable Register (RIER)	Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0
Transmitter Control Register (TCR)	Transmitter Status Register (TSR)	R/W	08	0	1	0	0
Transmitter Data Register (TDR)—16 bits[2]		W	0A	0	1	0	1
Transmitter Interrupt Enable Register (TIER)	Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0
Serial Interface Control Register (SICR)	Serial Interface Status Register (SISR)	R/W	10	1	0	0	0
Reserved[3]	Reserved[3]	R/W	12	1	0	0	1
Serial Interrupt Enable Register (SIER)	Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0
Protocol Select Register 2 (PSR2)	Protocol Select Register (PSR1)	R/W	18	1	1	0	0
Address Register 2 (AR2)	Address Register 1 (AR1)	R/W	1A	1	1	0	1
Baud Rate Divider Register 2 (BRDR2)	Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0
Error Control Register (ECR)	Clock Control Register (CCR)	R/W	1E	1	1	1	1

Notes:
1. Accessible register of the four word RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first word.
2. Accessible register of the four word TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first word.
3. Reserved registers may contain random bit values.

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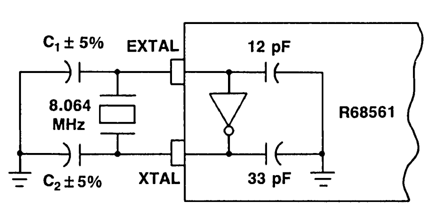
CLOCK OSCILLATOR

An on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in the figure below.



A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance (C_L), series resistance (R_s) and the crystal resonant frequency (F) must meet the following two relations:

$$C_1 = 2C_L - 12\ pF$$

$$C_2 = 2C_L - 33\ pF$$

$$R_s\ /\ R_{smax} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and C_L are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate R_{smax} based on F and C_L. The selected crystal must have a R_s less than the R_{smax}.

For example, if C_L = 20 pF for an 8.064 MHz parallel resonant crystal, then

C_1 = 40 − 12 = 28 pF (Use standard value of 27 pF.)

C_2 = 40 − 33 = 7 pF (Use standard value of 6.8 pF.)

Note: C_X = Total Shunt Capacitance including that due to board layout.

The series resistance of the crystal must be less than

$$R_{smax} = \frac{2 \times 10^6}{(8.064 \times 20)^2} = 77\ ohms$$

Table 1b. R68560 Accessible Registers (Byte Mode)

Register(s)	R/W	Addr (Hex.)	A4	A3	A2	A1	A0
7 … 0							
Receiver Status Register (RSR)	R/W	00	0	0	0	0	0
Receiver Control Register (RCR)	R/W	01	0	0	0	0	1
Receiver Data Register (RDR)—8 bits[1]	R	02	0	0	0	1	0
Reserved[3]		03	0	0	0	1	1
Receiver Interrupt Vector Number Register (RIVNR)	R/W	04	0	0	1	0	0
Receiver Interrupt Enable Register (RIER)	R/W	05	0	0	1	0	1
Transmitter Status Register (TSR)	R/W	08	0	1	0	0	0
Transmitter Control Register (TCR)	R/W	09	0	1	0	0	1
Transmitter Data Register (TDR)[2]—8 bits	W	0A	0	1	0	1	0
Reserved[3]		0B	0	1	0	1	1
Transmitter Interrupt Vector Number Register (TIVNR)	R/W	0C	0	1	1	0	0
Transmitter Interrupt Enable Register (TIER)	R/W	0D	0	1	1	0	1
Serial Interface Status Register (SISR)	R/W	10	1	0	0	0	0
Serial Interface Control Register (SICR)	R/W	11	1	0	0	0	1
Reserved[3]		12	1	0	0	1	0
Reserved[3]		13	1	0	0	1	1
Serial Interrupt Vector Number Register (SIVNR)	R/W	14	1	0	1	0	0
Serial Interrupt Enable Register (SIER)	R/W	15	1	0	1	0	1
Protocol Select Register 1 (PSR1)	R/W	18	1	1	0	0	0
Protocol Select Register 2 (PSR2)	R/W	19	1	1	0	0	1
Address Register 1 (AR1)	R/W	1A	1	1	0	1	0
Address Register 2 (AR2)	R/W	1B	1	1	0	1	1
Baud Rate Divider Register 1 (BRDR1)	R/W	1C	1	1	1	0	0
Baud Rate Divider Register 2 (BRDR2)	R/W	1D	1	1	1	0	1
Clock Control Register (CCR)	R/W	1E	1	1	1	1	0
Error Control Register (ECR)	R/W	1F	1	1	1	1	1

Notes:
1. Accessible register of the eight byte RxFIFO. The data is not initialized, however, $\overline{RES}$ resets the RxFIFO pointer to the start of the first byte.
2. Accessible register of the eight byte TxFIFO. The data is not initialized, however, $\overline{RES}$ resets the TxFIFO pointer to the start of the first byte.
3. Reserved registers may contain random bit values.

Table 2. MPCC Register Bit Assignments

R/W Access	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset[1] Value	Register
R/W	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
R/W	0	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABTEN	RRES	01	Receiver Control Register (RCR)
R	RECEIVER DATA (RxFIFO)[2]								— —	Receiver Data Register (RDR)
R/W	RECEIVER INTERRUPT VECTOR NUMBER (RIVN)								0F	Receiver Interrupt Vector Number Register (RIVNR)
R/W	RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0	00	Receiver Interrupt Enable Register (RIER)
R/W	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
R/W	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
W	TRANSMITTER DATA (TxFIFO)[2]								— —	Transmitter Data Register (TDR)
R/W	TRANSMITTER INTERRUPT VECTOR NUMBER (TIVN)								0F	Transmitter Interrupt Vector Number Register (TIVNR)
R/W	TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	0	00	Transmitter Interrupt Enable Register (TIER)
R/W	CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
R/W	RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0	00	Serial Interface Control Register (SICR)
	RANDOM BIT VALUES									(reserved)
	RANDOM BIT VALUES									(reserved)
R/W	SERIAL INTERRUPT VECTOR NUMBER (SIVN)								0F	Serial Interrupt Vector Number Register (SIVNR)
R/W	CTS IE	DSR IE	DCD IE	0	0	0	0	0	00	Serial Interrupt Enable Register (SIER)
R/W	0	0	0	0	0	0	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
R/W	WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
R/W	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
R/W	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
R/W	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
R/W	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
R/W	0	0	0	PSCDIV	TCLKO	RCLKIN	CLK DIV		00	Clock Control Register (CCR)
							CK2	CK1		
R/W	PAREN	ODDPAR	0	0	CFCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

Notes:
1. RESET = Register contents upon power up or $\overline{RESET}$.
2. 16-bits for R68561 (word mode); 8-bits for R68560 (byte mode).

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

Address = 00 Reset Value = $00

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by $\overline{\text{RESET}}$. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the next byte or word in the RxFIFO) must be read prior to resetting the corresponding status bit in the RSR. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR
7 RDA —Receiver Data Available. (RSR only).
0 The FxFIFO is empty (i.e., no received data is available).
1 RDA is set and an interrupt issued (if enabled) when the RxFIFO has 1 to 8 bytes, or 1 to 4 words, of data in it.

RDA Reset — RDA cannot be cleared or reset in software. It is initialized to 0 upon hardware reset and remains 0 if no data has been received. It is set to a 1 and an interrupt issued when a data byte/word is loaded to the RxFIFO with the negative edge of RxC coincident with the first bit of the next byte transmitted. It is automatically reset to 0 when the last byte/word is read from the RxFIFO by the host through RDR.

RSR
6 EOF —End of Frame. (BOP and BSC)
0 No end of frame has been detected.
1 The closing flag (BOP) or pad (BSC) has been detected. EOF is loaded in the RxFIFO along with the FSB with which it is associated. The EOF is loaded into the RSR and the interrupt issued, if enabled, (when the RxFIFO read pointer is positioned at the FSB) with the trailing edge of $\overline{\text{LDS}}$.

EOF Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the EOF bit. Then EOF may be reset by writing a 1 to RSR6.

RSR
5 RHW —Receive Half Word. (Frame Status only)*
0 The last word of the frame contains data on the upper half (D8–D15) and frame status on the lower half (D0–D7) of the data bus.
1 The lower half of the data bus (D0–D7) contains the frame status but the upper half (D8–D15) is blank or invalid.

*See Frame Status (RSR) on next page.

RSR
4 C/PERR —CRC/Parity Error.
0 No CRC or parity error detected.
1 CRC error detected (BOP, BSC) or parity error detected (ASYNC, ISOC and COP). The C/PERR bit is loaded into the RxFIFO with the negative-going RxC edge, along with the byte or word with which it is associated. For ASYNC, ISOCH or COP protocols, this is with the byte/word containing a parity error. For BOP or BSC, it is loaded to RxFIFO (after the CRC check) with the FSB. C/PERR is loaded into the RSR and the interrupt issued (when the read pointer is positioned at the FSB) with the trailing edge of $\overline{\text{LDS}}$.

C/PERR Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the C/PERR bit. Then it may be reset by writing a 1 to RSR4.

RSR
3 FRERR —Frame Error.
0 No frame error detected.
1 FRERR is set for receiver overrun, flag detected off boundary (BOP), or frame error (ASYNC, ISOCH). For receiver overrun, the FRERR bit is set in the RxFIFO with the last byte when the overrun is detected.

For BOP, a minimum message size is an opening flag, one address byte and one control byte. If the closing flag is detected before the control byte is sent, a short frame is indicated and a frame error results. For address extension, multi-address bytes may be received before the control byte is expected. The FRERR bit is latched in RxFIFO with the negative-going edge of RxC with the last address byte received upon detection of the flag off boundary. FRERR is loaded into the RSR and the interrupt issued when the read pointer is positioned at the FSB with the trailing edge of $\overline{\text{LDS}}$.

In ASYNC or ISOCH, a FRERR bit set indicates that the stop bit was detected off boundary (too early or too late for the number of bits expected by the setting of PSR2-3 and PSR2-4) or it was not the correct width (as expected by the setting of PSR2-6 and PSR2-5).

FRERR Reset — The byte/word containing the FSB must be read from the RxFIFO before resetting the C/PERR bit. The C/PERR bit may then be reset by writing a 1 to RSR3.

RSR
2 ROVRN —Receiver Overrun.
0 No receiver overrun detected.
1 Receiver overrun detected. Data is loaded into the RxFIFO on byte boundaries with the negative-going edge of RxC coincident with the first bit of the subsequent data being received. When the eighth byte, or fourth word, of data has been written into RxFIFO without any data being read out, the RxFIFO is full and the incremented write pointer "catches up" with the read pointer. The next attempt to write data to RxFIFO causes ROVRN bit to be loaded to the RSR and the interrupt issued (if enabled). The data in the RxFIFO is not affected, but new received data is lost.

ROVRN Reset — The ROVRN bit is not self-clearing when data is read from the RxFIFO, but may be reset by writing a 1 to RSR2.

RSR
1 RA/B —Receiver Abort/Break.
0 Normal Operation.
1 (BOP) When an ABORT (seven 1s) is detected after the opening flag, the RA/B bit is set in the RSR and an interrupt issued (if enabled). This bit is latched with the negative edge of RxC after the seventh 1 bit is detected. (NOTE: Because the previous byte can end in zero to five 1 bits, the abort could be recognized in the next byte as early as two to seven 1 bits.)

(BSC) When ENQ is detected in a block of text data, the RA/B bit is set in the RSR and the interrupt issued (if enabled) with the next negative edge of the RxC clock.

RA/B Reset — The RA/B bit is reset by writing a 1 to RSR1.

RSR
0 RIDLE —Receiver Idle. (BOP only).
0 Receiver is not idle.
1 15 or more 1s have been detected. The RIDLE bit is set in RSR with the negative edge of the next RxC after 15 consecutive 1s have been detected.

RIDLE Reset — The RIDLE is reset by writing a 1 to RSR0. (NOTE: The RIDLE bit will set again in 15 clock cycles if RxD is still in the idle condition.)

*Frame Status (RSR)

7	6	5	4	3	2	1	0
0	EOF	RHW	C/PERR	FRERR	ROVRN	RA/B	0

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the RxFIFO following the last data byte of each block. The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE. But, in addition to the RSR contents, the frame status byte has a RHW status in bit 5 which indicates either an even or odd boundary (applicable to word mode only).

If the MPCC is in word mode and the last data byte was on an even byte boundary (i.e., there was an even number of bytes in the message), a blank byte will be loaded into the RxFIFO prior to loading the frame status byte in order to force the "frame status" byte and the next frame to be on an even boundary. When RHW = 0, the last word of the frame contains data on the upper half and status on the lower half of the data bus. If RHW = 1, the lower half of the bus contains status but the upper half is a blank or invalid byte.

In the byte mode, the status byte will always immediately follow the last data byte of the block/frame (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the RxFIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
—	RDSREN	DONEEN	RSYNEN	STRSYN	0	RABEN	RRES

Address = 01 Reset value = $01

The Receiver Control Register (RCR) selects receiver control options.

RCR
7 —Not used.

RCR
6 RDSREN —Receiver Data Service Request Enable.
0 Disable receiver DMA mode.
1 Enable receiver DMA mode.

WORD MODE

ODD NUMBER OF BYTES (RHW = 0)

WORD	D15 DATA D8	D7 STATUS D0
N	DATA	STATUS
N + 1	NEXT	FRAME

EVEN NUMBER OF BYTES (RHW = 1)

WORD	D15 DATA D8	D7 STATUS D0
N	DATA	DATA
N + 1	BLANK	STATUS
N + 2	NEXT	FRAME

BYTE MODE

ODD NUMBER OF BYTES

BYTE	D7 D0
M	DATA
M + 1	STATUS
M + 2	NEXT FRAME

EVEN NUMBER OF BYTES

BYTE	D7 D0
M	DATA
M + 1	STATUS
M + 2	NEXT FRAME

Figure 3. BSC/BOP Block/Frame Status Location

RCR

5 DONEEN —DONE Output Enable.

0 Disable DONE output.

1 Enable DONE output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR

4 RSYNEN —RSYNEN Output Enable. Selects the DSR signal input or the RSYN SYNC signal output on the DSR pin.

0 Input DSR on DSR.

1 Output RSYN on DSR.

RCR

3 STRSYN —Strip SYN Character (COP only).

0 Do not strip SYN character.

1 Strip SYN character.

RCR

2 MUST BE ZERO

0

RCR

1 RABTEN —Receiver Abort Enable (BOP only).

0 Do not abort frame upon error detection.

1 Abort frame upon RxFIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame. (EOF is set upon abort).

RCR

0 RRES —Receiver Reset Command.

0 Enable normal receiver operation.

1 Reset receiver. Resets the receiver section including the RxFIFO and the RSR (but not the RCR). RRES is set by RESET or by writing a 1 into this bit and must be cleared by writing a 0 into this bit. RRES requires clearing after RESET.

Receiver Data Register (RDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1				LSB	MSB			Byte 0				LSB

Address = 02

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0				LSB

Address = 02

The receiver has an 8-byte (or 4-word) First In First Out (FIFO) register file (RxFIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the RxFIFO via the RDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. When the RxFIFO has a data byte/word ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Vector Number Register (RIVNR)

7	6	5	4	3	2	1	0
Receiver Interrupt Vector Number (RIVN)							

Address = 04 Reset value = $0F

If a receiver interrupt condition occurs (as reported by status bits in the RSR that correspond to interrupt enable bits in the RIER) and the corresponding bit is set in the RIER, IRQ output is asserted to request MPU receiver interrupt service. When the IACK input is asserted from the bus, the Receiver Interrupt Vector Number (RIVN) from the Receiver Interrupt Vector Number Register (RIVNR) is placed on the data bus.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	0	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	0

Address = 05 Reset value = $00

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the IRQ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER

7 RDA IE —Receiver Data Available Interrupt Enable.

0 Disable RDA Interrupt.

1 Enable RDA Interrupt.

RIER

6 EOF IE —End of Frame Interrupt Enable.

0 Disable EOF Interrupt.

1 Enable EOF Interrupt.

RIER

5 —Not used.

RIER

4 C/PERR IE —CRC/Parity Error Interrupt Enable.

0 Disable C/PERR Interrupt.

1 Enable C/PERR Interrupt.

RIER

3 FRERR IE —Frame Error Interrupt Enable.

0 Disable FRERR Interrupt.

1 Enable FRERR Interrupt.

RIER

2 ROVRN IE —Receiver Overrun Interrupt Enable.

0 Disable ROVRN Interrupt.

1 Enable ROVRN Interrupt.

RIER

1 RA/B IE —Receiver Abort/Break Interrupt Enable.

0 Disable RA/B Interrupt.

1 Enable RA/B Interrupt.

RIER

0 —Not used.

TRANSMITTER REGISTERS

Transmitter Status Register (TSR)

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

Address = 08 Reset value = $80

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by RESET. The IRQ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR
7 TDRA —Transmitter Data Register Available.

0 The TxFIFO is full.
1 The TxFIFO is available to be loaded via the TDR (1 to 8 bytes, or 1 to 4 words).

TDRA Reset — TDRA cannot be reset by the host in normal operation. It initializes to a 1 upon hardware or software reset of the MPCC. TDRA is not dependent on the serial clock.

TSR
6 TFC —Transmitted Frame Complete. (BOP, BSC and COP only).

0 (All) Frame not complete.
1 (BOP) Closing flag or ABORT has been transmitted. The TFC bit is set and the interrupt issued (if enabled) with the negative edge of TxC coincident with the end of the last bit of the flag. When TABT is set in TCR1, an ABORT is transmitted immediately but TFC is not issued until after the closing flag or 8 bits of the MARK idle condition after the TxFIFO is flushed of all current data bytes.

(BSC) Trailing pad has been transmitted. TFC bit set and/or interrupt issued with negative edge of TxC coincident with the end of the last bit of the trailing pad.

(COP) Last byte has been transmitted (TLAST set in TCR3). TFC bit set and/or interrupt issued with negative edge of the TxC coincident with the end of the last bit of the last byte.

TFC Reset — One full cycle of the serial clock (TxC) must elapse before the TFC bit can be reset by writing a 1 to TSR6.

TSR
5-3 —Not used.

TSR
2 TUNRN —Transmitter Underrun (BOP, BSC and COP only).

0 No TxFIFO underrun has occurred.
1 An empty TxFIFO was accessed for data.
(BOP) Underrun is treated as an ABORT in that eight consecutive 1s are transmitted followed by the idle condition of MARK or FLAG.

(BSC, COP) Underrun causes SYN characters to be transmitted until new data is available in the TxFIFO.

The TUNRN bit is set in TSR2 and the interrupt issued with the positive edge of the TxC coincident with the eighth bit of data prior to the ABORT in BOP or to SYN in BSC or COP.

TUNRN Reset — One full cycle of the serial clock (TxC) must elapse before the TUNRN bit can be reset by writing a 1 to TSR2.

TSR
1 TFERR —Transmit Frame Error (BOP only).

0 No frame error has occurred.
1 A short frame condition exists in that no control field is transmitted. (TLAST was issued early with an address byte.) TFERR bit is set and the interrupt issued with the positive edge of TxC coincident with the end of the last bit of the byte causing the error.

TFERR Reset — One full cycle of the serial clock (TxC) must elapse before TFERR bit can be reset by writing a 1 to TSR1.

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES

Address = 09 Reset value = $01

The Transmitter Control Register (TCR) selects transmitter control function.

TCR
7 TEN —Transmitter Enable.

0 Disable transmitter. TxD output is idled. The TxFIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR
6 TDSREN —Transmitter Data Service Request Enable.

0 Disable transmitter DMA mode.
1 Enable transmitter DMA mode.

TCR
5 TICS —Transmitter Idle Character Select. Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).

0 Mark Idle (TxD output is held high).
1 Content of AR2 (BSC and COP), BREAK condition (ASYNC and ISOC), or FLAG character (BOP).

TCR
4 THW —Transmit Half Word. (R68561, word mode only). This bit is used when the frame or block ends on an odd boundary in conjunction with the TLAST bit and indicates that the last word in the TxFIFO contains valid data in the upper byte only. This bit must always be 0 in byte mode (R68560).

0 Transmit full word (16 bits) from the TxFIFO.
1 Transmit upper byte (8 bits) from the TxFIFO.

4

TCR
3 **TLAST —Transmit Last Character** (BOP, BSC and COP only).
0 The next character is not the last character in a frame or block.
1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the TxFIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by DONE from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR
2 **TSYN —Transmit SYN** (BSC and COP only).
0 Do not transmit SYN characters.
1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR
1 **TABT —Transmit ABORT** (BOP only).
0 Enable normal transmitter operation.
1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the TxFIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the TxFIFO.

TCR
0 **TRES —Transmitter Reset Command.**
0 Enable normal transmitter operation.
1 Reset transmitter. Clears the transmitter section including the TxFIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by RESET or by writing a 1 into this bit and is cleared by writing a 0 into this bit. TRES requires clearing after RESET.

Transmit Data Register (TDR)

R68561 (Word Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB			Byte 1				LSB	MSB			Byte 0				LSB

Address = 0A

R68560 (Byte Mode)

7	6	5	4	3	2	1	0
MSB			Byte 0				LSB

Address = 0A

The transmitter has an 8-byte (or 4-word) FIFO register file (TxFIFO). Data to be transmitted is transferred from the bus into the TxFIFO via the TDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. The TDRA status bit in the TSR is set to 1 when the TxFIFO is ready to accept another data word/byte.

Transmitter Interrupt Vector Number Register (TIVNR)

7	6	5	4	3	2	1	0
Transmitter Interrupt Vector Number (TIVN)							

Address = 0C Reset value = $0F

If a transmitter interrupt condition occurs (as reported by status bits in the TSR that correspond to interrupt enable bits in the TIER) and the corresponding bit in the TIER is set, the IRQ output is asserted to request MPU transmitter interrupt service. When the IACK input is asserted from the bus, the Transmitter Interrupt Vector Number (TIVN) from the Transmitter Interrupt Vector Number Register (TIVNR) is placed on the data bus.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	0	0	0	TUNRN IE	TFERR IE	—

Address = 0D Reset value = $00

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the IRQ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER
7 **TDRA IE —Transmitter Data Register (TDR) Available Interrupt Enable.**
0 Disable TDRA Interrupt.
1 Enable TDRA Interrupt.

TIER
6 **TFC IE —Transmit Frame Complete (TFC) Interrupt Enable.**
0 Disable TFC Interrupt.
1 Enable TFC Interrupt.

TIER
5-3 **—Not used.**

TIER
2 **TUNRN IE —Transmitter Underrun (TUNRN) Interrupt Enable.**
0 Disable TUNRN Interrupt.
1 Enable TUNRN Interrupt.

TIER
1 **TFERR IE —Transmit Frame Error (TFERR) Interrupt Enable.**
0 Disable TFERR Interrupt.
1 Enable TFERR Interrupt.

TIER
0 **—Not used.**

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTST	DSRT	DCDT	CTSLVL	DSRLVL	DCDLVL	0	0

Address = 10 Reset value = $00

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTST, DSRT and DCDT) are cleared by writing a 1 into their respective positions, or by RESET. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The IRQ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR
7 CTST —Clear to Send Transition Status.
0 The input on CTS has not transitioned positive.
1 The input on CTS has transitioned positive from active to inactive. To detect this transition, RTS must be active (low) and the transmitter must be enabled (TRES in TCR0 = 0). The CTST bit is set in SISR7 and an interrupt issued (if enabled) with the negative edge of TxC.

CTST Reset — A negative transition of the serial clock (TxC) must occur after the CTS input goes high before the CTST bit can be reset by writing a 1 to SISR7.

SISR
6 DSRT —Data Set Ready Transition Status.
0 The input on DSR has not transitioned negative.
1 The input on DSR has transitioned negative from inactive to active. The DSRT bit is set in SISR7 and an interrupt issued (if enabled) with the negative edge of RxC. The receiver must be enabled (RRES in RCR0 = 0).

DSRT Reset — A negative transition of the serial clock (RxC) must occur after the DSR input goes high before the DSRT bit can be reset by writing a 1 to SISR6.

SISR
5 DCDT —Data Carrier Detect Transition Status.
0 The input on DCD has not transitioned positive.
1 The input on DCD has transitioned positive from active to inactive. The DCDT bit is set in SISR5 and an interrupt issued (if enabled) with the negative edge of RxC. The receiver must be enabled (RRES in RCR0 = 0).

DCDT Reset — A negative transition of the serial clock (RxC) must occur after the DCD input goes high before the DCDT bit can be reset by writing a 1 to SISR5.

SISR
4 CTSLVL —Clear to Send Level.
0 The input on CTS is negated (high, inactive).
1 The input on CTS is asserted (low, active).

CRSLVL Reset — The CTSLVL bit in SISR4 follows the state of the input to CTS and cannot be reset internally.

SISR
3 DSRLVL —Data Set Ready Level.
0 The input on DSR is negated (high, inactive).
1 The input on DSR is asserted (low, active).

DSRLVL Reset — The DSRLVL bit in SISR3 follows the state of the input to DSR and cannot be reset internally.

SISR
2 DCDLVL —Data Carrier Detect Level.
0 The input on DCD is negated (high, inactive).
1 The input on DCD is asserted (low, active).

DCDLVL Reset — The DCDLVL bit in SISR2 follows the state of the input to DCD and cannot be reset internally.

SISR
1-0 —Not used.

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	0	0	0	ECHO	TEST	0

Address = 11 Reset value = $00

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR
7 RTSLVL —Request to Send Level.
0 Negate RTS output (high).
1 Assert RTS output (low).

NOTE

In BOP, BSC, or COP, when the RTSLVL bit is cleared in the middle of data transmission, the RTS output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the RTS output is negated when the TxFIFO is empty. If the transmitter is idling when the RTSLVL bit is reset, the RTS output is negated within two bit times.

SICR
6 DTRLVL —Data Terminal Ready Level.
0 Negate DTR output (high).
1 Assert DTR output (low).

SICR
5-3 —Not used. These bits are initialized to 0 by RESET and must not be set to 1.

SICR
2 ECHO —Echo Mode Enable.
0 Disable Echo mode (enable normal operation).
1 Enable Echo mode. Received data (RxD) is routed back through the transmitter to TxD. The contents of the TxFIFO is undisturbed. This mode may be used for remote test purposes.

SICR
1 TEST —Self-test Enable.
0 Disable self-test (enable normal operation).
1 Enable self-test. The transmitted data (TxD) and clock (TxC) are routed back through to the receiver through RxD and RxC, respectively (DCD and CTS are ignored). This "loopback" self-test may be used for all protocols. RxC is external and CCR bits 2 and 3 must be a 1.

SICR
0 MUST BE ZERO
0

4

Serial Interrupt Vector Number Register (SIVNR)

7	6	5	4	3	2	1	0
Serial Interrupt Vector Number (SIVN)							

Address = 14 Reset value = $0F

If a serial interface interrupt condition occurs (as reported by status bits in the SISR that correspond to interrupt enable bits in the SIER) and the corresponding bit in the SIER is set, the $\overline{IRQ}$ output is asserted to request MPU serial interface interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Serial Interrupt Vector Number (SIVN) from the Serial Interrupt Vector Number Register (SIVNR) is placed on the data bus.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	0	0	0	0	0

Address = 15 Reset value = $00

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the $\overline{IRQ}$ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER
7 CTS IE —Clear to Send (CTS) Interrupt Enable.
0 Disable CTS Interrupt.
1 Enable CTS Interrupt.

SIER
6 DSR IE —Data Set Ready (DSR) Interrupt Enable.
0 Disable DSR Interrupt.
1 Enable DSR Interrupt.

SIER
5 DCD IE —Data Carrier Detect (DCD) Interrupt Enable.
0 Disable DCD Interrupt.
1 Enable DCD Interrupt.

SIER
4-0 —Not used.

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES in the TCR and RRES in the RCR should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTLEX	ADDEX

Address = 18 Reset value = $00

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1
7-2 —Not used.

PSR1
1 CTLEX —Control Field Extend (BOP only).
0 Select 8-bit control field.
1 Select 16-bit control field.

PSR1
0 ADDEX —Address Extend (BOP only).
0 Disable address extension. All eight bits of the address byte are utilized for addressing.
1 Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL		
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Address = 19 Reset value = $00

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2
7 WD/BYT —Data Bus Word/Byte Mode.
0 Select byte mode. Selects the number of data bits to be transferred from the RxFIFO and the registers to the data bus and to be transferred from the data bus to the TxFIFO and the registers. The MPCC is initialized by $\overline{RESET}$ to the byte mode.
1 Select word mode. For operation with the 16-bit bus, select the word mode by sending $80 on D7–D0 to address $19 prior to transferring subsequent data between the MPCC and the data bus.

PSR2
6-5 STOP BIT SEL —Number of Stop Bits Select. Selects the number of stop bits transmitted at the end of the data bits in ASYNC and ISOC modes.

6	5	No. of Stop Bits	
SB2	SB1	ASYNC	ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2
4-3 CHAR LEN SEL —Character Length Select. Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

4 CL2	3 CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2
2-0 PROTOCOL SEL—Protocol Select. Selects protocol and defines the protocol dependent control bits.

2 PS3	1 PS2	0 PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1) Address

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Address = 1A Reset value = $00

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BSC & COP SYN							

Address = 1B Reset value = $00

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of AR1 is used for address matching. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	AR1	AR2
BOP (Primary)	X	X
BOP (Secondary)	Address	X
BSC EBCDIC	Leading PAD	SYN
BSC ASCII	Leading PAD	SYN
COP	Leading PAD	SYN
*X = Not used		

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Address = 1C Reset value = $01

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

Address = 1D Reset value = $00

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH), With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{(\text{Prescaler Divider})\ (\text{Baud Rate})\ (K)}$$

where: K = 1 for isochronous or synchronous
2 for asynchronous

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
0	0	0	PSCDIV	TCLKO	RCLKIN	CLK DIV	
						CK2	CK1

Address = 1E Reset value = $00

The CCR selects various clock options.

CCR
7-5 —Not used.

CCR
4 PSCDIV —Prescaler Divider. The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.

0 Divide by 2.
1 Divide by 3.

CCR
3 TCLKO —Transmitter Clock Output Select.

0 Select TxC to be an input.
1 Select TxC to be an output. (1X clock)

4

Table 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider: Asynchronous			Baud Rate Divider: Isochronous and Synchronous		
	Decimal Value	PSCDIV (0 to 1)	Decimal Value	Hexadecimal Value BRDR2 (MSH)	Hexadecimal Value BRDR1 (LSH)	Decimal Value	Hexadecimal Value BRDR2 (MSH)	Hexadecimal Value BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

CCR
2 RCLKIN —Receiver Clock Internal Select (ASYNC only).

0 Select External RxC.
1 Select Internal RxC.

CCR
1-0 CLK DIV —External Receiver Clock Divider. Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16 (ASYNC) only
1	0	32 (ASYNC) only
1	1	64 (ASYNC) only

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CFCRC	CRCPRE	CRCSEL	
						CR2	CR1

Address = 1F Reset value = $04

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR
7 PAREN —Parity Enable. (ASYNC, ISOC and COP only).

0 Disable parity generation/checking.
1 Enable parity generation/checking.

ECR
6 ODDPAR —Odd/Even Parity Select (Effective only when PAREN = 1).

0 Generate/check even parity.
1 Generate/check odd parity.

ECR
5-4 —Not used.

ECR
3 CFCRC —Control Field CRC Enable. (BOP Only)

0 Disable control field CRC.
1 Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR
2 CRCPRE —CRC Generator Preset Select. (BOP, BSC Only)

0 Preset CRC Generator to 0. (For BSC)
1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder. (For BOP)

ECR
1-0 CRCSEL —CRC Polynominal Select. Selects one of the RC polynominals.

1 CR2	0 CR1	Polynominal
0	0	$x^{16}+x^{12}+x^5+1$ (CCITT V.41) (BOP)
0	1	$x^{16}+x^{15}+x^2+1$ (CRC-16) (BSC)
1	0	x^8+1 (VRC/LRC)* (BSC, ASCII, non-transparent)
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals:

	R68561	R68560
Address Lines	A1–A4	A0–A4
Data Lines	D0–D15	D0–D7
Read/Write	R/$\overline{W}$	R/$\overline{W}$
Data Transfer Acknowledge	$\overline{DTACK}$	$\overline{DTACK}$
Chip Select	$\overline{CS}$	$\overline{CS}$
Data Strobes	$\overline{UDS}$ and $\overline{LDS}$	$\overline{DS}$

Figures 10 and 11 show typical interface connections.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the MPCC for access to the internal registers and other operations. When $\overline{CS}$ is asserted, the data I/O buffer acts as an output driver during a read operation and as an input buffer during a write operation. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

When the R68561 is connected to the 16-bit bus for operation in the word mode (WD/BYT = 1 in the PSR2), address lines A1–A4 select the internal register(s) (the 8-bit control/status registers are accesed two at a time and the 16-bit data registers are accessed on even address boundaries). When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), 16 bits of register data are placed on the data bus when the data strobes ($\overline{LDS}$ and $\overline{UDS}$) are asserted. $\overline{LDS}$ strobes the eight data bits from the even numbered registers to the lower data bus lines (D0–D7) and $\overline{UDS}$ strobes the eight data bits from the odd numbered registers to the upper data bus lines (D8–D15). The MPCC asserts Data Transfer Acknowledge ($\overline{DTACK}$) prior to placing data on the data bus. Conversely, when the MPCC is selected ($\overline{CS}$ low) during a write (R/$\overline{W}$ low) $\overline{LDS}$ and $\overline{UDS}$ strobe data from the D0–D7 and D8–D15 data bus lines into the addressed even and odd numbered registers, respectively, and the MPCC asserts $\overline{DTACK}$. $\overline{DTACK}$ is negated when $\overline{CS}$ is negated. Figures 12 and 13 show the read and write timing relationships.

When the R68560 is connected to the 8-bit bus for operation in the byte mode (WD/BYT = 0 in the PSR2), address lines A0–A4 select one internal 8-bit register. When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), eight bits of register data are placed on data bus lines D0–D7 when the data strobe ($\overline{DS}$) is asserted. When the MPCC is selected ($\overline{CS}$ low) for a write (R/$\overline{W}$ low), $\overline{DS}$ strobes data from the D0–D7 data lines into the selected register.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers at up to 2 Mbytes per second when used with the MC68440 or MC68450 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which requires a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input ($\overline{DACK}$) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/$\overline{W}$ input to distinguish between the Transmitter Data Service Request ($\overline{TDSR}$ acknowledge and the Receiver Data Service Request ($\overline{RDSR}$) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the RxFIFO, Receiver Data Service Request ($\overline{RDSR}$) is asserted for one receiver clock period (BOP and BSC) to initiate the MPCC to memory DMA transfer. For asynchronous operation, $\overline{RDSR}$ is asserted for 2–3 periods of the system clock depending on prescale factor. The next $\overline{RDSR}$ cycle may be initiated as soon as the current $\overline{RDSR}$ cycle is completed (i.e., a full sequence of $\overline{DACK}$, $\overline{DS}$, and $\overline{DTC}$).

In response to $\overline{RDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to write, asserts the memory address, address strobe, and DMA acknowledge. The MPCC outputs data from the RxFIFO to the data bus and the DMAC asserts the data strobes. The memory latches the data and asserts $\overline{DTACK}$ to complete the data transfer. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data transfer is complete. Figure 14 shows the timing relationships for the receiver DMA mode.

$\overline{RDSR}$ is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when $\overline{RESET}$ is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the TxFIFO is available, Transmitter Data Service Request ($\overline{TDSR}$) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. For asynchronous operation, $\overline{TDSR}$ is asserted for a period of one-half the transmitter baud rate. The next $\overline{TDSR}$ cycle may be initiated as soon as the current $\overline{TDSR}$ cycle is completed.

In the transmitter DMA mode, the TxFIFO Is implicitly addressed. That is, when the transfer is from memory to the TxFIFO, only the memory is addressed. In response to $\overline{TDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to read, asserts the memory address, the address strobe, the data strobes and DMA acknowledge. The memory places data on the data bus and asserts $\overline{DTACK}$. Data is valid at this time and will remain valid until the data strobes are negated. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data is available. The MPCC loads the data into the TxFIFO on the negation (rising edge) of $\overline{DS}$ and the transfer is complete. When a TxFIFO underrun occurs, the TUNRN bit is set in TSR2, the interrupt is issued, and the ABORT sequence is entered (eight consecutive 1s are transmitted). The next word/byte in TxFIFO clears the ABORT bit and the idle mode is entered. When a transmission is aborted, it is expected that the interrupt will allow the host system to decide the next course of action; probably to reset the DMAC and retransmit the message. A timing diagram for the transmitter DMA Mode is shown in Figure 15.

$\overline{TDSR}$ is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when $\overline{RESET}$ is asserted.

DONE Signal

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts DONE which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode of operation, DONE is issued by the MPCC on an MPCC-to-memory transfer when the last byte/word is being transferred from the RxFIFO to the data bus (if DONEEN bit is set in RCR5). In the byte mode, this is the Frame Status Byte (FSB). In the word mode, this is the last data byte and FSB (for an odd number of data byte transfers) or FSB and blank (for an even number of data byte transfers).

DONE is asserted as a result of the FSB being transferred and not as a result of the error conditions. The EOF, C/PERR and FRERR are addendum bits in the RxFIFO which are written to FIFO when they occur and follow the data through the FIFO. The frame is aborted upon overrun or error detection if RCR1 = 1.

CAUTION

DONE is reasserted with each occurrence of DACK until EOF is cleared in the RSR.

INTERRUPTS

If an interrupt generating status occurs and the interrupt is enabled, the MPCC asserts the IRQ output. Upon receiving IACK for the pending interrupt request, the MPCC places an interrupt vector on D0-D7 data bus and asserts DTACK.

The MPCC has three vector registers: Receiver Interrupt Vector Number Register (RIVNR), Transmitter Interrupt Vector Number Register (TIVN), and Serial Interrupt Vector Number Register (SIVNR). The receiver interrupt has priority over the transmitter interrupt, and the transmitter interrupt has priority over the serial interface interrupt. For example, if a pending interrupt request has been generated simultaneously by the receiver and the transmitter, the Receiver Interrupt Vector Number (RIVN) is placed on D0-D7 when acknowledged by the MPU. Upon completion of the first interrupt request cycle (which clears the receiver interrupt), IRQ will remain low to start the transmitter interrupt cycle. IRQ is negated by clearing all bits set in a status register that could have caused the interrupt.

CAUTION

A higher priority interrupt occuring while IACK is low during transfer of a lower priority interrupt vector to the MPU will cause the lower priority interrupt vector on the data bus to be invalid if there are any 1's in the higher priority interrupt vector in the same bit poositions as any 0's in the lower priority interrupt vector. To prevent this problem from occuring, ensure that the higher priority interrupt vectors contain 1's only in bit positions where there are 1's in the lower priority interrupt vectors, e.g.:

Vector	Vector Value (Hex)	Vector Value (Binary)
Receiver Interrupt Vector Number (RIVN)	44	01000100
Transmitter Interrupt Vector Number (TIVN)	4C	01001100
Serial Interrupt Vector Number (SIVN)	5C	01011100

A timing diagram for the interrupt acknowledge sequence is shown in Figure 16.

SERIAL INTERFACE

The MPCC is a high speed, high performance device supporting the more popular bit and character oriented data protocols. The lower speed asynchronous (ASYNC) and isochronous (ISOCH) modes are also supported. An on-chip clock oscillator and baud rate generator provide an output data clock at a frequency of DC to a 4 MHz.. The clock can also be used in the ASYNC mode to provide a receive clock for the incoming data. The serial interface consists of the following signals:

RTS (Request to Send) Output

The RTS output to the DCE is controlled by the RTSLVL bit in the SICR inn conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the RTS output is asserted. When the RTSLVL bit is reset to 0 (no sooner than one full cycle of TxC after transmission has started), the RTS output remains asserted until the TxFIFO becomes empty, or the end of the message (or frame), complete with CRC code (if any), closing flag, and one full cycle of idle has been transmitted. RTS also is negated when the RTSLVL bit is reset during transmitter idle, or when the RESET input is asserted.

CTS (Clear to Send) Input

The CTS input signal is normally generated by the DCE to indicate whether or not the data set is ready to receive data. The CTST bit in the SISR reflects the transition status of the CTS input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the CTS pin asserts IRQ if the CTS IE bit in the SIER is set. The CTS input in an inactive state disables the start of transmission of each frame.

DCD (Data Carrier Detect) Input

The DCD input signal is normally gnerated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The DCDT bit in the SISR reports the transition status of the DCD input while the DCDLVL bit in the SISR contains the current level. A positive transition on the DCD pin asserts the IRQ output if the DCD IE bit in the SIER is set. A negated DCD input disables the start of the receiver but does not stop the operation of an incoming message already in progress.

$\overline{\text{DSR}}$ (Data Set Ready) Input/RSYN Output

The DSRT input from the DCE indicates the status of the local set. The DSRT bit in the SISR contains the transition status of the $\overline{\text{DSR}}$ input while the DSRLVL bit in the SISR reports the current level. A negative transition on the $\overline{\text{DSR}}$ pin asserts the $\overline{\text{IRQ}}$ output if the DSR IE bit in the SIER is set.

The $\overline{\text{DSR}}$ pin is used as an output for RSYN when enabled by a 1 in RSR4 (RSYNEN = 1). DSR output low indicates detection of a SYN (non-transparent) in BSC or COP protocols or DLE-SYN pair (transparent) in BSC protocol. It is asserted as a negative-going pulse one-bit time after the end of the SYN byte and lasts for one full serial clock cycle before being reset.

In BOP protocol, RSYN is asserted as a result of address match at the beginning of a frame. It is asserted one bit time after the end of the address byte(s) if an address match is made, and lasts for one full serial clock cycle.

$\overline{\text{DTR}}$ (Data Terminal Ready) Output

The $\overline{\text{DTR}}$ output is general purpose in nature and can be used to control switching of the DCE. The $\overline{\text{DTR}}$ output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCKLO control bit is reset, TxC is an input and the transmitter shift timing must be provided exernally. The TxD output changes state on the negative-going edge of the transmitter clock. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC input frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ data format. The first byte of a message transmitted out of the R68561 MPCC is the even byte of the 68000 bus (D8–D15). It is transmitted least significant bit (LSB) first.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC.

RxD (Received Data) Input

The serial data received by the MPCC is in NRZ data format. The first byte received in the MPCC RXFIFO is output to the 68000 bus on (D8–D15).

Serial Interface Timing

The timing for the serial interface clock and data lines is shown in Figure 18. The MPCC supports high speed synchronous operation. As shown, the TxD output changes with the negative-going edge of TxC and the received data on RxD is latched on the negative edge of RxC. This assures high speed two-way operation between two MPCCs connected as shown in Figure 17.

For low speed operation between the MPCC and a modem or RS-232C Data Communications Equipment (DCE), an inverter can be used in the TxC output lines as shown in Figure 17. RS-232 and RS-423 (covering serial data interface up to 100K baud) require that data be centered ±25% about the negative-going edge of the RxC. This criteria is met for frequencies up to 1.25 MHz using the inverter. Use of the inverter also allows MPCC to MPCC operation up to 2.17 MHz.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCHRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames, however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 4 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYNC) mode, data reception on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the RxFIFO and set appropriate status bits in the RSR when the character with an error reaches the last RxFIFO register where it is ready to be transferred onto the data bus via the RDR.

Isochronous Receive

In the isochronous (ISOC) mode, a times 1 clock on RxC is required with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data transmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character. Each frame is terminated with 1, 1½ or 2 stop bits as selected by PSR2 bits 5 and 6.

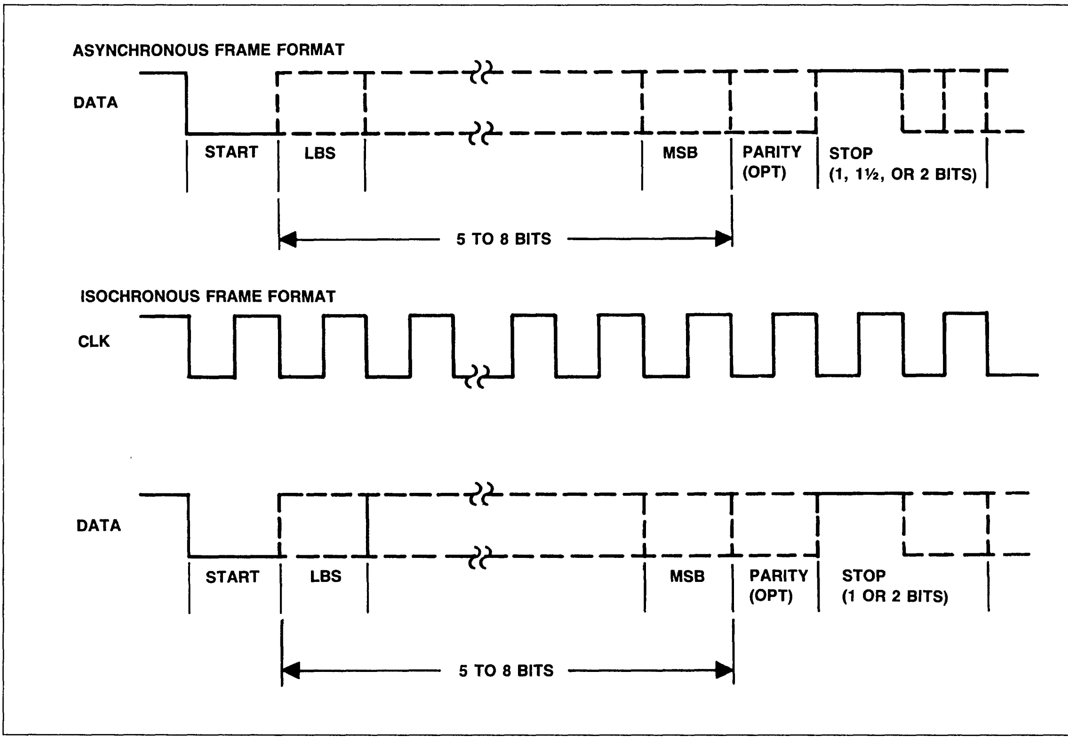


Figure 4. Asynchronous and Isochronous Frame Format

SYNCHRONOUS MODES

In synchronous modes, a times one clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 5).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. The first byte of the address field is automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made. The control field of one or two bytes is transparent to the MPCC and sent directly to the host without interpretation.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1s, and the 1s complement of the resulting remainder is transmitted. (See X.25 Recommendation.)

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110

Figure 5. Bit Oriented Protocol (BOP) Frame Format

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

The end of the frame is determined by the detection of the closing Flag special character which is the same is the opening Flag.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC and X.25 standards can be supported. Figure 6 compares the requirements of these options.

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a Flag. The receiver also continues to search for additional Flag, or Abort, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the Flag detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "011111101111110."

Character assembly and CRC accumulation are stopped when a closing Flag or Abort is detected. The CRC accumulation includes all the characters between the opening Flag and the closing Flag. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the Flag are not passed on to the RxFIFO.

If the Flag is a closing flag, checks for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an Abort (seven 1s) is detected, the remaining frame is discarded and the RA/B bit is set in the RSR. When a link idle (15 or more consecutive 1s) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of the first byte. If there is no address match, or if null address is received, the receiver ignores the remainder of the frame by searching for the Flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CFCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading Flag is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an Abort (11111111) is transmitted followed by continuous Flags or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the $\overline{\text{DONE}}$ signal from the DMAC.

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an Abort character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1s, and a 0 is inserted in the data stream each time this condition occurs (excluding Flag and Abort characters).

CRC accumulation begins with the first non-Flag character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control field. The final Frame Check Sequence is calculated over the balance of the frame.

4

IBM SDLC FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

Figure 6. Bit Oriented Protocols

LEADING PAD 1 BYTE (AR1)	SYN 1 BYTE (AR2)	SYN 1 BYTE (AR2)	BODY	BCC	TRAILING PAD 11111111

Figure 7. BSC Block Format

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 7. The MPCC can process both transparent and nontransparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 4.

Table 4. BSC Control Sequences—Inclusion in CRC Accumulation

ASCII			EBCDIC		
Command	**Byte 1**	**Byte 2**	**Command**	**Byte 1**	**Byte 2**
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

Note: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 5 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 8 shows various formats for Control/Response Blocks and Heading and Text Blocks.

Table 5. Transparent Mode BSC Control Sequences — Inclusion in CRC Accumulation

	Included in CRC Accumulation	
Character of Sequence	**Yes**	**No**
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

*If not preceded within the same block by transparent heading information.

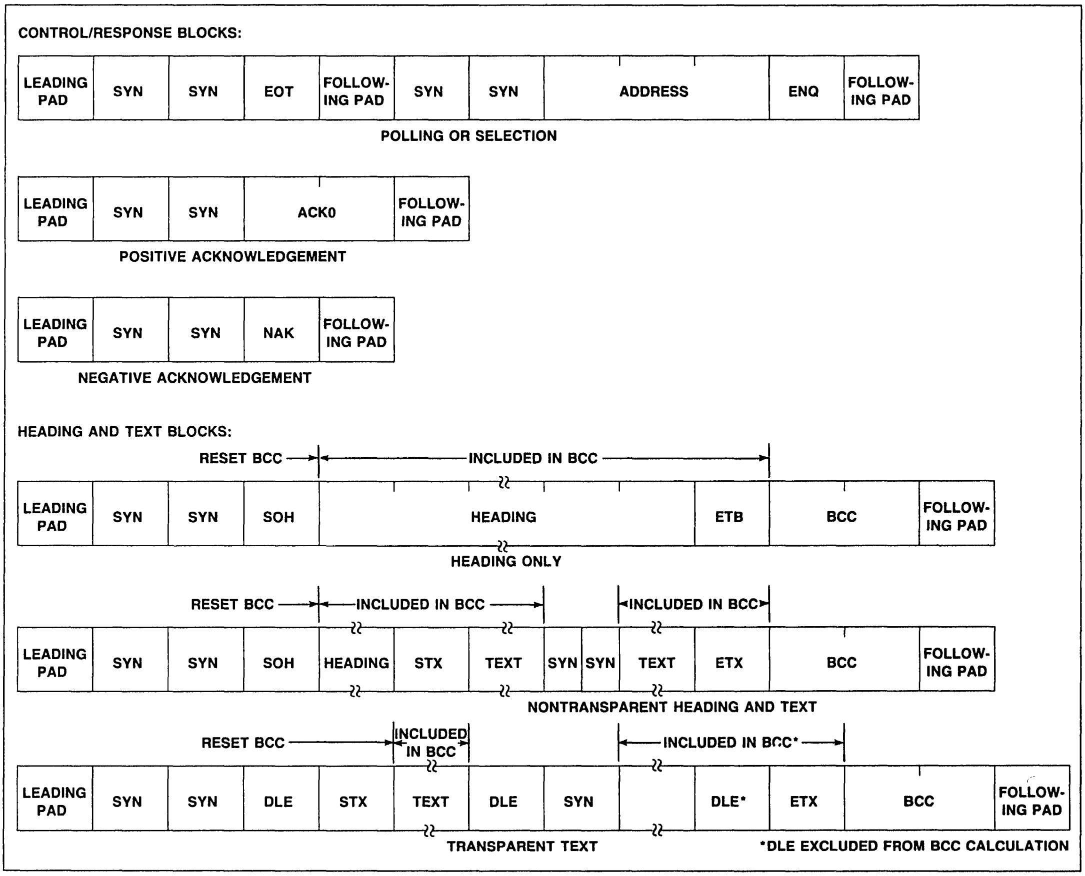


Figure 8. BSC Message Format Examples

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided that VRC/LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character pairs in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation and is discarded. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). The first SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available. The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 5 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO. ETB, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters. DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 9. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

DMA CONSIDERATIONS

When the R68561, in the word mode, is used with a DMAC, high throughput of bit-oriented protocols is achieved. However, problems can arise when trying to DMA byte-oriented data in the word mode.

BOP and BSC have well-defined message boundaries and the MPCC can detect the end of message, determine if there is an odd (single) byte at the end of a message, and so inform the host MPU by setting the Received Half Word (RHW) bit in the Frame Status byte.

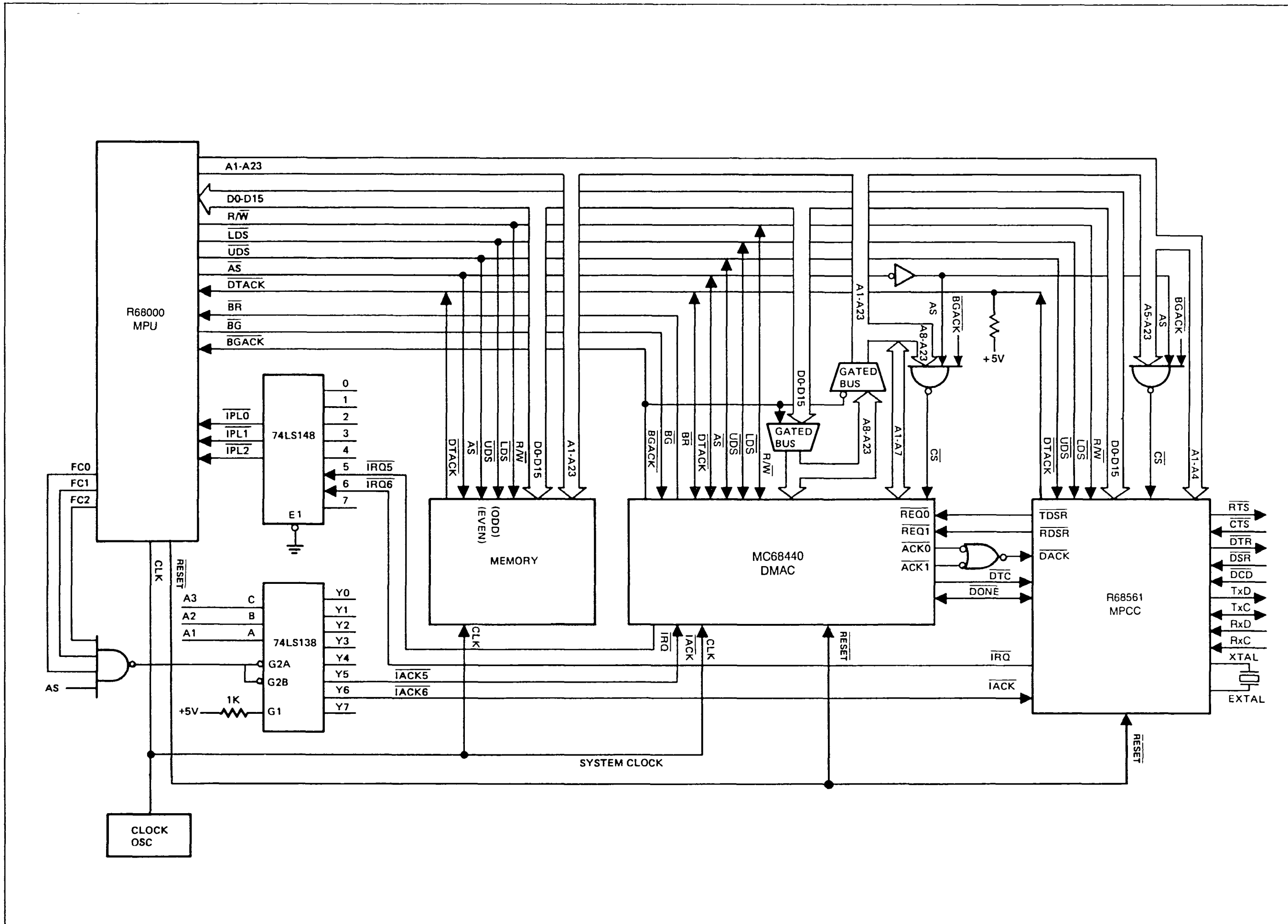
In byte-oriented protocols (such as ASYNC and COP) there is no defined message length. In the word mode, received bytes are grouped in pairs. In the byte mode, each byte is available through the RxFIFO as it is received. Thus, the MPCC in the word mode has no way of knowing when an odd (single) byte has been received at an end of a transmission to be passed onto the host MPU. In the word mode received bytes are grouped in pairs. In the byte mode each byte is available through the FIFO as it is received.

For transmission of data by the MPCC in the word mode, the MPCC provides a Transmit Half Word (THW) bit in the Transmit Control Register. When set, this bit informs the MPCC that the last word in the TxFIFO (marked by setting the TLAST bit with DONE) contains only the upper byte as valid data. However, the currently available DMACs have no method to inform the MPCC that the last word of the message contains a single byte and MPU intervention is necessary.

To handle byte-oriented protocols with DMAC, an R68561 in the byte mode or the R68560 (byte mode only) should be used.

LEADING PAD	SYN	SYN	MESSAGE
5-8 BITS	5-8 BITS	5-8 BITS	← 5-8 BIT CHARACTERS →
(AR1)	(AR2)	(AR2)	

Figure 9. Character Oriented Protocol Format



NOTE: $\overline{UDS}$ MAY BE TIED LOW (GROUND).

Figure 10. Typical Interface to 68000-Based System

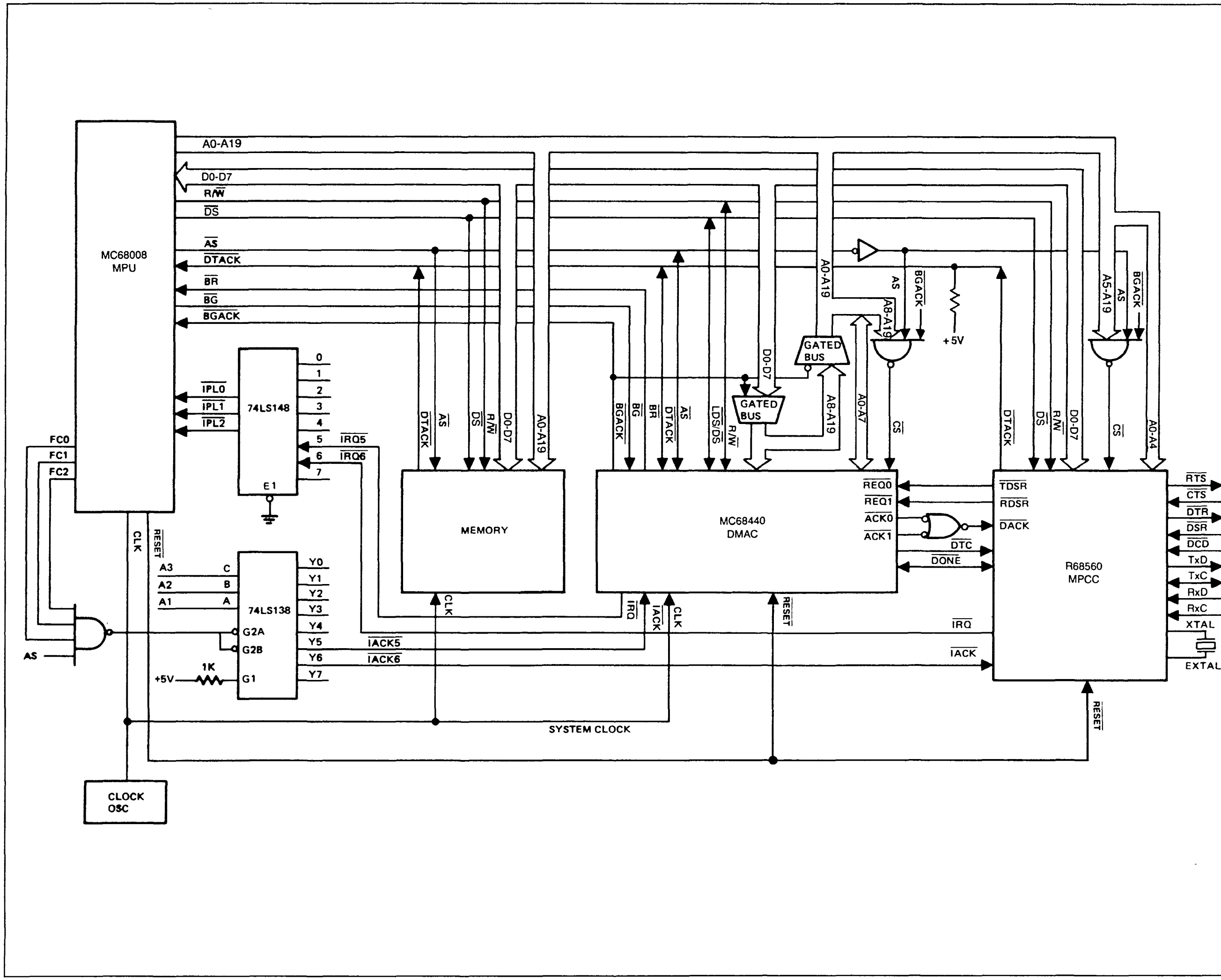
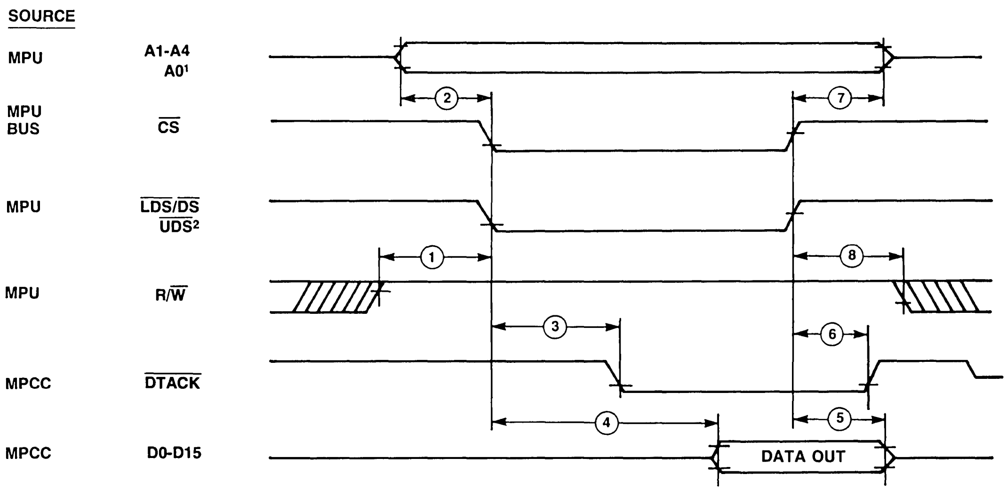
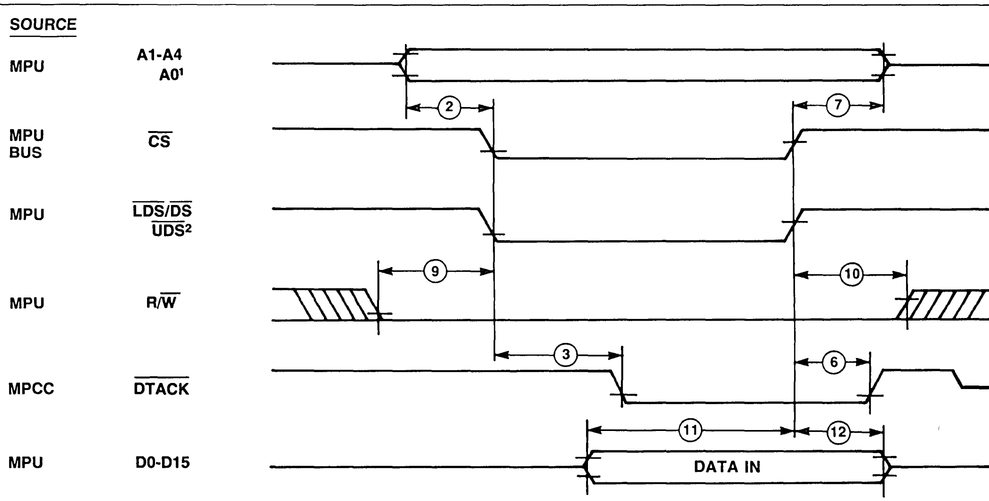


Figure 11. Typical Interface to 68008-Based System



NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
4. SEE ADDITIONAL NOTES ON PAGE 32.

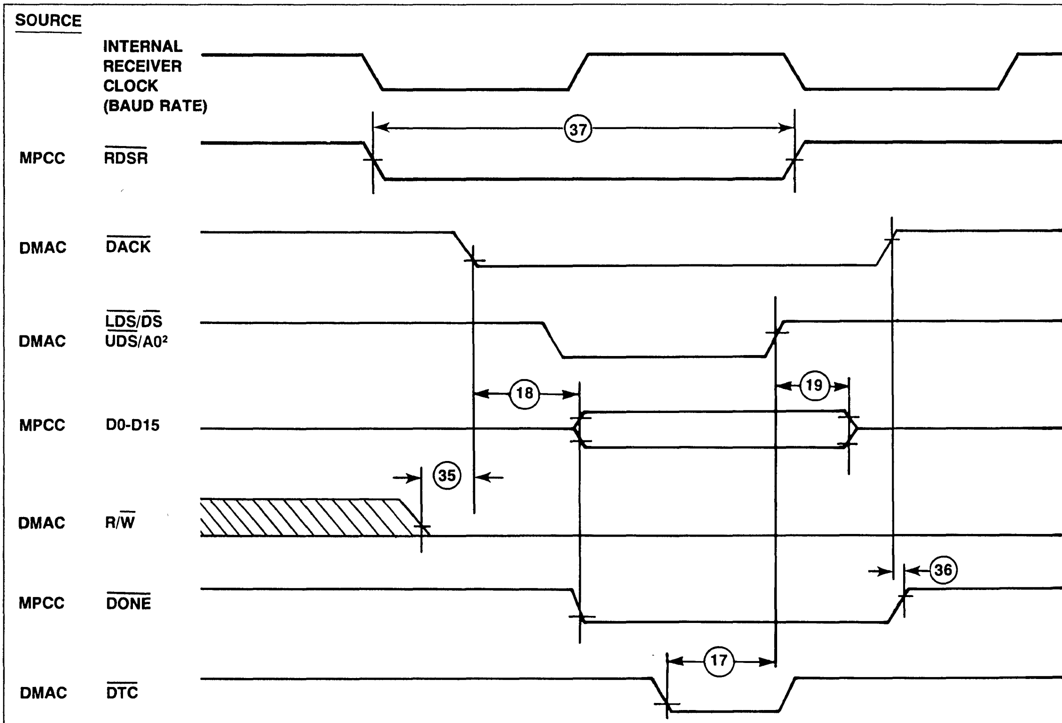
Figure 12. MPCC Read Cycle Timing



NOTES:
1. BYTE MODE WHEN CONNECTED TO A0 ON 68008 BUS.
2. WORD MODE WHEN CONNECTED TO UDS ON 68000 BUS.
3. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
4. SEE ADDITIONAL NOTES ON PAGE 32.

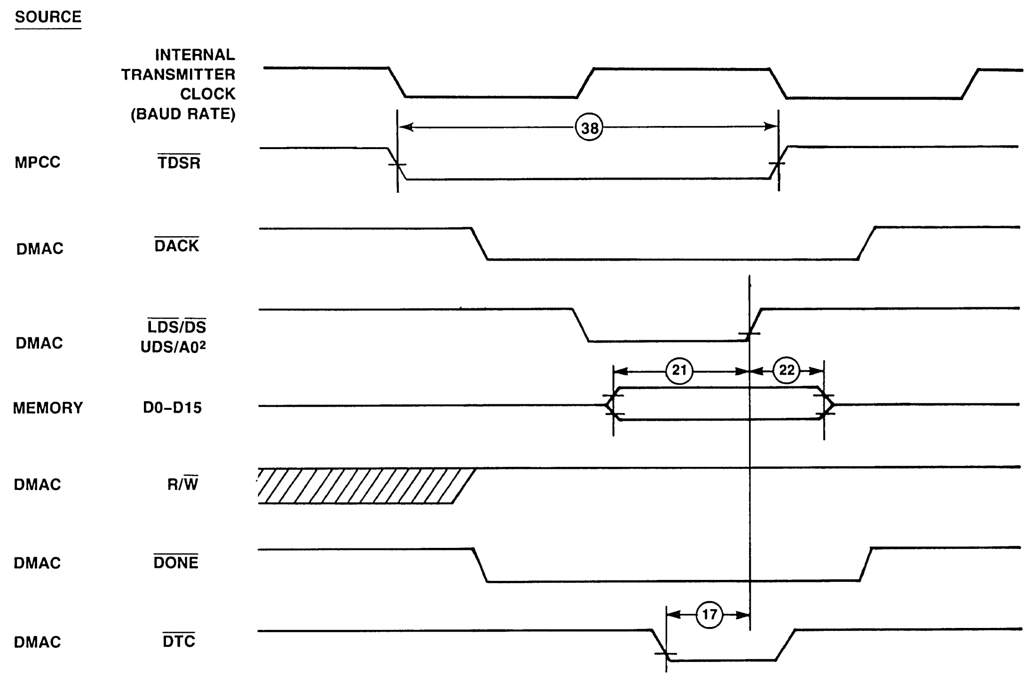
Figure 13. MPCC Write Cycle Timing

4



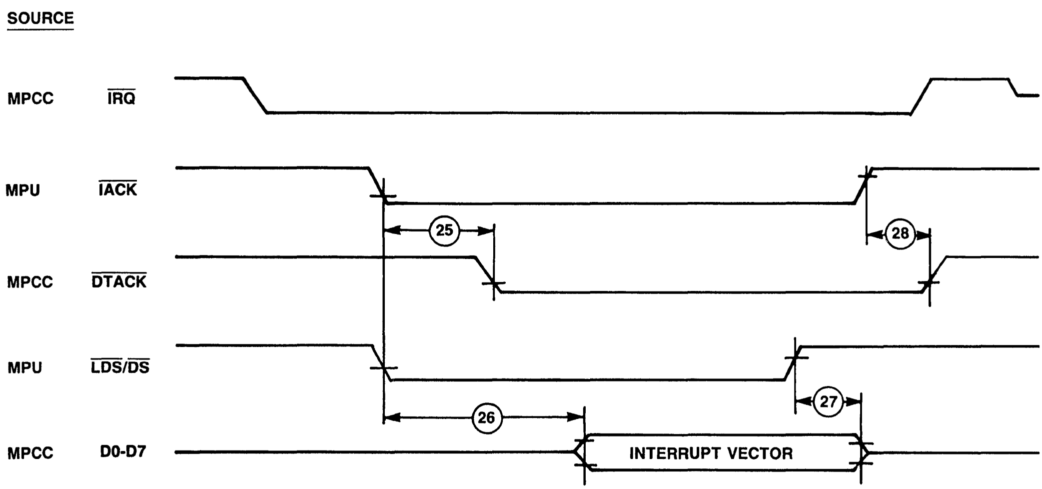
NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.
3. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 14. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE NOTED.
2. WORD MODE ONLY.
3. SEE ADDITIONAL NOTES ON PAGE 32.

Figure 15. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode)



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. IRQ IS NEGATED WHEN ALL BITS IN STATUS REGISTERS THAT COULD HAVE CAUSED THE INTERRUPT ARE CLEARED.
3. SEE ADDITIONIONAL NOTES ON PAGE 32.

Figure 16. Interrupt Request Cycle Timing

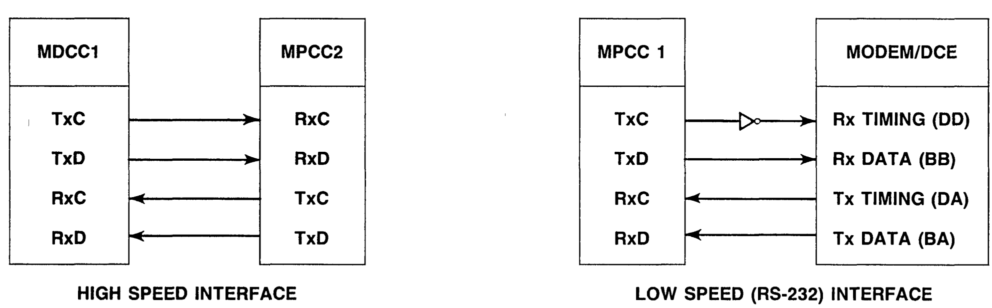


Figure 17. Serial Interface

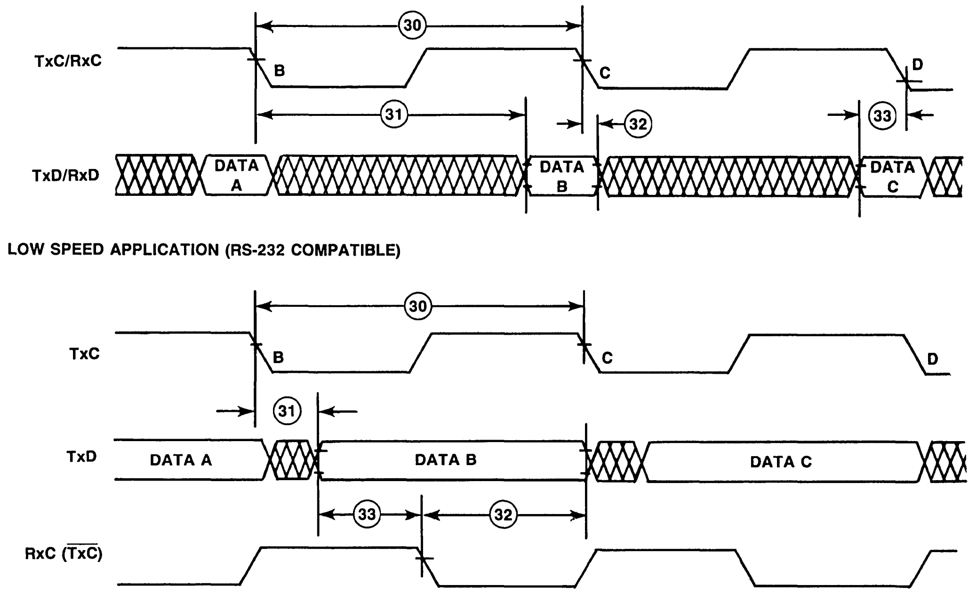
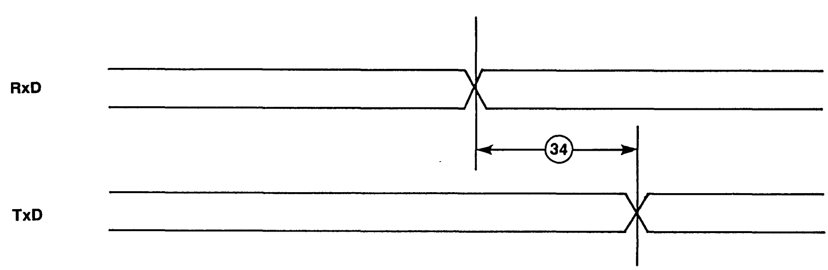


Figure 18. Serial Interface Timing



NOTE:
TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

Figure 19. Serial Interface Echo Mode Timing

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Number	Parameter	Symbol	Min	Max	Unit
1	R/W High to CS, DS Low	t_{RHSL}	0	—	ns
2	Address Valid to CS, DS Low	t_{AVSL}	30	—	ns
3[1]	CS Low to DTACK Low	t_{CLDAL}	0	60	ns
4[1]	CS, DS Low to Data Valid	t_{SLDV}	0	140	ns
5	DS High to Data Invalid	t_{SHDXR}	10	150	ns
6	DS High to DTACK High	t_{SHDAT}	0	40	ns
7	DS High to Address Invalid	t_{SHAI}	20	—	ns
8	CS, DS High to R/W Low	t_{SHRL}	20	—	ns
9	R/W Low to CS, DS Low	t_{RLSL}	0	—	ns
10	CS High, DS High to R/W High	t_{SHRH}	20	—	ns
11	Data Valid to CS, DS High	t_{DVSH}	60	—	ns
12	CS, DS High to Data Invalid	t_{SHDXW}	0	—	ns
17	DTC Low to DS High	t_{CLSH}	60	—	ns
18	DACK Low to Data Valid, DONE Low	t_{ALDV}	0	140	ns
19	DS High to Data Invalid	t_{SHDXDR}	10	150	ns
21	Data Valid to DS High	t_{DVSH}	60	—	ns
22	DS High to Data Invalid	t_{SHDXDW}	0	—	ns
25	IACK Low to DTACK Low	t_{IALAL}	0	40	ns
26	IACK, DS Low to Data Valid	t_{IALDV}	0	140	ns
27	DS High to Data Invalid	t_{ISHDI}	10	150	ns
28	IACK High to DTACK High	t_{IAHDAT}	0	40	ns
30	RxC and TxC Period	t_{CP}	248	—	ns
31	TxC Low to TxD Delay	t_{TCLTD}	0	200	ns
32	RxC Low to RxD Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to RxC Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to TxD Delay (Echo Mode)	t_{RDTD}	—	200	ns
35	R/W Low to DACK Low (Setup)	t_{RLAL}	0	—	ns
36	DACK High to DONE High	t_{AHDH}	0	—	ns
37[2,3]	RDSR Pulse Width	t_{RPW}	1	—	clock period
38[2,4]	TDSR Pulse Width	t_{TPW}	1	—	clock period

Notes:
1. For read cycle timing, the MPCC asserts DTACK within the MPU S4 clock low setup time requirement and establishes valid data (Data In) within the MPU S6 clock low setup time requirement.
2. For synchronous protocols, this is one full serial clock period of RxC for RDSR and TxC for TDSR.
3. For asynchronous protocols, RDSR is asserted for two system clock periods for a prescale factor of 2 and for three system clock periods for a prescale factor of 3.
4. For asynchronous protocols, TDSR is asserted for a period of one-half the baud rate.

*NOTES TO FIGURES 12–16.

Address, LDS, UDS and R/W are signals generated by the 68000 MPU and its bus timing prevails. CS is derived with external logic from the address bus and generally an Address Strobe (AS) signal from the MPU. It will naturally be delayed somewhat from the AS signal. The active read or write cycle timing in the MPCC is during the summation of the active signal time, i.e., the last active signal starts the timing sequence. For an MPCC read cycle, for example, the data out parameter (t_{SLDV}, item 4) will be available 0 to 140 ns from the falling edge of CS or LDS whichever is active last. The data out parameter (t_{SHDXR}, item 5) will remain valid for 0–150 ns after the negation of CS or LDS, whichever is negated first.

The minimum pulse widths for CS, LDS, UDS, DACK, IACK and DTC are not specified since they are system dependent and relate to system clock timing. For example, it is apparent that the minimum active time for "AND" condition of CS and LDS is 140 ns (t_{SLDV}, item 4) plus the setup time of the Data In to the receiving device if LDS high is used to strobe the data in. These same factors hold true for UDS, DACK and IACK. If DTC is used it must be true a minimum of 60 ns before the rising edge of LDS and thus this is the minimum pulse width. It may be connected to ground.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

DC CHARACTERISTICS

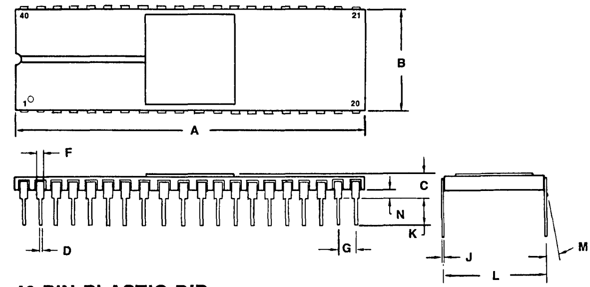
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input High Voltage All Inputs	V_{IH}	2.0	V_{CC}	V	
Input Low Voltage All Inputs	V_{IL}	−0.3	+0.8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RESET}$, $\overline{CS}$, A1-A4	I_{IN}	—	10.0	μA	V_{IN} = 0 to 5.25V V_{CC} = 5.25V
Three-State (Off State) Input Current $\overline{IRQ}$, $\overline{DTACK}$, D0-D15	T_{TSI}	—	10.0	μA	V_{IN} = 0.4 to 2.4V V_{CC} = 5.25V
Output High Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$, D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = −400 μA C_{LOAD} = 130 pF
BCLK	V_{OH}	V_{SS} + 2.4	—	V	V_{CC} = 4.75V I_{LOAD} = 0 C_{LOAD} = 30 pF
Output Low Voltage $\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$ D0-D15, $\overline{DSR}$, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC, BCLK,	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA
$\overline{DONE}$	V_{OL}	—	0.5	V	V_{CC} = 4.75V I_{LOAD} = 8.8 mA
Internal Power Dissipation	P_{INT}	—	1	W	T_A = 25°C
Input Capacitance	C_{IN}	—	13	pF	V_{IN} = 0V T_A = 25°C f = 1 MHz

4

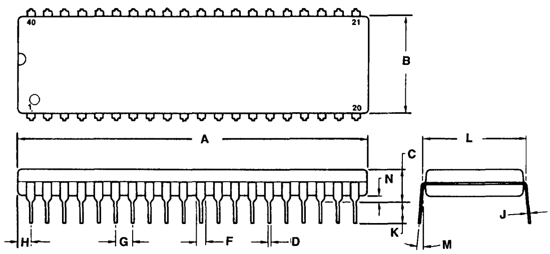
PACKAGE DIMENSIONS — 40-PIN DIP

40-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.73	15.24	0.580	0.600
C	3.30	4.32	0.130	0.170
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	1.02	1.52	0.040	0.060

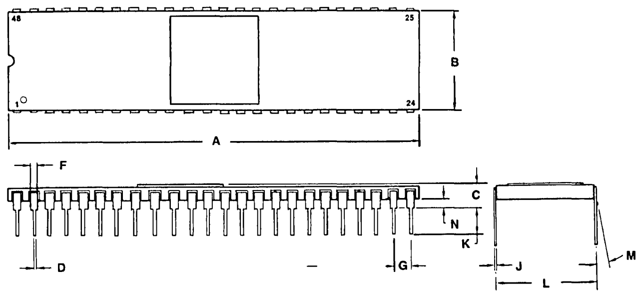
40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.40	1.91	0.055	0.075
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	14.48	16.00	0.570	0.630
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

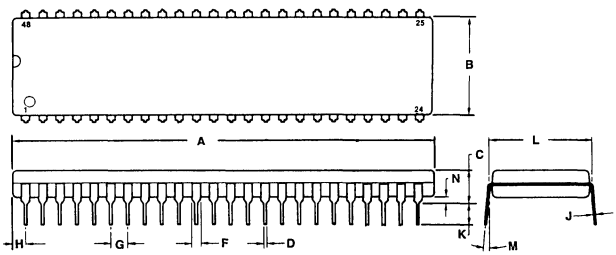
PACKAGE DIMENSIONS — 48-PIN DIP

48-PIN CERAMIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.73	15.24	0.580	0.600
C	3.30	4.32	0.130	0.170
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	14.99	15.49	0.590	0.610
M	0°	10°	0°	10°
N	1.02	1.52	0.040	0.060

48-PIN PLASTIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	60.83	61.85	2.395	2.435
B	13.72	14.22	0.540	0.560
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.40	1.91	0.055	0.075
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	14.48	16.00	0.570	0.630
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040