

Leading-performance 100 MHz Arm Cortex-M33 core, up to 512 KB code flash memory with background operation, 8 KB Data flash memory, and 128 KB SRAM with Parity. High-integration with USB 2.0 Full-Speed, Quad SPI, and advanced analog.

Features

- **Arm® Cortex®-M33 Core**
 - Armv8-M architecture with the main extension
 - Maximum operating frequency: 100 MHz
 - Arm Memory Protection Unit (Arm MPU)
 - Protected Memory System Architecture (PMSAv8)
 - Secure MPU (MPU_S): 8 regions
 - Non-secure MPU (MPU_NS): 8 regions
 - SysTick timer
 - Embeds two SysTick timers: Secure and Non-secure instance
 - Driven by LOCO or system clock
 - CoreSight™ ETM-M33
- **Memory**
 - Up to 512-KB code flash memory
 - 8-KB data flash memory (100,000 program/erase (P/E) cycles)
 - 128-KB SRAM
- **Connectivity**
 - Serial Communications Interface (SCI) × 4
 - Asynchronous interfaces
 - 8-bit clock synchronous interface
 - Smart card interface
 - Simple IIC
 - Simple SPI
 - Manchester coding (SCI3, SCI4)
 - I²C bus interface (IIC)
 - Serial Peripheral Interface (SPI)
 - Quad Serial Peripheral Interface (QSPI)
 - USB 2.0 Full-Speed Module (USBFS)
 - Control Area Network module (CAN)
- **Analog**
 - 12-bit A/D Converter (ADC12)
 - 12-bit D/A Converter (DAC12)
- **Timers**
 - General PWM Timer 32-bit (GPT32) × 2
 - General PWM Timer 16-bit (GPT16) × 2
 - Low Power Asynchronous General Purpose Timer (AGT) × 5
- **Security and Encryption**
 - Arm® TrustZone®
 - Up to three regions for the code flash
 - Up to two regions for the data flash
 - Up to three regions for the SRAM
 - Individual secure or non-secure security attribution for each peripheral
- **System and Power Management**
 - Low power modes
 - Battery backup function (VBATT)
 - Realtime Clock (RTC) with calendar and VBATT support
 - Event Link Controller (ELC)
 - Data Transfer Controller (DTC)
 - DMA Controller (DMAC) × 8
 - Power-on reset
 - Low Voltage Detection (LVD) with voltage settings
 - Watchdog Timer (WDT)
 - Independent Watchdog Timer (IWDT)
- **Multiple Clock Sources**
 - Main clock oscillator (MOSC) (8 to 24 MHz)
 - Sub-clock oscillator (SOSC) (32.768 kHz)
 - High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
 - Middle-speed on-chip oscillator (MOCO) (8 MHz)
 - Low-speed on-chip oscillator (LOCO) (32.768 kHz)
 - IWDT-dedicated on-chip oscillator (15 kHz)
 - Clock trim function for HOCO/MOCO/LOCO
 - PLL/PLL2
 - Clock out support
- **General-Purpose I/O Ports**
 - 5-V tolerance, open drain, input pull-up, switchable driving ability
- **Operating Voltage**
 - VCC: 2.7 to 3.6 V
- **Operating Temperature and Packages**
 - Ta = -40°C to +85°C
 - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
 - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm[®]-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex[®]-M33 core running up to 100 MHz with the following features:

- Up to 512 KB code flash memory
- 128 KB SRAM
- Quad Serial Peripheral Interface (QSPI)
- USBFS
- Analog peripherals
- Security and safety features

1.1 Function Outline

Regarding Security function, only the access control circuit, random number generation circuit, and unique ID are supported. The operation of the other circuits is not guaranteed.

Table 1.1 Arm core

| Feature | Functional description |
|---------------------|---|
| Arm Cortex-M33 core | <ul style="list-style-type: none"> • Maximum operating frequency: up to 100 MHz • Arm Cortex-M33 core: <ul style="list-style-type: none"> – Armv8-M architecture with security extension – Revision: r0p4-00rel0 • Arm Memory Protection Unit (Arm MPU) <ul style="list-style-type: none"> – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer <ul style="list-style-type: none"> – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33 |

Table 1.2 Memory

| Feature | Functional description |
|-----------------------|--|
| Code flash memory | Maximum 512 KB of code flash memory. |
| Data flash memory | 8 KB of data flash memory. |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. |
| SRAM | On-chip high-speed SRAM with or without parity bit. |

Table 1.3 System (1 of 2)

| Feature | Functional description |
|-----------------------------|--|
| Operating modes | Two operating modes: <ul style="list-style-type: none"> • Single-chip mode • SCI/USB boot mode |
| Resets | The MCU provides 13 resets. |
| Low Voltage Detection (LVD) | The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. |

Table 1.3 System (2 of 2)

| Feature | Functional description |
|--|--|
| Clocks | <ul style="list-style-type: none"> • Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL/PLL2 • Clock out support |
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. |
| Interrupt Controller Unit (ICU) | The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. |
| Low power modes | Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. |
| Battery backup function | A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. |
| Register write protection | The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). |
| Memory Protection Unit (MPU) | The MCU has one Memory Protection Unit (MPU). |

Table 1.4 Event link

| Feature | Functional description |
|-----------------------------|--|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. |

Table 1.5 Direct memory access

| Feature | Functional description |
|--------------------------------|---|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. |
| DMA Controller (DMAC) | The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. |

Table 1.6 External bus interface

| Feature | Functional description |
|--------------|--|
| External bus | <ul style="list-style-type: none"> • QSPI area (EQBIU): Connected to the QSPI (external device interface) |

Table 1.7 Timers (1 of 2)

| Feature | Functional description |
|-----------------------------------|---|
| General PWM Timer (GPT) | The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 2 channels and a 16-bit timer with GPT16 × 2 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. The GPT can also be used as a general-purpose timer. |
| Port Output Enable for GPT (POEG) | The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state |

Table 1.7 Timers (2 of 2)

| Feature | Functional description |
|--|--|
| Low Power Asynchronous General Purpose Timer (AGT) | The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. |
| Realtime Clock (RTC) | The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. |
| Watchdog Timer (WDT) | The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. |

Table 1.8 Communication interfaces

| Feature | Functional description |
|---|--|
| Serial Communications Interface (SCI) | The Serial Communications Interface (SCI) × 4 channels have asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) 8-bit clock synchronous interface Simple IIC (master-only) Simple SPI Smart card interface Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 3, 4, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. |
| I ² C bus interface (IIC) | The I ² C bus interface (IIC) has 1 channel. The IIC module conforms with and provides a subset of the NXP I ² C (Inter-Integrated Circuit) bus interface functions. |
| Serial Peripheral Interface (SPI) | The Serial Peripheral Interface (SPI) has 1 channel. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. |
| Control Area Network (CAN) | The Controller Area Network (CAN) module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. The CAN module requires an additional external CAN transceiver. |
| USB 2.0 Full-Speed module (USBFS) | The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. |
| Quad Serial Peripheral Interface (QSPI) | The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. |

Table 1.9 Analog

| Feature | Functional description |
|------------------------------|--|
| 12-bit A/D Converter (ADC12) | A 12-bit successive approximation A/D converter is provided. Up to 9 analog input channels are selectable. |
| 12-bit D/A Converter (DAC12) | A 12-bit D/A converter (DAC12) is provided. |

Table 1.10 Data processing

| Feature | Functional description |
|--|--|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. |
| Data Operation Circuit (DOC) | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. |

Table 1.11 I/O ports

| Feature | Functional description |
|------------------------|---|
| Programmable I/O ports | <ul style="list-style-type: none"> • I/O ports for the 64-pin LQFP <ul style="list-style-type: none"> – I/O pins: 43 – Input pins: 1 – Pull-up resistors: 44 – N-ch Open-drain outputs: 43 – 5-V tolerance: 9 • I/O ports for the 48-pin QFN <ul style="list-style-type: none"> – I/O pins: 29 – Input pins: 1 – Pull-up resistors: 30 – N-ch Open-drain outputs: 29 – 5-V tolerance: 4 |

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

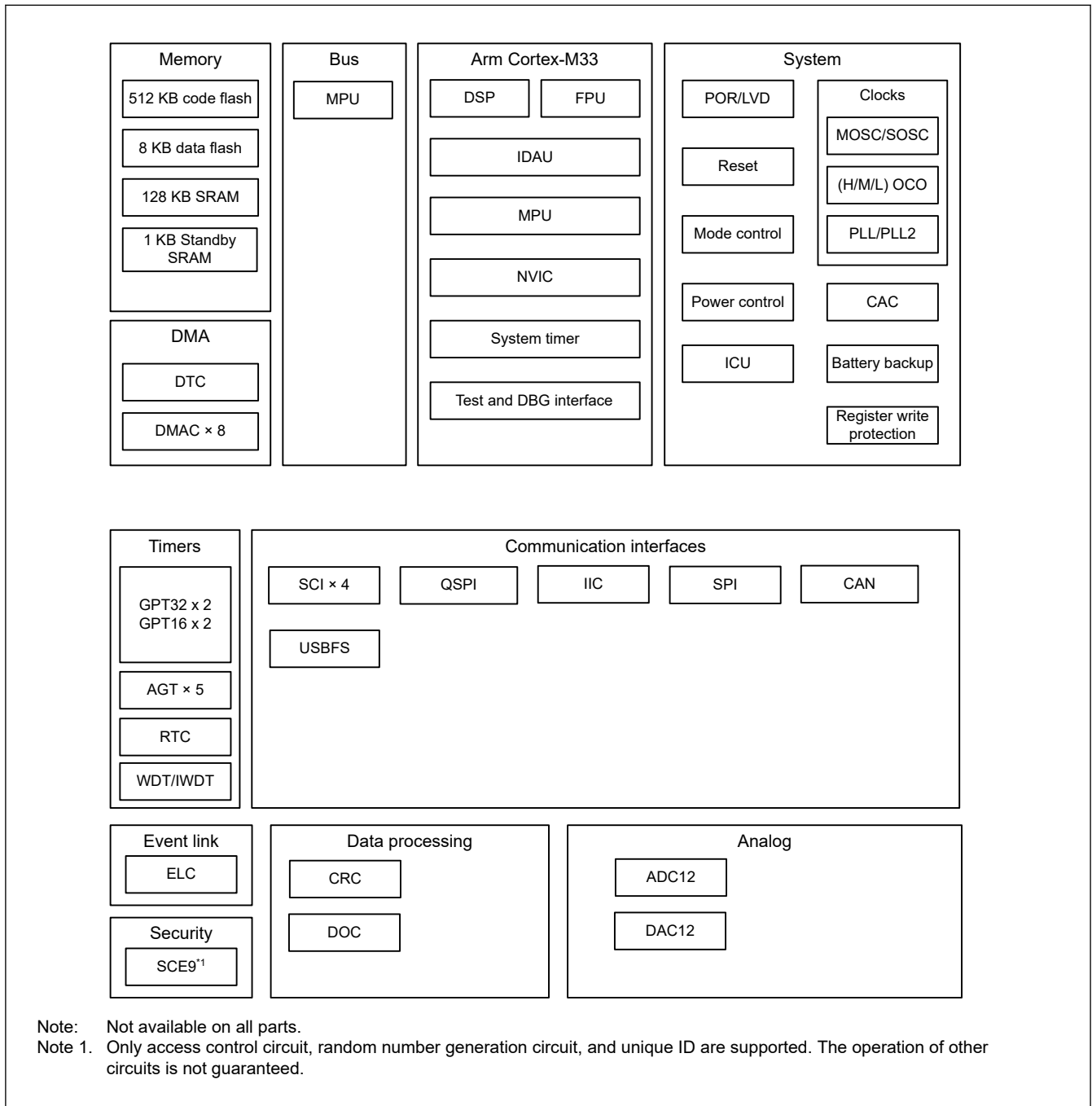


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

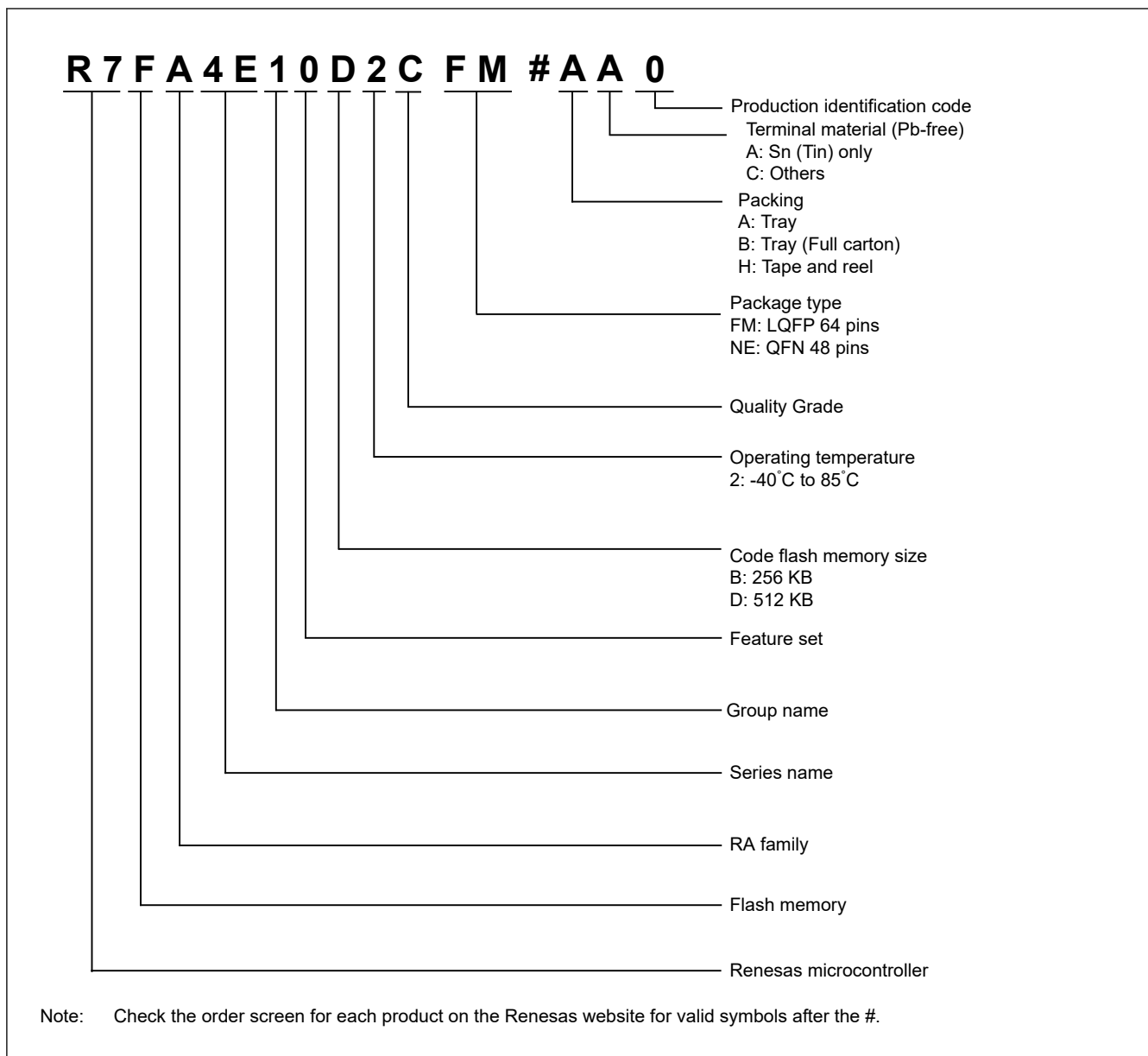


Figure 1.2 Part numbering scheme

Table 1.12 Product list

| Product part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---------------------|--------------|------------|------------|--------|-----------------------|
| R7FA4E10D2CFM | PLQP0064KB-C | 512 KB | 8 KB | 128 KB | -40 to +85°C |
| R7FA4E10D2CNE | PWQN0048KC-A | | | | |
| R7FA4E10B2CFM | PLQP0064KB-C | 256 KB | 8 KB | 128 KB | -40 to +85°C |
| R7FA4E10B2CNE | PWQN0048KC-A | | | | |

1.4 Function Comparison

Table 1.13 Function Comparison

| Parts number | | R7FA4E10D2CFM R7FA4E10B2CFM | R7FA4E10D2CNE R7FA4E10B2CNE |
|-------------------|-------------------------|--|--------------------------------|
| Pin count | | 64 | 48 |
| Package | | LQFP | QFN |
| Code flash memory | | 512KB 256KB | |
| Data flash memory | | 8 KB | |
| SRAM | | 128 KB | |
| | Parity | 64 KB | |
| Standby SRAM | | 1 KB | |
| DMA | DTC | Yes | |
| | DMAC | 8 | |
| System | CPU clock | 100 MHz (max.) | |
| | CPU clock sources | MOSC, SOSC, HOCO, MOCO, LOCO, PLL | |
| | CAC | Yes | |
| | WDT/IWDT | Yes | |
| | Backup register | 128 B | |
| Communication | SCI ^{*1} | 4 | |
| | IIC | 1 | |
| | SPI | 1 | |
| | CAN | 1 | |
| | USBFS | Yes | |
| | QSPI | Yes | |
| Timers | GPT32 ^{*1} | 2 | |
| | GPT16 ^{*1} | 2 | |
| | AGT ^{*1} | 5 | |
| | RTC | Yes | |
| Analog | ADC12 | 9 | 7 |
| | DAC12 | 1 | |
| Data processing | CRC | Yes | |
| | DOC | Yes | |
| Event control | ELC | Yes | |
| Security | | SCE9 ^{*2} , TrustZone, and Lifecycle management | |
| I/O ports | I/O pins | 43 | 29 |
| | Input pins | 1 | 1 |
| | Pull-up resistors | 44 | 30 |
| | N-ch Open-drain outputs | 43 | 29 |
| | 5-V tolerance | 9 | 4 |

Note 1. Available pins depend on the Pin count, about details see [section 1.7. Pin Lists](#).

Note 2. Only access control circuit, random number generation circuit, and unique ID are supported. The operation of other circuits is not guaranteed.

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

| Function | Signal | I/O | Description |
|------------------------|----------------------------------|--------|--|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1- μ F capacitor. The capacitor should be placed close to the pin. |
| | VCL | I/O | Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VBATT | Input | Battery Backup power pin |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOU and XCIN. |
| | XCOU | Output | |
| | CLKOUT | Output | Clock output pin |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state. |
| System control | RES | Input | Reset signal input pin. The MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Measurement reference clock input pin |
| On-chip emulator | TMS | I/O | On-chip emulator or boundary scan pins |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | SWO | Output | Serial wire trace output pin |
| | SWDIO | I/O | Serial wire debug data input/output pin |
| | SWCLK | Input | Serial wire clock pin |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQn | Input | Maskable interrupt request pins |
| | IRQn-DS | Input | Maskable interrupt request pins that can also be used in Deep Software Standby mode |
| GPT | GTETRG, GTETRGB, GTETRG, GTETRGD | Input | External trigger input pins |
| | GTIOCnA, GTIOCnB | I/O | Input capture, output compare, or PWM output pins |
| AGT | AGTEEn | Input | External event input enable signals |
| | AGTIO | I/O | External event input and pulse output pins |
| | AGTO | Output | Pulse output pins |
| | AGTOAn | Output | Output compare match A output pins |
| | AGTOBn | Output | Output compare match B output pins |
| RTC | RTCOUT | Output | Output pin for 1-Hz or 64-Hz clock |
| | RTICn | Input | Time capture event input pins |

Table 1.14 Pin functions (2 of 3)

| Function | Signal | I/O | Description |
|----------|------------------------------------|--------|---|
| SCI | SCKn | I/O | Input/output pins for the clock (clock synchronous mode) |
| | RXDn | Input | Input pins for received data (asynchronous mode/clock synchronous mode) |
| | TXDn | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode) |
| | CTS _n _RTS _n | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low. |
| | CTS _n | Input | Input for the start of transmission. |
| | SCLn | I/O | Input/output pins for the IIC clock (simple IIC mode) |
| | SDAn | I/O | Input/output pins for the IIC data (simple IIC mode) |
| | SCKn | I/O | Input/output pins for the clock (simple SPI mode) |
| | MISO _n | I/O | Input/output pins for slave transmission of data (simple SPI mode) |
| | MOSI _n | I/O | Input/output pins for master transmission of data (simple SPI mode) |
| | SS _n | Input | Chip-select input pins (simple SPI mode), active-low |
| IIC | SCLn | I/O | Input/output pins for the clock |
| | SDAn | I/O | Input/output pins for data |
| SPI | RSPCKA | I/O | Clock input/output pin |
| | MOSIA | I/O | Input or output pins for data output from the master |
| | MISOA | I/O | Input or output pins for data output from the slave |
| | SSLA0 | I/O | Input or output pin for slave selection |
| | SSLA1 to SSLA3 | Output | Output pins for slave selection |
| CAN | CRX _n | Input | Receive data |
| | CTX _n | Output | Transmit data |
| USBFS | VCC_USB | Input | Power supply pin |
| | VSS_USB | Input | Ground pin |
| | USB_DP | I/O | D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus. |
| | USB_DM | I/O | D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus. |
| | USB_VBUS | Input | USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller. |
| | USB_VBUSEN | Output | VBUS (5 V) supply enable signal for external power supply chip |
| | USB_OVRCURA-DS | Input | Overcurrent pins for USBFS that can also be used in Deep Software Standby mode. Connect the external overcurrent detection signals to these pins. |
| QSPI | QSPCLK | Output | QSPI clock output pin |
| | QSSL | Output | QSPI slave output pin |
| | QIO0 to QIO3 | I/O | Data0 to Data3 |

Table 1.14 Pin functions (3 of 3)

| Function | Signal | I/O | Description |
|---------------------|--------|--------|--|
| Analog power supply | AVCC0 | Input | Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin. |
| | AVSS0 | Input | Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin. |
| | VREFH | Input | Analog reference voltage supply pin for the D/A Converter. Connect this pin to AVCC0 when not using the D/A Converter. |
| | VREFL | Input | Analog reference ground pin for the D/A Converter. Connect this pin to AVSS0 when not using the D/A Converter. |
| | VREFH0 | Input | Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12. |
| | VREFL0 | Input | Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12. |
| ADC12 | ANmn | Input | Input pins for the analog signals to be processed by the A/D converter. (m: ADC unit number, n: pin number) |
| | ADTRGm | Input | Input pins for the external trigger signals that start the A/D conversion, active-low. |
| DAC12 | DAn | Output | Output pins for the analog signals processed by the D/A converter. |
| I/O ports | Pmn | I/O | General-purpose input/output pins (m: port number, n: pin number) |
| | P200 | Input | General-purpose input pin |

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

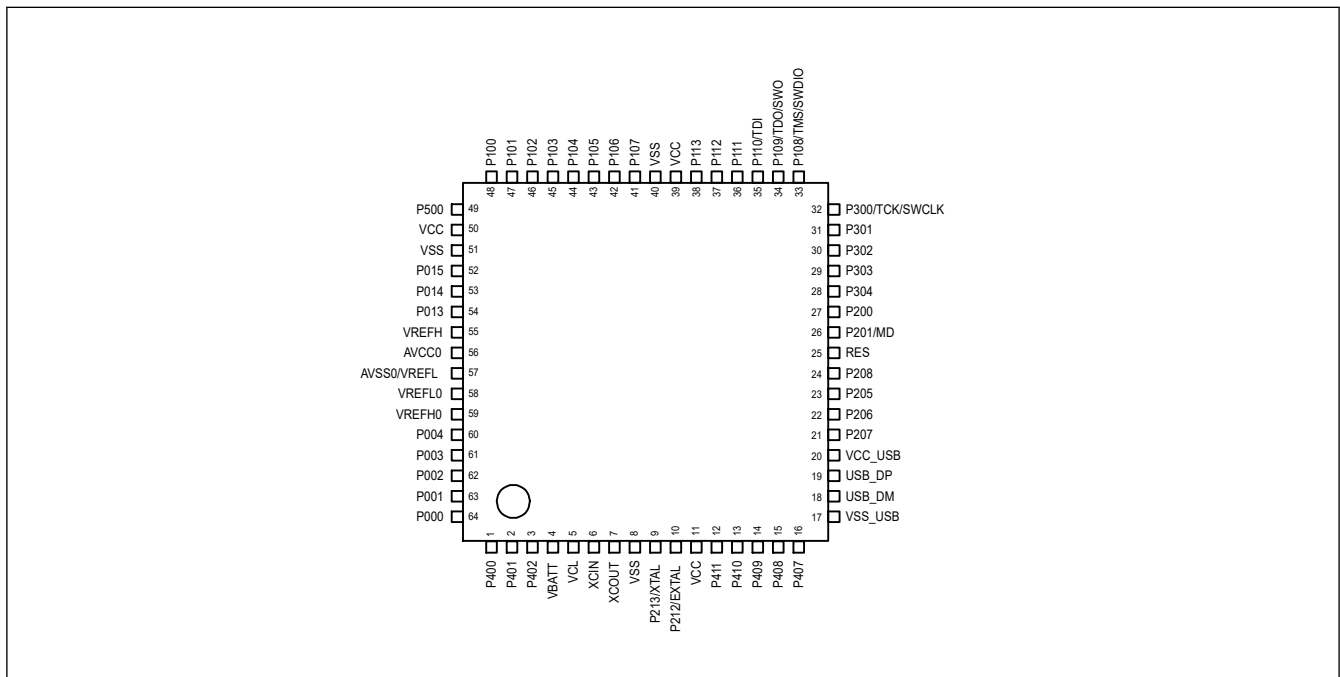
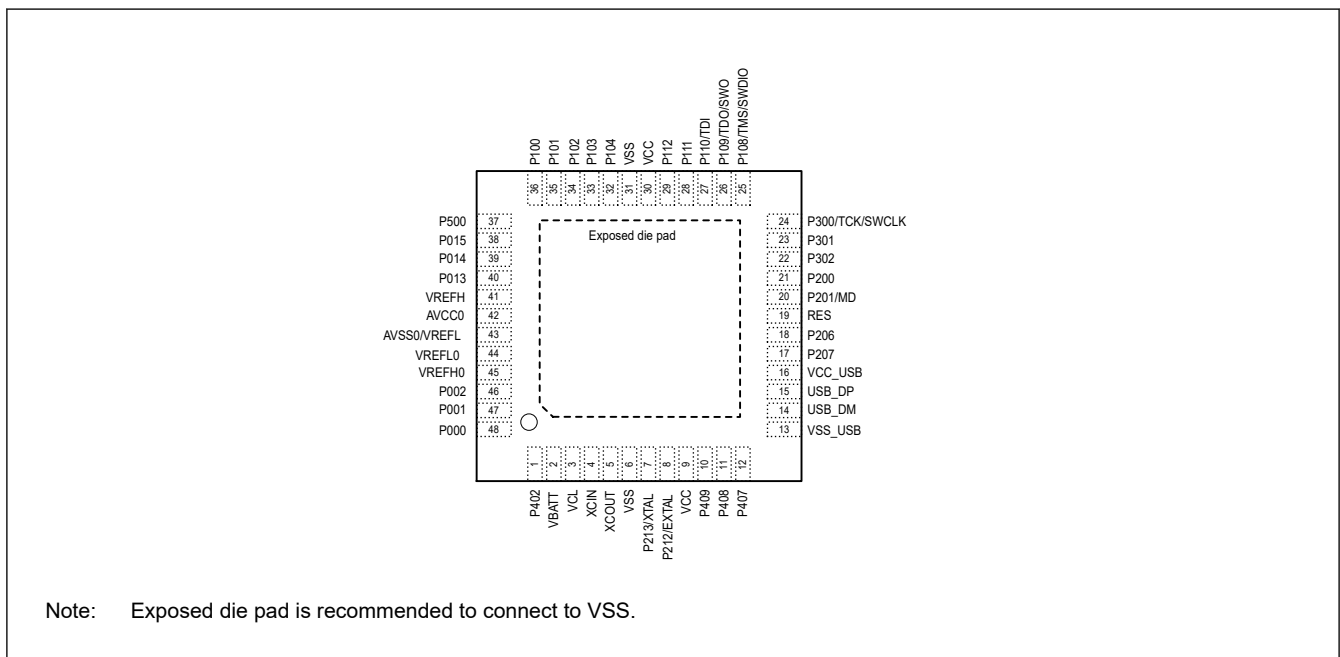


Figure 1.3 Pin assignment for LQFP 64-pin



Note: Exposed die pad is recommended to connect to VSS.

Figure 1.4 Pin assignment for QFN 48-pin

| | A | B | C | D | E | F | G | H | |
|---|--------|-------|------|---------|---------|-------|--------|--------|---|
| 8 | P407 | EXTAL | XTAL | XCOUT | XCIN | VCL0 | VBATT | P000 | 8 |
| 7 | USB_DM | P408 | P409 | P411 | P405 | P401 | P002 | P001 | 7 |
| 6 | USB_DP | P207 | P111 | P410 | P404 | P400 | P004 | P003 | 6 |
| 5 | P205 | P206 | P208 | P113 | P403 | AVSS0 | VREFL0 | VREFH0 | 5 |
| 4 | P200 | P201 | RES | P406 | P402 | AVCC0 | VREFL | VREFH | 4 |
| 3 | P304 | P303 | P302 | P106 | P105 | P104 | P102 | P014 | 3 |
| 2 | P300 | P301 | P110 | VCC_USB | VSS_USB | P103 | P101 | P015 | 2 |
| 1 | P108 | P109 | P112 | VCC | VCL | VSS | P100 | P500 | 1 |
| | A | B | C | D | E | F | G | H | |

Figure 1.5 Pin assignment for BGA 64-pin (top view, pad side down)

1.7 Pin Lists

Table 1.15 Pin list (1 of 2)

| LQFP64 | QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI | GPT/AGT/RTC | ADC12/DAC12 |
|--------|-------|--|--------------|---------------|--|------------------------------------|-------------|
| 1 | — | — | P400 | IRQ0 | SCK4/SCL0_A | AGTIO1 | — |
| 2 | — | — | P401 | IRQ5-DS | CTS4_RTS4/SS4/SDA0_A/CTX0 | GTETRGA | — |
| 3 | 1 | CACREF | P402 | IRQ4-DS | CTS4/CRX0 | AGTIO0/AGTIO1/AGTIO2/AGTIO3/RTCIC0 | — |
| 4 | 2 | VBATT | — | — | — | — | — |
| 5 | 3 | VCL | — | — | — | — | — |
| 6 | 4 | XCIN | — | — | — | — | — |
| 7 | 5 | XCOUT | — | — | — | — | — |
| 8 | 6 | VSS | — | — | — | — | — |
| 9 | 7 | XTAL | P213 | IRQ2 | — | GTETRGC/AGTEE2 | — |
| 10 | 8 | EXTAL | P212 | IRQ3 | — | GTETRGD/AGTEE1 | — |
| 11 | 9 | VCC | — | — | — | — | — |
| 12 | — | — | P411 | IRQ4 | TXD0/MOSI0/SDA0/CTS3_RTS3/SS3 | AGTOA1 | — |
| 13 | — | — | P410 | IRQ5 | RXD0/MISO0/SCL0/SCK3 | AGTOB1 | — |
| 14 | 10 | — | P409 | IRQ6 | TXD3/MOSI3/SDA3 | AGTOA2 | — |
| 15 | 11 | — | P408 | IRQ7 | CTS4/RXD3/MISO3/SCL3/SCL0_B | AGTOB2 | — |
| 16 | 12 | — | P407 | — | CTS4_RTS4/SS4/SDA0_B/USB_VBUS | AGTIO0/RTCOUT | ADTRG0 |
| 17 | 13 | VSS_USB | — | — | — | — | — |
| 18 | 14 | USB_DM | — | — | — | — | — |
| 19 | 15 | USB_DP | — | — | — | — | — |
| 20 | 16 | VCC_USB | — | — | — | — | — |
| 21 | 17 | — | P207 | — | TXD4/MOSI4/SDA4/QSSL | — | — |
| 22 | 18 | — | P206 | IRQ0-DS | RXD4/MISO4/SCL4/CTS9/USB_VBUSEN | — | — |
| 23 | — | CLKOUT | P205 | IRQ1-DS | TXD4/MOSI4/SDA4/CTS9_RTS9/SS9/USB_OVRCURA-DS | GTIOC4A/AGTO1 | — |
| 24 | — | — | P208 | — | QIO3 | — | — |
| 25 | 19 | RES | — | — | — | — | — |
| 26 | 20 | MD | P201 | — | — | — | — |
| 27 | 21 | — | P200 | NMI | — | — | — |
| 28 | — | — | P304 | IRQ9 | — | AGTEE2 | — |
| 29 | — | — | P303 | — | CTS9 | — | — |
| 30 | 22 | — | P302 | IRQ5 | SSLA3 | GTIOC4A | — |
| 31 | 23 | — | P301 | IRQ6 | CTS9_RTS9/SS9/SSLA2 | GTIOC4B/AGTIO0 | — |
| 32 | 24 | TCK/SWCLK | P300 | — | SSLA1 | — | — |
| 33 | 25 | TMS/SWDIO | P108 | — | CTS9_RTS9/SS9/SSLA0 | AGTOA3 | — |
| 34 | 26 | TDO/SWO/CLKOUT | P109 | — | TXD9/MOSI9/SDA9/MOSIA | GTIOC1A/AGTOB3 | — |
| 35 | 27 | TDI | P110 | IRQ3 | RXD9/MISO9/SCL9/MISOA | GTIOC1B/AGTEE3 | — |
| 36 | 28 | — | P111 | IRQ4 | SCK9/RSPCKA | AGTOA5 | — |
| 37 | 29 | — | P112 | — | SSLA0/QSSL | AGTOB5 | — |
| 38 | — | — | P113 | — | — | GTIOC2A/AGTEE5 | — |
| 39 | 30 | VCC | — | — | — | — | — |
| 40 | 31 | VSS | — | — | — | — | — |
| 41 | — | — | P107 | — | — | AGTOA0 | — |
| 42 | — | — | P106 | — | — | AGTOB0 | — |
| 43 | — | — | P105 | IRQ0 | — | GTETRGA/GTIOC1A/AGTO2 | — |
| 44 | 32 | — | P104 | IRQ1 | QIO2 | GTETRGB/GTIOC1B/AGTEE2 | — |
| 45 | 33 | — | P103 | — | CTS0_RTS0/SS0/CTX0/QIO3 | GTIOC2A/AGTIO2 | — |
| 46 | 34 | — | P102 | — | SCK0/CRX0/QIO0 | GTIOC2B/AGTO0 | ADTRG0 |
| 47 | 35 | — | P101 | IRQ1 | TXD0/MOSI0/SDA0/QIO1 | GTETRGB/GTIOC5A/AGTEE0 | — |

Table 1.15 Pin list (2 of 2)

| LQFP64 | QFN48 | Power, System, Clock, Debug, CAC | I/O ports | Ex. Interrupt | SCI/IIC/SPI/CAN/USBFS/QSPI | GPT/AGT/RTC | ADC12/DAC12 |
|--------|-------|----------------------------------|-----------|---------------|----------------------------|------------------------|-------------|
| 48 | 36 | — | P100 | IRQ2 | RXD0/MISO0/SCL0/QSPCLK | GTETRGA/GTIOC5B/AGTIO0 | — |
| 49 | 37 | CACREF | P500 | — | USB_VBUSEN/QSPCLK | AGTOA0 | AN016 |
| 50 | — | VCC | — | — | — | — | — |
| 51 | — | VSS | — | — | — | — | — |
| 52 | 38 | — | P015 | IRQ13 | — | — | AN013 |
| 53 | 39 | — | P014 | — | — | — | AN012/DA0 |
| 54 | 40 | — | P013 | — | — | — | AN011 |
| 55 | 41 | VREFH | — | — | — | — | — |
| 56 | 42 | AVCC0 | — | — | — | — | — |
| 57 | 43 | AVSS0/VREFL | — | — | — | — | — |
| 58 | 44 | VREFL0 | — | — | — | — | — |
| 59 | 45 | VREFH0 | — | — | — | — | — |
| 60 | — | — | P004 | IRQ9-DS | — | — | AN004 |
| 61 | — | — | P003 | — | — | — | AN003 |
| 62 | 46 | — | P002 | IRQ8-DS | — | — | AN002 |
| 63 | 47 | — | P001 | IRQ7-DS | — | — | AN001 |
| 64 | 48 | — | P000 | IRQ6-DS | — | — | AN000 |

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E, and _F. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- $VCC = AVCC0 = VCC_USB = VBATT = 2.7$ to 3.6 V
- $2.7 \leq VREFH0/VREFH \leq AVCC0$
- $VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0$ V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

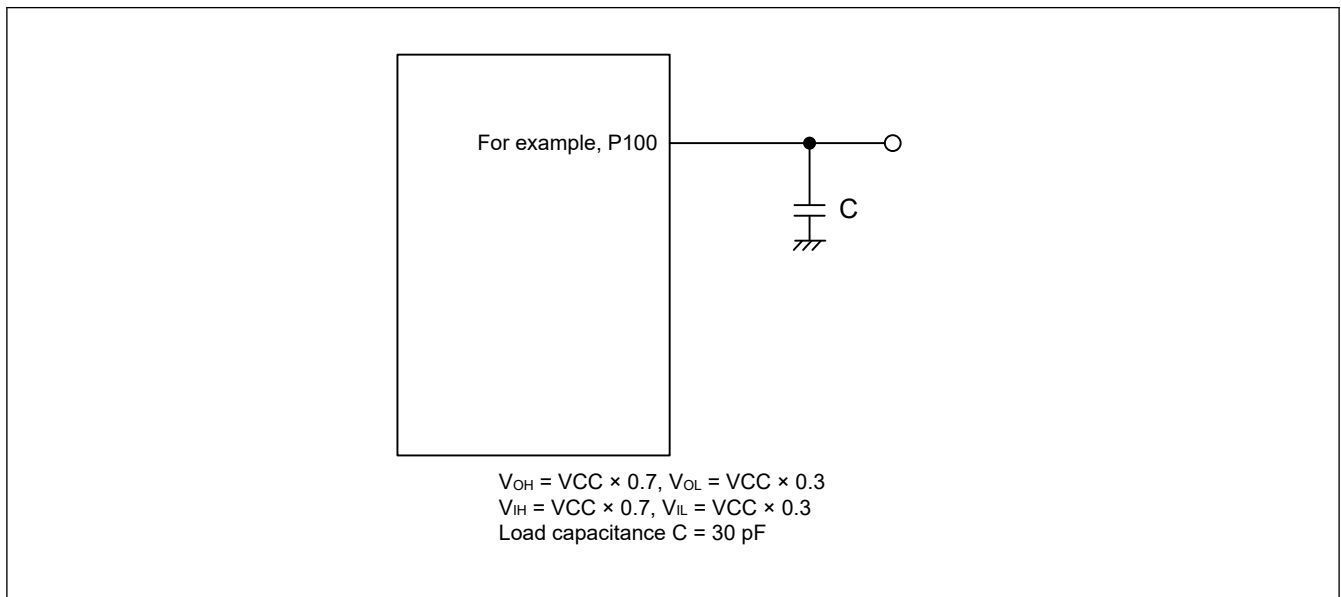


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

| Parameter | Symbol | Value | Unit |
|--|----------------------------|--------------------------------|------|
| Power supply voltage | VCC, VCC_USB ^{*2} | -0.3 to +4.0 | V |
| VBATT power supply voltage | VBATT | -0.3 to +4.0 | V |
| Input voltage (except for 5 V-tolerant ports ^{*1}) | V _{in} | -0.3 to VCC + 0.3 | V |
| Input voltage (5 V-tolerant ports ^{*1}) | V _{in} | -0.3 to + VCC + 4.0 (max. 5.8) | V |
| Reference power supply voltage | VREFH/VREFH0 | -0.3 to VCC + 0.3 | V |
| Analog power supply voltage | AVCC0 ^{*2} | -0.3 to +4.0 | V |
| Analog input voltage | V _{AN} | -0.3 to AVCC0 + 0.3 | V |
| Operating temperature ^{*3 *4} | T _{opr} | -40 to +85 | °C |
| Storage temperature | T _{stg} | -55 to +125 | °C |

Note 1. Ports P205, P206, P400, P401, and P407 to P411 are 5 V tolerant.

Note 2. Connect AVCC0 and VCC_USB to VCC.

Note 3. See [section 2.2.1. T_j/T_a Definition](#).

Note 4. Contact a Renesas Electronics sales office for information on derating operation when T_a = +85°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

| Parameter | Symbol | Value | Min | Typ | Max | Unit |
|------------------------------|---------------------|----------------------|-----|-----|-----|------|
| Power supply voltages | VCC | When USB is not used | 2.7 | — | 3.6 | V |
| | | When USB is used | 3.0 | — | 3.6 | V |
| | VSS | — | 0 | — | V | |
| USB power supply voltages | VCC_USB | — | VCC | — | V | |
| | VSS_USB | — | 0 | — | V | |
| VBATT power supply voltage | VBATT | 1.65 ^{*2} | — | 3.6 | V | |
| Analog power supply voltages | AVCC0 ^{*1} | — | VCC | — | V | |
| | AVSS0 | — | 0 | — | V | |

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

Note 2. Low CL crystal cannot be used below VBATT = 1.8V.

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +85°C

| Parameter | Symbol | Typ | Max | Unit | Test conditions |
|----------------------------------|----------------|-----|-----|------|--|
| Permissible junction temperature | T _j | — | 105 | °C | High-speed mode Low-speed mode Subosc-speed mode |

Note: Make sure that $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$, where total power consumption = $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | |
|---|-------------------------|--|-----------------|-----------|---------------------|---|
| Input voltage (except for Schmitt trigger input pins) | Peripheral function pin | EXTAL (external clock input), SPI (except RSPCK) | V _{IH} | VCC × 0.8 | — | V |
| | | | V _{IL} | — | — | |
| | IIC (SMBus) | V _{IH} | 2.1 | — | VCC + 3.6 (max 5.8) | |
| | | V _{IL} | — | — | 0.8 | |

Table 2.4 I/O V_{IH} , V_{IL} (2 of 2)

| Parameter | | | Symbol | Min | Typ | Max | Unit | | | |
|-------------------------------|-------------------------|-------------------------|--|-------------------------------------|-------------------|-------------------|--------------------------|---|--------------------------|---|
| Schmitt trigger input voltage | Peripheral function pin | IIC (except for SMBus) | | V_{IH} | $VCC \times 0.7$ | — | $VCC + 3.6$ (max 5.8) | V | | |
| | | | | V_{IL} | — | — | $VCC \times 0.3$ | | | |
| | | | | ΔV_T | $VCC \times 0.05$ | — | — | | | |
| | | 5 V-tolerant ports*1 *5 | | V_{IH} | $VCC \times 0.8$ | — | $VCC + 3.6$ (max 5.8) | | | |
| | | | | V_{IL} | — | — | $VCC \times 0.2$ | | | |
| | | | | ΔV_T | $VCC \times 0.05$ | — | — | | | |
| | | RTCIC0 | When using the Battery Backup Function | When VBATT power supply is selected | | V_{IH} | $V_{BATT} \times 0.8$ | | — | $V_{BATT} + 0.3$ |
| | | | | | | V_{IL} | — | | — | $V_{BATT} \times 0.2$ |
| | | | | | | ΔV_T | $V_{BATT} \times 0.05$ | | — | — |
| | | | | When VCC power supply is selected | | V_{IH} | $VCC \times 0.8$ | | — | Higher voltage either $VCC + 0.3$ V or $V_{BATT} + 0.3$ V |
| | | | | | | V_{IL} | — | | — | $VCC \times 0.2$ |
| | | | | | | ΔV_T | $VCC \times 0.05$ | | — | — |
| | | | When not using the Battery Backup Function | | V_{IH} | $VCC \times 0.8$ | — | | $VCC + 0.3$ | |
| | | | | | V_{IL} | — | — | | $VCC \times 0.2$ | |
| | | | | | ΔV_T | $VCC \times 0.05$ | — | | — | |
| | | | Other input pins*2 | | V_{IH} | $VCC \times 0.8$ | — | | — | |
| | | | | | V_{IL} | — | — | | $VCC \times 0.2$ | |
| | | | | | ΔV_T | $VCC \times 0.05$ | — | | — | |
| | | Ports | 5 V-tolerant ports*3 *5 | | V_{IH} | $VCC \times 0.8$ | — | | $VCC + 3.6$ (max 5.8) | V |
| | | | | | V_{IL} | — | — | | $VCC \times 0.2$ | |
| | | | Other input pins*4 | | V_{IH} | $VCC \times 0.8$ | — | | — | |
| V_{IL} | — | | | | — | $VCC \times 0.2$ | | | | |

Note 1. RES and peripheral function pins associated with Ports P205, P206, P400, P401, and P407 to P411 (total 10 pins).

Note 2. All input pins except for the peripheral function pins already described in the table.

Note 3. Ports P205, P206, P400, P401, and P407 to P411 (total 9 pins).

Note 4. All input pins except for the ports already described in the table.

Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O I_{OH} , I_{OL} Table 2.5 I/O I_{OH} , I_{OL}

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|--|---|----------------------------|-----------------------|-----|-----|------|------|
| Permissible output current (average value per pin) | Ports P000 to P004, P013 to P015, P201 | — | I_{OH} | — | — | -2.0 | mA |
| | | | I_{OL} | — | — | 2.0 | mA |
| | Ports P205, P206, P407 to P411 (total 7 pins) | Low drive ^{*1} | I_{OH} | — | — | -2.0 | mA |
| | | | I_{OL} | — | — | 2.0 | mA |
| | | Middle drive ^{*2} | I_{OH} | — | — | -4.0 | mA |
| | | | I_{OL} | — | — | 4.0 | mA |
| | | High drive ^{*3} | I_{OH} | — | — | -20 | mA |
| | | | I_{OL} | — | — | 20 | mA |
| | Other output pins ^{*4} | Low drive ^{*1} | I_{OH} | — | — | -2.0 | mA |
| | | | I_{OL} | — | — | 2.0 | mA |
| | | Middle drive ^{*2} | I_{OH} | — | — | -4.0 | mA |
| | | | I_{OL} | — | — | 4.0 | mA |
| | | High drive ^{*3} | I_{OH} | — | — | -16 | mA |
| | | | I_{OL} | — | — | 16 | mA |
| Permissible output current (max value per pin) | Ports P000 to P004, P013 to P015, P201 | — | I_{OH} | — | — | -4.0 | mA |
| | | | I_{OL} | — | — | 4.0 | mA |
| | Ports P205, P206, P407 to P411 (total 7 pins) | Low drive ^{*1} | I_{OH} | — | — | -4.0 | mA |
| | | | I_{OL} | — | — | 4.0 | mA |
| | | Middle drive ^{*2} | I_{OH} | — | — | -8.0 | mA |
| | | | I_{OL} | — | — | 8.0 | mA |
| | | High drive ^{*3} | I_{OH} | — | — | -40 | mA |
| | | | I_{OL} | — | — | 40 | mA |
| | Other output pins ^{*4} | Low drive ^{*1} | I_{OH} | — | — | -4.0 | mA |
| | | | I_{OL} | — | — | 4.0 | mA |
| | | Middle drive ^{*2} | I_{OH} | — | — | -8.0 | mA |
| | | | I_{OL} | — | — | 8.0 | mA |
| | | High drive ^{*3} | I_{OH} | — | — | -32 | mA |
| | | | I_{OL} | — | — | 32 | mA |
| Permissible output current (maxvalue of total of all pins) | Maximum of all output pins | | $\Sigma I_{OH} (max)$ | — | — | -80 | mA |
| | | | $\Sigma I_{OL} (max)$ | — | — | 80 | mA |

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. Except for P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 μ s.

2.2.4 I/O V_{OH} , V_{OL} , and Other CharacteristicsTable 2.6 I/O V_{OH} , V_{OL} , and other characteristics

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|-------------|-------------|-----|-----|---------------|--|
| Output voltage | IIC | V_{OL} | — | — | 0.4 | V | $I_{OL} = 3.0 \text{ mA}$ |
| | | V_{OL} | — | — | 0.6 | | $I_{OL} = 6.0 \text{ mA}$ |
| | IIC*1 | V_{OL} | — | — | 0.4 | | $I_{OL} = 15.0 \text{ mA}$ (ICFER.FMPE = 1) |
| | | V_{OL} | — | 0.4 | — | | $I_{OL} = 20.0 \text{ mA}$ (ICFER.FMPE = 1) |
| | Ports P205, P206, P407 to P411 (total 7 pins)*2 | V_{OH} | $VCC - 1.0$ | — | — | | $I_{OH} = -20 \text{ mA}$ $VCC = 3.3 \text{ V}$ |
| | | V_{OL} | — | — | 1.0 | | $I_{OL} = 20 \text{ mA}$ $VCC = 3.3 \text{ V}$ |
| | Other output pins | V_{OH} | $VCC - 0.5$ | — | — | | $I_{OH} = -1.0 \text{ mA}$ |
| | | V_{OL} | — | — | 0.5 | | $I_{OL} = 1.0 \text{ mA}$ |
| Input leakage current | RES | $ I_{in} $ | — | — | 5.0 | μA | $V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$ |
| | Port P200 | | — | — | 1.0 | | $V_{in} = 0 \text{ V}$ $V_{in} = VCC$ |
| Three-state leakage current (off state) | 5 V-tolerant ports | $ I_{TSI} $ | — | — | 5.0 | μA | $V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$ |
| | Other ports (except for port P200) | | — | — | 1.0 | | $V_{in} = 0 \text{ V}$ $V_{in} = VCC$ |
| Input pull-up MOS current | Ports P0 to P5 | I_p | -300 | — | -10 | μA | $VCC = 2.7 \text{ to } 3.6 \text{ V}$ $V_{in} = 0 \text{ V}$ |
| Input capacitance | Ports P014, P015 | C_{in} | — | — | 16 | pF | $V_{bias} = 0 \text{ V}$ $V_{amp} = 20 \text{ mV}$ $f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$ |
| | USB_DP and USB_DM | | — | — | 12 | | |
| | Ports P400, P401 | | — | — | 10 | | |
| | Other input pins | | — | — | 8 | | |

Note 1. SCL0_A, SDA0_A (total 2 pins).

Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|--|---|--|--|-------------------|-----------------------|----------------------|---|----|---|
| Supply current ^{*1} | High-speed mode | Maximum ^{*2 *13} | | — | — | 65 | ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz | | |
| | | CoreMark ^{®*5 *6 *12 *14} | | | | | | | |
| | | Normal mode | All peripheral clocks enabled, while (1) code executing from flash ^{*4 *12} | | — | 15.4 | | — | |
| | | | All peripheral clocks disabled, while (1) code executing from flash ^{*5 *6 *12 *14} | | — | 6.1 | | — | |
| | | Sleep mode ^{*5 *14} | | — | 4.4 ^{*6 *12} | 25 ^{*7 *13} | | | |
| | | Increase during BGO operation | Data flash P/E | | — | 6 | | — | |
| | Code flash P/E | | — | 8 | — | | | | |
| | Low-speed mode ^{*5 *10} | | — | 0.8 | — | ICLK = 1 MHz | | | |
| | Subosc-speed mode ^{*5 *11} | | — | 0.7 | — | ICLK = 32.768 kHz | | | |
| | Software Standby mode | | SNZCR.RXDREQEN = 1 | | — | — | 14 | — | |
| | | | SNZCR.RXDREQEN = 0 | | — | 0.7 | — | — | |
| | Deep Software Standby mode | Power supplied to Standby SRAM and USB resume detecting unit | | — | 16 | 96 | μA | — | |
| | | Power not supplied to SRAM or USB resume detecting unit | Power-on reset circuit low power function disabled | | — | 12 | 27 | — | |
| | | | Power-on reset circuit low power function enabled | | — | 5 | 17 | — | |
| | | Increase when the RTC and AGT are operating | When the low-speed on-chip oscillator (LOCO) is in use | | — | 4.4 | — | — | |
| When a crystal oscillator for low clock loads is in use | | | — | 1.0 | — | — | | | |
| When a crystal oscillator for standard clock loads is in use | | | — | 1.6 | — | — | | | |
| RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | | When a crystal oscillator for low clock loads is in use | | — | 0.6 | — | V _{BATT} = 1.8 V, VCC = 0 V | | |
| | | | | — | 1.2 | — | V _{BATT} = 3.3 V, VCC = 0 V | | |
| | | When a crystal oscillator for standard clock loads is in use | | — | 1.1 | — | V _{BATT} = 1.8 V, VCC = 0 V | | |
| | | | | — | 1.8 | — | V _{BATT} = 3.3 V, VCC = 0 V | | |
| Inrush current on returning from Deep Software Standby mode | | Inrush current ^{*8} | | I _{RUSH} | — | 160 | — | mA | |
| | | Energy of inrush current ^{*8} | | E _{RUSH} | — | 1.0 | — | μC | |
| Analog power supply current | During 12-bit A/D conversion | | A _{ICC} | | — | 0.8 | 1.1 | mA | — |
| | During D/A conversion | Without AMP output | | — | 0.1 | 0.2 | mA | — | |
| | | With AMP output | | — | 0.6 | 1.1 | mA | — | |
| | Waiting for A/D, D/A conversion | | — | 0.5 | 1.0 | mA | — | | |
| | ADC12, DAC12 in standby modes ^{*9} | | — | 0.4 | 4.0 | μA | — | | |

Table 2.7 Operating and standby current (2 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions | |
|--|-----------------------------------|---------------------|------------------------|----------------------|------|------|-----------------|---------|
| Reference power supply current (VREFH0) | During 12-bit A/D conversion | I _{AREFH0} | — | 70 | 120 | μA | — | |
| | Waiting for 12-bit A/D conversion | | — | 0.07 | 0.5 | μA | — | |
| | ADC12 in standby modes | | — | 0.07 | 0.5 | μA | — | |
| Reference power supply current (VREFH) | During D/A conversion | Without AMP output | I _{AREFH} | — | 0.1 | 0.4 | mA | — |
| | | With AMP output | | — | 0.1 | 0.4 | mA | — |
| | Waiting for D/A conversion | — | 0.07 | 0.8 | μA | — | | |
| USB operating current | Low speed | USB | I _{CCUSBLS} | — | 3.5 | 6.5 | mA | VCC_USB |
| | Full speed | USB | | I _{CCUSBFS} | — | 4.0 | 10.0 | mA |
| LDO on operating current (per unit) ^{*15} | | | I _{CCLDO} | — | 0.18 | — | mA | — |
| PLL2-LDO operating current | | | I _{CCPLL2LDO} | — | 0.21 | — | mA | — |

- Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
- Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
- Note 3. I_{CC} depends on f (ICLK) as follows.
 I_{CC} Max. = 0.53 × f + 12 (max. operation in high-speed mode)
 I_{CC} Typ. = 0.05 × f + 1.85 (normal operation in high-speed mode, all peripheral clocks disabled)
 I_{CC} Typ. = 0.12 × f + 0.69 (low-speed mode)
 I_{CC} Max. = 0.13 × f + 12 (sleep mode)
- Note 4. This does not include the BGO operation.
- Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
- Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.563 MHz).
- Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).
- Note 8. Reference value
- Note 9. When the MCU is in Software Standby mode or the MSTPCR.DMSTPD16 (12-Bit A/D Converter 0 Module Stop bit) and MSTPCR.DMSTPD20 (12-bit D/A converter module stop bit) are in the module-stop state.
- Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).
- Note 11. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.
- Note 12. PLL output frequency = 100MHz.
- Note 13. PLL output frequency = 200MHz.
- Note 14. PLL2-LDO disabled.
- Note 15. n = 0, 1

Table 2.8 Coremark and normal mode current

| Parameter | | | Symbol | Typ | Unit | Test conditions |
|------------------------------|------------------------------|--|-----------------|-----|--------|---|
| Supply Current ^{*1} | Coremark ^{*2 *3 *4} | | I _{CC} | 81 | μA/MHz | ICLK = 100 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1.56 MHz |
| | Normal mode | All peripheral clocks disabled, cache on, while (1) code executing from flash ^{*2 *3 *4} | | 60 | | |
| | | All peripheral clocks disabled, cache off, while (1) code executing from flash ^{*2 *3 *4} | | 118 | | |

- Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
- Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
- Note 3. PLL output frequency = 100MHz.
- Note 4. PLL2-LDO disabled.

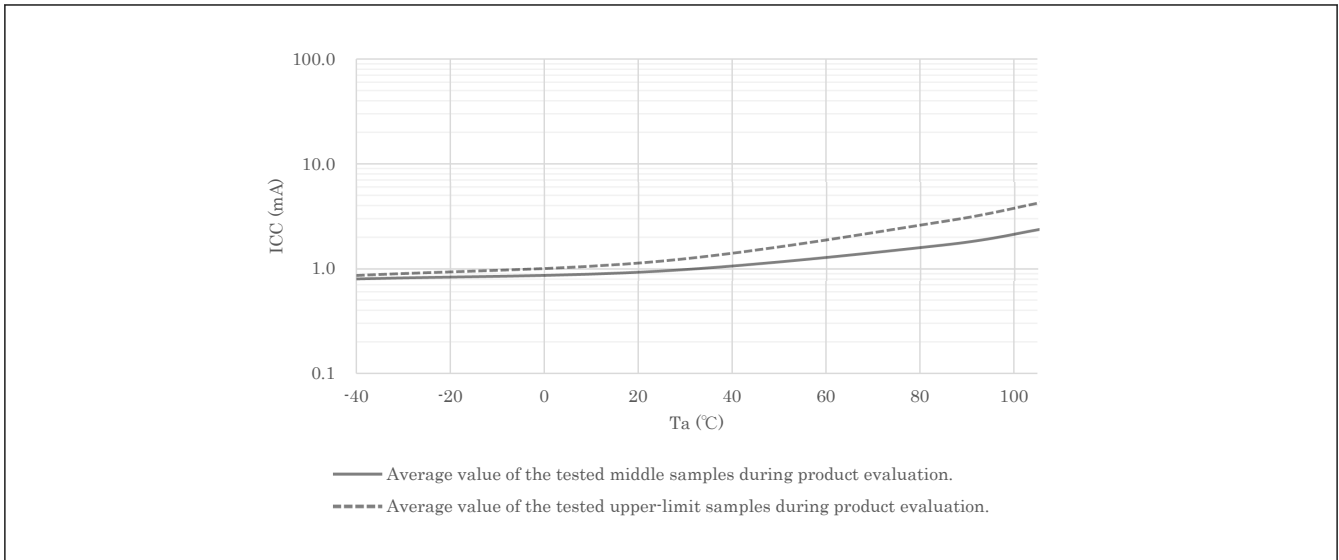


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

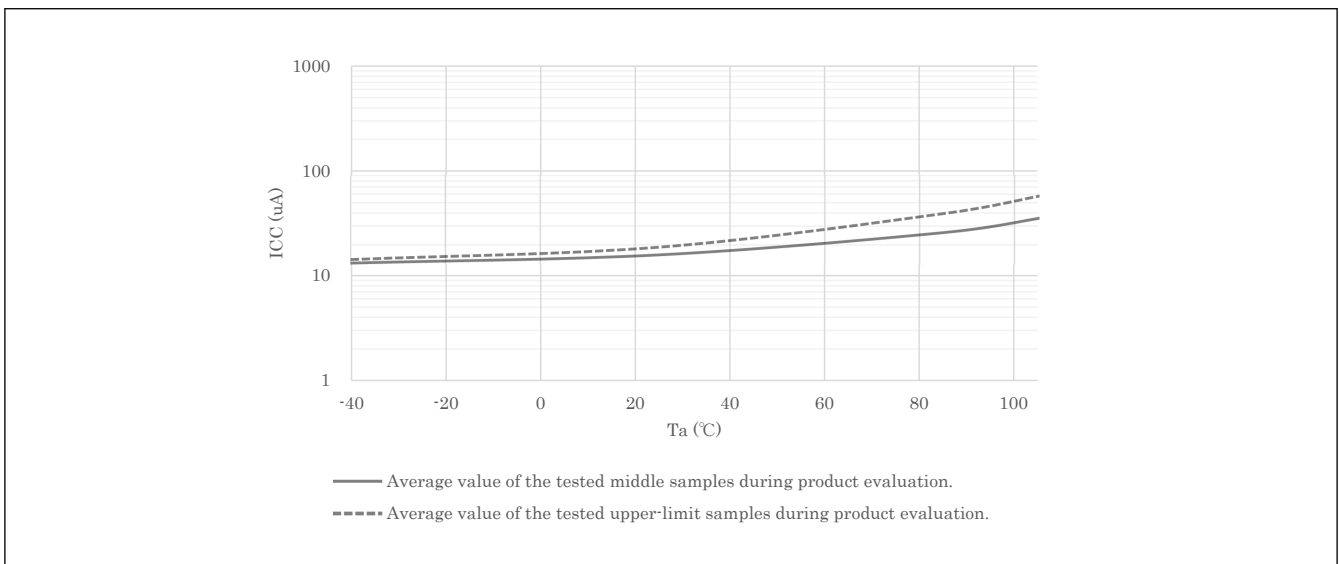


Figure 2.3 Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)

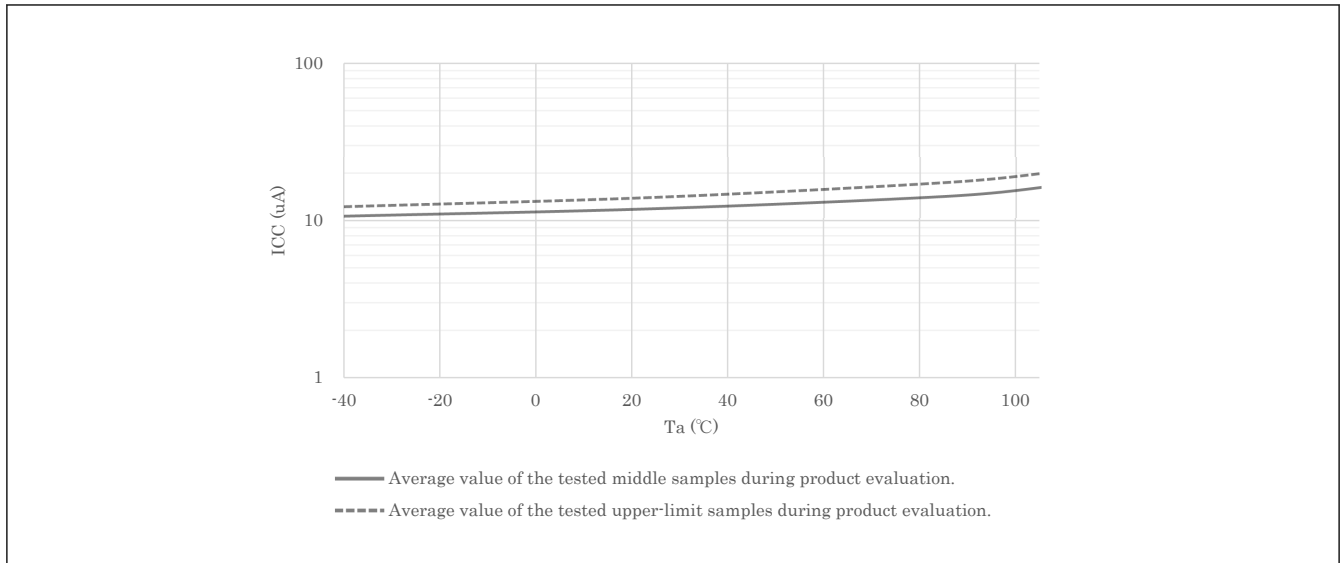


Figure 2.4 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)

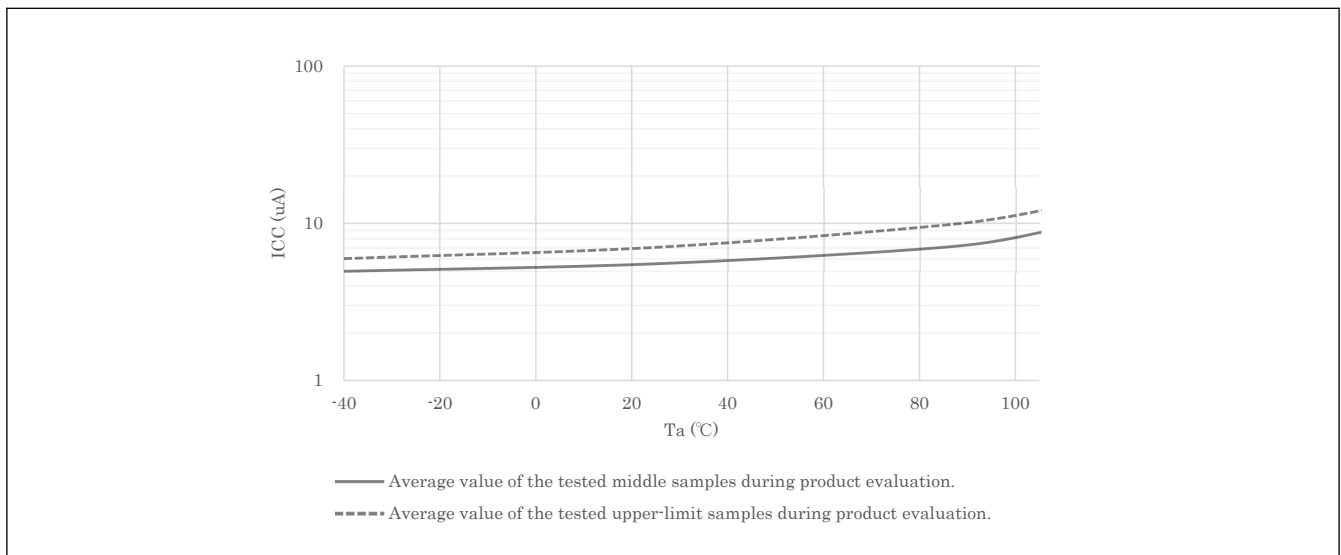


Figure 2.5 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.9 Rise and fall gradient characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------|---|--------|--------|-----|------|-----------------|
| VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC | 0.0084 | — | 20 | ms/V |
| | Voltage monitor 0 reset enabled at startup | | 0.0084 | — | — | |
| | SCI/USB boot mode*1 | | 0.0084 | — | 20 | |
| VCC falling gradient*2 | SfVCC | 0.0084 | — | — | ms/V | — |

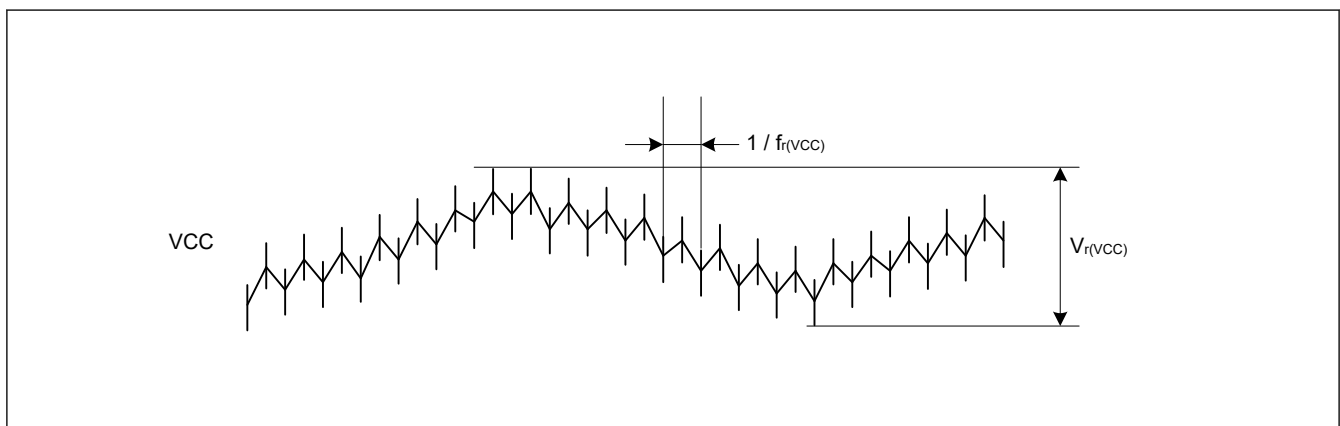
Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Note 2. This applies when VBATT is used.

Table 2.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds $VCC \pm 10\%$, the allowable voltage change rising and falling gradient $dt/dVCC$ must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--------------|-----|-----|-----|------|---|
| Allowable ripple frequency | $f_{r(VCC)}$ | — | — | 10 | kHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.2$ |
| | | — | — | 1 | MHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.08$ |
| | | — | — | 10 | MHz | Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | $dt/dVCC$ | 1.0 | — | — | ms/V | When VCC change exceeds $VCC \pm 10\%$ |

**Figure 2.6 Ripple waveform**

2.2.7 Thermal Characteristics

Maximum value of junction temperature (T_j) must not exceed the value of “[section 2.2.1. \$T_j/T_a\$ Definition](#)”.

T_j is calculated by either of the following equations.

- $T_j = T_a + \theta_{ja} \times \text{Total power consumption}$
- $T_j = T_t + \Psi_{jt} \times \text{Total power consumption}$
 - T_j : Junction Temperature ($^{\circ}\text{C}$)
 - T_a : Ambient Temperature ($^{\circ}\text{C}$)
 - T_t : Top Center Case Temperature ($^{\circ}\text{C}$)
 - θ_{ja} : Thermal Resistance of “Junction”-to-“Ambient” ($^{\circ}\text{C}/\text{W}$)
 - Ψ_{jt} : Thermal Resistance of “Junction”-to-“Top Center Case” ($^{\circ}\text{C}/\text{W}$)
- Total power consumption = Voltage \times (Leakage current + Dynamic current)
- Leakage current of IO = $\Sigma (I_{OL} \times V_{OL}) / \text{Voltage} + \Sigma (|I_{OH}| \times |VCC - V_{OH}|) / \text{Voltage}$
- Dynamic current of IO = $\Sigma IO (C_{in} + C_{load}) \times IO \text{ switching frequency} \times \text{Voltage}$
 - C_{in} : Input capacitance
 - C_{load} : Output capacitance

Regarding θ_{ja} and Ψ_{jt} , refer to [Table 2.11](#).

Table 2.11 Thermal Resistance

| Parameter | Package | Symbol | Value*1 | Unit | Test conditions |
|--------------------|----------------------------|---------------|---------|------|------------------------------|
| Thermal Resistance | 48-pin QFN (PWQN0048KC-A) | θ_{ja} | 23.9 | °C/W | JESD 51-2 and 51-7 compliant |
| | 64-pin LQFP (PLQP0064KB-C) | | 54.6 | | |
| | 48-pin QFN (PWQN0048KC-A) | Ψ_{jt} | 0.28 | °C/W | |
| | 64-pin LQFP (PLQP0064KB-C) | | 1.90 | | |

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.2.7.1 Calculation guide of I_{CCmax}

Table 2.12 shows the power consumption of each unit.

Table 2.12 Power consumption of each unit

| Dynamic current/ Leakage current | MCU Domain | Category | Item | Frequency [MHz] | Current [uA/MHz] | Current*1 [mA] |
|-------------------------------------|-----------------|-------------------------------|--------------------------|-----------------|------------------|----------------|
| Leakage current | Analog | LDO and Leak*2 | Ta = 75 °C*3 | — | — | 7.82 |
| | | | Ta = 85 °C*3 | — | — | 9.13 |
| Dynamic current | CPU | Operation with Flash and SRAM | Coremark | 100 | 55.556 | 5.56 |
| | Peripheral Unit | Timer | GPT16 (2ch)*4 | 100 | 1.788 | 0.18 |
| | | | GPT32 (2ch)*4 | 100 | 2.115 | 0.21 |
| | | | POEG (4 Groups) | 50 | 1.361 | 0.07 |
| | | | AGT (6ch)*4 | 50 | 9.228 | 0.46 |
| | | | RTC | 50 | 4.277 | 0.21 |
| | | | WDT | 50 | 0.764 | 0.04 |
| | | | IWDT | 50 | 0.339 | 0.02 |
| | | | Communication interfaces | USBFS | 50 | 9.385 |
| | | SCI (4ch)*4 | | 100 | 12.477 | 1.25 |
| | | IIC | | 50 | 1.684 | 0.08 |
| | | CAN | | 50 | 1.898 | 0.09 |
| | | SPI | | 100 | 3.024 | 0.30 |
| | | QSPI | | 100 | 2.051 | 0.21 |
| | | Analog | ADC12 | 100 | 2.287 | 0.23 |
| | DAC12 | | 100 | 0.435 | 0.05 | |
| | Event link | ELC | 50 | 0.865 | 0.04 | |
| | Security | SCE9 | 100 | 218.100 | 21.81 | |
| | Data processing | CRC | 100 | 0.600 | 0.06 | |
| | | DOC | 100 | 0.388 | 0.04 | |
| | System | CAC | 50 | 0.844 | 0.04 | |
| | DMA | DMAC | 100 | 4.479 | 0.45 | |
| | | DTC | 100 | 4.274 | 0.43 | |

Note 1. The values are guaranteed by design.

Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.

It is selected according to the temperature of Ta.

Note 3. $\Delta(T_j - T_a) = 20$ °C is considered to measure the current.

Note 4. To determine the current consumption per channel, group or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.13 shows the outline of operation for each unit.

Table 2.13 Outline of operation for each unit

| Peripheral | Outline of operation |
|------------|---|
| GPT | Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD. |
| POEG | Only clear module stop bit. |
| AGT | AGT is operating with PCLKB. |
| RTC | RTC is operating with LOCO. |
| WDT | WDT is operating with PCLKB. |
| IWDT | IWDT is operating with IWDTCLK. |
| USBFS | Transfer types is set to bulk transfer. USBFS is operating using Full-speed transfer (12 Mbps). |
| SCI | SCI is transmitting data in clock synchronous mode. |
| IIC | Communication format is set to I2C-bus format. IIC is transmitting data in master mode. |
| CAN | CAN is transmitting and receiving data in self-test mode 1. |
| SPI | SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data. |
| QSPI | QSPI is issuing Fast Read Quad I/O Instruction. |
| ADC12 | Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode. |
| DAC12 | DAC12 is outputting the conversion result while updating the value of data register. |
| ELC | Only clear module stop bit. |
| SCE9 | SCE9 is executing built-in self test. |
| CRC | CRC is generating CRC code using 32-bit CRC32-C polynomial. |
| DOC | DOC is operating in data addition mode. |
| CAC | Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy. |
| DMAC | Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0. |
| DTC | Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0. |

2.2.7.2 Example of T_j calculation

Assumption :

- Package 64-pin LQFP : $\theta_{ja} = 54.6 \text{ }^\circ\text{C/W}$
- $T_a = 80 \text{ }^\circ\text{C}$
- $I_{CCmax} = 40 \text{ mA}$
- $V_{CC} = 3.5 \text{ V}$ ($V_{CC} = AV_{CC} = V_{CC_USB}$)
- $I_{OH} = 1 \text{ mA}$, $V_{OH} = V_{CC} - 0.5 \text{ V}$, 12 Outputs
- $I_{OL} = 20 \text{ mA}$, $V_{OL} = 1.0 \text{ V}$, 8 Outputs
- $I_{OL} = 1 \text{ mA}$, $V_{OL} = 0.5 \text{ V}$, 12 Outputs
- $C_{in} = 8 \text{ pF}$, 16 pins, Input frequency = 10 MHz
- $C_{load} = 30 \text{ pF}$, 16 pins, Output frequency = 10 MHz

$$\begin{aligned}
 \text{Leakage current of IO} &= \Sigma (V_{OL} \times I_{OL}) / \text{Voltage} + \Sigma ((VCC - V_{OH}) \times I_{OH}) / \text{Voltage} \\
 &= (20 \text{ mA} \times 1 \text{ V}) \times 8 / 3.5 \text{ V} + (1 \text{ mA} \times 0.5 \text{ V}) \times 12 / 3.5 \text{ V} + ((VCC - (VCC - 0.5 \text{ V})) \times 1 \text{ mA}) \times 12 / 3.5 \text{ V} \\
 &= 45.7 \text{ mA} + 1.71 \text{ mA} + 1.71 \text{ mA} \\
 &= 49.1 \text{ mA}
 \end{aligned}$$

$$\begin{aligned}
 \text{Dynamic current of IO} &= \Sigma IO (C_{in} + C_{load}) \times \text{IO switching frequency} \times \text{Voltage} \\
 &= ((8 \text{ pF} \times 16) \times 10 \text{ MHz} + (30 \text{ pF} \times 16) \times 10 \text{ MHz}) \times 3.5 \text{ V} \\
 &= 21.3 \text{ mA}
 \end{aligned}$$

$$\begin{aligned}
 \text{Total power consumption} &= (I_{CCmax} \times \text{Voltage}) + (\text{Leakage current of IO} + \text{Dynamic current of IO}) \times \text{Voltage} \\
 &= (40 \text{ mA} \times 3.5 \text{ V}) + (49.1 \text{ mA} + 21.3 \text{ mA}) \times 3.5 \text{ V} \\
 &= 386 \text{ mW} (0.386 \text{ W})
 \end{aligned}$$

$$\begin{aligned}
 T_j &= T_a + \theta_{ja} \times \text{Total power consumption} \\
 &= 80 \text{ }^\circ\text{C} + 54.6 \text{ }^\circ\text{C/W} \times 0.386 \text{ W} \\
 &= 101.1 \text{ }^\circ\text{C}
 \end{aligned}$$

2.3 AC Characteristics

2.3.1 Frequency

Table 2.14 Operation frequency value in high-speed mode

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------|---------------------------------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK) | — | — | 100 | MHz |
| | Peripheral module clock (PCLKA) | — | — | 100 | |
| | Peripheral module clock (PCLKB) | — | — | 50 | |
| | Peripheral module clock (PCLKC) | —*2 | — | 50 | |
| | Peripheral module clock (PCLKD) | — | — | 100 | |
| | Flash interface clock (FCLK) | —*1 | — | 50 | |

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.

Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.15 Operation frequency value in low-speed mode

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------|------------------------------------|-----|-----|-----|------|
| Operation frequency | System clock (ICLK) | — | — | 1 | MHz |
| | Peripheral module clock (PCLKA) | — | — | 1 | |
| | Peripheral module clock (PCLKB) | — | — | 1 | |
| | Peripheral module clock (PCLKC) *2 | —*2 | — | 1 | |
| | Peripheral module clock (PCLKD) | — | — | 1 | |
| | Flash interface clock (FCLK)*1 | — | — | 1 | |

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.

Note 2. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 2.16 Operation frequency value in Subosc-speed mode

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---------------------|------------------------------------|--------|------|-----|------|------|
| Operation frequency | System clock (ICLK) | f | 29.4 | — | 36.1 | kHz |
| | Peripheral module clock (PCLKA) | | — | — | 36.1 | |
| | Peripheral module clock (PCLKB) | | — | — | 36.1 | |
| | Peripheral module clock (PCLKC) *2 | | — | — | 36.1 | |
| | Peripheral module clock (PCLKD) | | — | — | 36.1 | |
| | Flash interface clock (FCLK) *1 | | 29.4 | — | 36.1 | |

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.

Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.17 Clock timing except for sub-clock oscillator (1 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|-------------|------------------------|---------|--------|---------|---|-----------------|
| EXTAL external clock input cycle time | | t _{EXcyc} | 41.66 | — | — | ns | Figure 2.7 |
| EXTAL external clock input high pulse width | | t _{EXH} | 15.83 | — | — | ns | |
| EXTAL external clock input low pulse width | | t _{EXL} | 15.83 | — | — | ns | |
| EXTAL external clock rise time | | t _{EXr} | — | — | 5.0 | ns | |
| EXTAL external clock fall time | | t _{EXf} | — | — | 5.0 | ns | |
| Main clock oscillator frequency | | f _{MAIN} | 8 | — | 24 | MHz | |
| Main clock oscillation stabilization wait time (crystal) *1 | | t _{MAINOSCWT} | — | — | —*1 | ms | Figure 2.8 |
| LOCO clock oscillation frequency | | f _{LOCO} | 29.4912 | 32.768 | 36.0448 | kHz | — |
| LOCO clock oscillation stabilization wait time | | t _{LOCOWT} | — | — | 60.4 | μs | Figure 2.9 |
| ILOCO clock oscillation frequency | | f _{ILOCO} | 13.5 | 15 | 16.5 | kHz | — |
| MOCO clock oscillation frequency | | f _{MOCO} | 6.8 | 8 | 9.2 | MHz | — |
| MOCO clock oscillation stabilization wait time | | t _{MOCOWT} | — | — | 15.0 | μs | — |
| HOCO clock oscillator oscillation frequency | Without FLL | f _{HOCO16} | 15.78 | 16 | 16.22 | MHz | -20 ≤ Ta ≤ 85°C |
| | | f _{HOCO18} | 17.75 | 18 | 18.25 | | |
| | | f _{HOCO20} | 19.72 | 20 | 20.28 | | |
| | | f _{HOCO16} | 15.71 | 16 | 16.29 | | |
| | | f _{HOCO18} | 17.68 | 18 | 18.32 | | |
| | | f _{HOCO20} | 19.64 | 20 | 20.36 | | |
| | With FLL | f _{HOCO16} | 15.960 | 16 | 16.040 | -40 ≤ Ta ≤ 85°C Sub-clock frequency accuracy is ±50 ppm. | |
| | | f _{HOCO18} | 17.955 | 18 | 18.045 | | |
| | | f _{HOCO20} | 19.950 | 20 | 20.050 | | |
| HOCO clock oscillation stabilization wait time *2 | | t _{HOCOWT} | — | — | 64.7 | μs | — |
| HOCO period jitter | | — | — | ±85 | — | ps | — |
| FLL stabilization wait time | | t _{FLLWT} | — | — | 1.8 | ms | — |
| PLL clock frequency | | f _{PLL} | 100 | — | 200 | MHz | — |
| PLL2 clock frequency | | f _{PLL2} | 120 | — | 240 | MHz | — |
| PLL/PLL2 clock oscillation stabilization wait time | | t _{PLLWT} | — | — | 174.9 | μs | Figure 2.10 |

Table 2.17 Clock timing except for sub-clock oscillator (2 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------|--|-----|-----------|-----------|------|--|
| PLL/PLL2 period jitter | $f_{PLL}, f_{PLL2} \geq 120\text{MHz}$ | — | — | ± 100 | ps | — |
| | $f_{PLL}, f_{PLL2} < 120\text{MHz}$ | — | — | ± 120 | ps | — |
| PLL/PLL2 long term jitter | — | — | ± 300 | — | ps | Term: 1 μs , 10 μs |

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
 After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.18 Clock timing for the sub-clock oscillator

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|----------------|-----|--------|-----|------|-----------------|
| Sub-clock frequency | f_{SUB} | — | 32.768 | — | kHz | — |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | — | — | —*1 | s | Figure 2.11 |

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
 After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

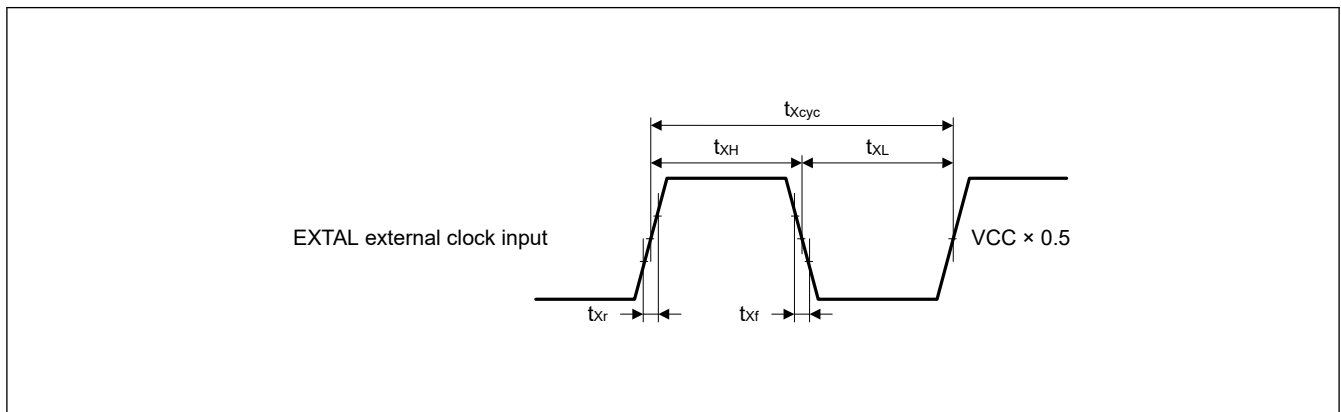


Figure 2.7 EXTAL external clock input timing

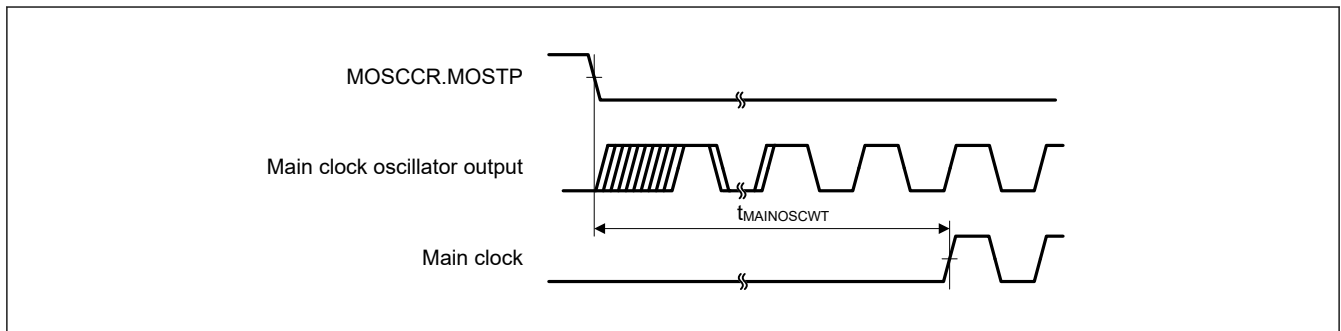


Figure 2.8 Main clock oscillation start timing

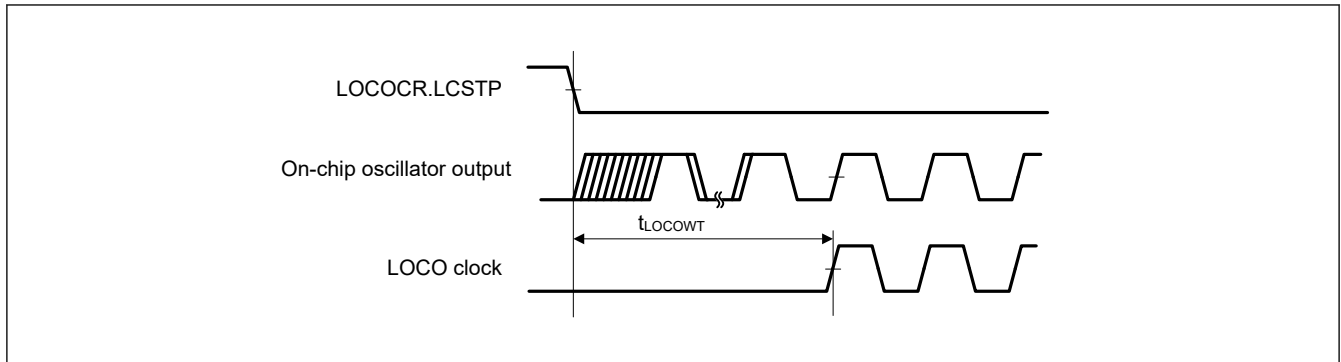


Figure 2.9 LOCO clock oscillation start timing

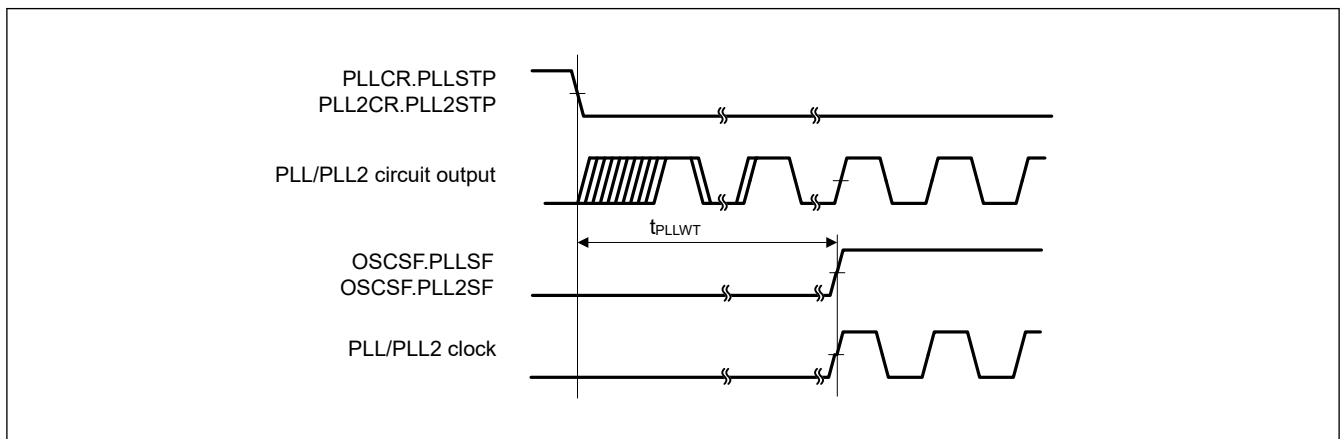


Figure 2.10 PLL/PLL2 clock oscillation start timing

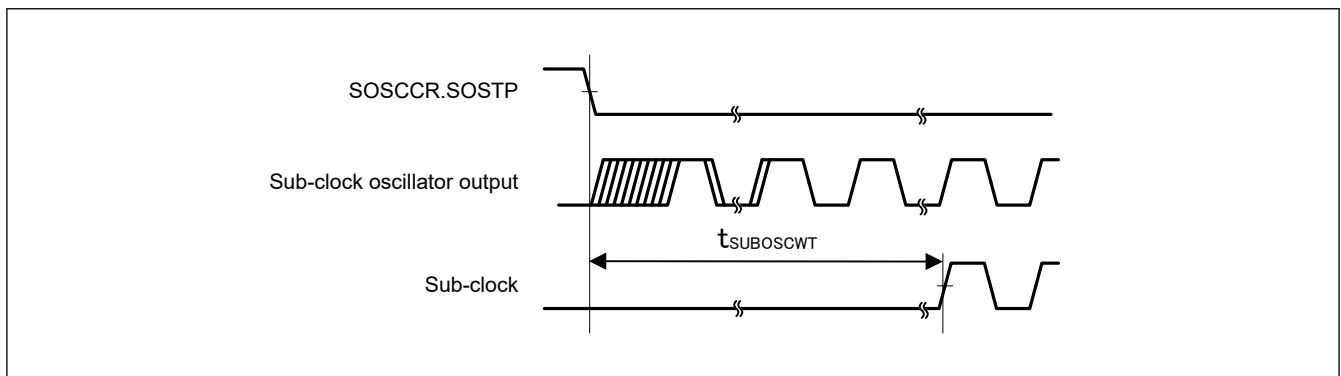


Figure 2.11 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.19 Reset timing (1 of 2)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------------|--|-------------|-----|------|------|---------|-----------------|
| RES pulse width | Power-on | t_{RESWP} | 0.7 | — | — | ms | Figure 2.12 |
| | Deep Software Standby mode | t_{RESWD} | 0.6 | — | — | ms | Figure 2.13 |
| | Software Standby mode, Subosc-speed mode | t_{RESWS} | 0.3 | — | — | ms | |
| | All other | t_{RESW} | 200 | — | — | μ s | |
| Wait time after RES cancellation | | t_{RESWT} | — | 37.3 | 41.2 | μ s | Figure 2.12 |

Table 2.19 Reset timing (2 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|-------------|-----|-----|-------|---------------|-----------------|
| Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, bus master MPU error reset, TrustZone error reset) | t_{RESW2} | — | 324 | 397.7 | μs | — |

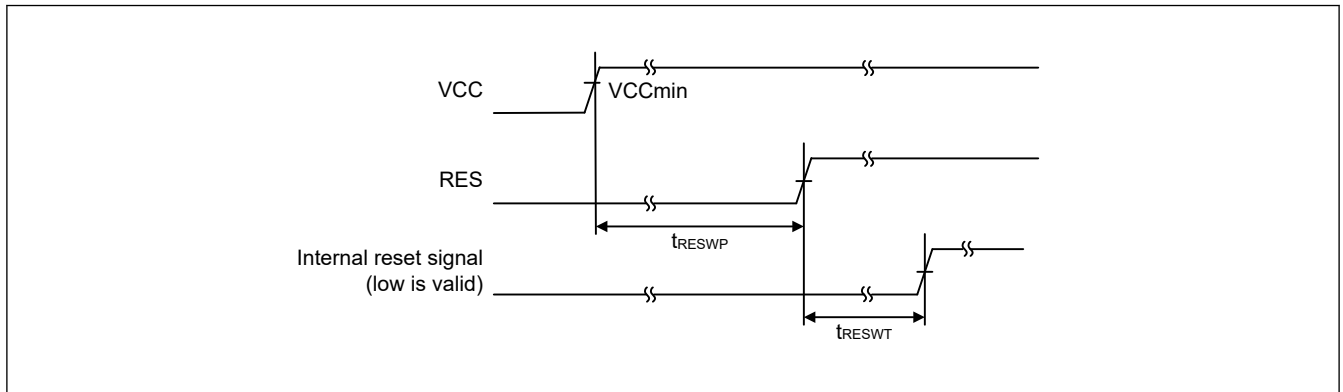


Figure 2.12 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

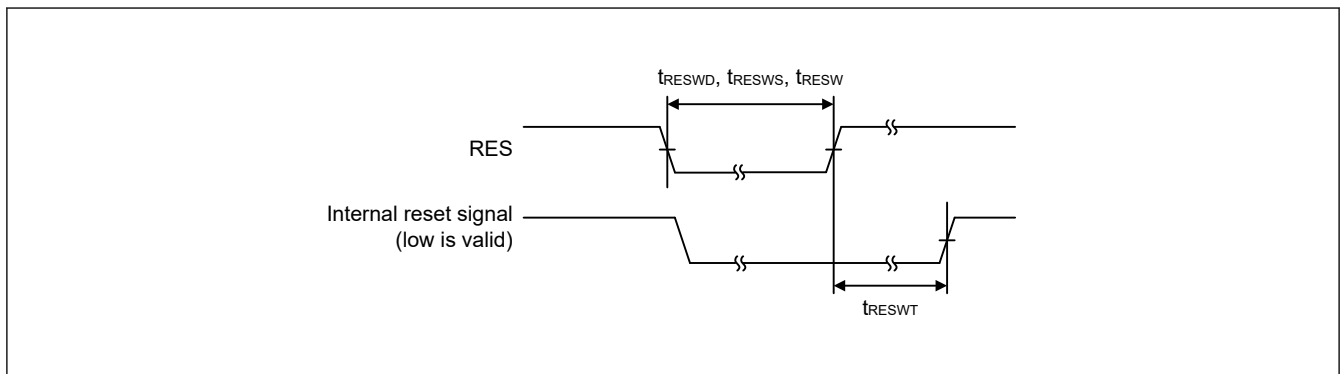


Figure 2.13 Reset input timing

2.3.4 Wakeup Timing

Table 2.20 Timing of recovery from low power modes (1 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | | |
|--|---|---|-------------------|-----|------|-----------------|---------------|--|
| Recovery time from Software Standby mode ^{*1} | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator ^{*2} | t_{SBYMC}^{*13} | — | 2.1 | 2.4 | ms | Figure 2.14 The division ratio of all oscillators is 1. |
| | | System clock source is PLL with main clock oscillator ^{*3} | t_{SBYPC}^{*13} | — | 2.2 | 2.6 | ms | |
| | External clock input to main clock oscillator | System clock source is main clock oscillator ^{*4} | t_{SBYEX}^{*13} | — | 45 | 125 | μs | |
| | | System clock source is PLL with main clock oscillator ^{*5} | t_{SBYPE}^{*13} | — | 170 | 255 | μs | |
| | System clock source is sub-clock oscillator ^{*6 *11} | t_{SBYSC}^{*13} | — | 0.7 | 0.8 | ms | | |
| | System clock source is LOCO ^{*7 *11} | t_{SBYLO}^{*13} | — | 0.7 | 0.9 | ms | | |
| | System clock source is HOCO clock oscillator ^{*8} | t_{SBYHO}^{*13} | — | 55 | 130 | μs | | |
| | System clock source is PLL with HOCO ^{*9} | t_{SBYPH}^{*13} | — | 175 | 265 | μs | | |
| | System clock source is MOCO clock oscillator ^{*10} | t_{SBYMO}^{*13} | — | 35 | 65 | μs | | |

Table 2.20 Timing of recovery from low power modes (2 of 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|--|---|-------------------|-----|-------------------|-------------------|-----------------|-------------|
| Recovery time from Deep Software Standby mode | DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E | t _{DSBY} | — | 0.38 | 0.54 | ms | Figure 2.15 |
| | DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19 | t _{DSBY} | — | 0.55 | 0.73 | ms | |
| Wait time after cancellation of Deep Software Standby mode | t _{DSBYWT} | 56 | — | 57 | t _{cyc} | | |
| Recovery time from Software Standby mode to Snooze mode | High-speed mode when system clock source is HOCO (20 MHz) | t _{SNZ} | — | 35 ^{*12} | 70 ^{*12} | μs | Figure 2.16 |
| | High-speed mode when system clock source is MOCO (8 MHz) | t _{SNZ} | — | 11 ^{*12} | 14 ^{*12} | μs | |

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:

Total recovery time = recovery time for an oscillator as the system clock source + the longest t_{SBYOSCWT} in the active oscillators - t_{SBYOSCWT} for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop)

- Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
- Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
- Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
- Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
- Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
- Note 7. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
- Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
- Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
- Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
- Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
- Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 μs (typical), 48 μs (maximum).
- Note 13. The recovery time can be calculated with the equation of t_{SBYOSCWT} + t_{SBYSEQ}. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

| Wakeup time | TYP | | MAX | | Unit |
|--------------------|-----------------------------|--|-----------------------------|--|------|
| | t _{SBYOSCWT} | t _{SBYSEQ} | t _{SBYOSCWT} | t _{SBYSEQ} | |
| t _{SBYMC} | (MSTS[7:0]*32 + 3) / 0.262 | 35 + 18 / f _{ICLK} + 4n / f _{MAIN} | (MSTS[7:0]*32 + 14) / 0.236 | 62 + 18 / f _{ICLK} + 4n / f _{MAIN} | μs |
| t _{SBYPC} | (MSTS[7:0]*32 + 34) / 0.262 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | (MSTS[7:0]*32 + 45) / 0.236 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYEX} | 10 | 35 + 18 / f _{ICLK} + 4n / f _{EXMAIN} | 62 | 62 + 18 / f _{ICLK} + 4n / f _{EXMAIN} | μs |
| t _{SBYPE} | 135 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | 192 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYSC} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{SUB} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{SUB} | μs |
| t _{SBYLO} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{LOCO} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{LOCO} | μs |
| t _{SBYHO} | 20 | 35 + 18 / f _{ICLK} + 4n / f _{HOCO} | 67 | 62 + 18 / f _{ICLK} + 4n / f _{HOCO} | μs |
| t _{SBYPH} | 140 | 35 + 18 / f _{ICLK} + 4n / f _{PLL} | 202 | 62 + 18 / f _{ICLK} + 4n / f _{PLL} | μs |
| t _{SBYMO} | 0 | 35 + 18 / f _{ICLK} + 4n / f _{MOCO} | 0 | 62 + 18 / f _{ICLK} + 4n / f _{MOCO} | μs |

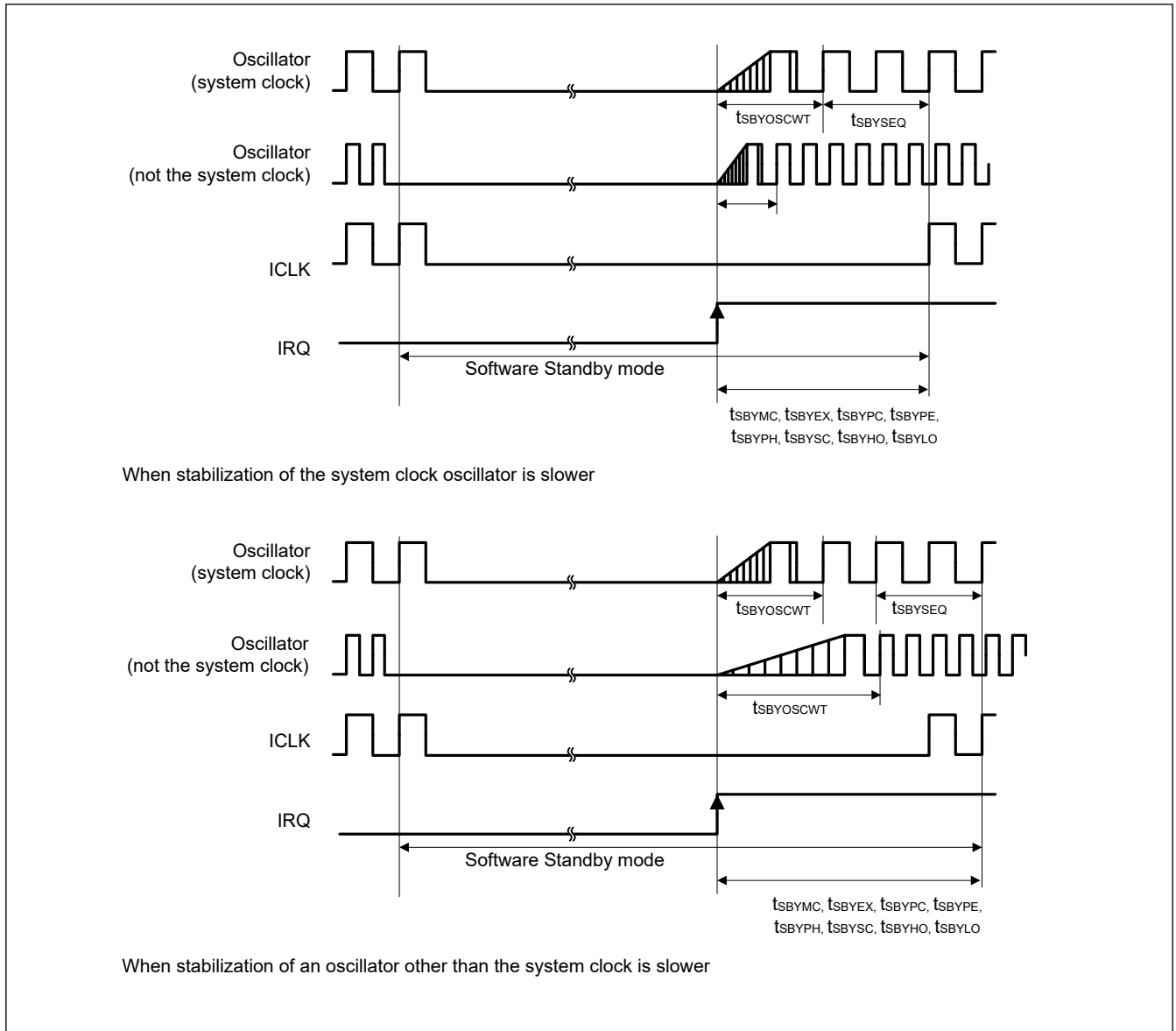


Figure 2.14 Software Standby mode cancellation timing

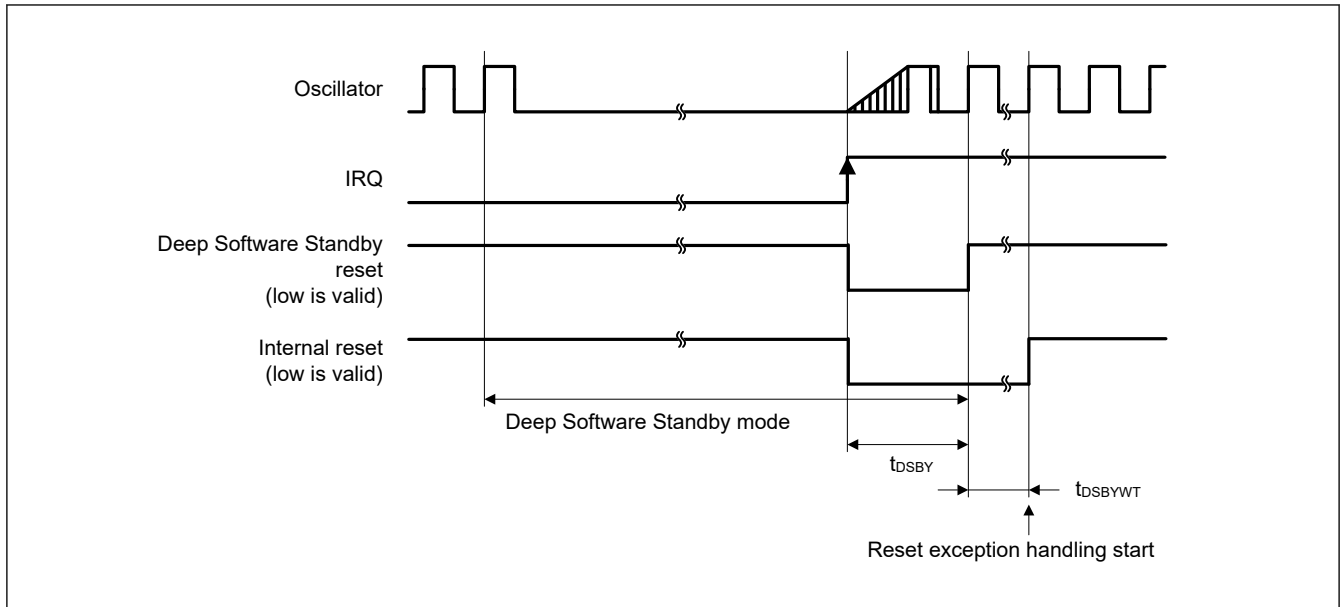
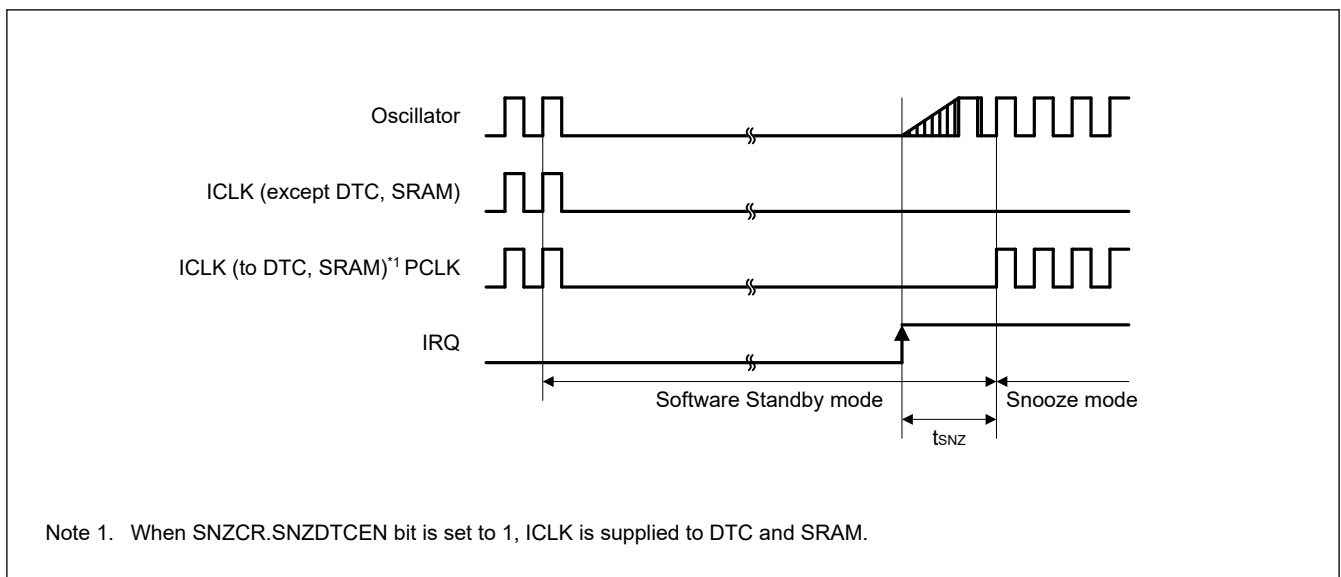


Figure 2.15 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.16 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.21 NMI and IRQ noise filter

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|-----------------|------------|-----------------------------|-----|-----|------|-----------------------------|----------------------------------|
| NMI pulse width | t_{NMIW} | 200 | — | — | ns | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2^{*1}$ | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | NMI digital filter enabled | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5^{*2}$ | — | — | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | t_{IRQW} | 200 | — | — | ns | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2^{*1}$ | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | IRQ digital filter enabled | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5^{*3}$ | — | — | | | $t_{IRQCK} \times 3 > 200$ ns |

- Note: 200 ns minimum in Software Standby mode.
- Note: If the clock source is switched, add 4 clock cycles of the switched source.
- Note 1. t_{Pcyc} indicates the PCLKB cycle.
- Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
- Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

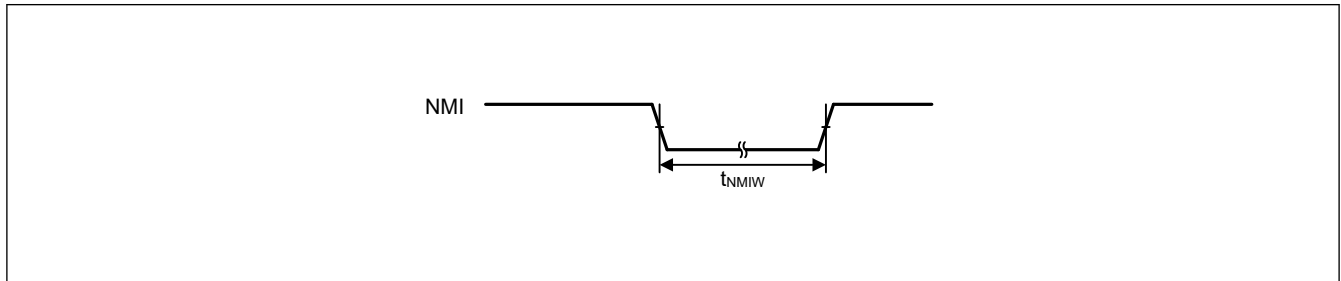


Figure 2.17 NMI interrupt input timing

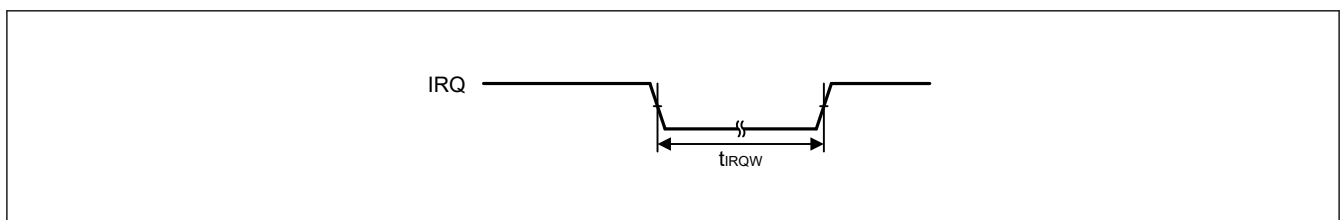


Figure 2.18 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 2.22 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing

GPT32 Conditions:
 High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
 AGT Conditions:
 Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions | | |
|--|--|------------------------|------------------|------|--|---|-----------------------------|
| I/O ports | Input data pulse width | t_{PRW} | 1.5 | — | t_{Pcyc} Figure 2.19 | | |
| POEG | POEG input trigger pulse width | t_{POEW} | 3 | — | t_{Pcyc} Figure 2.20 | | |
| GPT | Input capture pulse width | Single edge | t_{GTICW} | 1.5 | — | t_{PDcyc} Figure 2.21 | |
| | | Dual edge | | 2.5 | — | | |
| | GTIOCxY output skew (x = 1, 2, Y = A or B) | Middle drive buffer | t_{GTISK}^{*1} | — | 4 | ns | Figure 2.22 |
| | | High drive buffer | | — | 4 | | |
| | GTIOCxY output skew (x = 4, 5, Y = A or B) | Middle drive buffer | | — | 4 | | |
| | | High drive buffer | | — | 4 | | |
| GTIOCxY output skew (x = 1, 2, 4, 5, Y = A or B) | Middle drive buffer | — | | 6 | | | |
| | High drive buffer | — | | 6 | | | |
| AGT | AGTIO, AGTEE input cycle | t_{ACYC}^{*2} | 100 | — | ns | Figure 2.23 | |
| | AGTIO, AGTEE input high width, low width | t_{ACKWH}, t_{ACKWL} | 40 | — | ns | | |
| | AGTIO, AGTO, AGTOA, AGTOB output cycle | t_{ACYC2} | 62.5 | — | ns | | |
| ADC12 | ADC12 trigger input pulse width | t_{TRGW} | 1.5 | — | t_{Pcyc} Figure 2.24 | | |

- Note: t_{Pcyc} : PCLKB cycle, t_{PDcyc} : PCLKD cycle.
- Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
- Note 2. Constraints on input cycle:
 When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
 When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

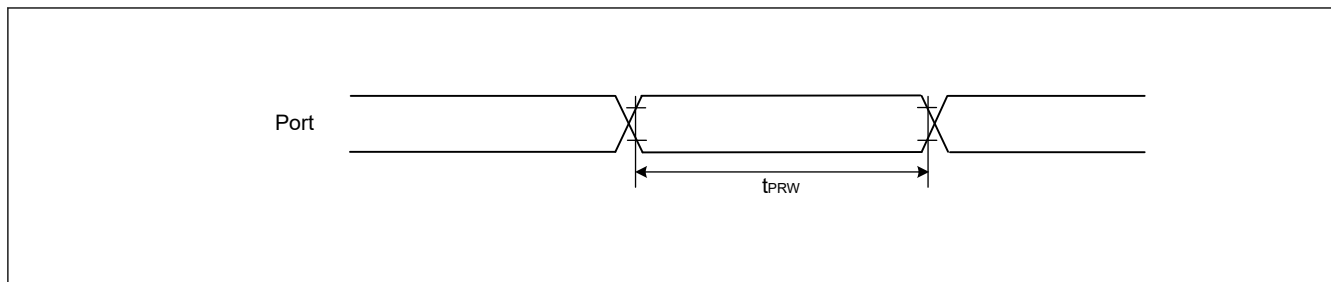


Figure 2.19 I/O ports input timing

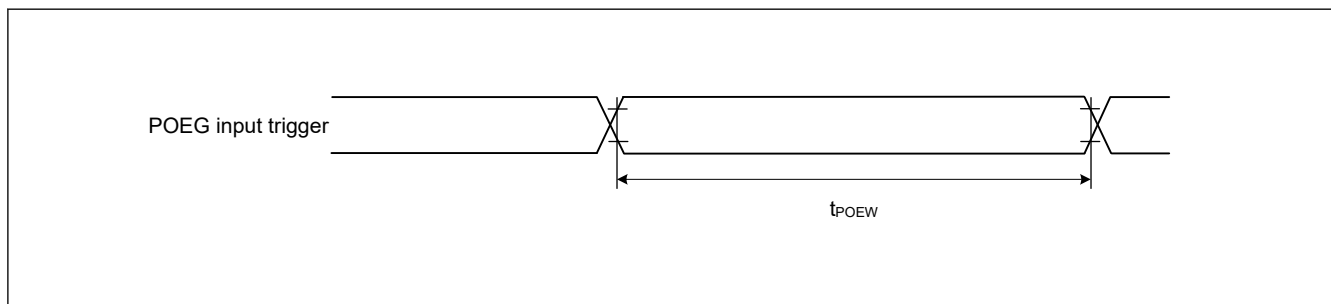


Figure 2.20 POEG input trigger timing

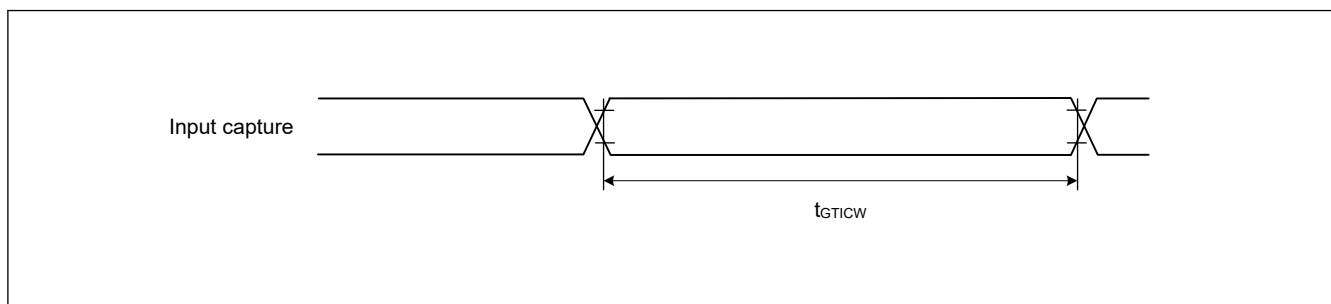


Figure 2.21 GPT input capture timing

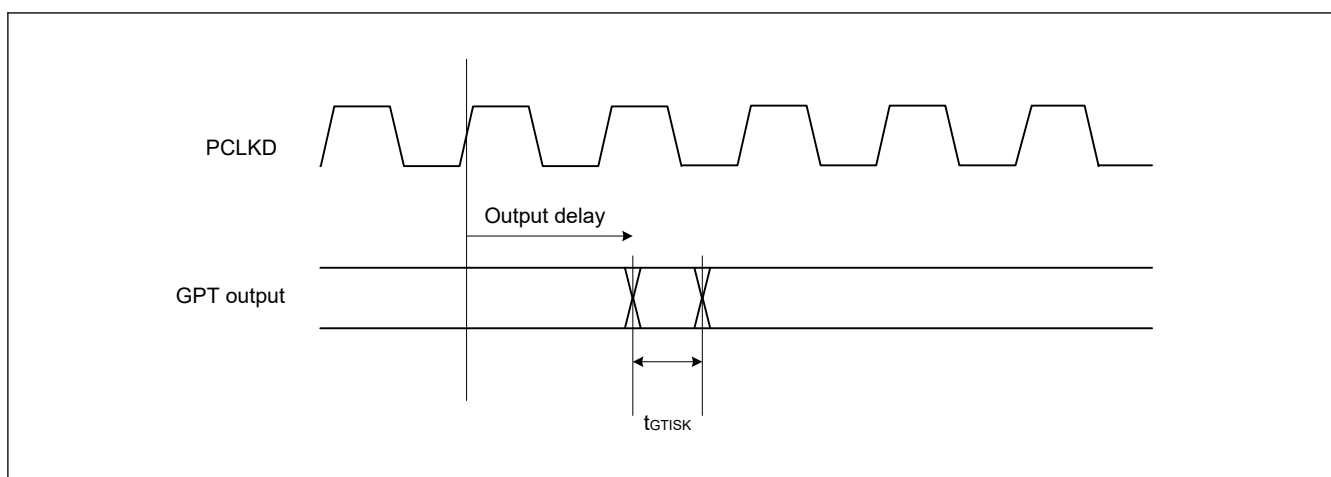


Figure 2.22 GPT output delay skew

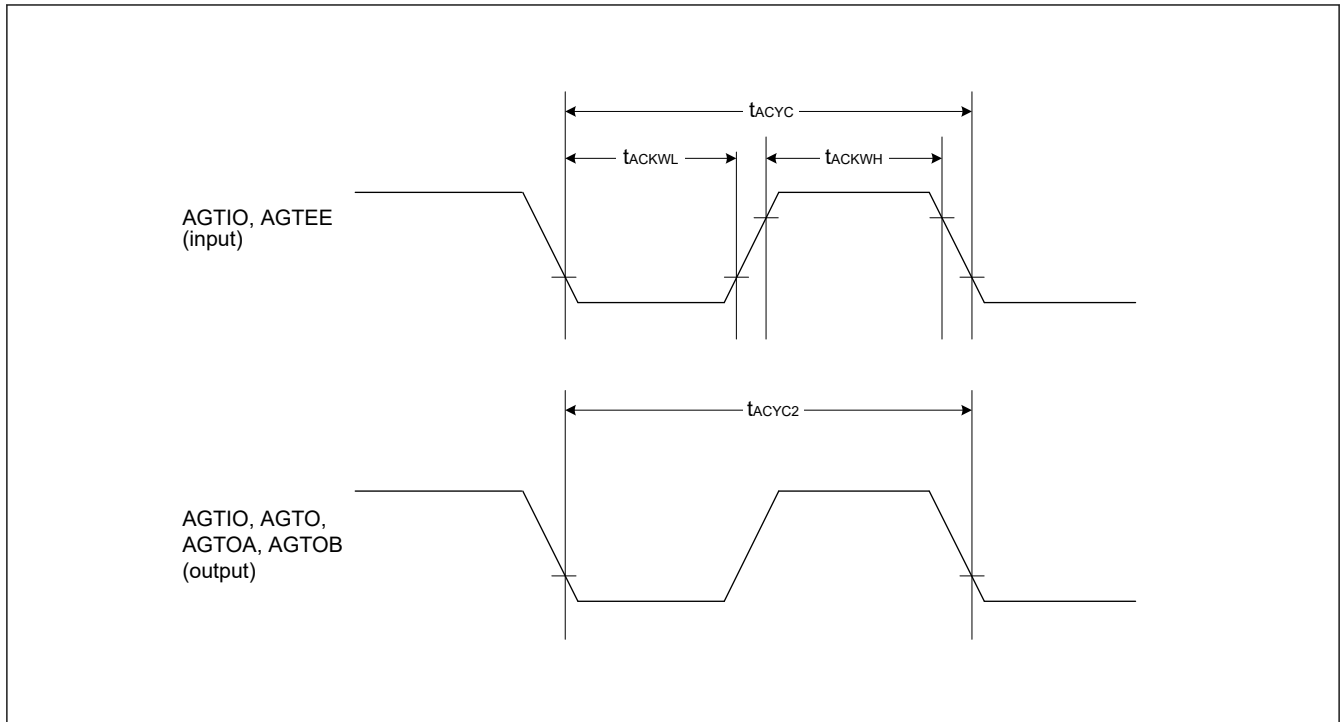


Figure 2.23 AGT input/output timing

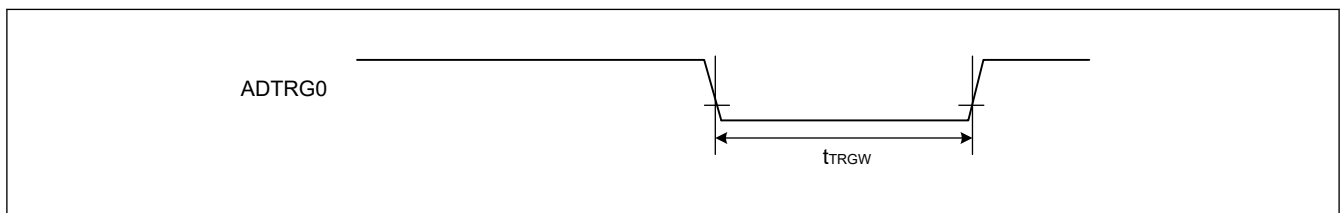


Figure 2.24 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.23 CAC timing

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|-----------|--------------------------|--------------|-------------------------------|---|-----|------|-----------------|
| CAC | CACREF input pulse width | t_{CACREF} | $t_{PBcyc} \leq t_{cac}^{*1}$ | — | — | ns | — |
| | | | $t_{PBcyc} > t_{cac}^{*1}$ | $4.5 \times t_{cac} + 3 \times t_{PBcyc}$ | — | — | |

Note: t_{PBcyc} : PCLKB cycle.

Note 1. t_{cac} : CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.24 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions | |
|-------------------------|--|-------------------|------------|---|------|-----------------|-------------|
| SCI | Input clock cycle | Asynchronous | t_{Scyc} | 4 | — | t_{Pcyc} | Figure 2.25 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | |
| | Input clock rise time | | t_{SCKr} | — | 5 | ns | |
| | Input clock fall time | | t_{SCKf} | — | 5 | ns | |
| | Output clock cycle | Asynchronous | t_{Scyc} | 6 (other than SCI1, SCI2) 8 (SCI1, SCI2) | — | t_{Pcyc} | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | |
| | Output clock rise time | | t_{SCKr} | — | 5 | ns | |
| | Output clock fall time | | t_{SCKf} | — | 5 | ns | |
| Transmit data delay | Clock synchronous master mode (internal clock) | t_{TXD} | — | 5 | ns | Figure 2.26 | |
| | Clock synchronous slave mode (external clock) | t_{TXD} | — | 25 | ns | | |
| Receive data setup time | Clock synchronous master mode (internal clock) | t_{RXS} | 15 | — | ns | | |
| | Clock synchronous slave mode (external clock) | t_{RXS} | 5 | — | ns | | |
| Receive data hold time | Clock synchronous | t_{RXH} | 5 | — | ns | | |

Note: t_{Pcyc} : PCLKA cycle.

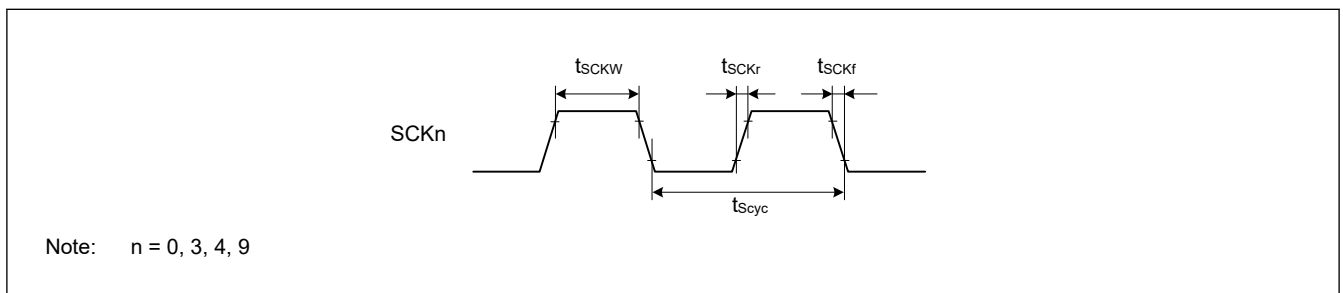


Figure 2.25 SCK clock input/output timing

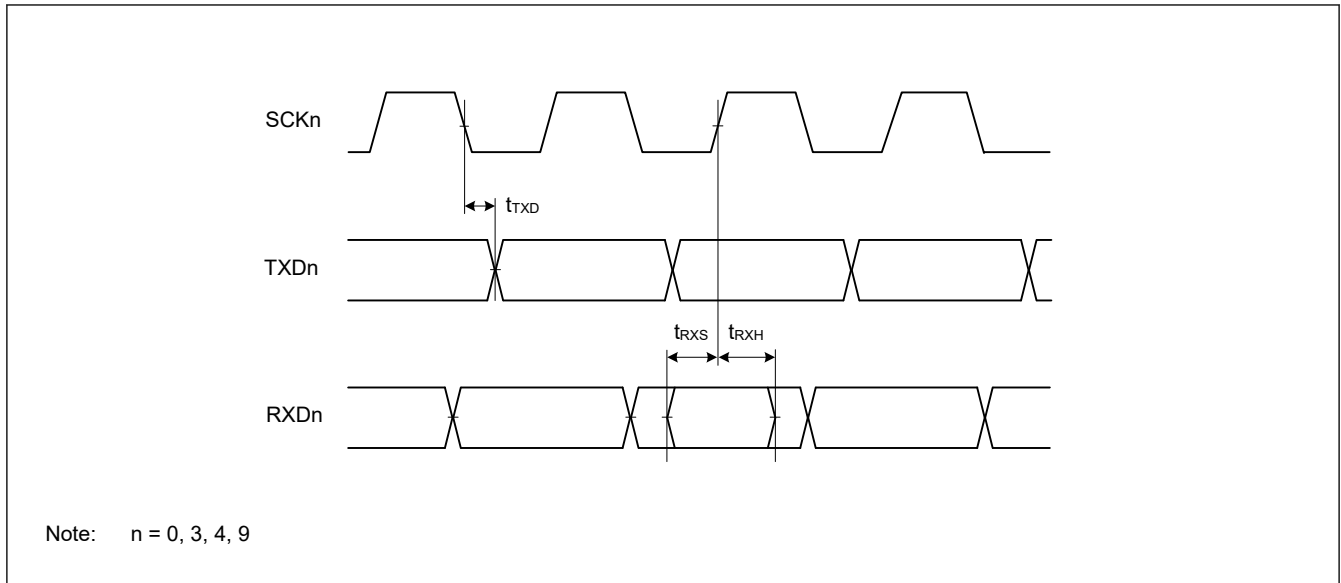


Figure 2.26 SCI input/output timing in clock synchronous mode

Table 2.25 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions | | |
|---------------------------|---------------------------------|------------------------|--------------------------|--------------------------|-------------|-----------------|-------------|----------------------------|
| Simple SPI | SCK clock cycle output (master) | t_{SPCyc} | 4 | 65536 | t_{PCyc} | Figure 2.27 | | |
| | SCK clock cycle input (slave) | | 6 | 65536 | | | | |
| | SCK clock high pulse width | t_{SPCKWH} | 0.4 | 0.6 | t_{SPCyc} | | | |
| | SCK clock low pulse width | t_{SPCKWL} | 0.4 | 0.6 | t_{SPCyc} | | | |
| | SCK clock rise and fall time | t_{SPCKr}, t_{SPCKf} | — | 5 | ns | | | |
| | Data input setup time | master | t_{SU} | 15 | — | | ns | Figure 2.28 to Figure 2.31 |
| | | slave | | 5 | — | | | |
| | Data input hold time | t_H | 5 | — | ns | | | |
| | SS input setup time | t_{LEAD} | 1 | — | t_{SPCyc} | | | |
| | SS input hold time | t_{LAG} | 1 | — | t_{SPCyc} | | | |
| | Data output delay | master | t_{OD} | — | 5 | | ns | |
| | | slave | | — | 25 | | | |
| | Data output hold time | t_{OH} | -5 | — | ns | | | |
| | Data rise and fall time | t_{Dr}, t_{Df} | — | 5 | ns | | | |
| | SS input rise and fall time | t_{SSLr}, t_{SSLf} | — | 5 | ns | | | |
| | Slave access time | t_{SA} | — | $3 \times t_{PCyc} + 25$ | ns | | Figure 2.31 | |
| Slave output release time | t_{REL} | — | $3 \times t_{PCyc} + 25$ | ns | | | | |

Note: t_{PCyc} : PCLKA cycle.

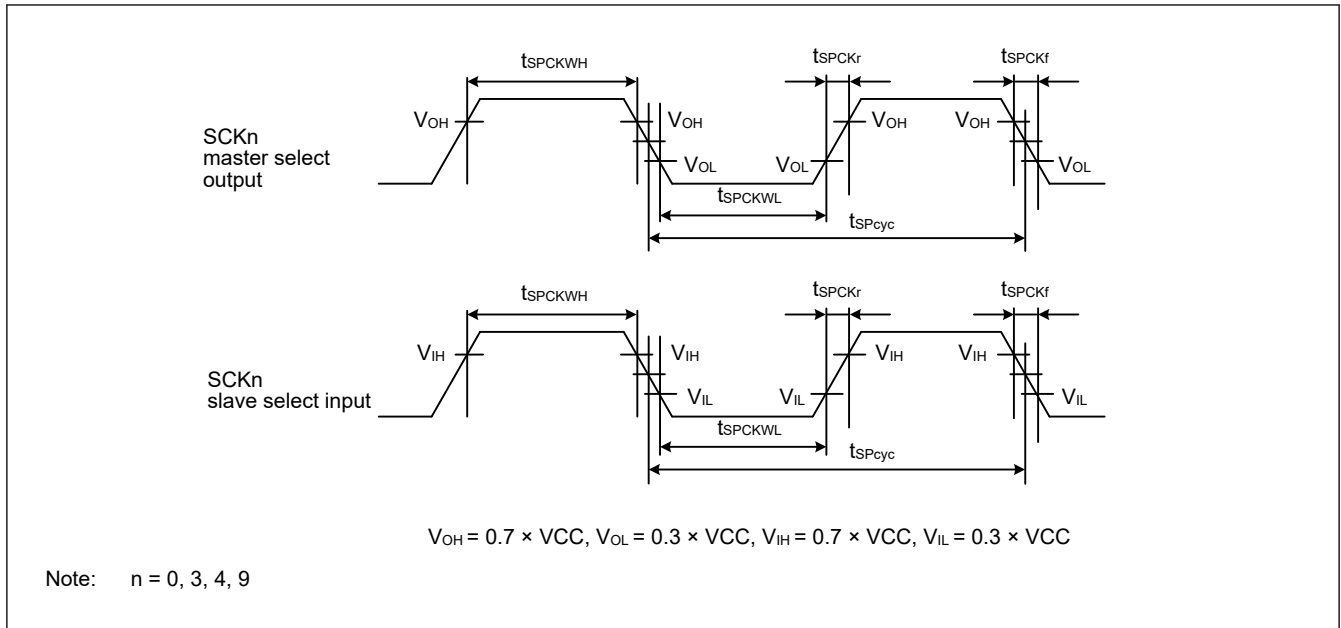


Figure 2.27 SCI simple SPI mode clock timing

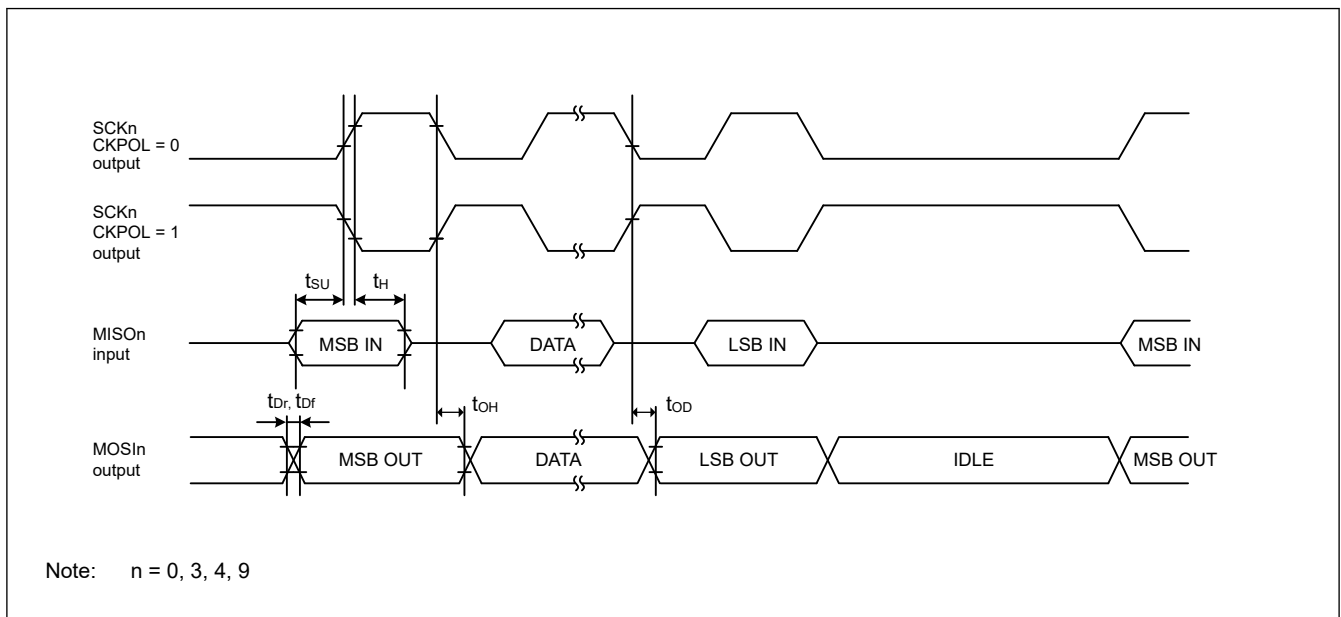


Figure 2.28 SCI simple SPI mode timing for master when CKPH = 1

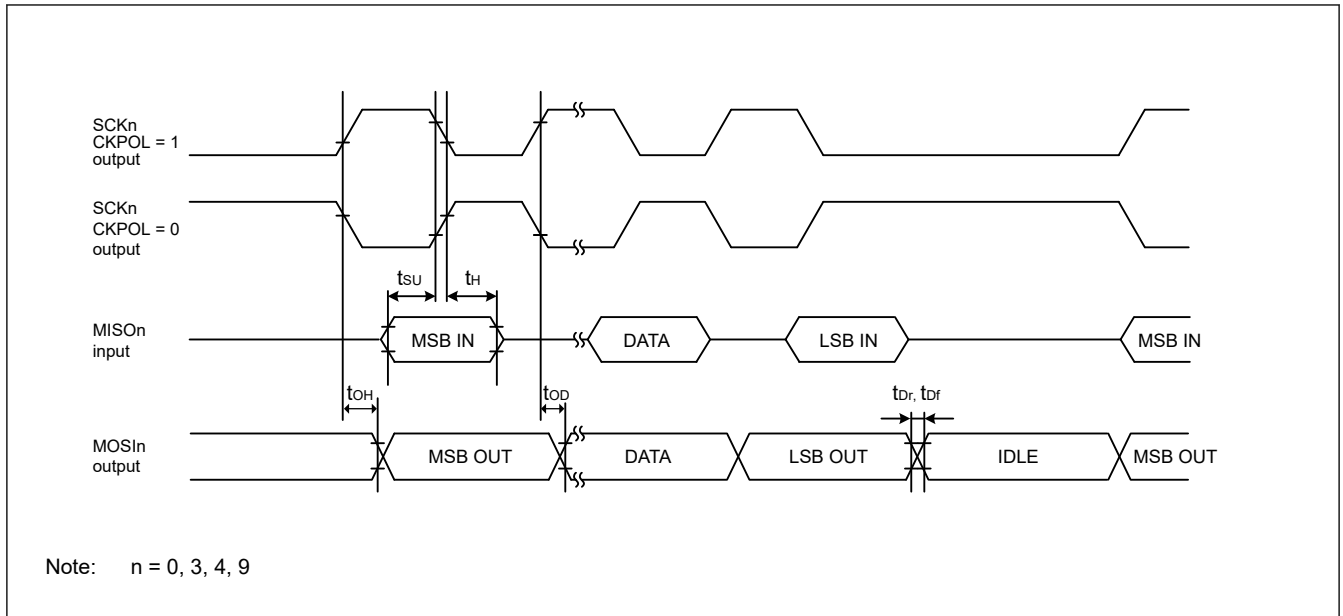


Figure 2.29 SCI simple SPI mode timing for master when CKPH = 0

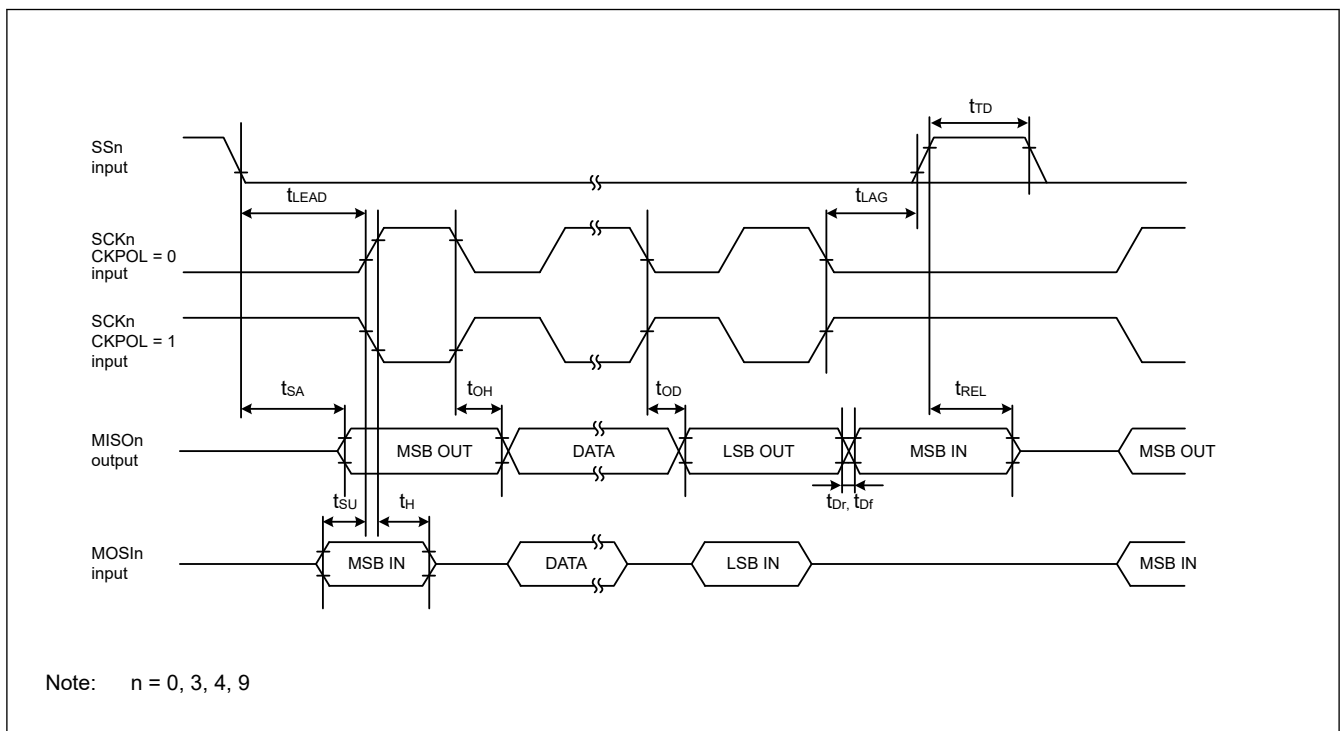


Figure 2.30 SCI simple SPI mode timing for slave when CKPH = 1

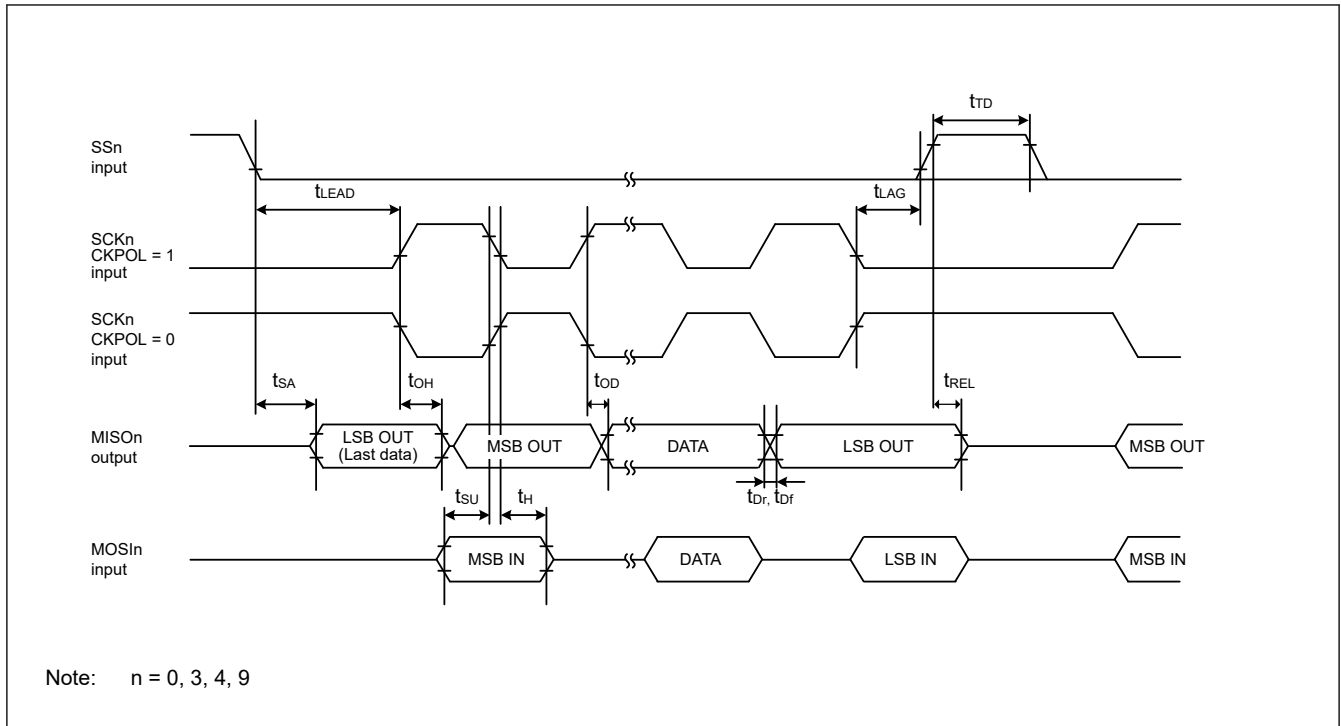


Figure 2.31 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.26 SCI timing (3)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions | |
|----------------------------|------------------------------------|------------|-----|-----------------------|-----------------|-------------|
| Simple IIC (Standard mode) | SDA input rise time | t_{Sr} | — | 1000 | ns | Figure 2.32 |
| | SDA input fall time | t_{Sf} | — | 300 | ns | |
| | SDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{IICcyc}$ | ns | |
| | Data input setup time | t_{SDAS} | 250 | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b^{*1} | — | 400 | pF | |
| Simple IIC (Fast mode) | SDA input rise time | t_{Sr} | — | 300 | ns | Figure 2.32 |
| | SDA input fall time | t_{Sf} | — | 300 | ns | |
| | SDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{IICcyc}$ | ns | |
| | Data input setup time | t_{SDAS} | 100 | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b^{*1} | — | 400 | pF | |

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle.

Note 1. C_b indicates the total capacity of the bus line.

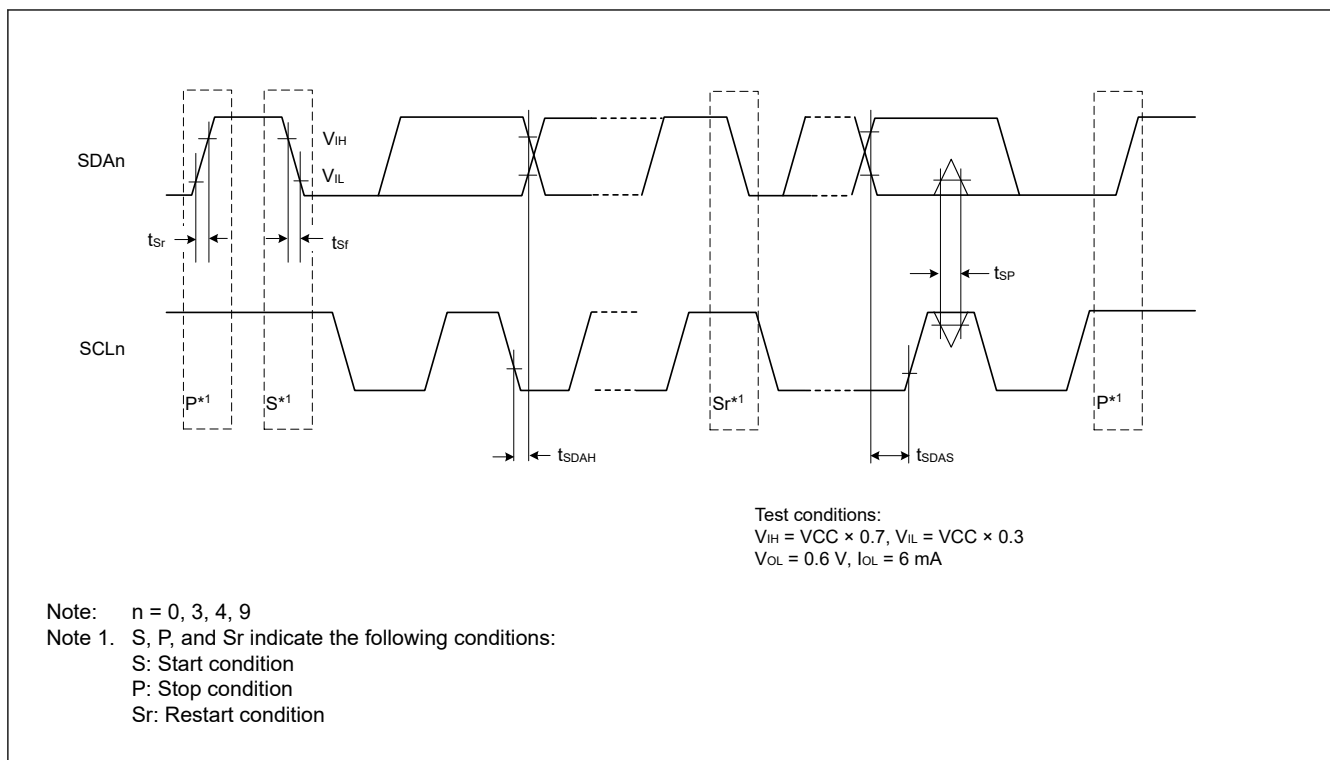


Figure 2.32 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.27 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions | | |
|----------------------------------|--------------------------------|---|---------------------------------|---|---------------------------------|-----------------------------|-------------|----------------------------|
| SPI | RSPCK clock cycle | Master | t_{SPCyc} | 2 | 4096 | t_{Pcyc} | Figure 2.33 | |
| | | Slave | | 4 | 4096 | | | |
| | RSPCK clock high pulse width | Master | t_{SPCKWH} | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | | |
| | | Slave | | 0.4 | 0.6 | t_{SPCyc} | | |
| | RSPCK clock low pulse width | Master | t_{SPCKWL} | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | | |
| | | Slave | | 0.4 | 0.6 | t_{SPCyc} | | |
| | RSPCK clock rise and fall time | Master | t_{SPCKr}, t_{SPCKf} | — | 5 | ns | | |
| | | Slave | | — | 1 | μs | | |
| | Data input setup time | Master | t_{SU} | 4 | — | ns | | Figure 2.34 to Figure 2.39 |
| | | Slave | | 5 | — | | | |
| | Data input hold time | Master (PCLKA division ratio set to 1/2) | t_{HF} | 0 | — | ns | | |
| | | Master (PCLKA division ratio set to a value other than 1/2) | t_H | t_{Pcyc} | — | | | |
| | | Slave | t_H | 20 | — | | | |
| | SSL setup time | Master | t_{LEAD} | $N \times t_{SPCyc} - 10^{*1}$ | $N \times t_{SPCyc} + 100^{*1}$ | ns | | |
| | | Slave | | $4 \times t_{Pcyc}$ | — | ns | | |
| | SSL hold time | Master | t_{LAG} | $N \times t_{SPCyc} - 10^{*2}$ | $N \times t_{SPCyc} + 100^{*2}$ | ns | | |
| Slave | | | $4 \times t_{Pcyc}$ | — | ns | | | |
| Data output delay | Master | t_{OD1} | — | 6.3 | ns | | | |
| | | t_{OD2} | — | 6.3 | | | | |
| | Slave | t_{OD} | — | 20 | | | | |
| Data output hold time | Master | t_{OH} | 0 | — | ns | | | |
| | Slave | | 0 | — | | | | |
| Successive transmission delay | Master | t_{TD} | $t_{SPCyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPCyc} + 2 \times t_{Pcyc}$ | ns | | | |
| | Slave | | $4 \times t_{Pcyc}$ | | | | | |
| MOSI and MISO rise and fall time | Output | t_{Dr}, t_{Df} | — | 5 | ns | | | |
| | Input | | — | 1 | | μs | | |
| SSL rise and fall time | Output | t_{SSLr}, t_{SSLf} | — | 5 | ns | | | |
| | Input | | — | 1 | | μs | | |
| Slave access time | | t_{SA} | — | 25 | ns | Figure 2.38 and Figure 2.39 | | |
| Slave output release time | | t_{REL} | — | 25 | | | | |

Note: t_{Pcyc} : PCLKA cycle.

Note: Must use pins that have a letter appended to their name, for instance “_A”, “_B”, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.

Note 1. N is set to an integer from 1 to 8 by the SPCKD register.

Note 2. N is set to an integer from 1 to 8 by the SSLND register.

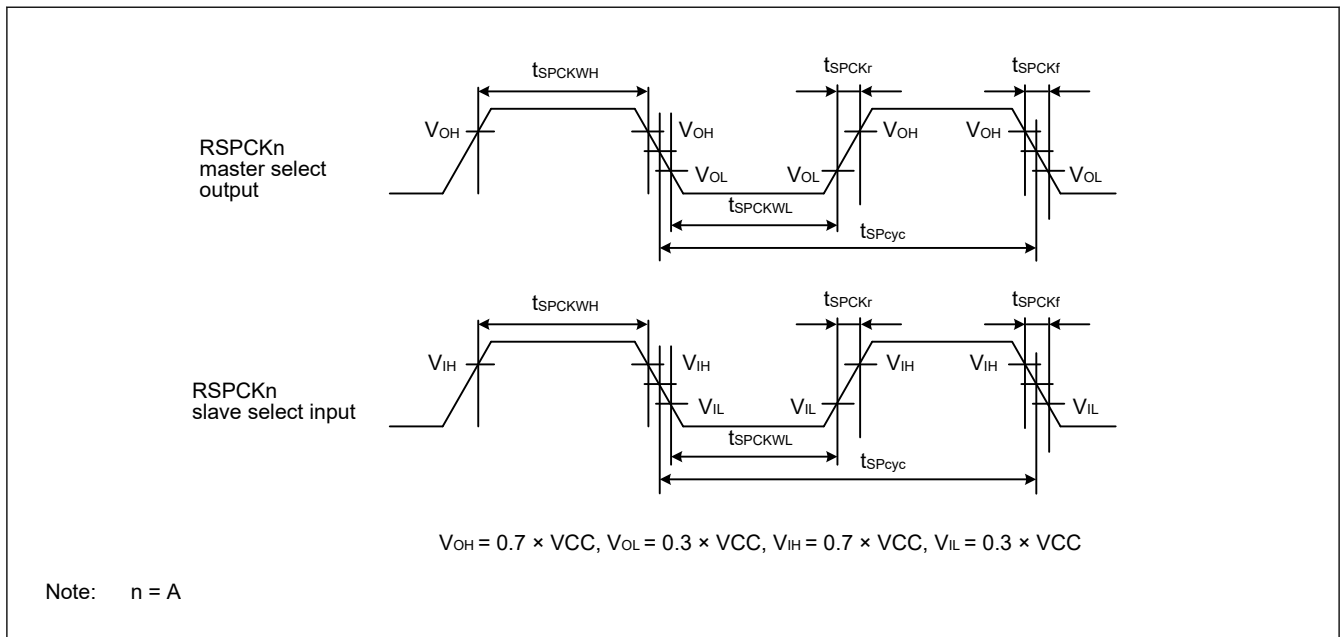


Figure 2.33 SPI clock timing

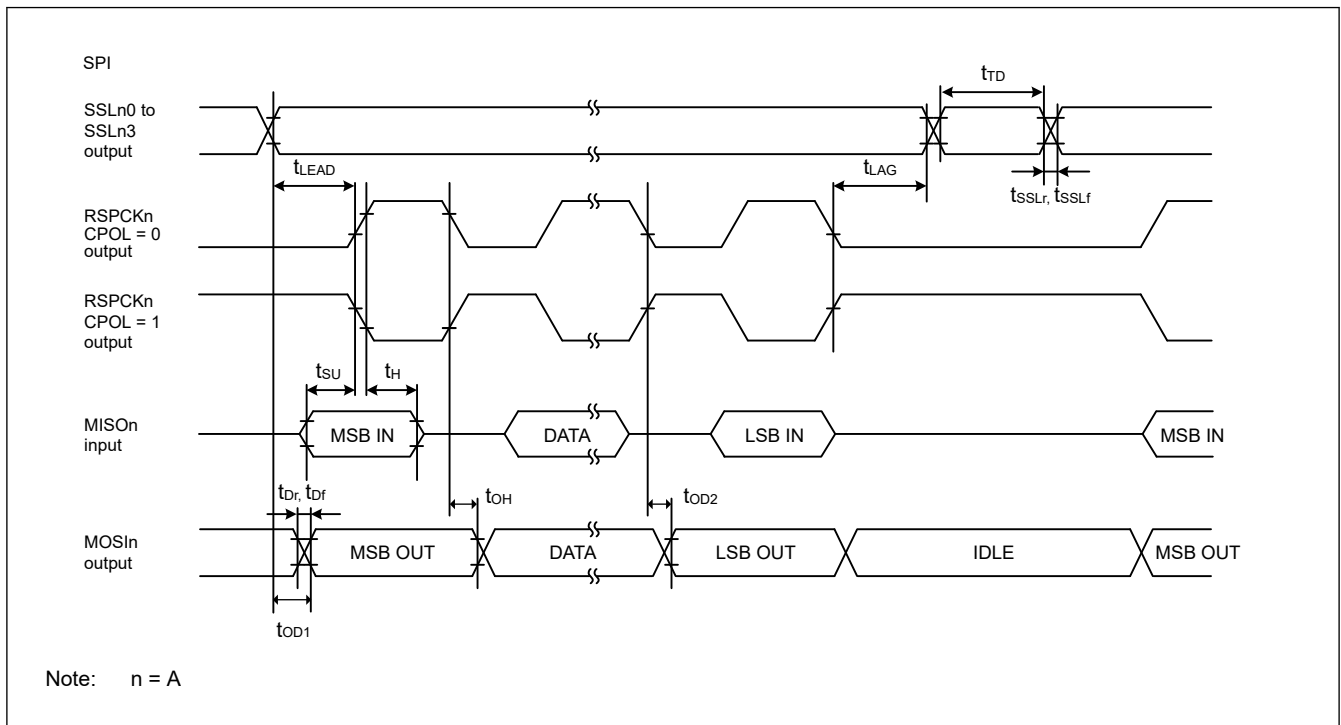


Figure 2.34 SPI timing for master when CPHA = 0

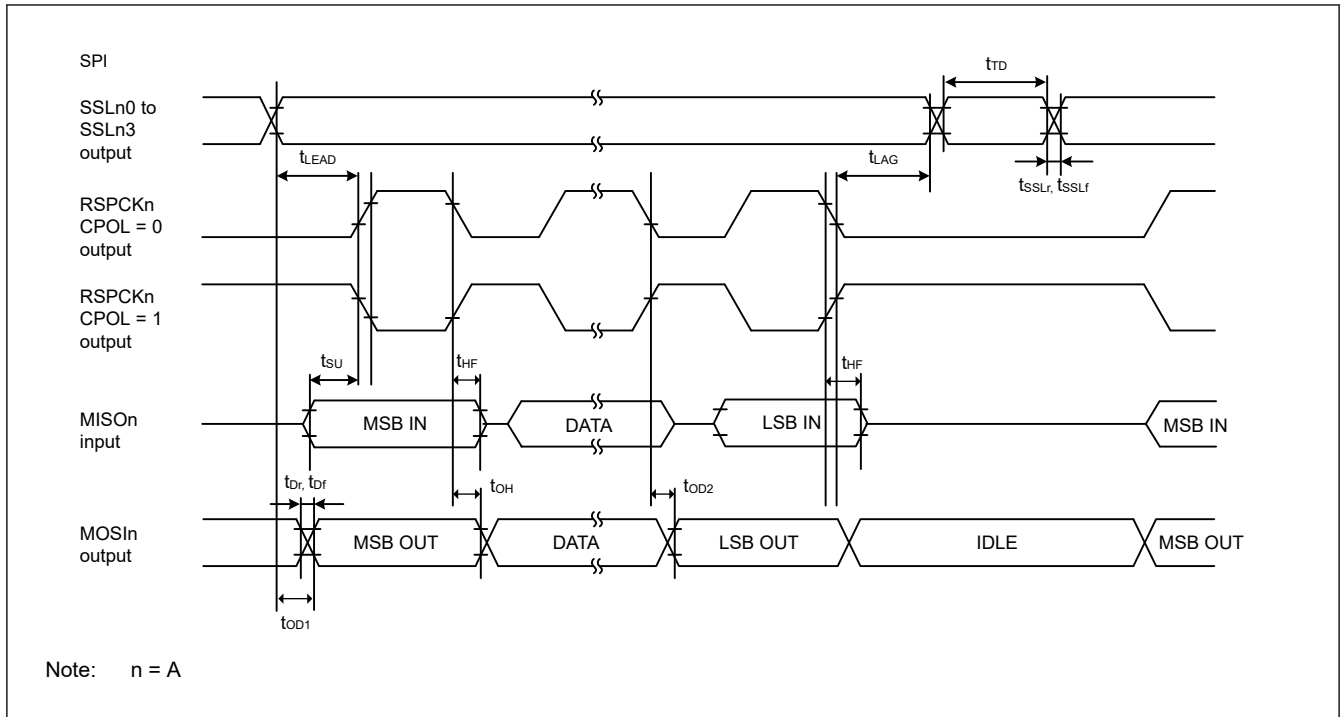


Figure 2.35 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

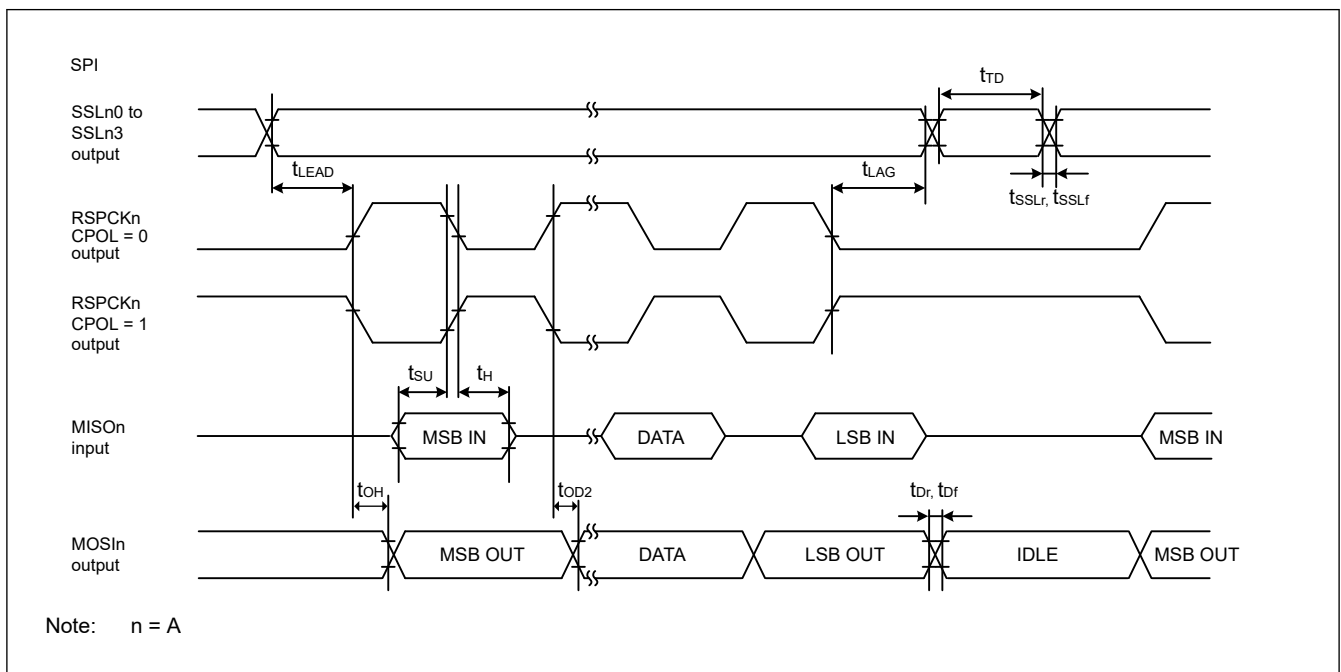


Figure 2.36 SPI timing for master when CPHA = 1

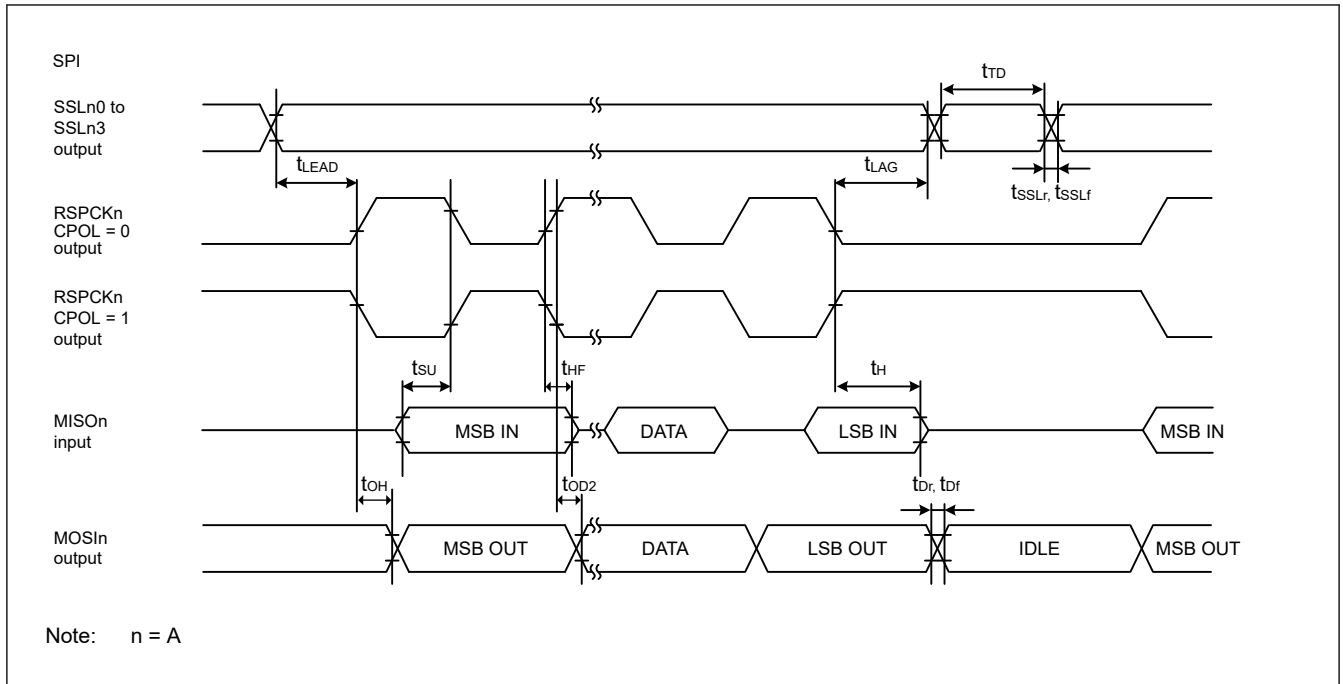


Figure 2.37 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

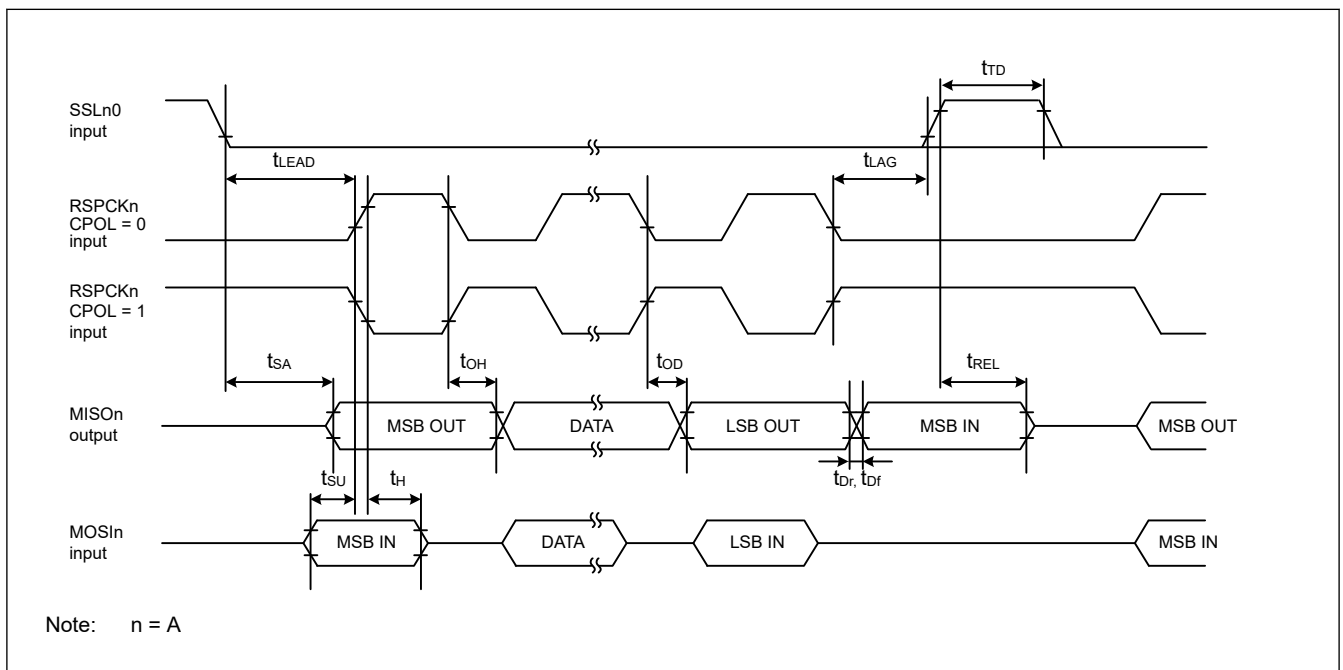


Figure 2.38 SPI timing for slave when CPHA = 0

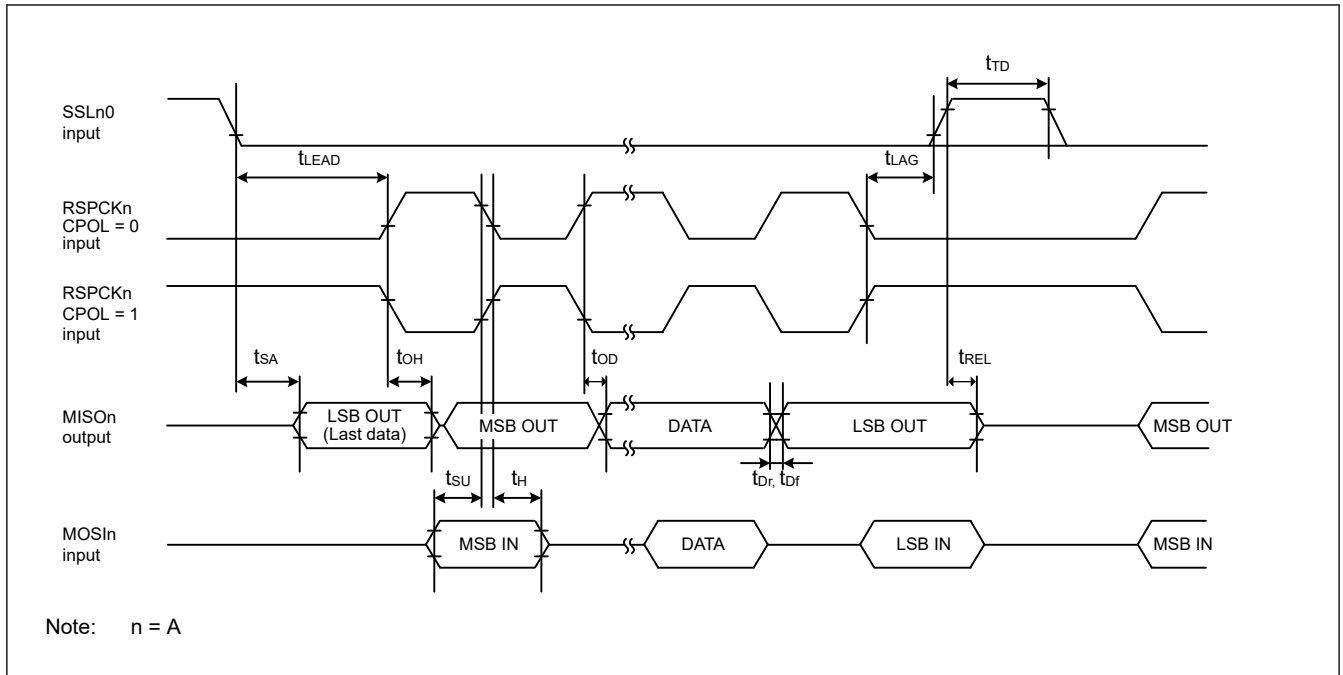


Figure 2.39 SPI timing for slave when CPHA = 1

2.3.10 QSPI Timing

Table 2.28 QSPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions | |
|-----------|-------------------------------|-------------|---------------------------------------|---|-----------------|-------------|
| QSPI | QSPCK clock cycle | t_{QScyc} | 2 | 48 | t_{Pcyc} | Figure 2.40 |
| | QSPCK clock high pulse width | t_{QSWH} | $t_{QScyc} \times 0.4$ | — | ns | |
| | QSPCK clock low pulse width | t_{QSWL} | $t_{QScyc} \times 0.4$ | — | ns | |
| QSPI | Data input setup time | t_{Su} | 10 | — | ns | Figure 2.41 |
| | Data input hold time | t_{IH} | 0 | — | ns | |
| | QSSL setup time | t_{LEAD} | $(N + 0.5) \times t_{QScyc} - 5^{*1}$ | $(N + 0.5) \times t_{QScyc} + 100^{*1}$ | ns | |
| | QSSL hold time | t_{LAG} | $(N + 0.5) \times t_{QScyc} - 5^{*2}$ | $(N + 0.5) \times t_{QScyc} + 100^{*2}$ | ns | |
| | Data output delay | t_{OD} | — | 4 | ns | |
| | Data output hold time | t_{OH} | -3.3 | — | ns | |
| | Successive transmission delay | t_{TD} | 1 | 16 | t_{QScyc} | |

Note: t_{Pcyc} : PCLKA cycle.

Note 1. N is set to 0 or 1 in SFMSLD.

Note 2. N is set to 0 or 1 in SFMSHD.

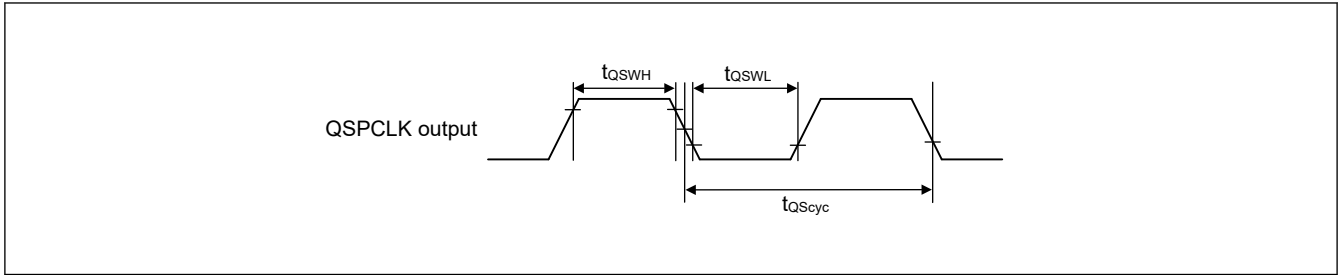


Figure 2.40 QSPI clock timing

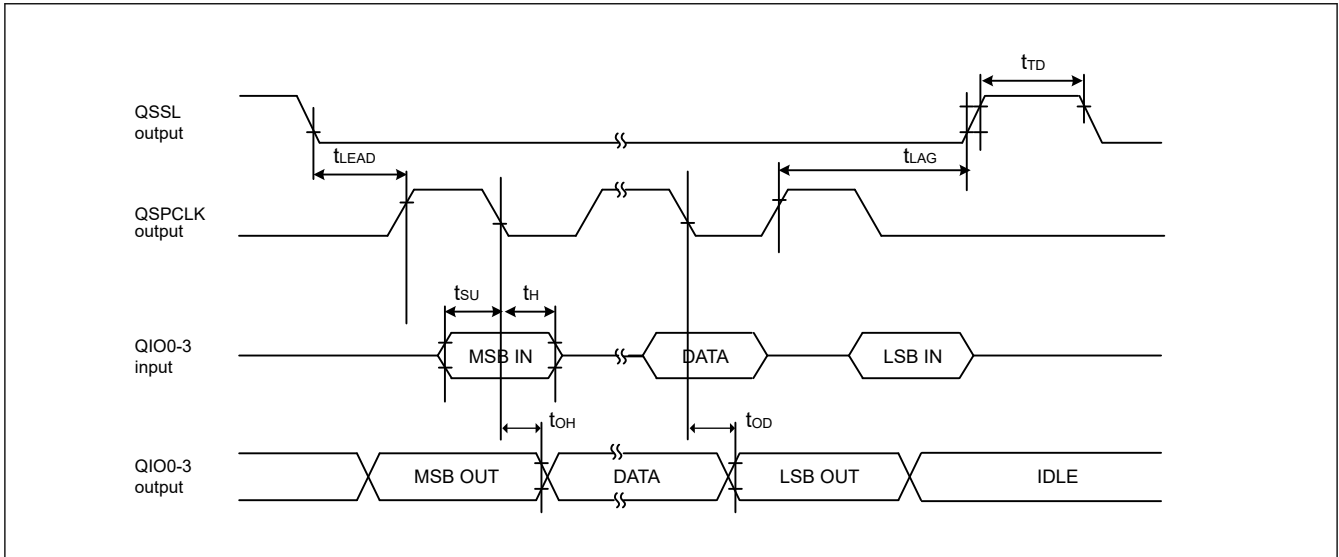


Figure 2.41 Transmit and receive timing

2.3.11 IIC Timing

Table 2.29 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B.

(2) The following pins do not require setting: SCL0_A, SDA0_A.

(3) Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | Symbol | Min | Max | Unit | Test conditions | |
|--|--|------------|---|---------------------------|-----------------|-------------|
| IIC (Standard mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | t_{SCL} | $6 (12) \times t_{IICcyc} + 1300$ | — | ns | Figure 2.42 |
| | SCL input high pulse width | t_{SCLH} | $3 (6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | t_{SCLL} | $3 (6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA rise time | t_{Sr} | — | 1000 | ns | |
| | SCL, SDA fall time | t_{Sf} | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1 (4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 300$ | — | ns | |
| | SDA input bus free time when wakeup function is enabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | — | ns | |
| | START condition input hold time when wakeup function is disabled | t_{STAH} | $t_{IICcyc} + 300$ | — | ns | |
| | START condition input hold time when wakeup function is enabled | t_{STAH} | $1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$ | — | ns | |
| | Repeated START condition input setup time | t_{STAS} | 1000 | — | ns | |
| | STOP condition input setup time | t_{STOS} | 1000 | — | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b^{*2} | — | 400 | pF | |

Table 2.29 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B.

(2) The following pins do not require setting: SCL0_A, SDA0_A.

(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|--------------------------|--|------------|--|---------------------------|------|-----------------|
| IIC (Fast mode) | SCL input cycle time | t_{SCL} | $6 (12) \times t_{IICcyc} + 600$ | — | ns | Figure 2.42 |
| | SCL input high pulse width | t_{SCLH} | $3 (6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | t_{SCLL} | $3 (6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA rise time | t_{Sr} | $20 \times (\text{external pullup voltage}/5.5V)^{*1}$ | 300 | ns | |
| | SCL, SDA fall time | t_{Sf} | $20 \times (\text{external pullup voltage}/5.5V)^{*1}$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1 (4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 300$ | — | ns | |
| | SDA input bus free time when wakeup function is enabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$ | — | ns | |
| | START condition input hold time when wakeup function is disabled | t_{STAH} | $t_{IICcyc} + 300$ | — | ns | |
| | START condition input hold time when wakeup function is enabled | t_{STAH} | $1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$ | — | ns | |
| | Repeated START condition input setup time | t_{STAS} | 300 | — | ns | |
| | STOP condition input setup time | t_{STOS} | 300 | — | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| SCL, SDA capacitive load | C_b^{*2} | — | 400 | pF | | |

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle.

Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Note 1. Only supported for SCL0_A and SDA0_A.

Note 2. C_b indicates the total capacity of the bus line.

Table 2.30 IIC timing (2)

Setting of the SCL0_A, SDA0_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions | |
|---------------------------------------|--|------------|---|---------------------------|-----------------|-------------|
| IIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | t_{SCL} | $6 (12) \times t_{IICcyc} + 240$ | — | ns | Figure 2.42 |
| | SCL input high pulse width | t_{SCLH} | $3 (6) \times t_{IICcyc} + 120$ | — | ns | |
| | SCL input low pulse width | t_{SCLL} | $3 (6) \times t_{IICcyc} + 120$ | — | ns | |
| | SCL, SDA rise time | t_{Sr} | — | 120 | ns | |
| | SCL, SDA fall time | t_{Sf} | $20 \times (\text{external pullup voltage} / 5.5V)$ | 120 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1 (4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 120$ | — | ns | |
| | SDA input bus free time when wakeup function is enabled | t_{BUF} | $3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 120$ | — | ns | |
| | Start condition input hold time when wakeup function is disabled | t_{STAH} | $t_{IICcyc} + 120$ | — | ns | |
| | START condition input hold time when wakeup function is enabled | t_{STAH} | $1 (5) \times t_{IICcyc} + t_{Pcyc} + 120$ | — | ns | |
| | Restart condition input setup time | t_{STAS} | 120 | — | ns | |
| | Stop condition input setup time | t_{STOS} | 120 | — | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 30$ | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| SCL, SDA capacitive load | C_b^{*1} | — | 550 | pF | | |

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle.

Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 1. C_b indicates the total capacity of the bus line.

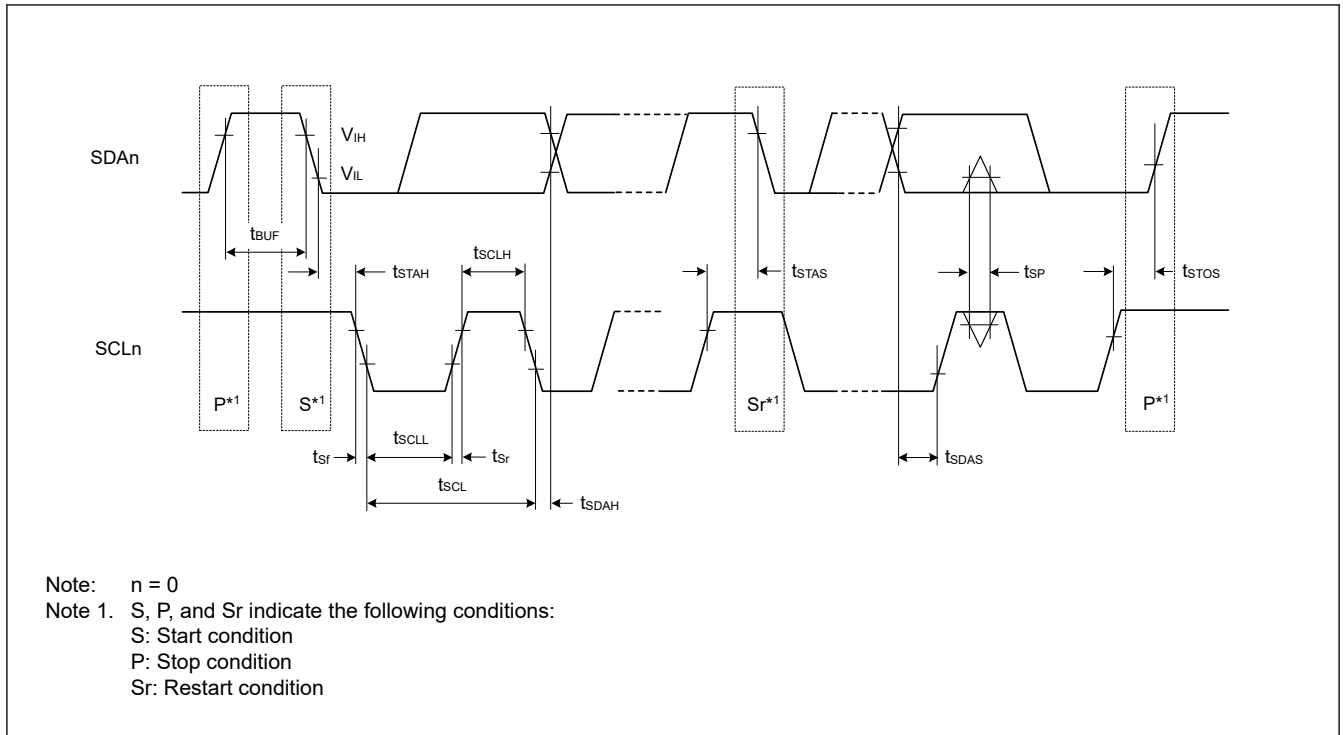


Figure 2.42 I²C bus interface input/output timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.31 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, $2.7 \leq VREFH0/VREFH \leq AVCC0$, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---------------------------------------|--|-----------------------------------|-------|-----|-------|-----------------|-----------------------------------|
| Input characteristics | Input high voltage | V _{IH} | 2.0 | — | — | V | |
| | Input low voltage | V _{IL} | — | — | 0.8 | V | |
| | Differential input sensitivity | V _{DI} | 0.2 | — | — | V | USB_DP - USB_DM |
| | Differential common-mode range | V _{CM} | 0.8 | — | 2.5 | V | — |
| Output characteristics | Output high voltage | V _{OH} | 2.8 | — | 3.6 | V | I _{OH} = -200 μA |
| | Output low voltage | V _{OL} | 0.0 | — | 0.3 | V | I _{OL} = 2 mA |
| | Cross-over voltage | V _{CRS} | 1.3 | — | 2.0 | V | Figure 2.43 |
| | Rise time | t _{LR} | 75 | — | 300 | ns | |
| | Fall time | t _{LF} | 75 | — | 300 | ns | |
| | Rise/fall time ratio | t _{LR} / t _{LF} | 80 | — | 125 | % | t _{LR} / t _{LF} |
| Pull-up and pull-down characteristics | USB_DP and USB_DM pull-down resistance in host controller mode | R _{pd} | 14.25 | — | 24.80 | kΩ | — |

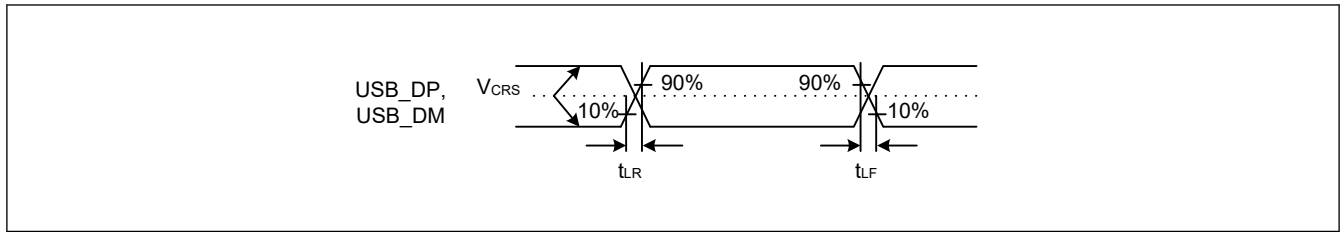


Figure 2.43 USB_DP and USB_DM output timing in low-speed mode

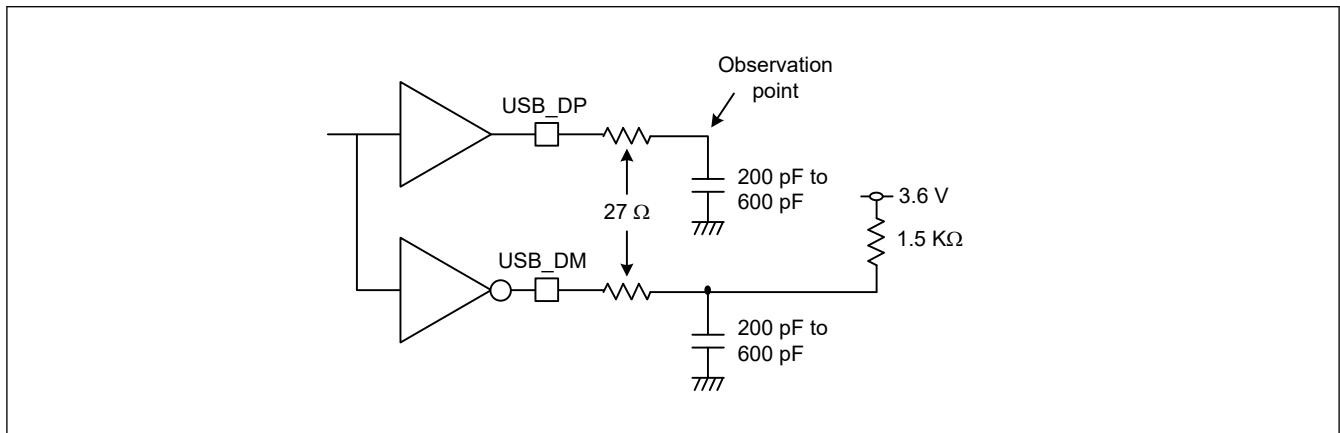


Figure 2.44 Test circuit in low-speed mode

Table 2.32 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------|--|-----------------------------------|-------|-----|--------|-----------------|
| Input characteristics | Input high voltage | V _{IH} | 2.0 | — | — | V |
| | Input low voltage | V _{IL} | — | — | 0.8 | V |
| | Differential input sensitivity | V _{DI} | 0.2 | — | — | V |
| | Differential common-mode range | V _{CM} | 0.8 | — | 2.5 | V |
| Output characteristics | Output high voltage | V _{OH} | 2.8 | — | 3.6 | V |
| | Output low voltage | V _{OL} | 0.0 | — | 0.3 | V |
| | Cross-over voltage | V _{CRS} | 1.3 | — | 2.0 | V |
| | Rise time | t _{LR} | 4 | — | 20 | ns |
| | Fall time | t _{LF} | 4 | — | 20 | ns |
| | Rise/fall time ratio | t _{LR} / t _{LF} | 90 | — | 111.11 | % |
| | Output resistance | Z _{DRV} | 28 | — | 44 | Ω |
| Pull-up and pull-down characteristics | DM pull-up resistance in device controller mode | R _{pu} | 0.900 | — | 1.575 | kΩ |
| | | R _{pu} | 1.425 | — | 3.090 | kΩ |
| | USB_DP and USB_DM pull-down resistance in host controller mode | R _{pd} | 14.25 | — | 24.80 | kΩ |

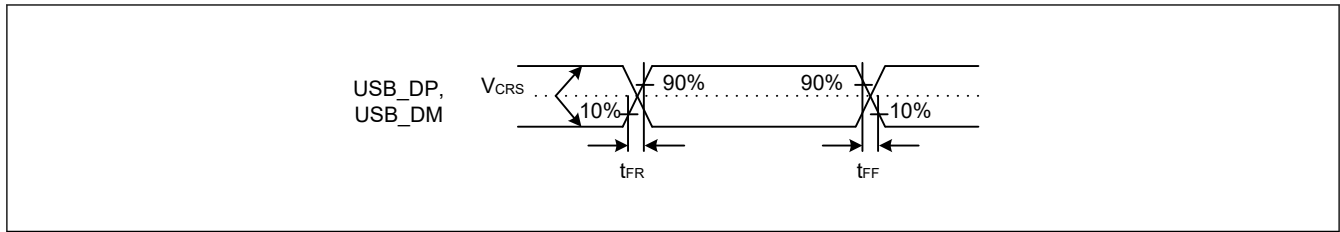


Figure 2.45 USB_DP and USB_DM output timing in full-speed mode

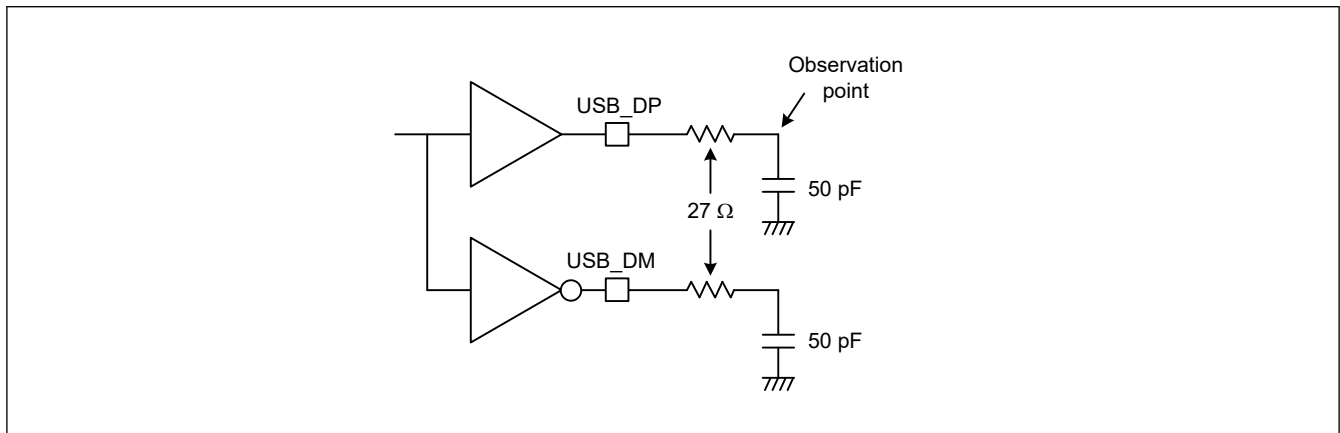


Figure 2.46 Test circuit in full-speed mode

Table 2.33 USBFS characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|--------------------------------|------------------------|----------------------|------|-----|------|-----------------|-------------------------|
| Battery Charging Specification | D+ sink current | I _{DP_SINK} | 25 | — | 175 | μA | — |
| | D- sink current | I _{DM_SINK} | 25 | — | 175 | μA | — |
| | DCD source current | I _{DP_SRC} | 7 | — | 13 | μA | — |
| | Data detection voltage | V _{DAT_REF} | 0.25 | — | 0.4 | V | — |
| | D+ source voltage | V _{DP_SRC} | 0.5 | — | 0.7 | V | Output current = 250 μA |
| | D- source voltage | V _{DM_SRC} | 0.5 | — | 0.7 | V | Output current = 250 μA |

2.5 ADC12 Characteristics

Table 2.34 A/D conversion characteristics for unit 0 (1 of 2)

Conditions: PCLKC = 1 to 50 MHz

| Parameter | Min | Typ | Max | Unit | Test conditions |
|--------------------------|-----|------|-----|------|-----------------|
| Frequency | 1 | — | 50 | MHz | — |
| Analog input capacitance | — | — | 30 | pF | — |
| Quantization error | — | ±0.5 | — | LSB | — |
| Resolution | — | — | 12 | Bits | — |

Table 2.34 A/D conversion characteristics for unit 0 (2 of 2)

Conditions: PCLKC = 1 to 50 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|--|--|---|---------------------------|------|------|------|--|
| High-precision high-speed channels (AN000 to AN002) | Conversion time* ¹ (operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.52 (0.26)* ² | — | — | μs | Sampling in 13 states |
| | | Max. = 400 Ω | 0.40 (0.14)* ² | — | — | μs | Sampling in 7 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0 |
| | Offset error | | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±2.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±4.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±1.5 | LSB | — |
| INL integral nonlinearity error | | — | ±1.0 | ±2.5 | LSB | — | |
| High-precision normal-speed channels (AN003, AN004, AN011 to AN013) | Conversion time* ¹ (Operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.92 (0.66)* ² | — | — | μs | Sampling in 33 states |
| | | Offset error | — | ±1.0 | ±2.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±2.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±4.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±1.5 | LSB | — |
| | INL integral nonlinearity error | | — | ±1.0 | ±2.5 | LSB | — |
| Normal-precision normal-speed channels (AN016) | Conversion time* ¹ (Operation at PCLKC = 50 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.92 (0.66)* ² | — | — | μs | Sampling in 33 states |
| | | Offset error | — | ±1.0 | ±5.5 | LSB | — |
| | Full-scale error | | — | ±1.0 | ±5.5 | LSB | — |
| | Absolute accuracy | | — | ±2.0 | ±7.5 | LSB | — |
| | DNL differential nonlinearity error | | — | ±0.5 | ±4.5 | LSB | — |
| | INL integral nonlinearity error | | — | ±1.0 | ±5.5 | LSB | — |

Note: These specification values apply when there is no access to the external memory during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.

The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH0, VREFL0, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.35 A/D internal reference voltage characteristics

| Parameter | Min | Typ | Max | Unit | Test conditions |
|--------------------------------|------|------|------|------|-----------------|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V | — |
| Sampling time | 4.15 | — | — | μs | — |

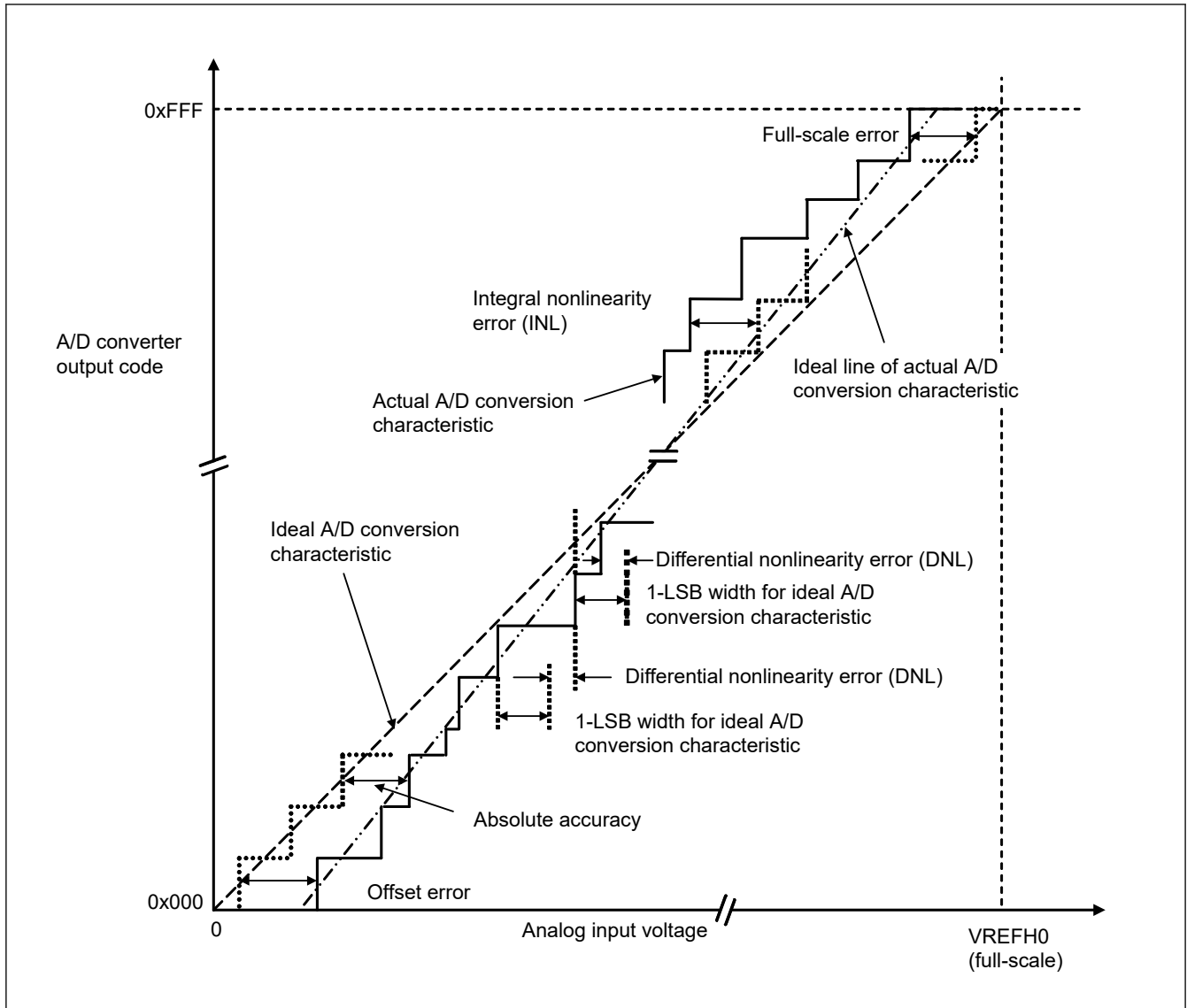


Figure 2.47 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage $V_{REFH0} = 3.072$ V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ± 5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.36 D/A conversion characteristics

| Parameter | Min | Typ | Max | Unit | Test conditions |
|--------------------------|-----|------|-------------|------|--|
| Resolution | — | — | 12 | Bits | — |
| Without output amplifier | | | | | |
| Absolute accuracy | — | — | ±24 | LSB | Resistive load 2 MΩ |
| INL | — | ±2.0 | ±8.0 | LSB | Resistive load 2 MΩ |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| Output impedance | — | 8.5 | — | kΩ | — |
| Conversion time | — | — | 3 | μs | Resistive load 2 MΩ, Capacitive load 20 pF |
| Output voltage range | 0 | — | VREFH | V | — |
| With output amplifier | | | | | |
| INL | — | ±2.0 | ±4.0 | LSB | — |
| DNL | — | ±1.0 | ±2.0 | LSB | — |
| Conversion time | — | — | 4.0 | μs | — |
| Resistive load | 5 | — | — | kΩ | — |
| Capacitive load | — | — | 50 | pF | — |
| Output voltage range | 0.2 | — | VREFH – 0.2 | V | — |

2.7 OSC Stop Detect Characteristics

Table 2.37 Oscillation stop detection circuit characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------|----------|-----|-----|-----|------|-----------------|
| Detection time | t_{dr} | — | — | 1 | ms | Figure 2.48 |

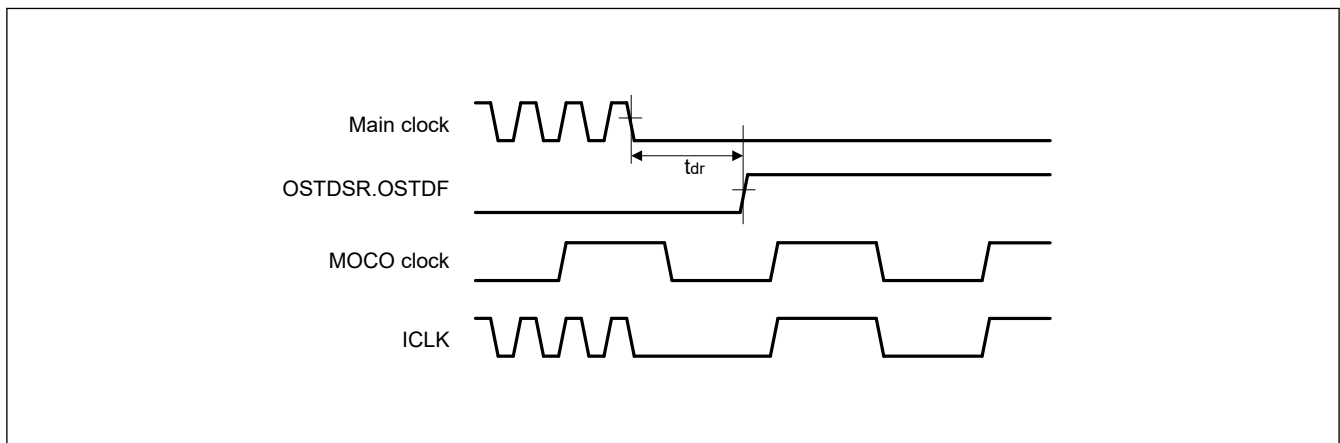


Figure 2.48 Oscillation stop detection timing

2.8 POR and LVD Characteristics

Table 2.38 Power-on reset circuit and voltage detection circuit characteristics (1)

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|----------------------------------|------------------------------------|---------------|--------------|------|------|-------------|-----------------|----------------------------|
| Voltage detection level | Power-on reset (POR) | DPSBYCR.DEEPCUT[1:0] = 00b or 01b. | V_{POR} | 2.5 | 2.6 | 2.7 | V | Figure 2.49 | |
| | | DPSBYCR.DEEPCUT[1:0] = 11b. | | 1.8 | 2.25 | 2.7 | | | |
| | Voltage detection circuit (LVD0) | | V_{det0_1} | 2.84 | 2.94 | 3.04 | | Figure 2.50 | |
| | | | V_{det0_2} | 2.77 | 2.87 | 2.97 | | | |
| | | | V_{det0_3} | 2.70 | 2.80 | 2.90 | | | |
| | Voltage detection circuit (LVD1) | | V_{det1_1} | 2.89 | 2.99 | 3.09 | | Figure 2.51 | |
| | | | V_{det1_2} | 2.82 | 2.92 | 3.02 | | | |
| | | | V_{det1_3} | 2.75 | 2.85 | 2.95 | | | |
| | Voltage detection circuit (LVD2) | | V_{det2_1} | 2.89 | 2.99 | 3.09 | | Figure 2.52 | |
| | | | V_{det2_2} | 2.82 | 2.92 | 3.02 | | | |
| | | | V_{det2_3} | 2.75 | 2.85 | 2.95 | | | |
| | Internal reset time | Power-on reset time | | t_{POR} | — | 4.5 | | — | ms |
| LVD0 reset time | | | t_{LVD0} | — | 0.51 | — | Figure 2.50 | | |
| LVD1 reset time | | | t_{LVD1} | — | 0.38 | — | Figure 2.51 | | |
| LVD2 reset time | | | t_{LVD2} | — | 0.38 | — | Figure 2.52 | | |
| Minimum VCC down time ^{*1} | | | | t_{VOFF} | 200 | — | — | μ s | Figure 2.49, Figure 2.50 |
| Response delay | | | | t_{det} | — | — | 200 | μ s | Figure 2.50 to Figure 2.52 |
| LVD operation stabilization time (after LVD is enabled) | | | | $t_{d(E-A)}$ | — | — | 10 | μ s | Figure 2.51, Figure 2.52 |
| Hysteresis width (LVD1 and LVD2) | | | | V_{LVH} | — | 70 | — | mV | |

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for POR and LVD.

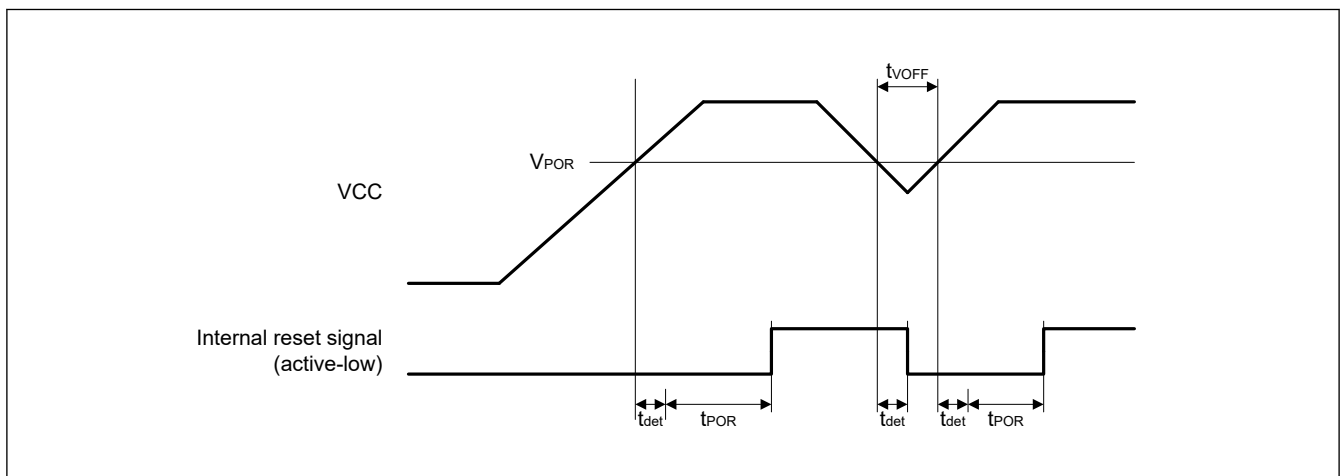


Figure 2.49 Power-on reset timing

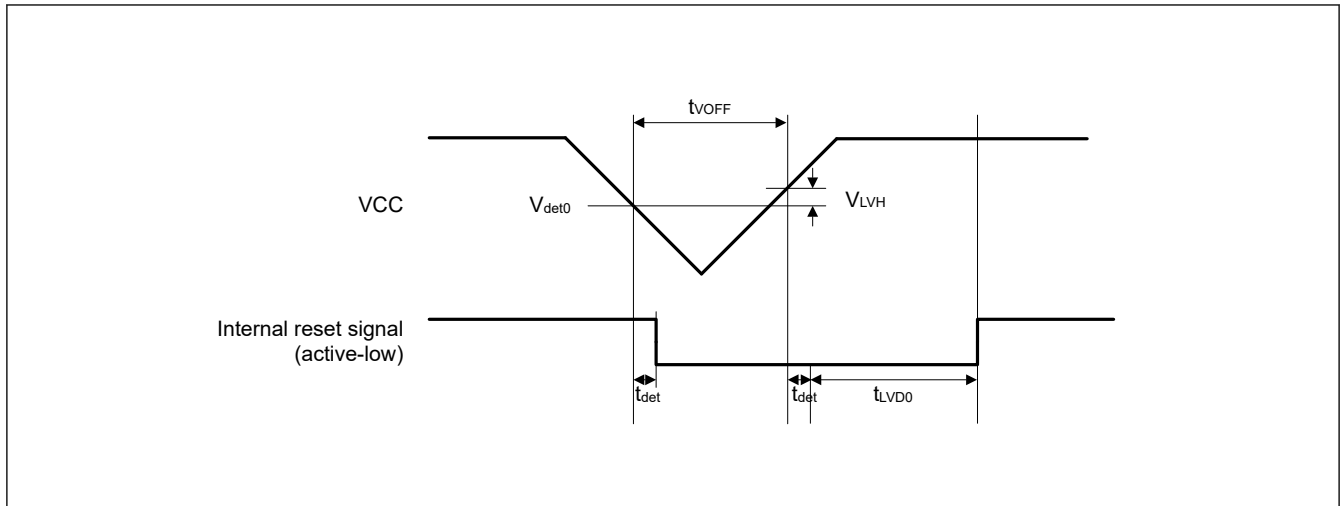


Figure 2.50 Voltage detection circuit timing (V_{det0})

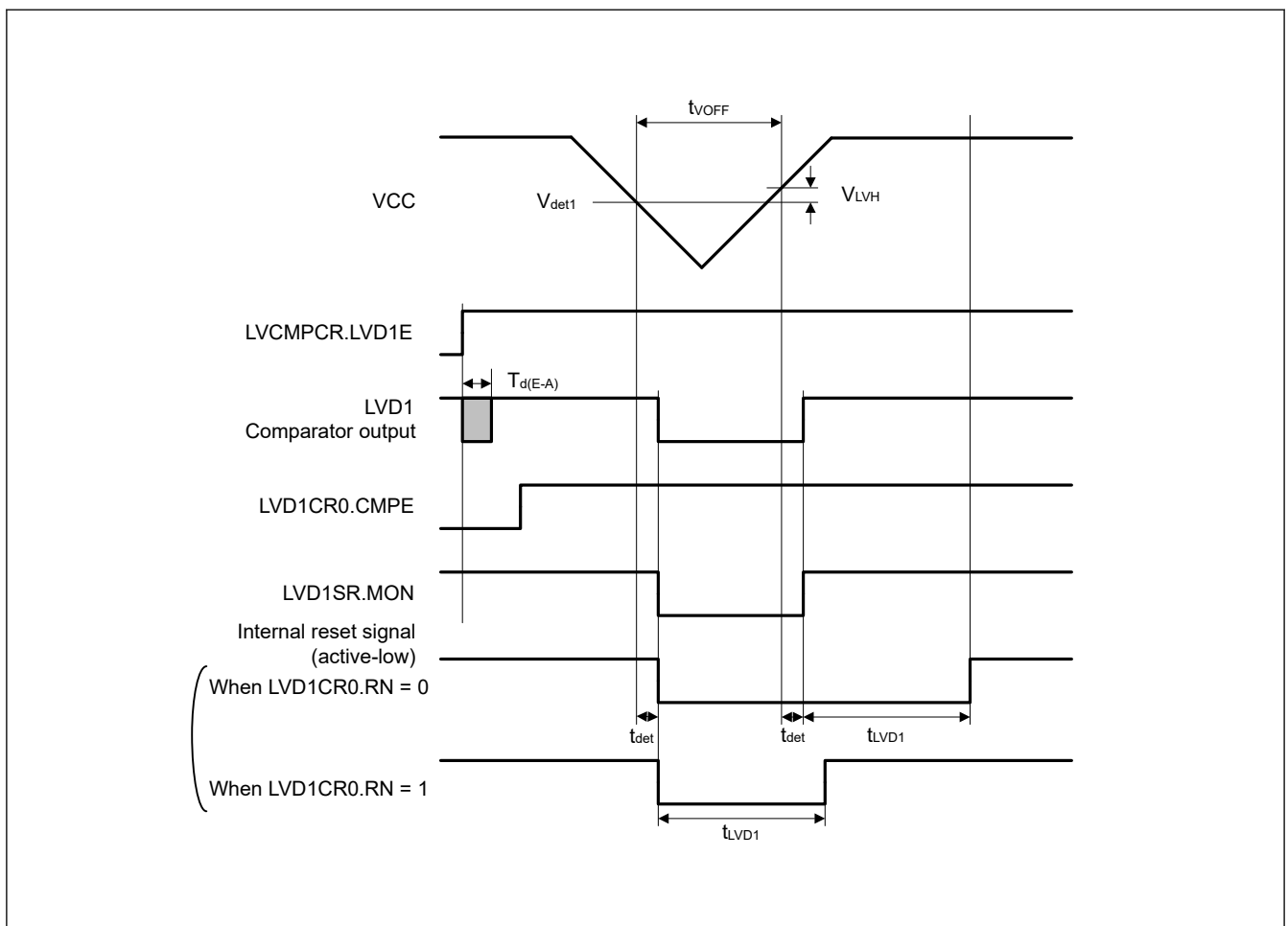


Figure 2.51 Voltage detection circuit timing (V_{det1})



Figure 2.52 Voltage detection circuit timing (V_{det2})

2.9 VBATT Characteristics

Table 2.39 Battery backup function characteristics

Conditions: $VCC = AVCC0 = VCC_USB = 2.7$ to 3.6 V, $2.7 \leq VREFH0/VREFH \leq AVCC0$, $VBATT = 1.65$ to 3.6 V*1

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|------------------|------|------|------|---------|-----------------|
| Voltage level for switching to battery backup | $V_{DET\ BATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 2.53 |
| Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop | $V_{BATT\ SW}$ | 2.70 | — | — | V | |
| VCC-off period for starting power supply switching | $t_{VOFF\ BATT}$ | 200 | — | — | μs | |
| VBATT low voltage detection level | $V_{batt\ det}$ | 1.8 | 1.9 | 2.0 | V | Figure 2.54 |
| Minimum VBATT down time | $t_{BATT\ OFF}$ | 200 | — | — | μs | |
| Response delay | $t_{BATT\ det}$ | — | — | 200 | μs | |
| VBATT monitor operation stabilization time (after VBATTMNSLR.VBATTMNSEL is changed to 1) | $t_{d(E-A)}$ | — | — | 20 | μs | |
| VBATT current increase (when VBATTMNSLR.VBATTMNSEL is 1 compared to the case that VBATTMNSLR.VBATTMNSEL is 0) | $I_{VBATT\ SEL}$ | — | 140 | 350 | nA | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DET\ BATT}$).

Note 1. Low CL crystal cannot be used below $VBATT = 1.8$ V.

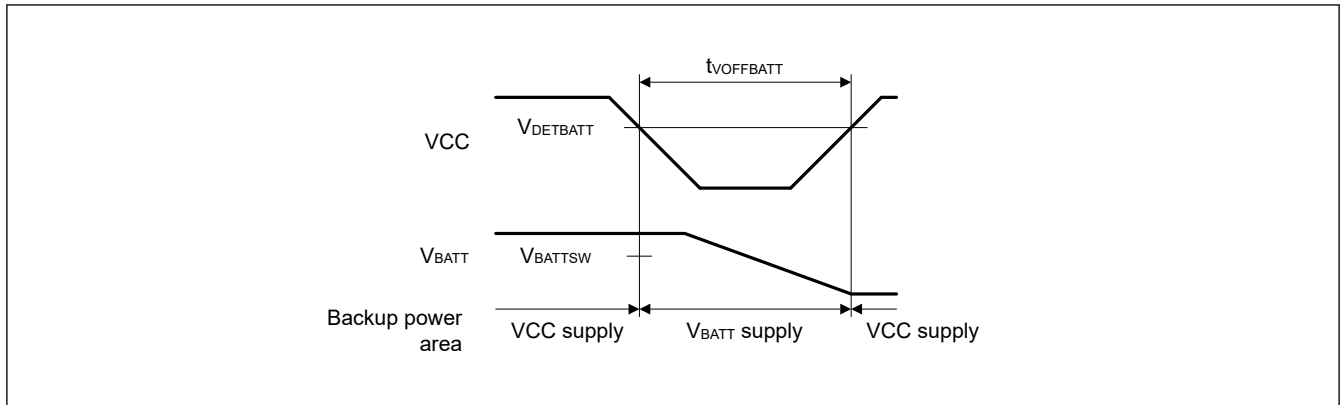


Figure 2.53 Battery backup function characteristics

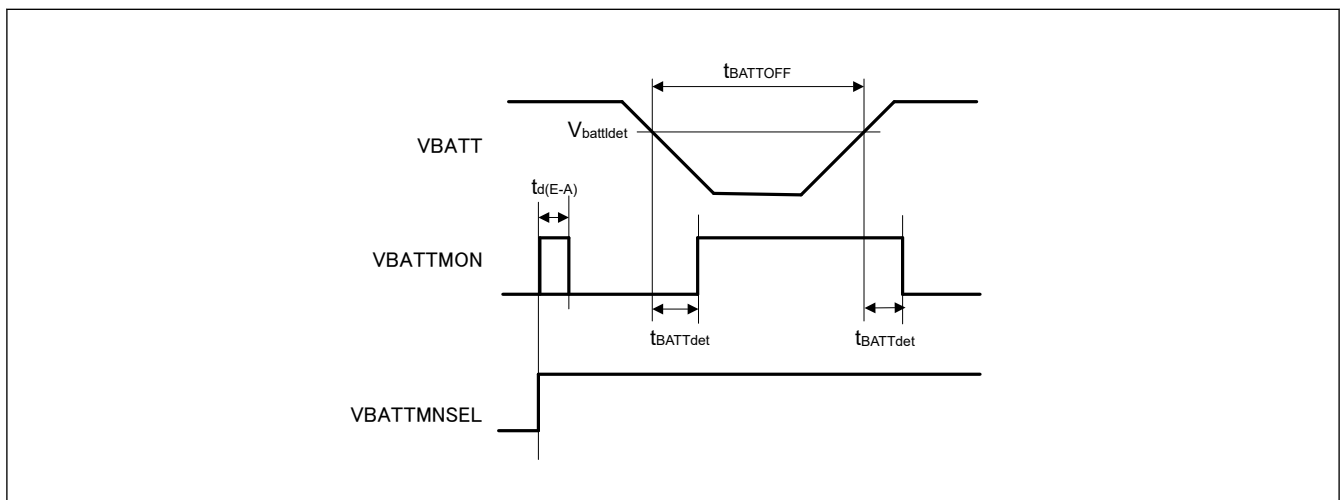


Figure 2.54 Battery backup function characteristics

2.10 Flash Memory Characteristics

2.10.1 Code Flash Memory Characteristics

Table 2.40 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions | |
|--|------------------|-------------------|-------|------|------------------------|-------|------|-------|-----------------|--|
| | | Min | Typ*6 | Max | Min | Typ*6 | Max | | | |
| Programming time N _{PEC} ≤ 100 times | 128-byte | t _{P128} | — | 0.75 | 13.2 | — | 0.34 | 6.0 | ms | |
| | 8-KB | t _{P8K} | — | 49 | 176 | — | 22 | 80 | ms | |
| | 32-KB | t _{P32K} | — | 194 | 704 | — | 88 | 320 | ms | |
| Programming time N _{PEC} > 100 times | 128-byte | t _{P128} | — | 0.91 | 15.8 | — | 0.41 | 7.2 | ms | |
| | 8-KB | t _{P8K} | — | 60 | 212 | — | 27 | 96 | ms | |
| | 32-KB | t _{P32K} | — | 234 | 848 | — | 106 | 384 | ms | |
| Erasure time N _{PEC} ≤ 100 times | 8-KB | t _{E8K} | — | 78 | 216 | — | 43 | 120 | ms | |
| | 32-KB | t _{E32K} | — | 283 | 864 | — | 157 | 480 | ms | |
| Erasure time N _{PEC} > 100 times | 8-KB | t _{E8K} | — | 94 | 260 | — | 52 | 144 | ms | |
| | 32-KB | t _{E32K} | — | 341 | 1040 | — | 189 | 576 | ms | |
| Reprogramming/erasure cycle*4 | N _{PEC} | 10000*1 | — | — | 10000*1 | — | — | Times | | |

Table 2.40 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|--------------------|---------------------|-------------------|-----|------------------------|-------------------|-----|-------|-----------------|
| | | Min | Typ ^{*6} | Max | Min | Typ ^{*6} | Max | | |
| Suspend delay during programming | t _{SPD} | — | — | 264 | — | — | 120 | μs | |
| Programming resume time | t _{PRT} | — | — | 110 | — | — | 50 | μs | |
| First suspend delay during erasure in suspend priority mode | t _{SESD1} | — | — | 216 | — | — | 120 | μs | |
| Second suspend delay during erasure in suspend priority mode | t _{SESD2} | — | — | 1.7 | — | — | 1.7 | ms | |
| Suspend delay during erasure in erasure priority mode | t _{SEED} | — | — | 1.7 | — | — | 1.7 | ms | |
| First erasing resume time during erasure in suspend priority mode ^{*5} | t _{REST1} | — | — | 1.7 | — | — | 1.7 | ms | |
| Second erasing resume time during erasure in suspend priority mode | t _{REST2} | — | — | 144 | — | — | 80 | μs | |
| Erasing resume time during erasure in erasure priority mode | t _{REET} | — | — | 144 | — | — | 80 | μs | |
| Forced stop command | t _{FD} | — | — | 32 | — | — | 20 | μs | |
| Data hold time ^{*2} | t _{DRP} | 10 ^{*2} *3 | — | — | 10 ^{*2} *3 | — | — | Years | |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

Note 6. The reference value at VCC = 3.3V and room temperature.

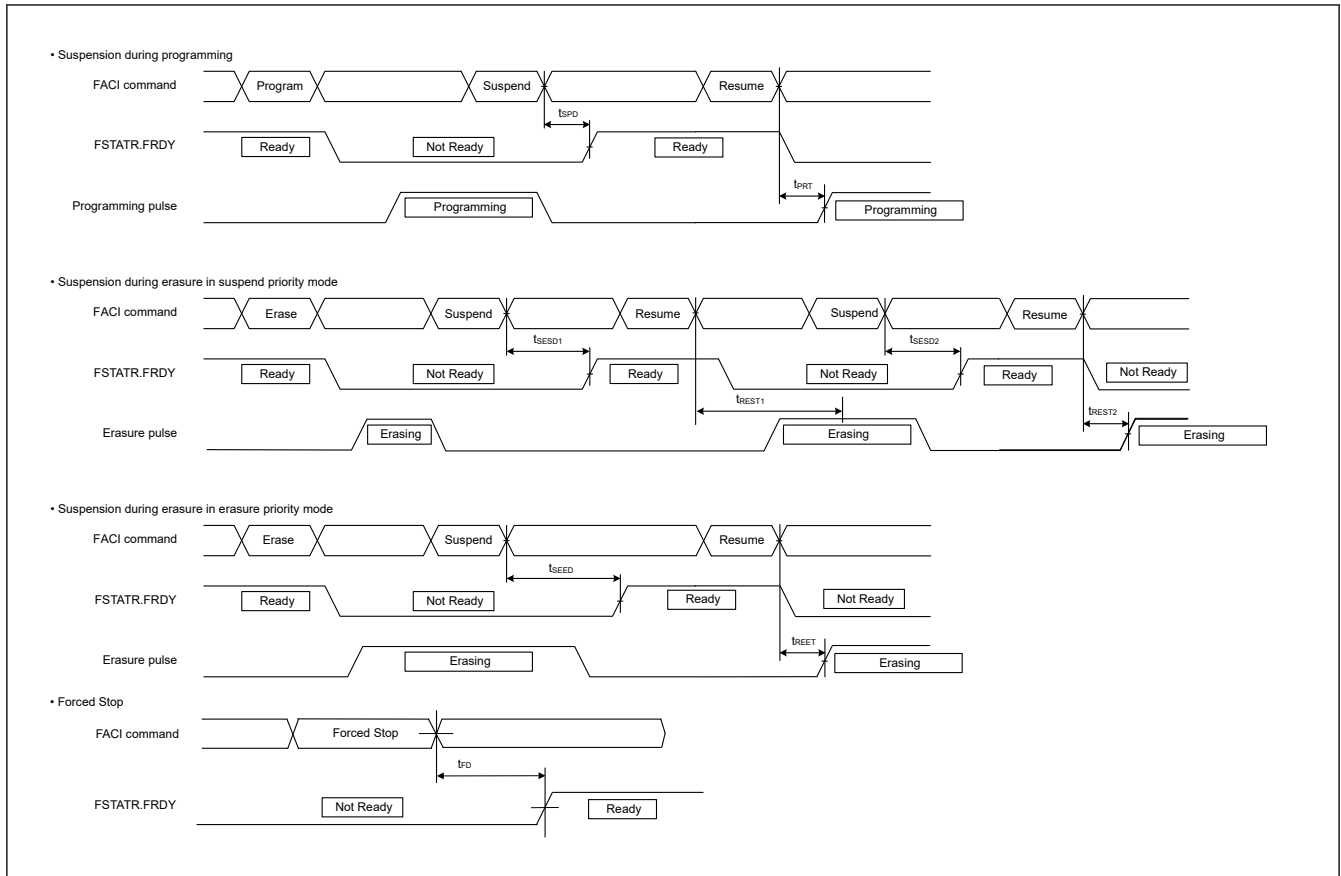


Figure 2.55 Suspension and forced stop timing for flash memory programming and erasure

2.10.2 Data Flash Memory Characteristics

Table 2.41 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
 Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|---|----------|---------------------|-------|------|------------------------|-------|------|------|-----------------|
| | | Min | Typ*6 | Max | Min | Typ*6 | Max | | |
| Programming time | 4-byte | t _{DP4} | — | 0.36 | 3.8 | — | 0.16 | 1.7 | ms |
| | 8-byte | t _{DP8} | — | 0.38 | 4.0 | — | 0.17 | 1.8 | |
| | 16-byte | t _{DP16} | — | 0.42 | 4.5 | — | 0.19 | 2.0 | |
| Erasure time | 64-byte | t _{DE64} | — | 3.1 | 18 | — | 1.7 | 10 | ms |
| | 128-byte | t _{DE128} | — | 4.7 | 27 | — | 2.6 | 15 | |
| | 256-byte | t _{DE256} | — | 8.9 | 50 | — | 4.9 | 28 | |
| Blank check time | 4-byte | t _{DBC4} | — | — | 84 | — | — | 30 | μs |
| Reprogramming/erasure cycle*1 | NDPEC | 125000*2 | — | — | 125000*2 | — | — | — | — |
| Suspend delay during programming | 4-byte | t _{DSPD} | — | — | 264 | — | — | 120 | μs |
| | 8-byte | | — | — | 264 | — | — | 120 | |
| | 16-byte | | — | — | 264 | — | — | 120 | |
| Programming resume time | | t _{DPRT} | — | — | 110 | — | — | 50 | μs |
| First suspend delay during erasure in suspend priority mode | 64-byte | t _{DSESD1} | — | — | 216 | — | — | 120 | μs |
| | 128-byte | | — | — | 216 | — | — | 120 | |
| | 256-byte | | — | — | 216 | — | — | 120 | |

Table 2.41 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions | |
|---|---------------------|---------------------|-------|-----|------------------------|-------|-----|------|-----------------|--|
| | | Min | Typ*6 | Max | Min | Typ*6 | Max | | | |
| Second suspend delay during erasure in suspend priority mode | 64-byte | t _{DSESD2} | — | — | 300 | — | — | 300 | μs | |
| | 128-byte | | — | — | 390 | — | — | 390 | | |
| | 256-byte | | — | — | 570 | — | — | 570 | | |
| Suspend delay during erasing in erasure priority mode | 64-byte | t _{DSEED} | — | — | 300 | — | — | 300 | μs | |
| | 128-byte | | — | — | 390 | — | — | 390 | | |
| | 256-byte | | — | — | 570 | — | — | 570 | | |
| First erasing resume time during erasure in suspend priority mode*5 | t _{DREST1} | — | — | 300 | — | — | 300 | μs | | |
| Second erasing resume time during erasure in suspend priority mode | t _{DREST2} | — | — | 126 | — | — | 70 | μs | | |
| Erasing resume time during erasure in erasure priority mode | t _{DREET} | — | — | 126 | — | — | 70 | μs | | |
| Forced stop command | t _{FD} | — | — | 32 | — | — | 20 | μs | | |
| Data hold time*3 | t _{DRP} | 10*3*4 | — | — | 10*3*4 | — | — | Year | | |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 4. This result is obtained from reliability testing.

Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

Note 6. The reference value at VCC = 3.3 V and room temperature.

2.10.3 Option Setting Memory Characteristics

Table 2.42 Option setting memory characteristics

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

| Parameter | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | Test conditions |
|--|------------------|--------------|-------|-----|------------------------|-------|-----|-------|-----------------|
| | | Min | Typ*4 | Max | Min | Typ*4 | Max | | |
| Programming time N _{OPC} ≤ 100 times | t _{OP} | — | 83 | 309 | — | 45 | 162 | ms | |
| Programming time N _{OPC} > 100 times | t _{OP} | — | 100 | 371 | — | 55 | 195 | ms | |
| Reprogramming cycle | N _{OPC} | 20000*1 | — | — | 20000*1 | — | — | Times | |
| Data hold time*2 | t _{DRP} | 10*2*3 | — | — | 10*2*3 | — | — | Years | |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reference value at VCC = 3.3 V and room temperature.

2.11 Boundary Scan

Table 2.43 Boundary scan characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--------------------------------------|--------------|-------------|-----|-----|------|-----------------|
| TCK clock cycle time | t_{TCKcyc} | 100 | — | — | ns | Figure 2.56 |
| TCK clock high pulse width | t_{TCKH} | 45 | — | — | ns | |
| TCK clock low pulse width | t_{TCKL} | 45 | — | — | ns | |
| TCK clock rise time | t_{TCKr} | — | — | 5 | ns | |
| TCK clock fall time | t_{TCKf} | — | — | 5 | ns | |
| TMS setup time | t_{TMSS} | 20 | — | — | ns | Figure 2.57 |
| TMS hold time | t_{TMSh} | 20 | — | — | ns | |
| TDI setup time | t_{TDis} | 20 | — | — | ns | |
| TDI hold time | t_{TDIH} | 20 | — | — | ns | |
| TDO data delay | t_{TDOD} | — | — | 40 | ns | Figure 2.58 |
| Boundary scan circuit startup time*1 | T_{BSSTUP} | t_{RESWP} | — | — | — | |

Note 1. Boundary scan does not function until the power-on reset becomes negative.

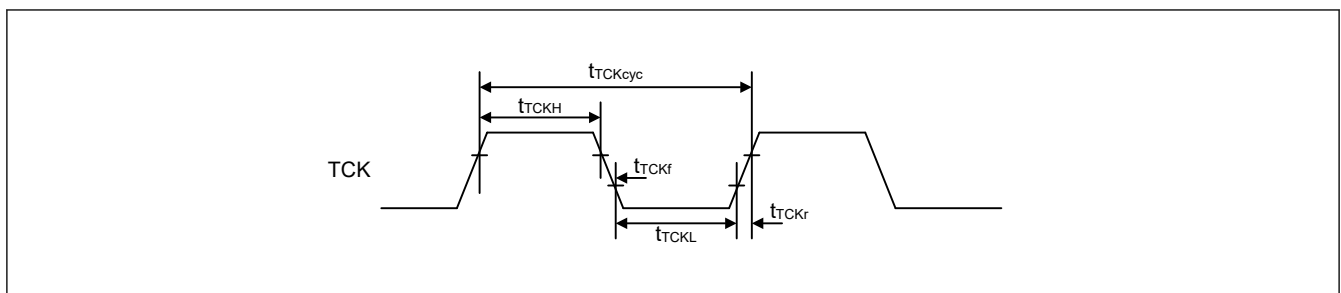


Figure 2.56 Boundary scan TCK timing

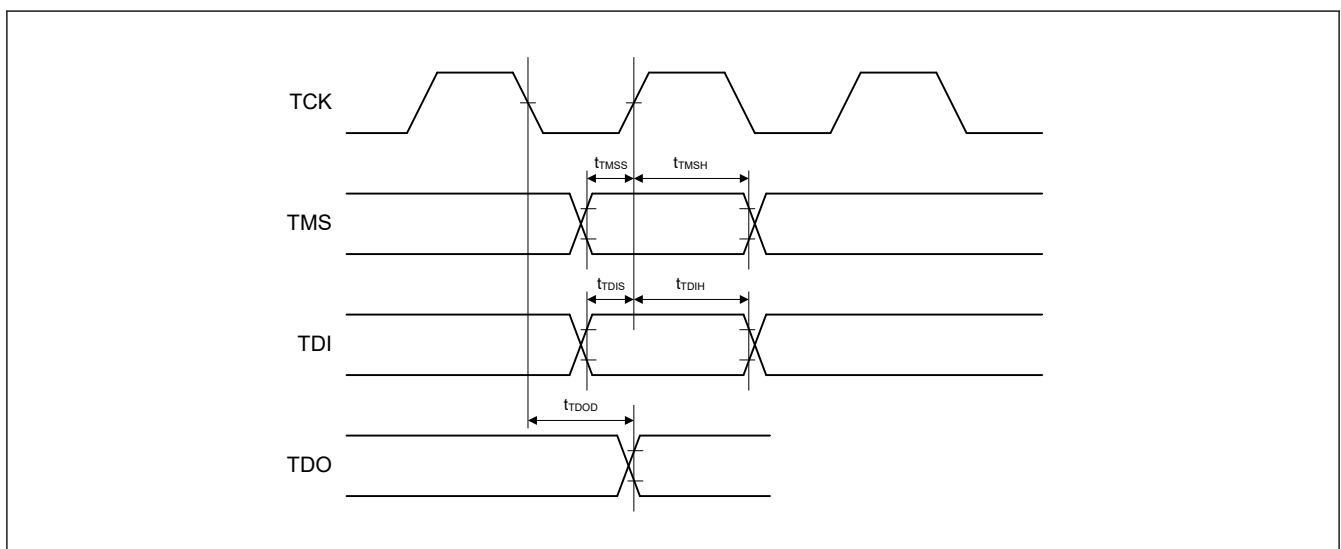


Figure 2.57 Boundary scan input/output timing

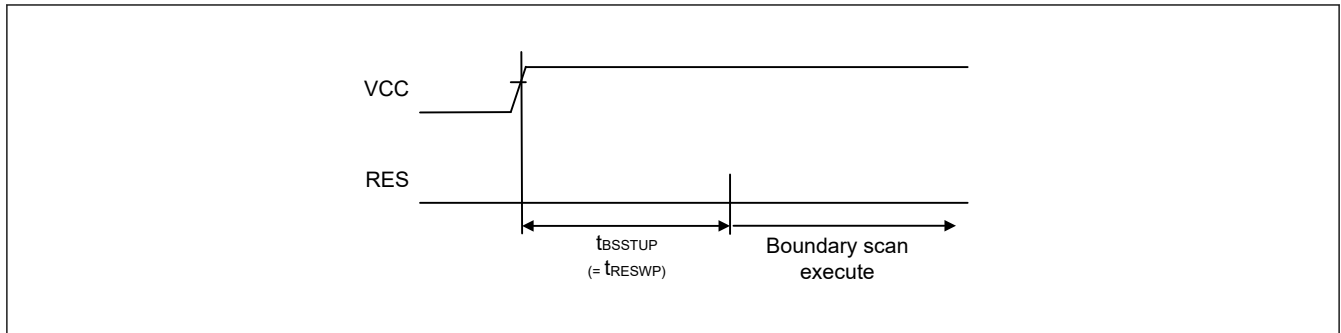


Figure 2.58 Boundary scan circuit startup timing

2.12 Joint Test Action Group (JTAG)

Table 2.44 JTAG

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------|--------------|-----|-----|-----|------|-----------------|
| TCK clock cycle time | t_{TCKcyc} | 40 | — | — | ns | Figure 2.59 |
| TCK clock high pulse width | t_{TCKH} | 15 | — | — | ns | |
| TCK clock low pulse width | t_{TCKL} | 15 | — | — | ns | |
| TCK clock rise time | t_{TCKr} | — | — | 5 | ns | |
| TCK clock fall time | t_{TCKf} | — | — | 5 | ns | |
| TMS setup time | t_{TMSS} | 8 | — | — | ns | Figure 2.60 |
| TMS hold time | t_{TMSH} | 8 | — | — | ns | |
| TDI setup time | t_{TDIS} | 8 | — | — | ns | |
| TDI hold time | t_{TDIH} | 8 | — | — | ns | |
| TDO data delay time | t_{TDOD} | — | — | 20 | ns | |

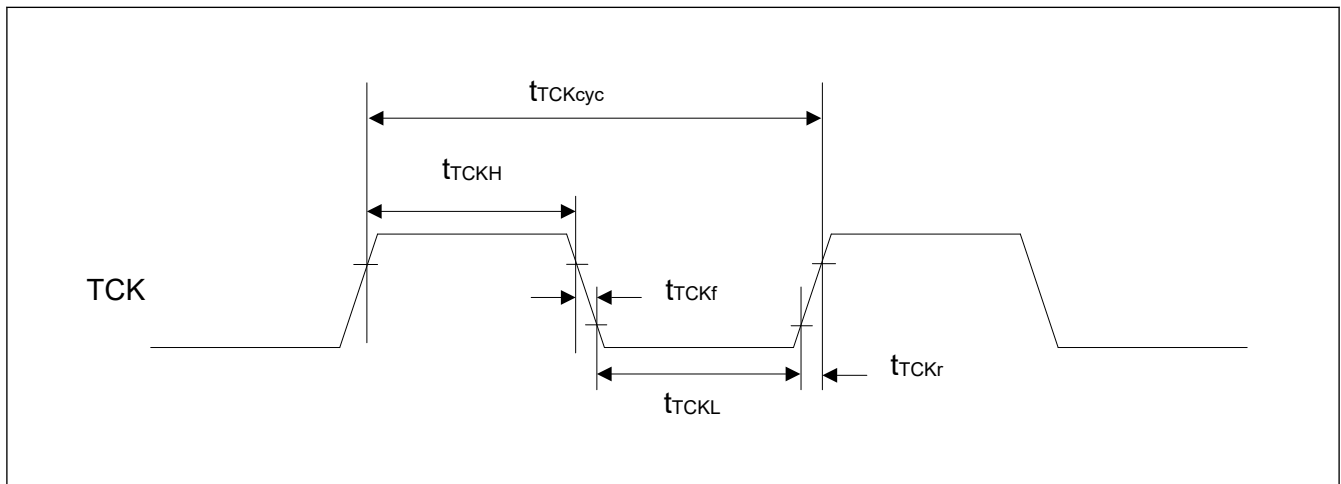


Figure 2.59 JTAG TCK timing

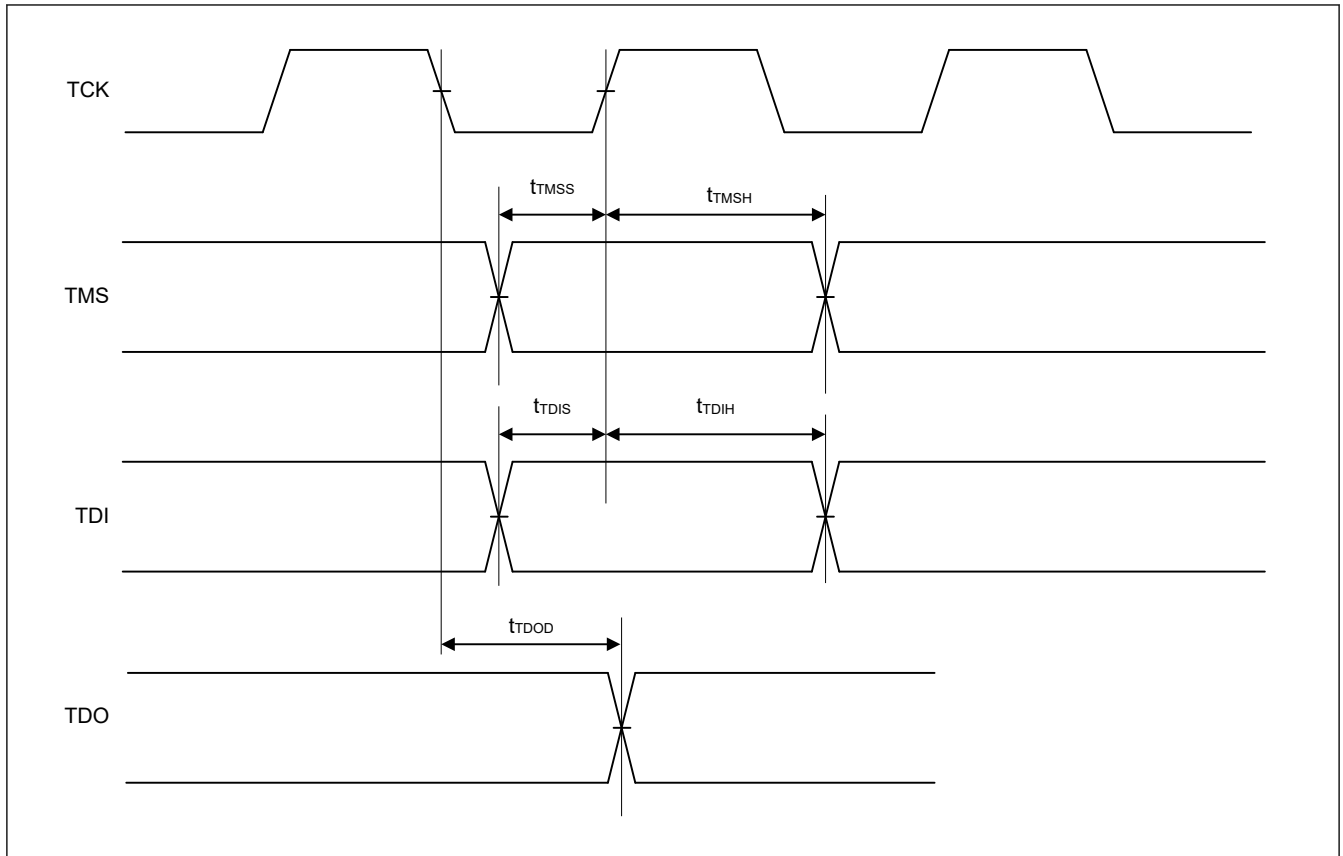


Figure 2.60 JTAG input/output timing

2.13 Serial Wire Debug (SWD)

Table 2.45 SWD

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|------------------------------|----------------|-----|-----|-----|------|-----------------|
| SWCLK clock cycle time | $t_{SWCLKcyc}$ | 40 | — | — | ns | Figure 2.61 |
| SWCLK clock high pulse width | t_{SWCKH} | 15 | — | — | ns | |
| SWCLK clock low pulse width | t_{SWCKL} | 15 | — | — | ns | |
| SWCLK clock rise time | t_{SWCKr} | — | — | 5 | ns | |
| SWCLK clock fall time | t_{SWCKf} | — | — | 5 | ns | |
| SWDIO setup time | t_{SWDS} | 8 | — | — | ns | Figure 2.62 |
| SWDIO hold time | t_{SWDH} | 8 | — | — | ns | |
| SWDIO data delay time | t_{SWDD} | 2 | — | 28 | ns | |

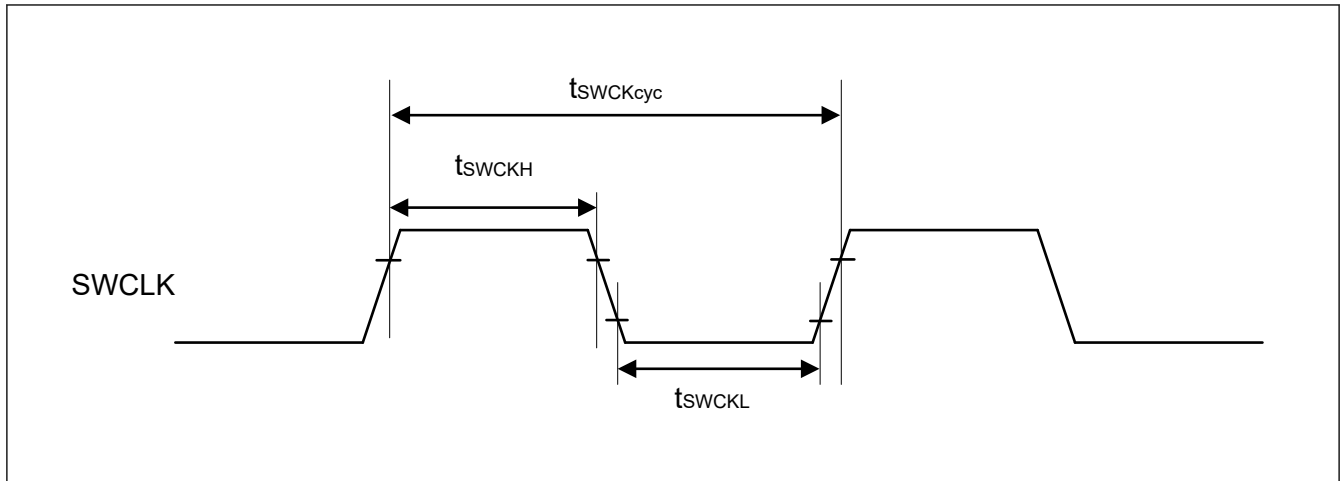


Figure 2.61 SWD SWCLK timing

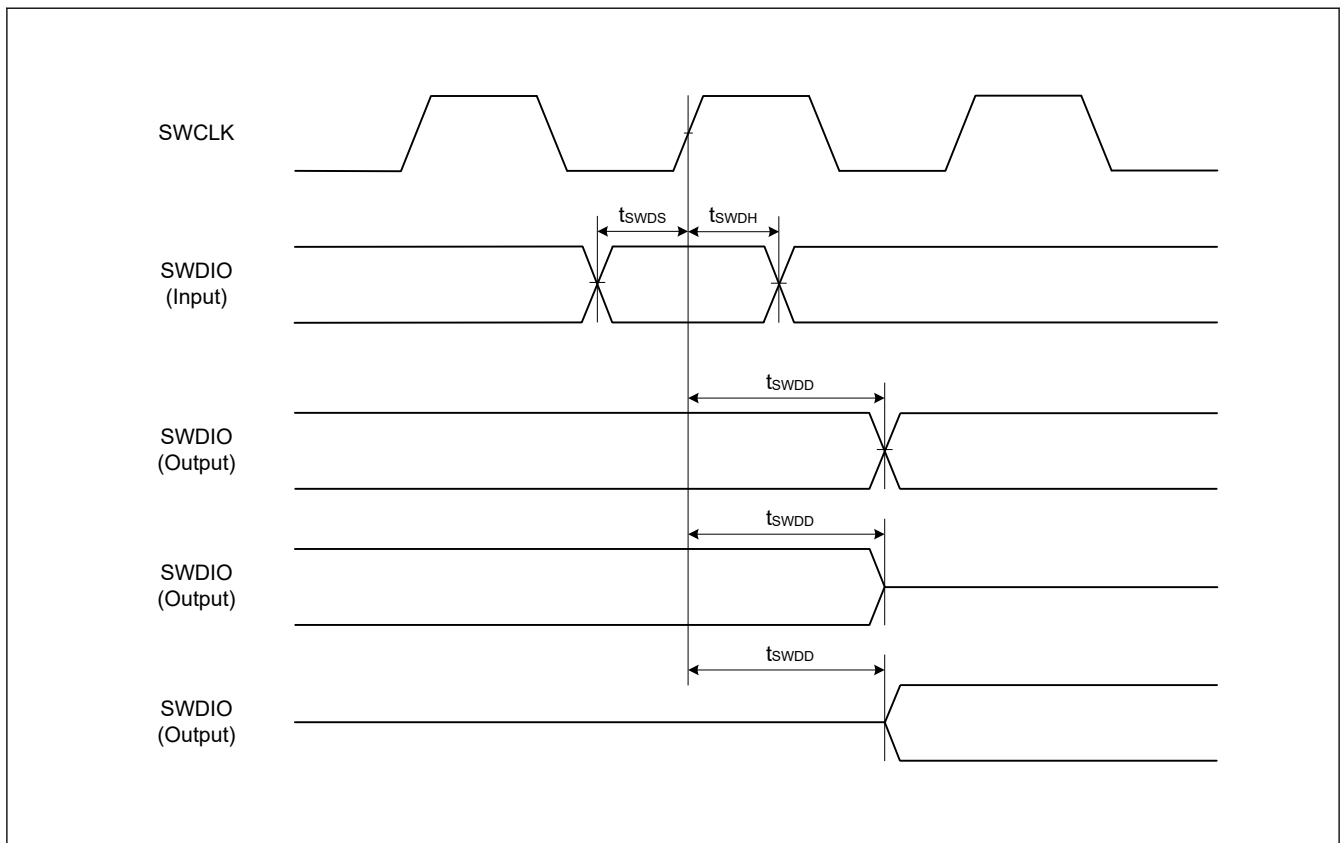


Figure 2.62 SWD input/output timing

Appendix 1. Port States in Each Processing Mode

| Function | Pin function | Reset | Software Standby mode | Deep Software Standby mode | After Deep Software Standby mode is canceled (return to startup mode) | |
|----------|--|---------|---|----------------------------|---|--------------------------|
| | | | | | IOKEEP = 0 | IOKEEP = 1 ^{*1} |
| Mode | MD | Pull-up | Keep-O | Keep | Hi-Z | Keep |
| JTAG | TCK/TMS/TDI | Pull-up | Keep-O | Keep | Hi-Z | Keep |
| | TDO | output | Keep-O | Keep | TDO output | Keep |
| IRQ | IRQx | Hi-Z | Keep-O ^{*2} | Keep | Hi-Z | Keep |
| | IRQx-DS | Hi-Z | Keep-O ^{*2} | Keep ^{*3} | Hi-Z | Keep |
| AGT | AGTIO _n | Hi-Z | Keep-O ^{*2} | Keep | Hi-Z | Keep |
| | AGTIO _n (n=1,3) | Hi-Z | Keep-O ^{*2} | Keep ^{*3} | Hi-Z | Keep |
| SCI | RXD0 | Hi-Z | Keep-O ^{*2} | Keep | Hi-Z | Keep |
| IIC | SCL _n /SDA _n | Hi-Z | Keep-O ^{*2} | Keep | Hi-Z | Keep |
| USBFS | USB_OVRCUR _x | Hi-Z | Keep-O ^{*2} | Keep | Hi-Z | Keep |
| | USB_OVRCUR _x -DS/ USB_VBUS | Hi-Z | Keep-O ^{*2} | Keep ^{*3} | Hi-Z | Keep |
| | USB_DP/USB_DM | Hi-Z | Keep-O ^{*4} | Keep ^{*3} | Hi-Z | Keep |
| RTC | RTCIC _x | Hi-Z | Keep-O ^{*2} | Keep ^{*3} | Hi-Z | Keep |
| | RTCCOUT | Hi-Z | [RTCCOUT selected] RTCCOUT output | Keep | Hi-Z | Keep |
| CLKOUT | CLKOUT | Hi-Z | [CLKOUT selected] CLKOUT output | Keep | Hi-Z | Keep |
| DAC | DA _n | Hi-Z | [DA _n output (DAOE = 1)] D/A output retained | Keep | Hi-Z | Keep |
| Others | — | Hi-Z | Keep-O | Keep | Hi-Z | Keep |

Note: H: High-level

L: Low-level

Hi-Z: High-impedance

Keep-O: Output pins retain their previous values. Input pins go to high-impedance.

Keep: Pin states are retained during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.

Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.

Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

Note 4. Input is enabled while the pin is used as an input pin.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

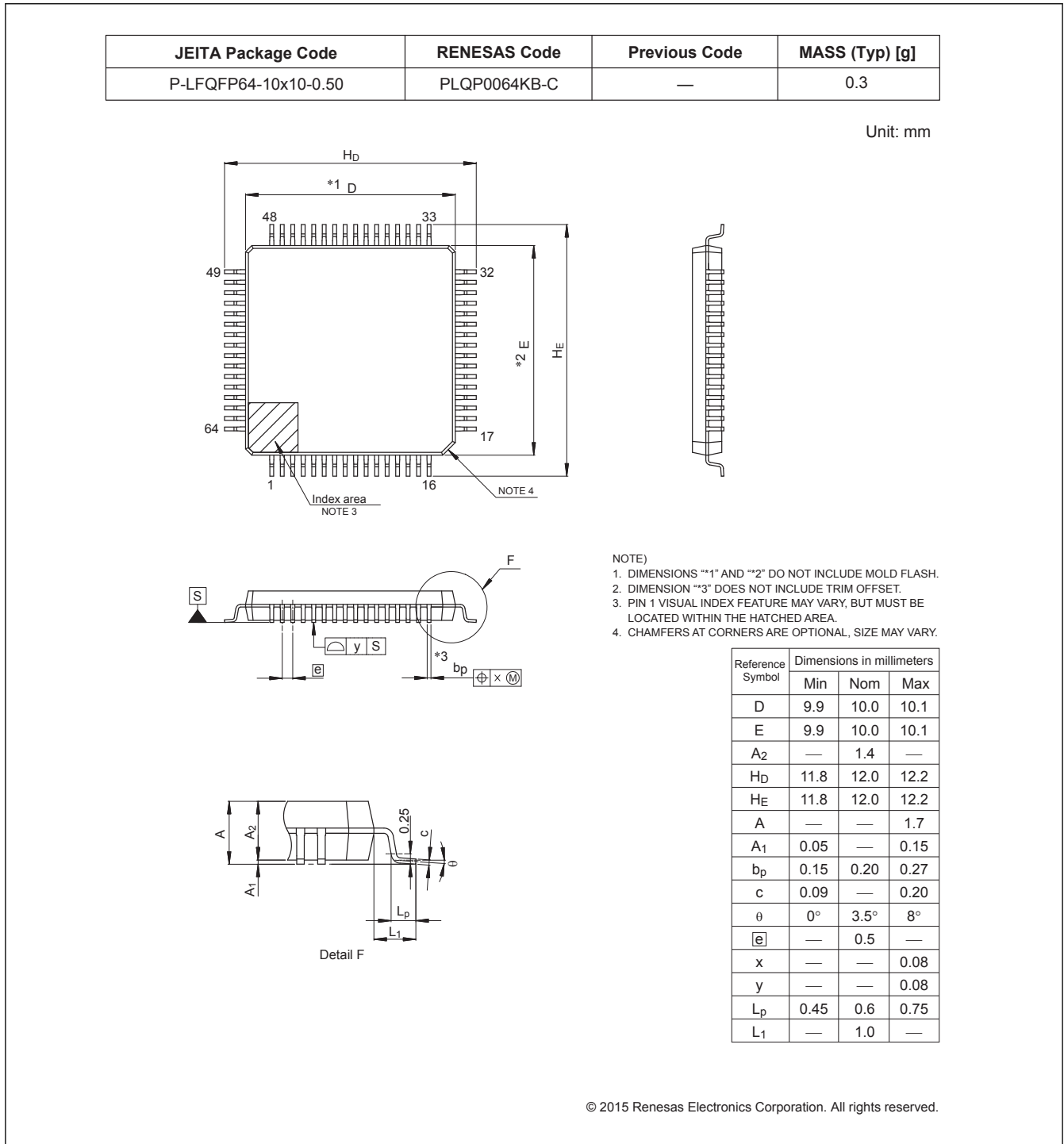


Figure 2.1 LQFP 64-pin

| | | |
|---------------------|--------------|---------------|
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
| P-HWQFN048-7x7-0.50 | PWQN0048KC-A | 0.13 g |

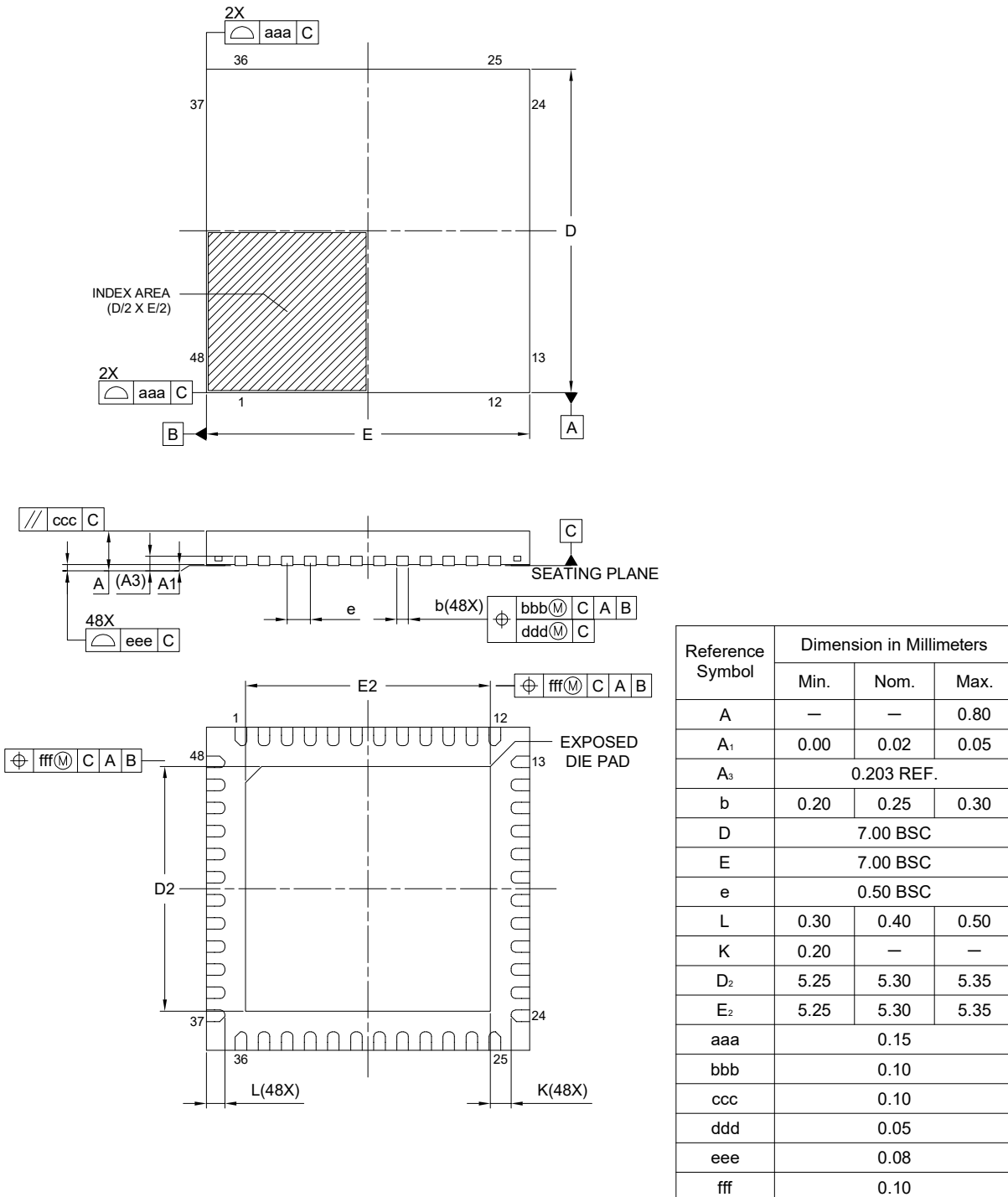


Figure 2.2 QFN 48-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. [Table 3.1](#) shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

| Name | Description | Base address |
|--------|--|--------------|
| RMPU | Renesas Memory Protection Unit | 0x4000_0000 |
| TZF | TrustZone Filter | 0x4000_0E00 |
| SRAM | SRAM Control | 0x4000_2000 |
| BUS | BUS Control | 0x4000_3000 |
| DMAC0 | Direct memory access controller 0 | 0x4000_5000 |
| DMAC1 | Direct memory access controller 1 | 0x4000_5040 |
| DMAC2 | Direct memory access controller 2 | 0x4000_5080 |
| DMAC3 | Direct memory access controller 3 | 0x4000_50C0 |
| DMAC4 | Direct memory access controller 4 | 0x4000_5100 |
| DMAC5 | Direct memory access controller 5 | 0x4000_5140 |
| DMAC6 | Direct memory access controller 6 | 0x4000_5180 |
| DMAC7 | Direct memory access controller 7 | 0x4000_51C0 |
| DMA | DMAC Module Activation | 0x4000_5200 |
| DTC | Data Transfer Controller | 0x4000_5400 |
| ICU | Interrupt Controller | 0x4000_6000 |
| CPSCU | CPU System Security Control Unit | 0x4000_8000 |
| DBG | Debug Function | 0x400_1B000 |
| FCACHE | Flash Cache | 0x400_1C100 |
| SYSC | System Control | 0x4001_E000 |
| PORT0 | Port 0 Control Registers | 0x4008_0000 |
| PORT1 | Port 1 Control Registers | 0x4008_0020 |
| PORT2 | Port 2 Control Registers | 0x4008_0040 |
| PORT3 | Port 3 Control Registers | 0x4008_0060 |
| PORT4 | Port 4 Control Registers | 0x4008_0080 |
| PORT5 | Port 5 Control Registers | 0x4008_00A0 |
| PFS | Pmn Pin Function Control Register | 0x4008_0800 |
| ELC | Event Link Controller | 0x4008_2000 |
| RTC | Realtime Clock | 0x4008_3000 |
| IWDT | Independent Watchdog Timer | 0x4008_3200 |
| WDT | Watchdog Timer | 0x4008_3400 |
| CAC | Clock Frequency Accuracy Measurement Circuit | 0x4008_3600 |
| MSTP | Module Stop Control A, B, C, D | 0x4008_4000 |
| POEG | Port Output Enable Module for GPT | 0x4008_A000 |
| USBFS | USB 2.0 FS Module | 0x4009_0000 |
| IIC0 | Inter-Integrated Circuit 0 | 0x4009_F000 |

Table 3.1 Peripheral base address (2 of 2)

| Name | Description | Base address |
|--------|--|--------------|
| IIC0WU | Inter-Integrated Circuit 0 Wake-up Unit | 0x4009_F014 |
| CAN0 | CAN0 Module | 0x400A_8000 |
| PSCU | Peripheral Security Control Unit | 0x400E_0000 |
| AGT0 | Low Power Asynchronous General purpose Timer 0 | 0x400E_8000 |
| AGT1 | Low Power Asynchronous General purpose Timer 1 | 0x400E_8100 |
| AGT2 | Low Power Asynchronous General purpose Timer 2 | 0x400E_8200 |
| AGT3 | Low Power Asynchronous General purpose Timer 3 | 0x400E_8300 |
| AGT5 | Low Power Asynchronous General purpose Timer 5 | 0x400E_8500 |
| CRC | CRC Calculator | 0x4010_8000 |
| DOC | Data Operation Circuit | 0x4010_9000 |
| SCI0 | Serial Communication Interface 0 | 0x4011_8000 |
| SCI3 | Serial Communication Interface 3 | 0x4011_8300 |
| SCI4 | Serial Communication Interface 4 | 0x4011_8400 |
| SCI9 | Serial Communication Interface 9 | 0x4011_8900 |
| SPI0 | Serial Peripheral Interface 0 | 0x4011_A000 |
| SCE9 | Secure Cryptographic Engine | 0x4016_1000 |
| GPT321 | General PWM 32-Bit Timer 1 | 0x4016_9100 |
| GPT322 | General PWM 32-Bit Timer 2 | 0x4016_9200 |
| GPT164 | General PWM 16-Bit Timer 4 | 0x4016_9400 |
| GPT165 | General PWM 16-Bit Timer 5 | 0x4016_9500 |
| ADC120 | 12bit A/D Converter 0 | 0x4017_0000 |
| DAC12 | 12-bit D/A converter | 0x4017_1000 |
| FLAD | Data Flash | 0x407F_C000 |
| FACI | Flash Application Command Interface | 0x407F_E000 |
| QSPI | Quad-SPI | 0x6400_0000 |

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 3)

| Peripherals | Address | | Number of access cycles | | | | Cycle Unit | Related function |
|--|-------------|-------------|-------------------------|-----------------|---------------------------|----------------------|------------|--|
| | | | ICLK = PCLK | | ICLK > PCLK ^{*1} | | | |
| | From | To | Read | Write | Read | Write | | |
| RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU | 0x4000_0000 | 0x4000_6FFF | 2 | 2 | 2 | 2 | ICLK | Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller |
| CPSCU, DBG, FCACHE | 0x4000_8000 | 0x4001_CFFF | 4 | 3 | 4 | 3 | ICLK | CPU System Security Control Unit, Debug Function, Flash Cache |
| SYSC | 0x4001_E000 | 0x4001_E3FF | 5 | 4 | 5 | 4 | ICLK | System Control |
| SYSC | 0x4001_E400 | 0x4001_E5FF | 9 | 8 | 5 to 8 | 5 to 8 | PCLKB | System Control |
| PORTn, PFS | 0x4008_0000 | 0x4008_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Port n Control Registers, Pmn Pin Function Control Register |
| ELC, RTC, IWDTC, WDT, CAC | 0x4008_2000 | 0x4008_3FFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit |
| MSTP | 0x4008_4000 | 0x4008_4FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Module Stop Control |
| POEG | 0x4008_A000 | 0x4008_AFFF | 5 | 4 | 3 to 5 | 2 to 4 | PCLKB | Port Output Enable Module for GPT |
| USBFS | 0x4009_0000 | 0x4009_03FF | 6 | 5 | 3 to 6 | 3 to 5 | PCLKB | USB 2.0 FS Module |
| USBFS | 0x4009_0400 | 0x4009_04FF | 4 | 3 | 1 to 4 | 1 to 3 | PCLKB | USB 2.0 FS Module |
| IICn, IIC0WU | 0x4009_2000 | 0x4009_FFFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Inter-Integrated Circuit n, Inter-Integrated Circuit 0 Wake-up Unit |
| CANn | 0x400A_8000 | 0x400A_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | CANn Module |
| PSCU | 0x400E_0000 | 0x400E_0FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKB | Peripheral Security Control Unit |
| AGTn | 0x400E_8000 | 0x400E_8FFF | 7 | 4 | 5 to 7 | 2 to 4 | PCLKB | Low Power Asynchronous General purpose Timer n |
| CRC, DOC | 0x4010_8000 | 0x4010_9FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | CRC Calculator, Data Operation Circuit |
| SCIn | 0x4011_8000 | 0x4011_8FFF | 5 ^{*2} | 4 ^{*2} | 2 to 5 ^{*2} | 2 to 4 ^{*2} | PCLKA | Serial Communication Interface n |
| SPIn | 0x4011_A000 | 0x4011_AFFF | 5 ^{*3} | 4 ^{*3} | 2 to 5 ^{*3} | 2 to 4 ^{*3} | PCLKA | Serial Peripheral Interface n |
| SCE9 | 0x4016_1000 | 0x4016_1FFF | 6 | 4 | 3 to 6 | 2 to 4 | PCLKA | Secure Cryptographic Engine |
| GPT32n, GPT16n, GPT_OPS | 0x4016_9000 | 0x4016_9FFF | 7 | 4 | 4 to 7 | 2 to 4 | PCLKA | General PWM 32-Bit Timer n, General PWM 16-Bit Timer n, Output Phase Switching Controller |
| ADC12n, DAC12 | 0x4017_0000 | 0x4017_2FFF | 5 | 4 | 2 to 5 | 2 to 4 | PCLKA | 12bit A/D Converter n, 12-bit D/A converter |

Table 3.2 Access cycles (2 of 3)

| Peripherals | Address | | Number of access cycles | | | | Cycle Unit | Related function |
|-------------|-------------|-------------|-------------------------|----------|---------------------------|----------|------------|------------------|
| | | | ICLK = PCLK | | ICLK > PCLK* ¹ | | | |
| | From | To | Read | Write | Read | Write | | |
| QSPI | 0x6400_0000 | 0x6400_000F | 5 | 14 to *4 | 2 to 5 | 14 to *4 | PCLKA | Quad-SPI |
| QSPI | 0x6400_0010 | 0x6400_0013 | 25 to *4 | 6 to *4 | 25 to *4 | 5 to *4 | PCLKA | Quad-SPI |
| QSPI | 0x6400_0014 | 0x6400_0037 | 5 | 14 to *4 | 2 to 5 | 14 to *4 | PCLKA | Quad-SPI |
| QSPI | 0x6400_0804 | 0x6400_0807 | 4 | 3 | 1 to 4 | 1 to 3 | PCLKA | Quad-SPI |

Table 3.2 Access cycles (3 of 3)

| Peripherals | Address | | Number of access cycles | | | | Cycle Unit | Related function |
|-------------|-------------|-------------|-------------------------|-------|---------------------------|--------|------------|---|
| | | | ICLK = FCLK | | ICLK > FCLK* ¹ | | | |
| | From | To | Read | Write | Read | Write | | |
| FLAD, FACL | 0x407F_C000 | 0x407F_EFFF | 3 | 3 | 2 to 3 | 2 to 3 | FCLK | Data Flash, Flash Application Command Interface |

- Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
- Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in [Table 3.2](#). When accessing an 8-bit register (including FTDRH, FTDL, FRDRH, and FRDL), the access cycles are as shown in [Table 3.2](#).
- Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in [Table 3.2](#). When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in [Table 3.2](#).
- Note 4. The access cycles depend on the QSPI bus cycles.

Appendix 4. Related Documents

| Component | Document Type | Description |
|-------------------------|----------------------------------|--|
| Microcontrollers | Data sheet | Features, overview, and electrical characteristics of the MCU |
| | User's Manual: Hardware | MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions |
| | Application Notes | Technical notes, board design guidelines, and software migration information |
| | Technical Update (TU) | Preliminary reports on product specifications such as restriction and errata |
| Software | User's Manual: Software | Command set, API reference and programming information |
| | Application Notes | Project files, guidelines for software programming, and application examples to develop embedded software applications |
| Tools & Kits, Solutions | User's Manual: Development Tools | User's manuals and quick start guides for developing embedded software applications with Software Packages, Development Kits, Starter Kits, Promotion Kits, Product Examples, and Application Examples |
| | Quick Start Guide | |
| | Application Notes | Project files, guidelines for software programming, and application examples to develop embedded software applications |

Revision History

Revision 1.00 — September 15, 2021

First edition, issued

Revision 1.10 — February 4, 2022**1. Overview:**

- Added the introduction to 1.1 Function Outline.
- Removed the sentence on brushless DC motors from GPT functional description in Table 1.7 Timers.
- Added Table 1.11 I/O ports to 1.1 Function Outline.
- Fixed the note 1 in Figure 1.1 Block diagram.
- Fixed the row of QSPI in Table 1.13 Function Comparison.
- Added the row of I/O ports to Table 1.13 Function Comparison.
- Fixed the note 2 in Table 1.13 Function Comparison.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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