RASJ810
High Speed Low-Power Single Port

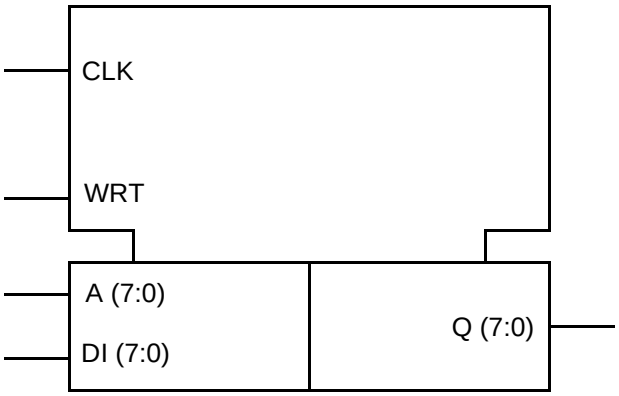
AMI5HG 0.5 micron CMOS Gate Array Memories

Features

- Self-timed design allows flexibility in clock duty cycle while maintaining fast cycle time
- 256 x 8 instantiation block
- Always active outputs
- Low standby power when the clock is stopped
- Separate input and output ports with full parallel access
- Altera Flex10 equivalent functionality
- Precharged design for faster operation with lower power consumption

FIGURE 1: LOGIC SYMBOL

RASJ810



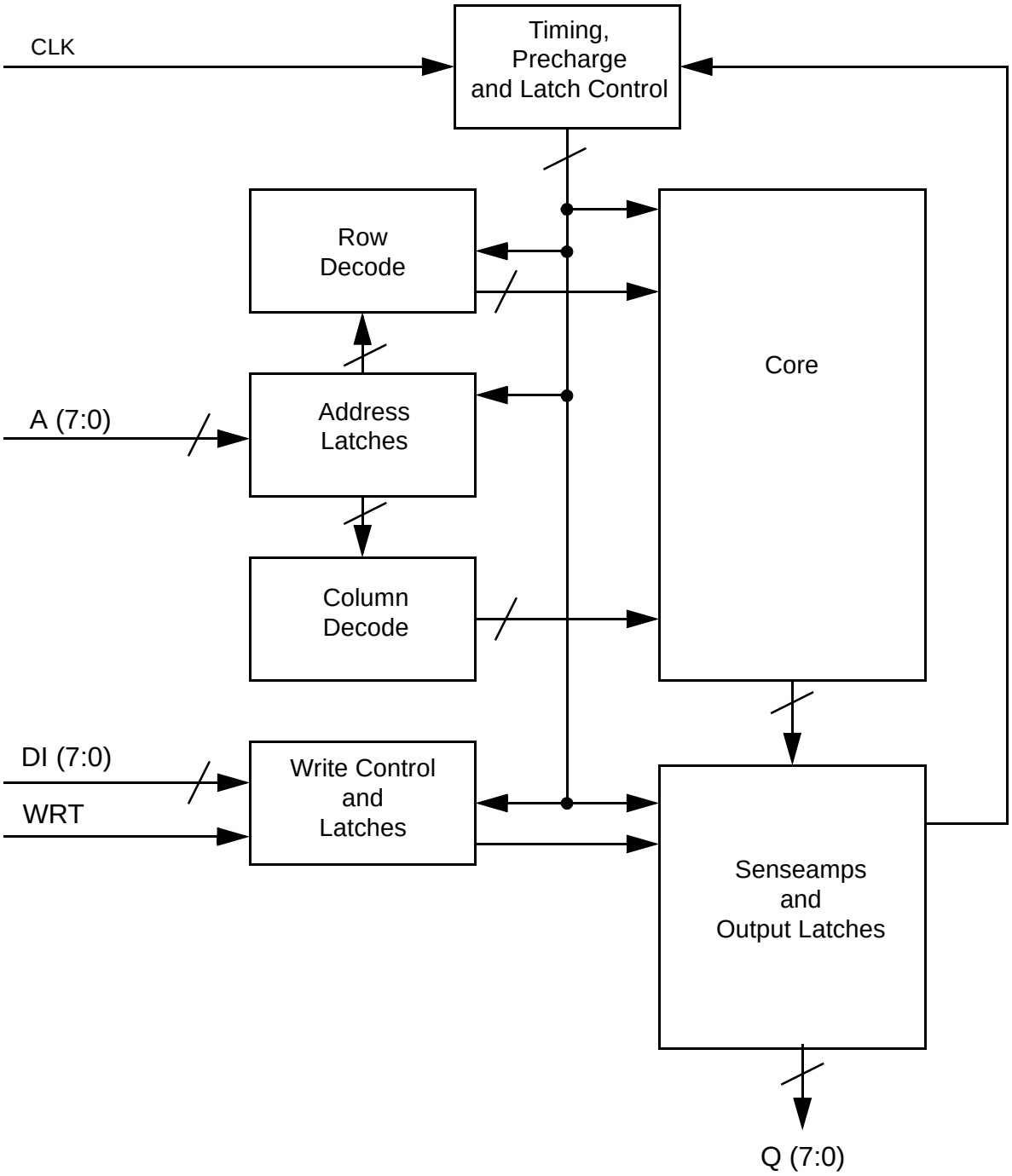
Note: A0 is the LSB.

RASJ810: High Speed Low-Power Single Port Description

This 256x8 SRAM block is built into AMI's base arrays. When your application requires static RAM memory, use these RAMs. The self timed feature of this RAM allows flexibility in the clock duty cycle while maintaining fast cycle times. All timing is relative to the risting edge of the clock input (CLK). When CLK rises, all inputs are latched and the READ or WRITE operation occurs. The RAM will stay in the READ mode and not start precharging until the READ operations is complete, even if CLK falls. The outputs become valid a short time after the rising edge of CLK and stay valid unil the next rising edge of CLK. All of the inputs including CLK can be held stable indefinately with no loss of memory as long as power is supplied to the RAM. See figure 2 for a block diagram of the RAM.

To obtain additional data or an EDA model contact your sales representative or the factory.

FIGURE 2: RAM BLOCK DIAGRAM



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Pin Loading (Equivalent Loads)

SIGNAL	TYPE	256 X 8	SIGNAL DESCRIPTIONS
Ai	I	2.81	Address inputs
CLK	I	11.91	Clock input
DI	I	2.81	Data inputs
WRT	I	2.81	Write control

Address and Word Size

PARAMETER	VALUE
Address inputs	8
Address locations (words)	256
Word size (data outputs)	8
Total bits in a core (word size times address locations)	2048

Area relative to a 2-Input Nand (eq gates)

256 x 8 : 8400

Bolt Syntax

Q (7) ... Q1 Q0 .RASj810 A(7) ... A1 A0 CLK DI(7) ... DI1 DI0 WRT;

Note: A0 is the LSB.

Power Dissipation

PARAMETER	256 X 8
Typical EQL_{pd} (Equivalent Power Dissipation Load)	1500
Typical Static I_{DD} (T_J = 85°C) (µA)	3.96 µA

See power notes in data book.

Testing Notes

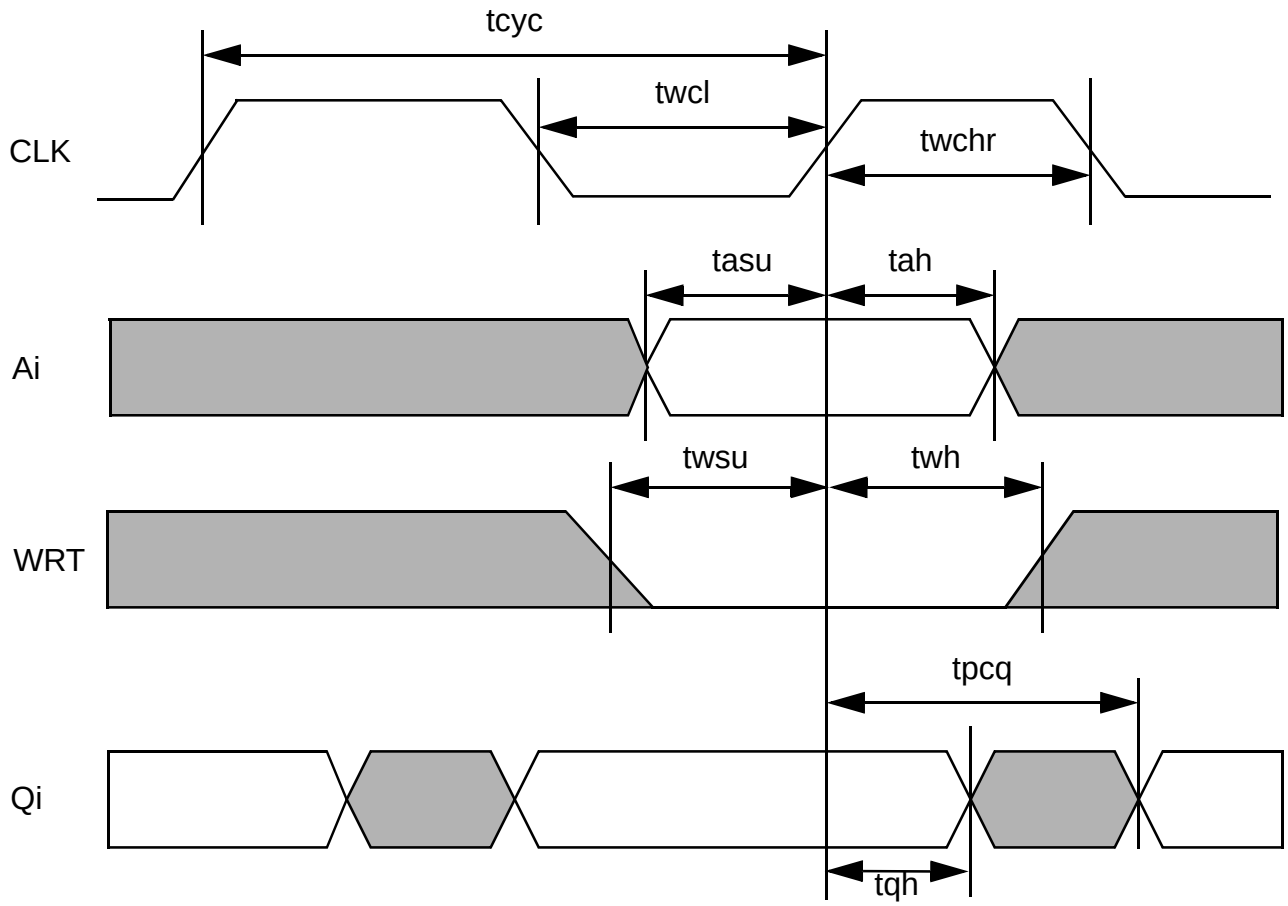
Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. The minimum pattern used to test a RAM should write and read both a zero and a one to every core bit. In addition, a variable pattern should be used to test for address decode faults and write disturb problems by writing the entire memory then reading it all back. One example of a variable pattern for these tests is to write the address value to each location. There are many methodologies for testing RAMs that have test time versus fault coverage trade-off. For more information on testing RAMs, refer to the AMI Application Note titled “Testing RAM Elements in IC Designs.”

Timing Characteristics: 256 X 8 @ Typical; Vdd = 5.0V

CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/EQL)	t(5EQL) (ns)
Min CLK high to CLK high cycle time	tcyc	4.17		
Min CLK width low	twcl	0.78		
Min CLK width high during read	twchr	1.49		
Min CLK width high during write	twchw	1.38		
Min address setup before CLK rises[1]	tasu	1.72		
Min address hold after CLK rises[1]	tah	-0.17		
Min WRT setup before CLK rises	twsu	0.06		
Min WRT hold after CLK rises	twh	-0.17		
Min data in setup before CLK rises	tdsu	0.10		
Min data in hold after CLK rises	tdh	-0.17		
Min Q hold after CLK rises	tqh	0.91		
Max CLK rise to Q valid	tpcq	3.61	0.03	3.31

Note: 1. If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it may not show corrupted data during a read cycle.

Read Cycle Timing



Write Cycle Timing