SHARP

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To;

SPECIFICATIONS

Product Type VIDEO PROCESSING IC FOR THE TFT LCD

Model No. RB5P006AM

※This specifications contains 52 pages including the cover and appendix.
If you have any objections,please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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● Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

1. General Description

The Sharp RB5P006AM is a video processing IC for the TFT color LCD panel using the source driver which power supply voltage is 5V. It converts composite video signals, Y/C separate video signals and RGB signals to the signals suited for the specific requirements of the TFT color LCD panel.

This IC has the serial data control function and it can simplify the external circuit drastically.

Features

- Low power consumption : 125mW (TYP.)
- Conforms to the source driver which power supply voltage is 5V.
- Supports composit video signals, Y/C separate video signals and analog RGB signals.
- Built-in common driver.
- Built-in automatic gain control circuit of Y signal (AGC level adjustment function is available).
- Built-in image enhancement circuit .
- Built-in gamma correction circuit.
- Built-in polarity inverting circuit.
- Blanking function is available.
- Contrast and brightness adjustment function is available.
- White balance adjustment function is available.
- Power save function is available.
- Serial data control interface.
- Built-in 15ch DAC.

*Not designed or rated as radiation hardened.	
*Package material:	Plastic
*Chip material and wafer substrate type:	P type silicon
*Number of pins and package type:	48-pin quad flat package (pin pitch 0.75mm)
*Process (Structure) :	Bipolar

Applications

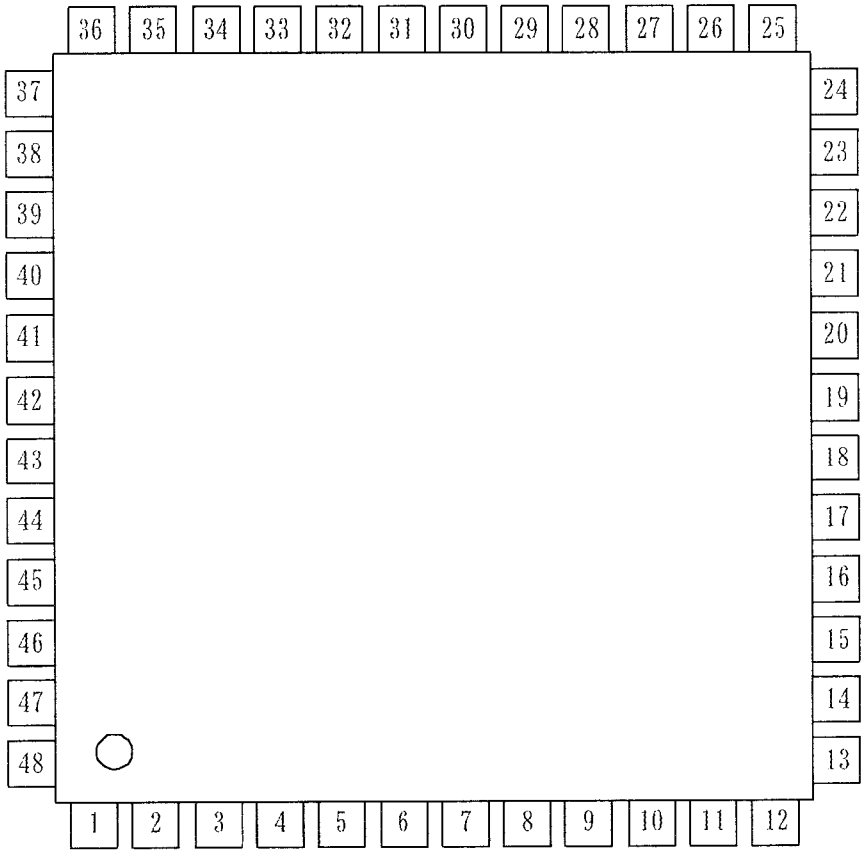
TFT LCD color monitors

2. Terminal Name

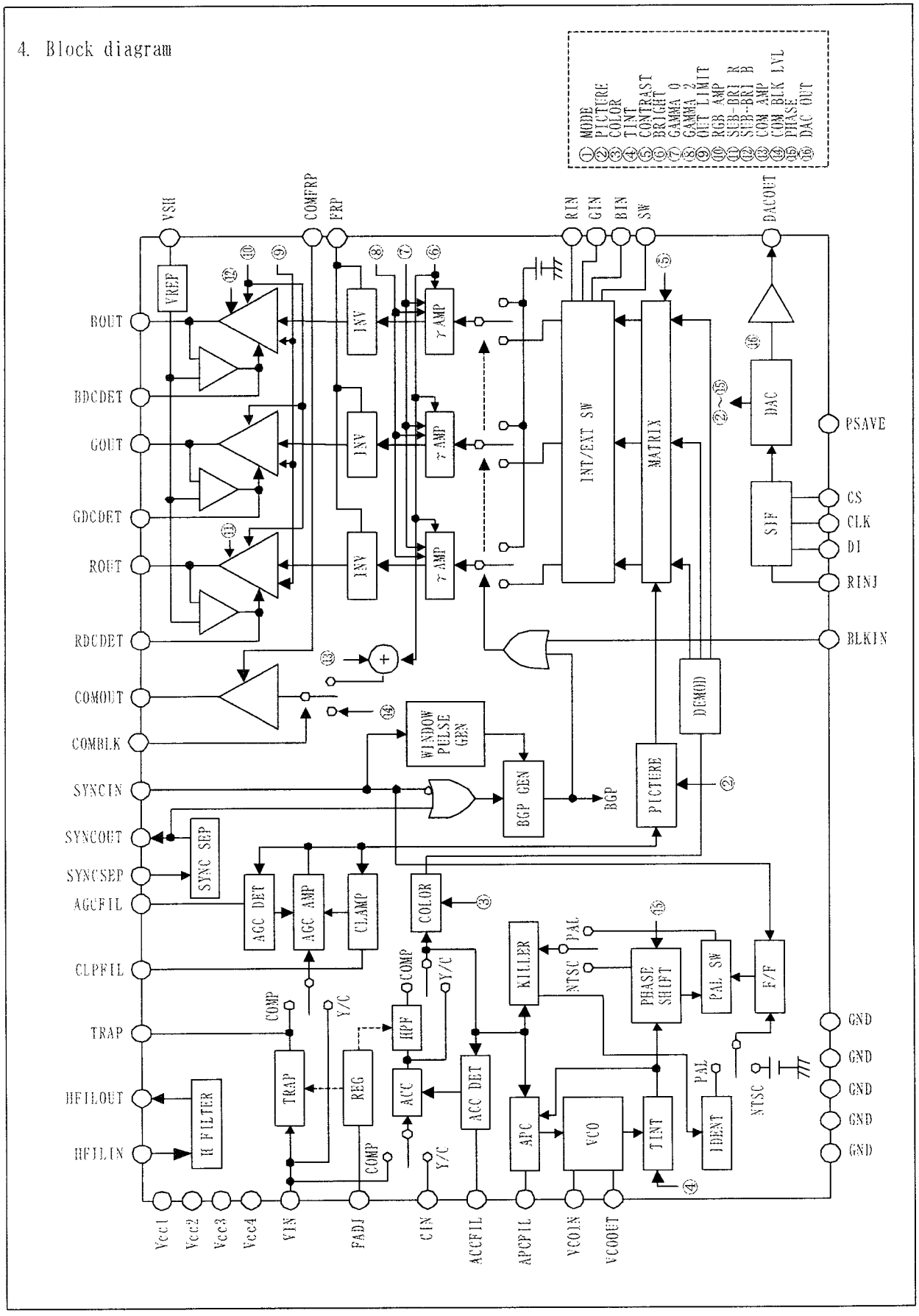
Pin No.	Terminal Name	Pin No.	Terminal Name	Pin No.	Terminal Name
1	CLK	17	FADJ	33	GOUT
2	DI	18	AGCFIL	34	RDCDET
3	RINJ	19	RIN	35	ROUT
4	ACCFIL	20	GIN	36	N. C.
5	CIN	21	BIN	37	Vcc2
6	Vcc1	22	SW	38	Vcc3
7	GND	23	BLKIN	39	COMOUT
8	Vcc4	24	VSH	40	GND
9	SYNCSEP	25	VCOIN	41	COMFRP
10	SYNCOUT	26	APCFIL	42	FRP
11	SYNCIN	27	VCOOUT	43	COMBLK
12	GND	28	BDCDET	44	DACOUT
13	VIN	29	BOUT	45	N. C.
14	PSAVE	30	GDCDET	46	HFILOUT
15	TRAP	31	GND	47	HFILIN
16	CLPFIL	32	GND	48	CS

※N. C. :Non Connection Terminal

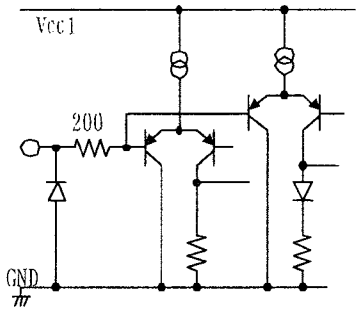
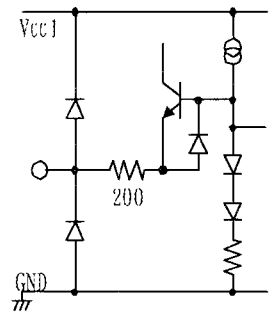
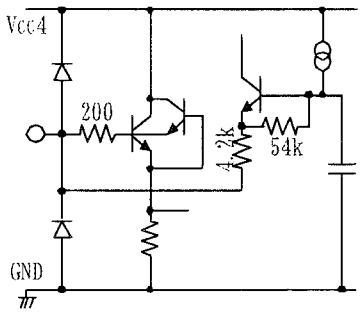
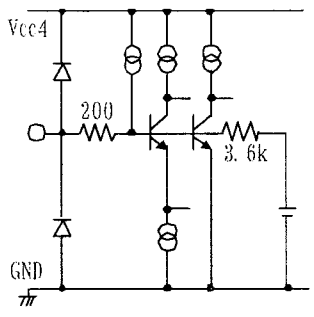
3. Terminal Connections

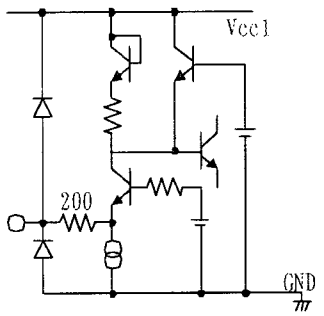
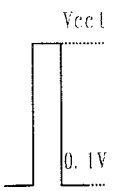
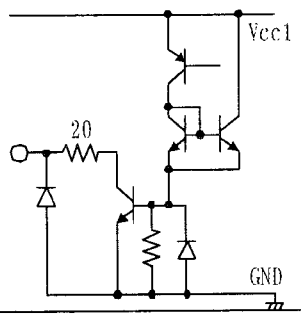
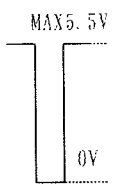
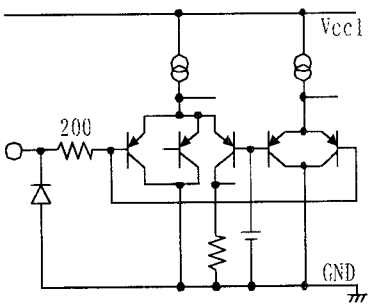


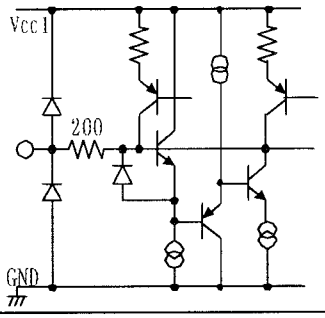
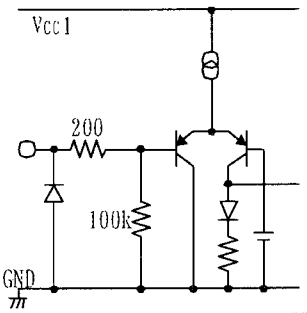
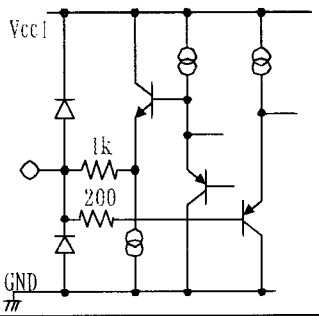
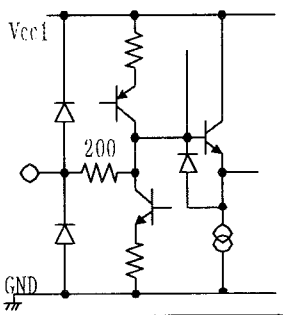
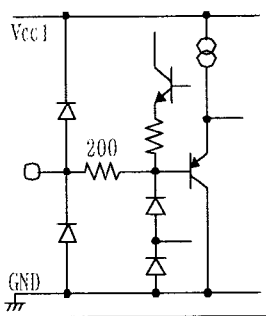
4. Block diagram

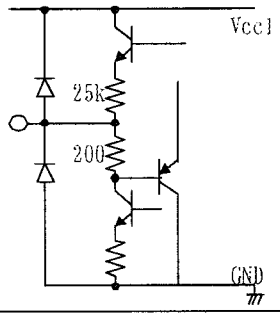
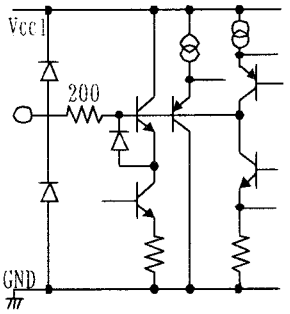
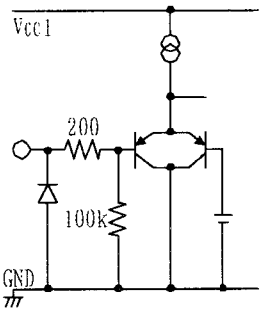
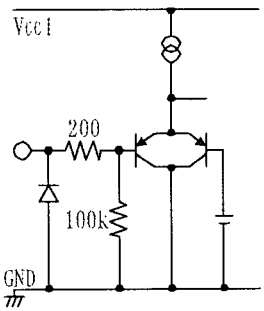
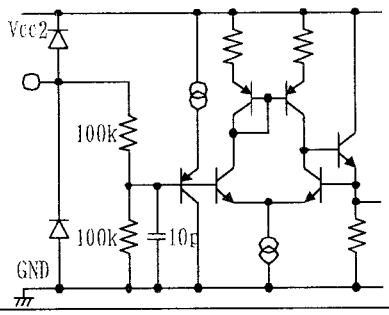


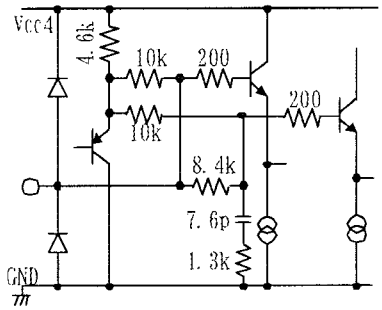
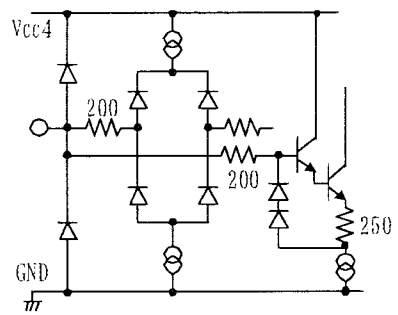
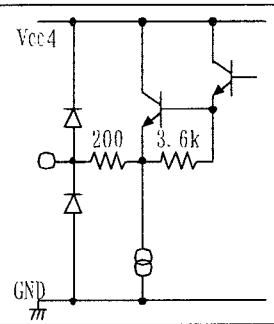
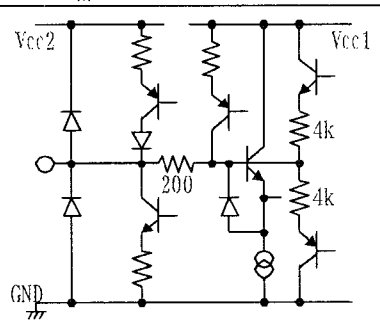
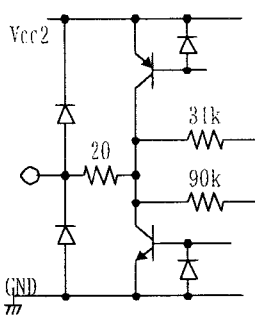
5. Description of terminals

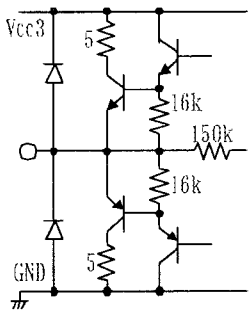
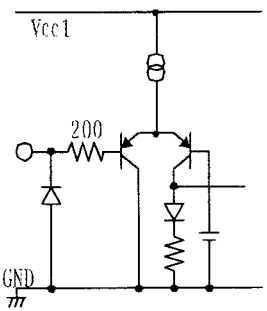
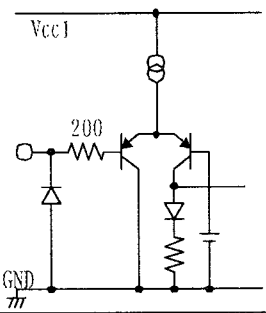
Term. No	Term. name	Voltage	Equivalent Circuit	Description
1	CLK	Threshold L→H: 1.6V H→L: 1.0V hysteresis input		This is the input terminal of the clock for the serial interface. The serial data is accepted at the rising edge of this clock.
2	DI			This is the input terminal of the data for the serial interface.
48	CS			This is the chip select terminal of the serial interface. When this is low, the serial data is acceptable.
3	RINJ	0.7V		The value of the resistor connected to this terminal decides the injection current of the serial interface logic circuit. Connect to GND via 15kΩ.
4	ACCFIL	1.8V (at typical color bar input)		This terminal is connected to the ACC detection filter.
5	CIN	2.55V		When using the Y/C video signal, input the chrominance signal.

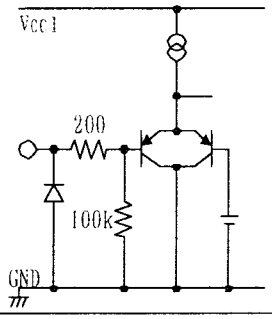
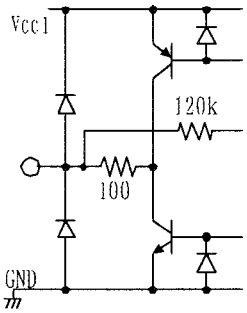
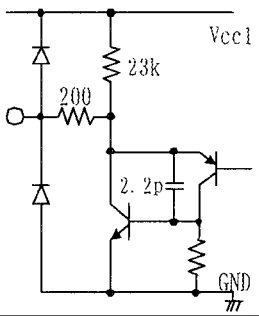
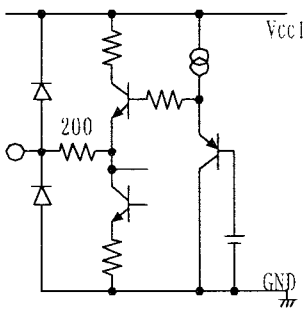
Term. No.	Term. name	Voltage	Equivalent Circuit	Description
6	Vcc1			This is the power supply terminal for the circuits except the RGB output circuits, the COM output circuit and the CHROMA signal processing circuits. Connect to the 3V power
7	GND			This is the GND terminal.
8	Vcc4			This is the power supply terminal for the CHROMA signal processing circuits. Connect to the 5V power supply.
9	SYNCSEP	1.1V		This is the input terminal for the sync separator circuit. Input the signal of the HFILOUT output. (Refer to the application circuit example)
10	SYNCOUT			This is the output terminal of the composite synchronizing pulse separated by the sync separator circuit. (Active High) Because of the output is provided by an open circuit, connect to Vcc via 1kΩ.
11	SYNCIN	Threshold 1.5V 		This is the input terminal of the horizontal synchronizing pulse. The rising edge of SYNCIN input pulse must be before the falling edge of SYNCOUT output pulse.
12	GND			This is the GND terminal.

Term. No	Term. name	Voltage	Equivalent Circuit	Description
13	VIN	1.8V		This is the input terminal of the composite video signal. (When using the Y/C video signal, input the luminance signal.)
14	PSAVE	Threshold 1.5V		This is the power down control terminal for the signal processing circuits. When this is low, this circuits turn off. Even at this time the memorized data is not initialized. This terminal is internally pulled down to GND at 100kΩ.
15	TRAP	1.0V		This terminal is connected to the TRAP filter. Output impedance:1kΩ
16	CLPFIL	2.0V		This is the connection terminal of the capacitors for the pedestal clamp of luminance signal. Because of the high impedance, use low leakage capacitors.
17	FADJ	1.2V		The resistor between this terminal and the ground adjusts the frequency characteristics of the inner filters. Usual resistance:100kΩ Resistance accuracy:±2%, Temp. stability:±200ppm/℃

Term. No	Term. name	Voltage	Equivalent Circuit	Description
18	AGCFIL	1.04V at the input P.30 SG3 (APL 50%)		This terminal is connected to the AGC detection filter for luminance signal.
19	RIN	1.8V		These are the input terminals for analog RGB signals.
20	GIN			
21	BIN			
22	SW	Threshold 1.5V		This terminal selects the input mode as follows: Hi: RGB input mode Lo or Open: composite or Y/C input mode This terminal is internally pulled down to GND at 100kΩ.
23	BLKIN	Threshold 1.5V		This is the input terminal of the blanking pulse. The RGB output signals turn to pedestal level when this terminal is high level. This terminal is internally pulled down to GND at 100kΩ.
24	VSH			The voltage of this terminal decides the central voltage of the RGB output. The central voltage of the RGB output is regulated to become half of the voltage of this terminal. Connect to the power supply of the source driver.

Term. No	Term. name	Voltage	Equivalent Circuit	Description
25	VCOIN	4.2V		This is the input terminal of the VCO circuit.
26	APCFIL	2.3V		This terminal is connected to the APC detection filter.
27	VCOOUT	2.7V		This is the output terminal of the VCO circuit.
28 30 34	BDCDET GDCDET RDCDET	1.8V		These are the connection terminals of the smoothing capacitors of the feedback circuits which control the DC levels of the RGB output signals. Connect to GND via the capacitor. Use low leakage capacitors.
29 33 35	BOUT GOUT ROUT	VSH/2 (central voltage)		These are the output terminals of the LCD compliant RGB signals.

Term. No	Term. name	Voltage	Equivalent Circuit	Description
31	GND			This is the GND terminal.
32	GND			This is the GND terminal.
37	Vcc2			This is the power supply terminal for the RGB output circuits. Connect to the 5V power supply.
38	Vcc3			This is the power supply terminal for the COM output circuit. Connect to the 13V power supply.
39	COMOUT	Vcc3/2 (central voltage)		This is the output terminal of the COM signal. This output can drive a capacitive load up to 12000pF directly.
40	GND			This is the GND terminal.
41	COMFRP	Threshold 1.5V		This is the input terminal of the polarity control pulse for the COM output. The COM output voltage becomes high when this is low and becomes low when this is high.
42	FRP	Threshold 1.5V		This is the input terminal of the polarity control pulse for the RGB outputs. The RGB outputs is inverted when this is low and not inverted when this is high.

Term. No.	Term. name	Voltage	Equivalent Circuit	Description
43	COMBLK	Threshold 1.5V		This is the input terminal of the blanking pulse for the COM output. When this is high, the COM output is blanked. This terminal is internally pulled down to GND at 100kΩ.
44	DACOUT			This is the output terminal of the voltage adjusted by the internal DAC (DAC OUT).
46	HFILOUT			The synchronizing area of the signal applied to Pin 47 for sync separator circuit, is amplified, then pass through the LPF, and then output from this terminal.
47	HFILIN			This is the input terminal for the HFILTER. Input the same signal applied to Pin 13. The tip of the synchronizing signal is clamped by an external capacitor.

7. Functional Operation

・Video AGC circuit

This circuit makes a gain change corresponding to the APL level of the luminance signal.

This circuit prevents the image from being whitish or being blackish.

・TRAP

In the case of the composite video input, the TRAP rejects the chroma signal from the luminance signal.

The frequency of the TRAP is switched between 3.58MHz (NTSC) and 4.43MHz (PAL).

For the Y/C input, the signal does not pass through the TRAP.

・ACC detector, ACC amplifier

The ACC circuit detects the peak of the amplitude of the burst signal to form the ACC loop.

・VCO, APC detector

The local oscillator circuit (VCO) is a pierce type X'tal oscillator circuit.

The APC and the VCO form the PLL loop to eliminate the adjustment work.

The APC detector compares the phase of the burst signal with that of the VCO oscillator output, and regulates the oscillation frequency of the VCO.

・RGB inputs

Because the each terminal of the RGB inputs is clamped, the signal is required to be AC coupled.

When giving the "Hi" level to the SW input, the RGB inputs are valid, and when giving the "Lo" level to it or opening it, the composite or Y/C input is valid. The RGB inputs accept the analog signals.

・Gamma correction

The relations while the inputted signal and the outputted signal are made nonlinear as the figure 1 to make it cope with the character of the LCD panel. Relative relations with GAMMA1 and GAMMA0 can be adjusted by built-in DAC [GAMMA0]. And relative relations with GAMMA1 and GAMMA2 can be adjusted by built-in DAC [GAMMA2].

The position of PEAKLIMIT follows the position of GAMMA2.

When built-in DAC [BRIGHT] is made to change, the position of all the tune points (GAMMA0, GAMMA1, GAMMA2, PEAKLIMIT) changes at the same time.

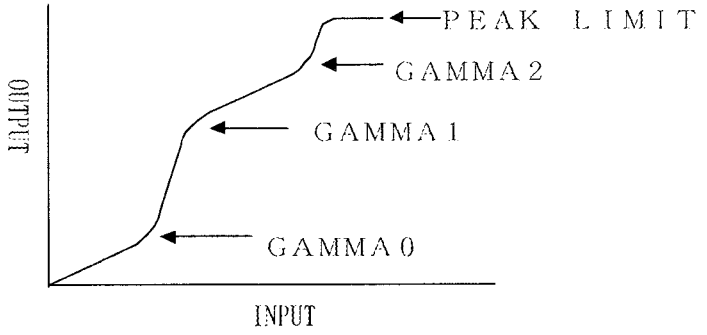
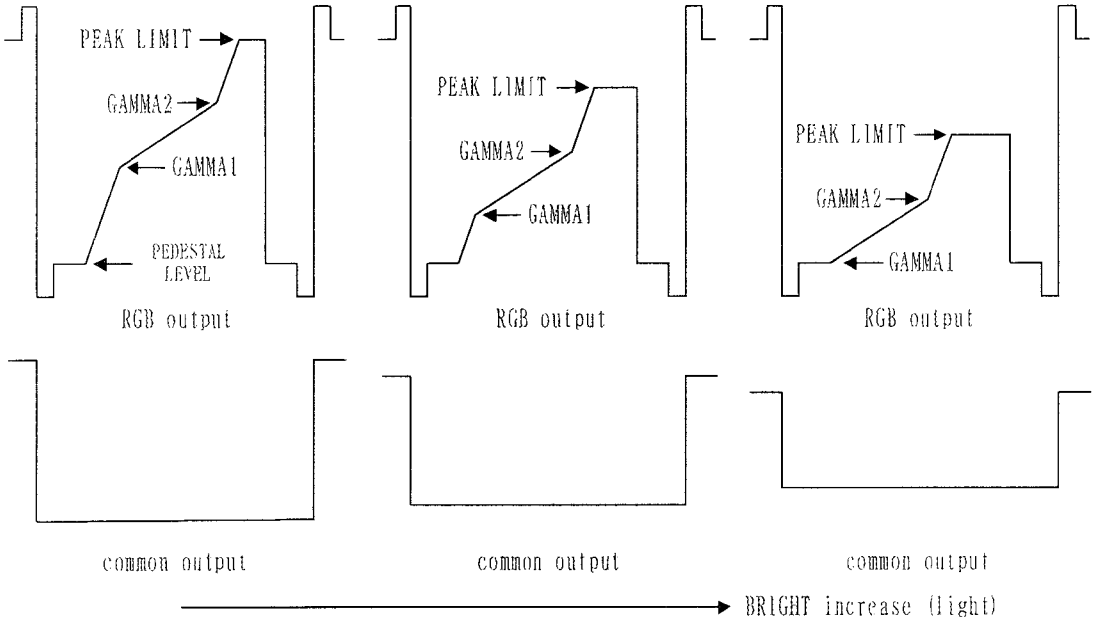


FIGURE 1

· Bright adjustment

When built-in DAC [BRIGHT] is made to change, the gamma compensation point of the RGB output and the voltage of the common output change as the figure 2. The relations between the voltage of the common output and the gamma compensation point can be adjusted by built-in DAC [COM AMPLITUDE].



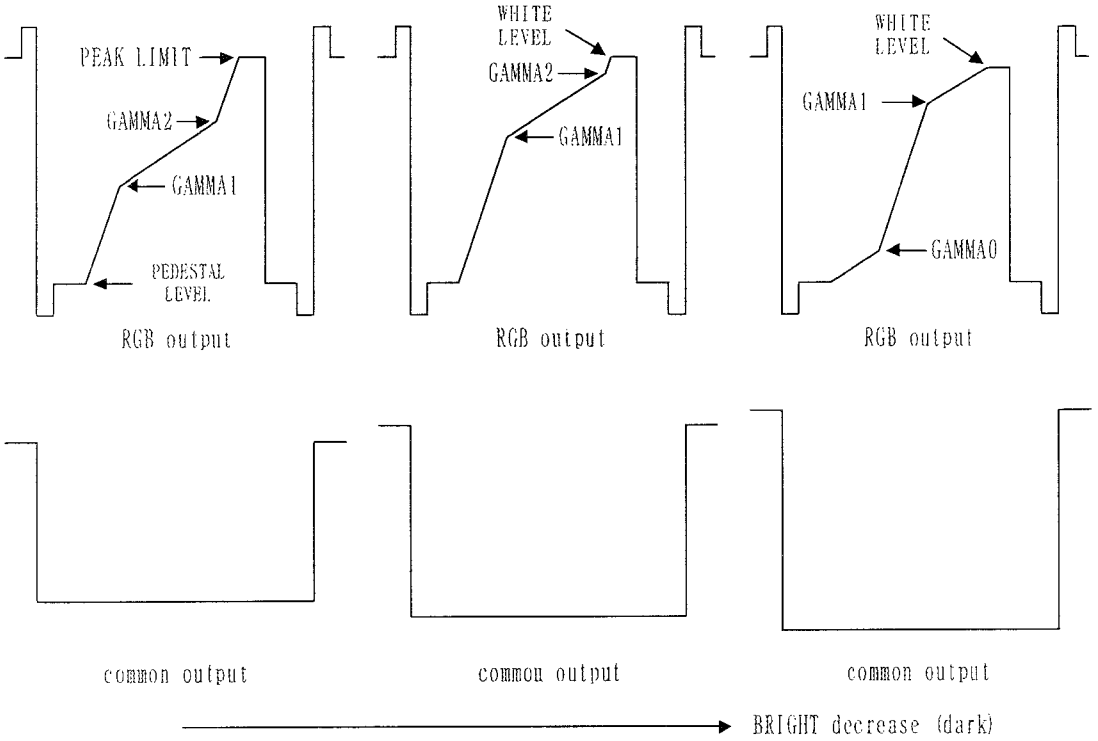


FIGURE 2

· RGB outputs

The pulse turned over by every horizontal period is inputted to the FRP terminal, and the polarity of the RGB output is turned over as the figure 3 by every horizontal period. The feedback loop makes the DC voltage of the output signal to 1/2 of the voltage of the VSH terminal.

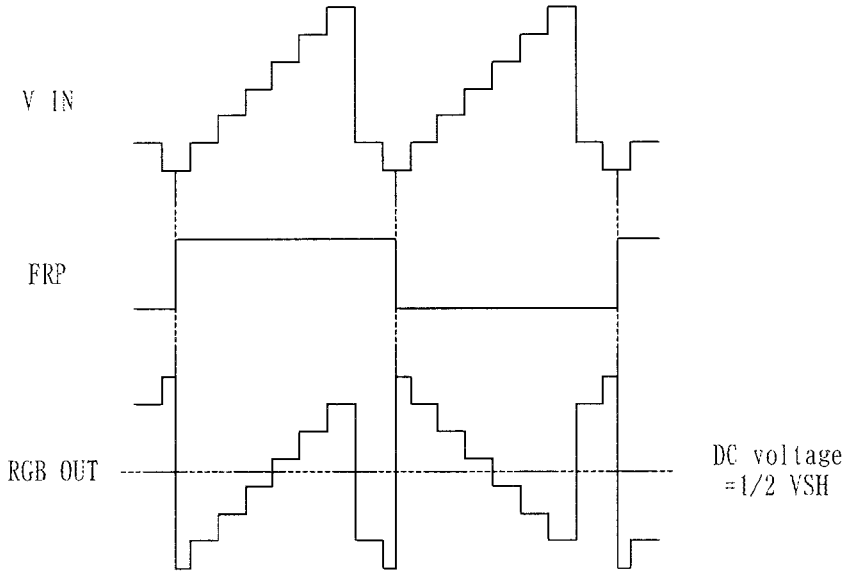


FIGURE 3

· Wide screen mode

A black mask territory can be inserted over and under the LCD screen. Make the BLKIN terminal high in the period which wants to make a black mask.

A black mask territory without an influence of built-in DAC [BRIGHT] is made by applying High level to COMBLK terminal at the suitable timing.

· About common output

COMOUT output can drive a capacitive load up to 12,000pF directly.

In the case of driving a capacitive load more than 12,000pF, connect to the external buffer amplifier.

· Color burst mask function

This IC clamps the pedestal level of the non-reversal period of the RGB outputs at the RGB outputs stage to stabilize the pedestal level of the RGB outputs.
But when a color burst pulse is remaining in the clamp period of the image signal, the pedestal level changes by every frame, and there is a possibility that a screen flickers. To avoid this, a blanking pulse is internally generated in the clamp period, and the image signal of the clamp period is masked in the black level.

When it is usually used, a BSTMASK bit is made '1' (the image signal is masked in the black level.

· Power save function

The electric power of the signal processing circuits are cut down by making the PSAVE terminal low.

Even at this time the memorized data on built-in DAC do not change.

・About the internal clamp pulse

Internal clamp pulse, which width is 3μs* (typically), rises when the SYNC OUT pulse falls. The clamp pulse is able to generate during the WINDOW pulse is "Hi", that is 6μs* (typically) after SYNC IN pulse rises (Figure 4).

・The timing of the SYNC IN pulse

The SYNC IN pulse must be synchronized with HD.

Make sure the rising edge of SYNC IN is not behind the falling edge of SYNC OUT, because the black level might not be provided precisely if the picture area of the video signal is clamped (Figure 4).

Make sure the falling edge of SYNC IN does not cover the end of the picture area of the video signal, to avoid vertical lines on the LCD panels (Figure 4).

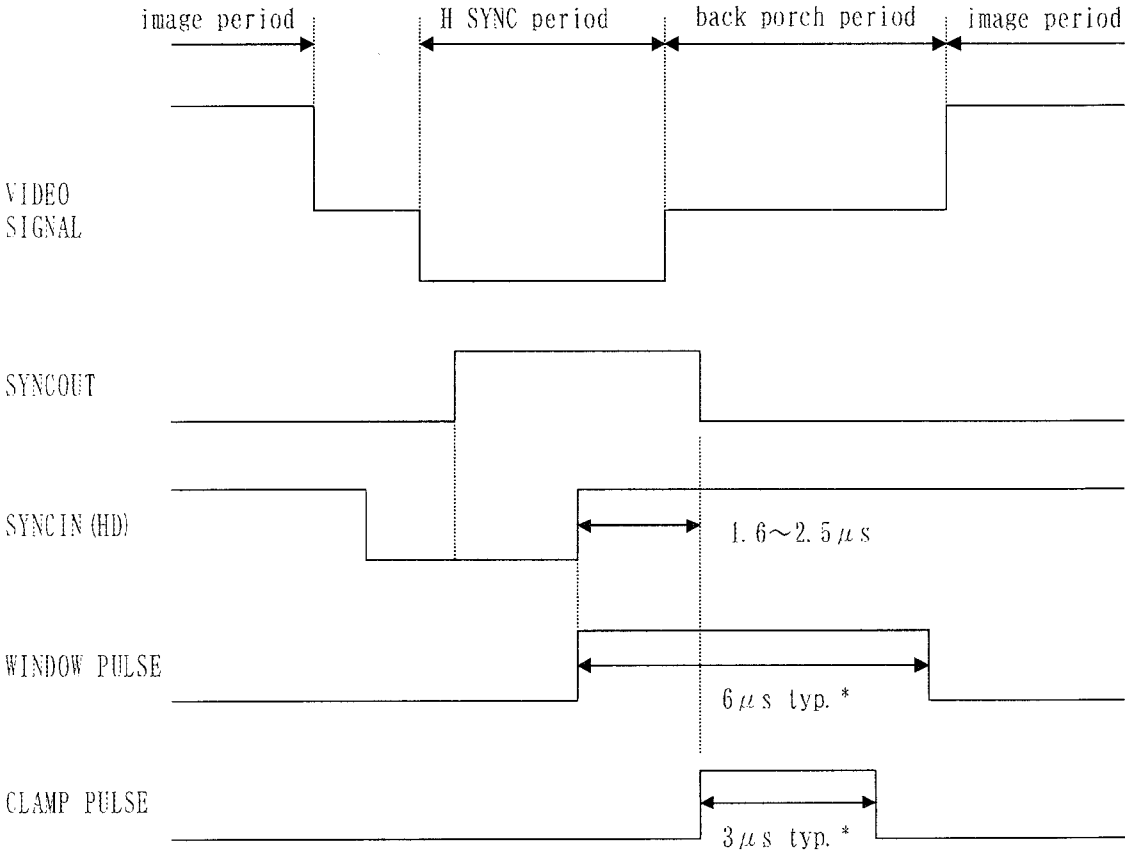


FIGURE 4

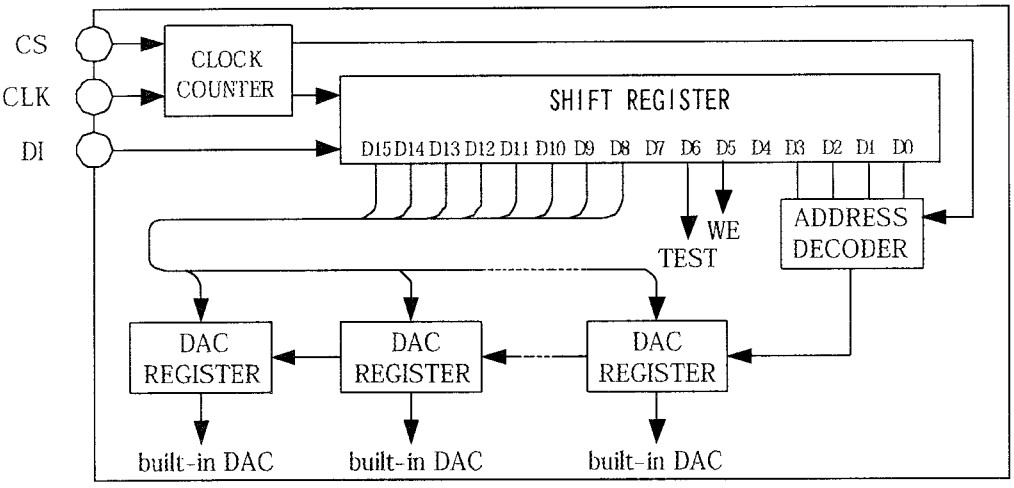
* It is the value when the external resistance of 100kΩ is connected with the FADJ terminal.

・Serial interface logic circuit

The serial interface logic circuit is composed by the I^2L logic circuit that decodes and memorizes the serial data, and the D/A converter circuit which gives each department an adjustment voltage.

When the power is turn on, the value of the register is initialized (refer P. 17).

SERIAL INTERFACE LOGIC CIRCUIT BLOCK DIAGRAM

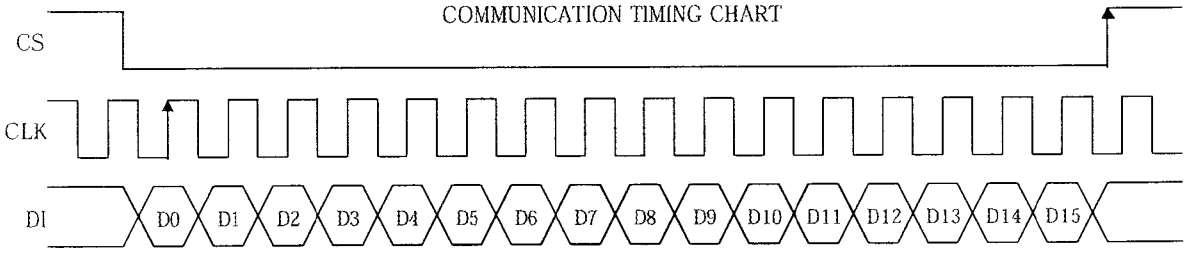


① Serial communication timing

A DI signal is taken in the shift register at the timing when a CLK signal stands up. The data taken in the shift register are transferred to the DAC register at the timing when a CS signal stands up.

The data are abandoned when the data taken in the shift register are less than 16 bits. When the data exceeds 16 bits, the last 16 bits taken in will be effective.

COMMUNICATION TIMING CHART



② Construction of the serial data

The construction of the serial data which input DI terminal, is shown in the following.

First LSB — Last MSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
REGISTER ADDRESS				*1	*2	*3	*1	DATA							

*1:Don't care *2:Writing permission bit *3:DAC test bit

REGISTER NAME	ADDRESS D0	D1	D2	D3	RESOLUTION	THE ACTION WHEN VALUE INCREASED	VALUE IN RESETTING D8·····D15							
INPUT MODE/SW	0	0	0	0	6 (D8～D14)	※1	0	0	1	0	1	0	–	–
PICTURE	1	0	0	0	6 (D8～D13)	PICTURE → SHARP	0	0	0	0	0	1	–	–
COLOR	0	1	0	0	8 (D8～D15)	COLOR → DEEP	0	0	1	0	1	1	1	0
PHASE	1	1	0	0	6 (D8～D13)	R-Y/B-Y PHASE → LARGE	0	0	0	0	0	1	–	–
CONTRAST	0	0	1	0	8 (D8～D15)	CONTRAST → STRONG	0	0	0	1	1	0	0	1
BRIGHT	1	0	1	0	8 (D8～D15)	BRIGHTNESS → LIGHT	0	0	0	0	0	0	0	1
GAMMA 0	0	1	1	0	8 (D8～D15)	SEPARATE FROM γ1→ LARGE	0	0	0	0	1	0	1	0
GAMMA 2	1	1	1	0	8 (D8～D15)	SEPARATE FROM γ1→ LARGE	0	0	0	0	0	0	1	0
OUT LIMIT	0	0	0	1	5 (D8～D12)	AMPLITUDE → SMALL	0	1	0	0	1	–	–	–
RGB AMPLITUDE	1	0	0	1	8 (D8～D15)	AMPLITUDE → LARGE	0	0	0	0	0	1	0	1
SUB-BRIGHT R	0	1	0	1	8 (D8～D15)	RED AMPLITUDE→LARGE	0	0	0	0	0	0	0	1
SUB-BRIGHT B	1	1	0	1	8 (D8～D15)	BLUE AMPLITUDE→LARGE	0	0	0	0	0	0	0	1
COM AMPLITUDE	0	0	1	1	8 (D8～D15)	AMPLITUDE → LARGE	0	0	0	0	1	0	0	1
COM BLACK LEV	1	0	1	1	5 (D8～D12)	AMPLITUDE → SMALL	0	0	0	0	1	–	–	–
DAC OUT	0	1	1	1	8 (D8～D15)	VOLTAGE → HIGH	0	0	0	0	0	0	0	1
TINT	1	1	1	1	8 (D8～D15)	TINT → GREEN	0	0	0	0	0	0	0	1

※1 THE CONSTRUCTION OF THE INPUT MODE/SW REGISTER

bit	FUNCTION NAME	EXPLANATION
D8	XCOP	Input mode choice. 0:COMPOSIT VIDEO INPUT 1:Y/C VIDEO INPUT
D9	PNS	PAL / NTSC mode choice. 0:NTSC 1:PAL
D10	AGCL0	AGC level set
D11	AGCL1	AGC level set
D12	BSTMASK	COLOR BURST MASKING function enable. 0:OFF 1:ON
D13	GAMTEST	TEST function for gamma adjustment enable. When this is turned on, an image signal is restricted in a gamma 1 point. 0:OFF 1:ON
D14	(Don't care)	
D15	(Don't care)	

· About the DAC test bit (D6) and the writing permission bit (D5).

When a D6 bit is '1', the voltage set up in the register chosen with D0-D3 is outputted in the DACOUT terminal.

When a D5 bit is '0', data are not written in the register.

The voltage set up in the register can be confirmed without changing the value of the register when a D5 bit is made '0' and a D6 bit is made '1'.

When the value of the register is 0, the voltage outputted in the DACOUT terminal rises most. But, as for the DACOUT register, the lowest voltage is outputted when the value is 0.

When a D6 bit is '0', the voltage set up in the register is outputted in the DACOUT terminal.

When it is usually used, a D5 bit is made '1', and a D6 bit is made '0'.

7. Precautions

- Power supply pins
  All GND terminals (Pin 7, 12, 31, 32, and 40) must be at the same potential. Every wiring patterns from a bypass capacitor to Vcc or GND must be thick and short as much as possible.

- RINJ terminal
  A long, noise sensitive wiring of RINJ terminal may cause a malfunction at maximum clock rate of the serial interface. Connect 4.7kΩ resistor and 0.1μF capacitor in series between RINJ and GND (parallel connected to 15kΩ resistor of RINJ) to avoid this situation.

- White balance adjustment
  Adjusting built-in DAC [SUB-BRIGHT R] [SUB-BRIGHT B] or other white balance for each every product is recommended. Otherwise, the white balance of eachevery product may be uneven because of the deviation of the electrical parts.

- COM amplitude adjustment
  Adjusting built-in DAC [COM AMPLITUDE] for every product is recommended. Otherwise, the brightness of each product may be uneven because of the deviation of the amplitude of the COMOUT output.

- RGB output amplitude
  Do not set the black limit level of the non-inverted RGB output under 0.2V by adjusting built-in DAC [RGB AMPLITUDE] [OUT LIMIT]. If the minimum voltage level becomes under 0.2V, the waveform on inversion and non-inversion become asymmetric by transistors' saturation, which results central voltage stabilize circuit or other circuit operates wrong.

- Bright adjustable range (GAMMA0 variable range)
  In the case of varying the built-in DAC [BRIGHT], make the GAMMA0 point of the RGB output be below 1V above the pedestal level, to avoid clamp failed.

- Input of the signal
  Synchronize all the input signals connected to the IC.

- Input signals that are unusual
  Be careful to input signals which luminance changes each horizontal period (for instance, signals that repeats black level invert output and white level non-invert output), because irregular output might occur. This irregular output may be eased by increasing the capacitance connected to the DCDET terminals. Although it will take more time to stabilize the screen after the power is on.

- Sync separator input
  Make the impedance of the signal source connected to the sync-separator input as low as possible. Otherwise, the ability of the sync-separator may decrease.

- FADJ terminal (pin 17)
  Because the impedance of this terminal is high, the crosstalk with neighboring signal lines may occur. Therefore, place the resistor connected to this terminal by the IC and design the PWB patterns in order to minimize the crosstalk.

- SYNCIN (pin 11)
  The horizontal synchronizing pulse synchronized with the output pulse of SYNCOUT (pin 10) must be applied to pin 11.

- POWER SAVE
  When PSAVE is on, make sure a current doesn't flow into IC from the RGB outputs.

- Circuits surrounding VCO
  Performance of the X'tal oscillator required is as follows.
  a. Load capacitance 16pF
  b. Frequency tolarance ±30ppm
  c. Temperature stability ±30ppm
  d. Frequency characteristics comparable to AT-49 of DAISHINKU CORPORATION
  Wiring between VCOIN (terminal 25) and X'tal oscillator should be made to keep the capacitive effect to minimum.

- Crosstalk between inputs
  A high frequency signal should not input into the input terminal of the side which is not chosen with SW terminal, because the cross talk waveform of RGB outputs may appear by leak lump of the signal from RGB inputs side at the time of composite video input mode selection, and from composite video input side at the time of RGB inputs mode selection.

8. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC1}		-0.3 ~ 4	V
	V_{CC2}		-0.3 ~ 7	V
	V_{CC3}		-0.3 ~ 16.5	V
	V_{CC4}		-0.3 ~ 7	V
Power dissipation	P_D	Ta≦25℃	725	mW
Derating ratio	ΔP_D	Ta>25℃	5.8	mW/℃
Operating temperature range	T_{opr}		-30 ~ 85	℃
Storage temperature range	T_{stg}		-55 ~ 150	℃
SYNC IN input signal voltage			GND-0.3 ~ 6	V
SYNC OUT output withstand voltage			7	V
COM FRP input signal voltage			GND-0.3 ~ 6	V
FRP input signal voltage			GND-0.3 ~ 6	V
COM BLK input signal voltage			GND-0.3 ~ 6	V
BLACK IN input signal voltage			GND-0.3 ~ 6	V
CLK, DI, CS input signal voltage			GND-0.3 ~ 6	V
VSH input signal voltage			GND-0.3 ~ Vcc2+0.3	V

9. Recommended Operating Conditions

Parameter	Symbol	Condition	Rating			Unit
			MIN.	TYP.	MAX.	
Operating supply power voltage	V_{CC1}		2.7	3	3.6	V
	V_{CC2}		4.5	5	5.5	V
	V_{CC3}		11	13	15.5	V
	V_{CC4}		4.5	5	5.5	V
Composite video signal input voltage	V_{CMP}	B/W amplitude at 100% color bar input	0	0.35	0.45	V_{P-P}
Y signal input voltage	V_Y	B/W amplitude at 100% color bar input	0	0.35	0.45	V_{P-P}
C signal input voltage	V_C	Burst amplitude at 100% color bar input	0	0.15	0.3	V_{P-P}
RGB signal input voltage	V_{RGB}	B/W amplitude at 100% color bar input	0	0.7	1	V_{P-P}
VSH terminal voltage	VSH		2.7	-	Vcc2	V

10. Electrical Characteristics

DC Characteristics
Unless otherwise specified : Ta=25℃, Vcc1=3V, Vcc2=Vcc4=5V, Vcc3=13V, VSH=5V

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Current supply 1	ICC1	3V power supply current, Vcc1.		21	30	mA
Current supply 2	ICC2	5V power supply current, Vcc2.		4.5	6.6	mA
Current supply 3	ICC3	13V power supply current, Vcc3.		0.3	0.5	mA
Current supply 4	ICC4	5V power supply current, Vcc4.		7.0	10.2	mA
Current supply 1 (At the signal processor is powered down)	IPSP1	P SAVE=0, 3V power supply current.		4.9	7.2	mA
Current supply 2 (At the signal processor is powered down)	IPSP2	P SAVE=0, 5V power supply current.		39	65	μA
Current supply 3 (At the signal processor is powered down)	IPSP3	P SAVE=0, 13V power supply current.		26	43	μA
Current supply 4 (At the signal processor is powered down)	IPSP4	P SAVE=0, 5V power supply current.		93	155	μA
RINJ terminal voltage	V3		0.4	0.7	1.0	V
CIN terminal voltage	V5		2.3	2.6	2.9	V
VIN terminal voltage	V13		1.5	1.8	2.1	V
FADJ terminal voltage	V17		0.9	1.2	1.5	V
RIN terminal voltage	V19		1.5	1.8	2.1	V
GIN terminal voltage	V20		1.5	1.8	2.1	V
BIN terminal voltage	V21		1.5	1.8	2.1	V
BDCDET terminal voltage	V28		1.5	1.8	2.1	V
GDCDET terminal voltage	V30		1.5	1.8	2.1	V
RDCDET terminal voltage	V34		1.5	1.8	2.1	V
HFILOUT terminal voltage	V46		1.88	2.18	2.48	V
CLK terminal current	IL1	CLK = 0V.		-0.8	-4.0	μA
DI terminal current	IL2	DI = 0V.		-0.8	-4.0	μA
SYNCIN terminal current	IL11	SYNCIN = 0V.		-0.4	-1.0	μA
APCFIL terminal current	IL26	APCFIL = 0V.		-0.1	-1.0	μA
COMFRP terminal current	IL41	COMFRP = 0V.		-0.1	-1.0	μA
FRP terminal current	IL42	FRP = 0V.		-0.1	-1.0	μA
CS terminal current	IL48	CS = 0V.		-0.8	-4.0	μA
PSAVE input impedance	Z14		70	100	130	kΩ
TRAP input impedance	Z15		0.7	1	1.3	kΩ
SW input impedance	Z22		70	100	130	kΩ
BLKIN input impedance	Z23		70	100	130	kΩ
COMBLK input impedance	Z43		70	100	130	kΩ

AC characteristics

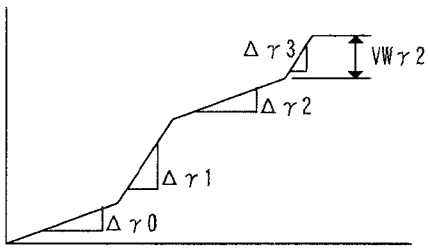
Unless otherwise specified : Ta=25℃, Vcc1=3V, Vcc2=Vcc4=5V, Vcc3=13V.
TP11=SG1, TP22=0V, TP41=TP42=SG2.
SW4→ON, SW5→a, SW9→ON, SW10→ON, SW16→ON, SW26→ON, the other is OFF.
DAC setting is CONTRAST=70h, BRIGHT=00h, GAMMA0=GAMMA2=FFh, OUT LIMIT=00h, COLOR=58h, and RGB AMPLITUDE=FFh, the other is preset value. ('h' means hexadecimal).
The sensitivity of each DAC is measured at the center of setting range.

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
AGC amplitude characteristics	AGC LEV0	VA10	INPUT MODE/SW=10h, RGBAMP=FFh, TP13=SG3. Measure the amplitude of TP33 from the pedestal level to the fourth step. VA10:APL10%, VA20:APL50%, VA30:APL90%	1.5	2.0	2.6	Vp-p
		VA20		1.2	1.6	2.1	
		VA30		1.0	1.4	1.9	
	AGC LEV1	VA11	INPUT MODE/SW=14h. Measuring condition is same as AGC LEV0.	2.0	2.7	3.6	
		VA21		1.6	2.2	2.9	
		VA31		1.1	1.5	2.0	
	AGC LEV2	VA12	INPUT MODE/SW=18h. Measuring condition is same as AGC LEV0.	2.5	3.4	4.4	
		VA22		2.1	2.9	3.8	
		VA32		1.3	1.8	2.4	
	AGC LEV3	VA13	INPUT MODE/SW=1Ch. Measuring condition is same as AGC LEV0.	2.9	3.9	4.7	
		VA23		2.7	3.6	4.6	
		VA33		1.6	2.2	2.9	
Image quality control variable range	NTSC	GpCN1	PICTURE=00h, TP13=SG4, SW33→ON. Sign wave amplitude ratio of TP33 (loaded 100pF) when SG4 is 100kHz to 2.0MHz.	-11	-7	-3	dB
		GpCN2	PICTURE=3Fh	2	6	10	
	PAL	GpCP1	INPUT MODE/SW=16h, PICTURE=00h	-9	-5	-1	
		GpCP2	INPUT MODE/SW=16h, PICTURE=3Fh	4	8	12	
	Y/C	GpYC1	INPUT MODE/SW=15h, PICTURE=00h, TP13=SG4, SW33→ON. Sign wave amplitude ratio of TP33 (loaded 100pF) when SG4 is 100kHz to 2.5MHz.	-4	0	4	
		GpYC2	INPUT MODE/SW=15h, PICTURE=3Fh	10	14	18	
Color control variable range		Gc11	TP13=SG9 (3.58MHz, 0dB, burst/chroma phase=180°). The amplitude ratio of COLOR=00h to COLOR=58h at TP29.		-30	-20	dB
		Gc12	CONTRAST=3Ch. The amplitude ratio of COLOR=FFh to COLOR=58h at TP29.	10	13		
Y maximum gain		GMY	CONTRAST=FFh, TP13=SG5. Calculate gain from the amplitude of TP33.	34	37	40	dB
RGB maximum gain		GMRGB	TP22=3V, TP21, 20, 19=SG5. Calculate gain from the amplitude of TP29, 33, 35.	21	24	27	dB
Contrast attenuate ratio		Gcon	TP13=SG5. The amplitude ratio of TP33 at CONTRAST=00h to CONTRAST=FFh.		-30	-20	dB
DC reproduction ratio		K	TP13=SG3 (APL10%, 90%). Measure the amplitude (black-black) of TP33 at 10% and 90%. Define the each value as V1 and V2. K=(V1-(V1-V2))/V1*100	95	100		%

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Trap attenuation ratio (NTSC)	GcfN	TP13=SG4 (100kHz, 3.58MHz). Define the amplitude of TP15 at 100kHz as V1. Define the amplitude of TP15 at 3.58MHz as V2. GcfN=20log (V2/V1)		-45	-30	dB
Trap attenuation ratio (PAL)	GcfP	INPUT MODE/SW=16h, TP13=SG4 (100kHz, 4.43MHz). Measure the amplitude of TP15 at 100kHz and 4.43M. Define each value as V3 and V4. GcfP=20log (V4/V3)		-45	-30	dB
ACC characteristic (1) (Composite NTSC in)	GA1NV	TP13=SG9 (0dB, +6dB, -25dB). Measure the amplitude of TP29 at 0dB, +6dB, -25dB. Define the each value as V0, V1 and V2. GA1NV=20log (V1/V0) GA2NV=20log (V2/V0)		0	2.0	dB
ACC characteristic (2) (Composite NTSC in)	GA2NV		-15.0	-10.0		dB
ACC characteristic (3) (Y/C NTSC in)	GA1NY	INPUT MODE/SW=15h, TP5=SG9 (0dB, +6dB, -25dB). Measure the amplitude of TP29 at 0dB, +6dB, -25dB. Define the each value as V0, V1 and V2. GA1NY=20log (V1/V0) GA2NY=20log (V2/V0)		0	2.0	dB
ACC characteristic (4) (Y/C NTSC in)	GA2NY		-9.0	-4.0		dB
ACC characteristic (5) (composite PAL in)	GA1PV	INPUT MODE/SW=16h, TP13=SG9 (0dB, +6dB, -25dB). Measure the amplitude of TP29 at 0dB, +6dB, -25dB. Define the each value as V0, V1 and V2. GA1PV=20log (V1/V0) GA2PV=20log (V2/V0)		0	2.0	dB
ACC characteristic (6) (composite PAL in)	GA2PV		-17.0	-12.0		dB
ACC characteristic (7) (Y/C PAL in)	GA1PY	INPUT MODE/SW=17h, TP5=SG9 (0dB, +6dB, -25dB). Measure the amplitude of TP29 at 0dB, +6dB, -25dB. Define the each value as V0, V1 and V2. GA1PY=20log (V1/V0) GA2PY=20log (V2/V0)		0	2.0	dB
ACC characteristic (8) (Y/C PAL in)	GA2PY		-11.0	-6.0		dB
APC capture range (NTSC, upper side)	fN+	INPUT MODE/SW=15h, TP5=SG9. Decrease the frequency from 3.584545MHz until output of TP29 is appeared. Work out the difference between the frequency at this time and 3.579545MHz.	+500	+1600		Hz
APC capture range (NTSC, lower side)	fN-	INPUT MODE/SW=15h, TP5=SG9. Increase the frequency from 3.574545MHz until output of TP29 is appeared. Work out the difference between the frequency at this time and 3.579545MHz.		-1600	-500	Hz
APC capture range (PAL, upper side)	fP+	INPUT MODE/SW=17h, TP5=SG9. Decrease the frequency from 4.438619MHz until output of TP29 is appeared. Work out the difference between the frequency at this time and 4.433619MHz.	+500	+1800		Hz
APC capture range (PAL, lower side)	fP-	INPUT MODE/SW=17h, TP5=SG9. Increase the frequency from 4.428619MHz until output of TP29 is appeared. Work out the difference between the frequency at this time and 4.433619MHz.		-1800	-500	Hz

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Killer operating input level (NTSC)	Vbk1A	INPUT MODE/SW=15h, TP5=SG9. Observe the waveform of TP29. Decrease the burst amplitude from 150mVp-p until the killer is turned on. Define the burst amplitude as VKIL1 (mVp-p). Then, increase the burst amplitude from that situation until the killer is turned off. Define the burst amplitude as VKIL2 (mVp-p). Vbk1A=20log (VKIL1/150), Vbk1B=20log (VKIL2/150). PAL mode : INPUT MODE/SW=17h. Measuring condition is same as NTSC.		-43	-38	dB
	Vbk1B				-35	
Killer operating input level (PAL)	Vbk2A			-47	-42	dB
	Vbk2B				-39	
Killer color ghost (NTSC)	Vbs1	Measuring condition is same as Vbk1A and Vbk2A (the killer is turned on). Measure the amplitude of the color difference output of TP29.		50	100	mV
Killer color ghost (PAL)	Vbs2			50	100	mV
Demodulation output amplitude ratio (1) (NTSC)	R-Y / B-Y	INPUT MODE/SW=15h, TP5=SG9. Vary the chroma phase and observe the each amplitude of TP29, TP33 and TP35. Define the each maximum amplitude of TP29, TP33 and TP35 as VB, VG and VR. (R-Y) / (B-Y) =VR/VB, (G-Y) / (B-Y) =VG/VB	0.56	0.66	0.76	
Demodulation output amplitude ratio (2) (NTSC)	G-Y / B-Y		0.29	0.36	0.44	
Demodulation output amplitude ratio (3) (PAL)	R-Y / B-Y	INPUT MODE/SW=17h, TP5=SG9. Vary the chroma phase and observe the each amplitude of TP29, TP33 and TP35. Define the each maximum amplitude of TP29, TP33 and TP35 as VB, VG and VR. (R-Y) / (B-Y) =VR/VB, (G-Y) / (B-Y) =VG/VB	0.56	0.66	0.76	
Demodulation output amplitude ratio (4) (PAL)	G-Y / B-Y		0.29	0.36	0.44	
Demodulation relative phase (1) (NTSC)	QRB	INPUT MODE/SW=15h, TP5=SG9. Vary the chroma phase and observe the each amplitude and phase of TP29, TP33 and TP35. Define the phase causing the maximum amplitude of TP29 as θB, of TP33 as θG, of TP35 as θR. QRB=θR-θB, QGB=θG-θB	80	90	100	deg
Demodulation relative phase (2) (NTSC)	QGB		230	240	250	deg
Demodulation relative phase (3) (PAL)	QRB	INPUT MODE/SW=17h, TP5=SG9. Vary the chroma phase and observe the each amplitude and phase of TP29, TP33 and TP35. Define the phase causing the maximum amplitude of TP29 as θB, of TP33 as θG, of TP35 as θR. QRB=θR-θB, QGB=θG-θB	80	90	100	deg
Demodulation relative phase (4) (PAL)	QGB		230	240	250	deg

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Demodulation output residual carrier (NTSC)	VCRN	TP42=3V, INPUT MODE/SW=15h, TP5=SG9. Adjust the chroma phase for maximizing the amplitude of TP29. Measure the ratio of the 7.15909MHz component to the 15.737kHz component with SPECTRUM ANALYZER.		-40	-30	dB
Demodulation output residual carrier (PAL)	VCRP	TP42=3V, INPUT MODE/SW=17h, TP5=SG9. Adjust the chroma phase for maximizing the amplitude of TP29. Measure the ratio of the 8.867238MHz component to the 15.625kHz component with SPECTRUM ANALYZER.		-50	-40	dB
TINT variable range	Q+	INPUT MODE/SW=15h, TP5=SG9 (NTSC). With TINT=80h (preset value), define the chroma phase causing the maximum amplitude of TP29 as $\theta 0$. Define the each chroma phase causing the maximum amplitude of TP29 at TINT=00h and TINT=FFh as $\theta 1$ and $\theta 2$. $Q+=\theta 1-\theta 0$, $Q-=\theta 2-\theta 0$	40	55	70	deg
	Q-		-60	-45	-30	deg
PHASE variable range	PQ+	INPUT MODE/SW=15h, TP5=SG9 (NTSC)。 With PHASE=20h (preset value), define the chroma phase causing the maximum amplitude of TP29 as $\theta 0$. Define the each chroma phase causing the maximum amplitude of TP29 at PHASE=00h and PHASE=3Fh as $\theta 1$ and $\theta 2$. $PQ+=\theta 1-\theta 0$, $PQ-=\theta 2-\theta 0$	13	19	25	deg
	PQ-		-22	-16	-10	deg
Frequency characteristics (Y/C input)	fyc1	SW29, 33, 35→ON, INPUT MODE/SW=15h, PICTURE=00h, TP13=SG4 (amplitude is 20mV). Measure the frequency when the amplitude of TP29, 33, 35 (loaded 100pF) decreases 3dB compared to the amplitude of it at the frequency 100kHz.	2.0	4.0		MHz
	fyc2	PICTURE=3Fh. Measuring condition is same as fyc1.	6.0	8.0		
Frequency characteristics (RGB input)	frgb	SW29, 33, 35→ON, TP22=3V TP21, 20, 19=SG4 (amplitude is 50mV). Measure the frequency when the amplitude of TP29, 33, 35 (loaded 100pF) decreases 3dB compared to the amplitude of it at the frequency 100kHz.	4.5	6.0		MHz

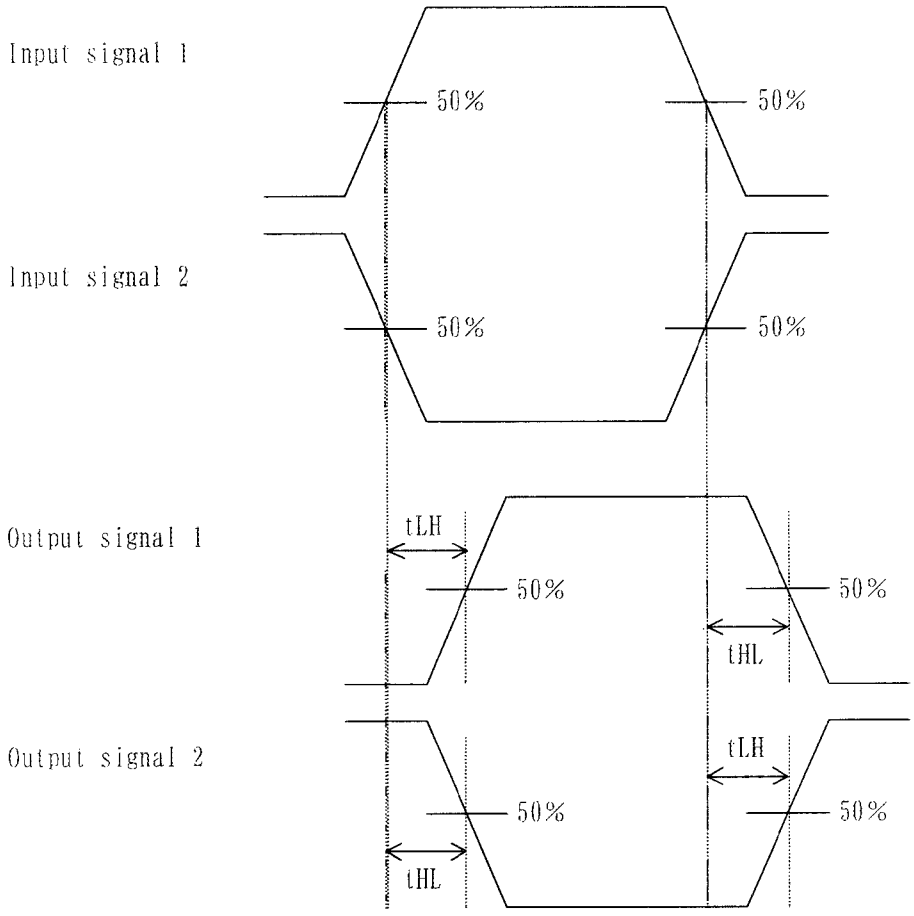
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gamma correction characteristics	Δγ1	TP22=3V, TP21, 20, 19=SG7 (0.5VP-P). Compute the gain at TP29, 33, 35. BRIGHT=FFh, GAMMA2=FFh when measure Δγ2. BRIGHT=AFh, GAMMA2=00h when measure Δγ3, VWγ2. GAMMA0=00h when measure Δγ0. VWγ2 is voltage between γ2 and PEAK LIMIT. 	21	24	27	dB
	Δγ2		0.5	3.5	6.5	
	Δγ3		18.5	21.5	24.5	
	Δγ0		-2	0.5	3	
	VWγ2		0.6	0.9	1.4	V
RGB AMP variable range	VRGB1	TP22=3V, RGB AMPLITUDE=00h. Measure the amplitude between black level of TP33 output.	1.9	2.2	2.5	VP-P
	VRGB2	TP22=3V, RGB AMPLITUDE=FFh	4.3	4.6	4.9	
RGB AMP sensitivity	ΔVRGB	The amplitude varying per 1LSB.	7	10	13	mVP-P
SUB-BRIGHT variable range	ΔVSB1	TP22=3V, TP21, 20, 19=SG5 ("Hi" level=100mV). Measure the amplitude varying between white levels of TP29, 35 when SUB-BRIGHT R, B=00h based on 80h.	1.2	1.5	1.8	V
	ΔVSB2	Measure the amplitude varying between white levels of TP29, 35 when SUB-BRIGHT R, B=FFh based on 80h.	-1.8	-1.5	-1.2	
SUB-BRIGHT sensitivity	ΔVSB	The amplitude varying per 1LSB.	9	12	16	mV
OUT LIMIT variable range	VBL1	OUT LIMIT=00h, RGB AMPLITUDE=00h, TP22=3V, TP20=SG6 (amplitude is 100mV). Measure non-inverted output voltage of TP33 between pedestal level and black limit level.	0.45	0.65	0.85	V
	VBL2	OUT LIMIT=1Fh		0.0	0.2	
OUT LIMIT sensitivity	ΔVBL	The amplitude varying per 1LSB.	14	20	27	mV
Gain difference among RGB	ΔGRGB	TP22=3V, TP21, 20, 19=SG7 (50mVP-P). Measure the ratio of maximum to minimum amplitude (white-black) among TP29, 33, 35 non-inverted output.	-0.8	0	0.8	dB
Gain difference between inverted and non-inverted	ΔGINV	Measure the ratio of the amplitude (white-black) of inverted to non-inverted output of TP29, 33, 35. Measuring condition is same as ΔGRGB.	-0.7	0	0.7	dB
Difference among RGB output black level	ΔVBKL	TP22=3V. Voltage difference of pedestal level among TP29, 33, 35.	-300	0	300	mV
DC voltage of RGB output	Vc	DC voltage of TP29, 33, 35 output.	2.3	2.5	2.7	V
DC voltage difference among RGB output	ΔVc	DC voltage difference among TP29, 33, 35 output.	-100	0	100	mV

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
COM AMP adjustable range	VCOM1	BRIGHT=80h, COM AMPLITUDE=00h. Measure the amplitude of TP39 output.	1.5	2.2	2.8	VP-P
	VCOM2	COM AMPLITUDE=FFh	7.6	8.3	9.0	
COM AMP sensitivity	ΔVCOM	The amplitude varying per 1LSB.	18	24	30	mV
COM-Gamma tracking ratio	Rγ	INPUT MODE/SW=34h, TP22=3V, TP21, 20, 19=SG7 (700mVP-P). Measure varying ratio of amplitude between inverted and non-inverted white level of TP33 to amplitude of TP39, when BRIGHT=60h and A0h.	0.93	1.00	1.07	
COM BLACK LEV adjustable range	VCB1	TP43=3V, COM BLACK LEV=00h. Measure the amplitude of TP39 output.	8.4	9.1		VP-P
	VCB2	COM BLACK LEV=1Fh		3.9	4.6	
COM BLACK LEV sensitivity	ΔVCB	The amplitude varying per 1LSB.	140	190	240	mV
DAC OUT variable range	VDAC1	DAC OUT=00h. TP44 voltage at 0.5mA sink.			0.3	V
	VDAC2	DAC OUT=00h. TP44 voltage at 0.5mA source.	2.7			
DAC OUT sensitivity	ΔVDAC	The amplitude varying per 1LSB.	9	11	13	mV
Carrier leak	CR	INPUT MODE/SW=15h, PICTURE=3Fh, COLOR=FFh, TP42=3V, TP5=SG9 (NTSC). Measure the ratio of the 3.579545MHz component to the 15.734kHz component in the output of TP33 with SPECTRUM ANALYZER.		-35	-20	dB
Crosstalk among RGB	CTRGB	TP22=TP42=3V, TP21=SG4 (1MHz, 300mV). Measure the amplitude of 1MHz component of TP29, 33 and 35 with SPECTRUM ANALYZER. Calculate the amplitude ratio of TP33 and TP35 to TP29. Similarly, TP20=SG4 (1MHz, 300mV), calculate the amplitude ratio of TP29 and TP35 to TP33. Similarly, TP19=SG4 (1MHz, 300mV), calculate the amplitude ratio of TP29 and TP33 to TP35.		-50	-40	dB
Crosstalk between inputs (EXT→INT)	CTEI	TP42=3V. With TP21=SG4 (1MHz, 300mV), TP22=3V and SPECTRUM ANALYZER. Measure the amplitude of 1MHz component of TP29. Then with TP22=0V, measure the attenuation of 1MHz component on TP29. Similarly, with TP20=SG4 (1MHz, 300mV), measure the one of TP33. Similarly, with TP19=SG4 (1MHz, 300mV), measure the one of TP35.		-45	-35	dB
Crosstalk between inputs (INT→EXT)	CTIE	TP42=3V, TP13=SG4 (1MHz, 300mV). With TP22=0V and SPECTRUM ANALYZER. Measure the amplitude of 1MHz component of TP29, TP33 and TP35. Then with TP22=3V, measure the attenuation of 1MHz component of TP29, TP33 and TP35.		-45	-35	dB

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Sync separator input current sensitivity	ISYNC	SW9→OFF. Flow out the current from TP9. Measure the current when TP10 turns "Hi" from "Lo".		38	55	μA
Sync separator output ON-state voltage	VON	SW9→OFF. Measure the voltage of TP10			0.3	V
Sync separator OFF-state current leak	IOFF	SW9, 10→OFF, TP10=10V. Flow out the 100μA current from TP9. Measure the current from TP10 into pin 10.			1	μA
SYNC IN threshold voltage	VTHSYN	TP11	1.2	1.5	1.8	V
FRP threshold voltage	VTHFRP	TP42	1.2	1.5	1.8	V
COM FRP threshold voltage	VTHCFRP	TP41	1.2	1.5	1.8	V
COM BLACK threshold voltage	VTHCBLK	TP43	1.2	1.5	1.8	V
BLACK IN threshold voltage	VTHBKIN	TP23	1.0	1.3	1.6	V
Serial input L→H threshold voltage	VTHLH	TP1, TP2, TP48		1.6	1.9	V
Serial input H→L threshold voltage	VTHHL	TP1, TP2, TP48	0.7	1.0		V
Input-Output propagation delay time (RGB input)	tLH1	SW29, 33, 35→ON, TP21, 20, 19=SG5, TP22=3V. Measure the propagation delay time of TP29, 33, 35 output when the output rises(tLH1) and falls(tHL1).	30	70	110	ns
	tHL1		30	70	110	
Input-Output propagation delay time (composite input)	tLH2	SW29, 33, 35→ON, TP13=SG5. Measure the propagation delay time of TP29, 33, 35 output when the output rises(tLH2) and falls(tHL2)	240	570	800	ns
	tHL2		240	570	800	
Input-Output propagation delay time (Y/C input)	tLH3	SW29, 33, 35→ON, INPUT MODE/SW=15h. TP13=SG5. Measure the propagation delay time of TP29, 33, 35 output when the output rises(tLH3) and falls(tHL3)	160	260	360	ns
	tHL3		160	260	360	
BLACK IN propagation delay time	tLH4	SW29, 33, 35→ON. TP13=SG8, TP23=SG5("Hi" level=3V). Measure the propagation delay time of TP29, 33, 35 output when the output rises(tLH4) and falls(tHL4)	100	170	240	ns
	tHL4		70	130	190	
FRP propagation delay time	tLH5	SW29, 33, 35→ON. Measure the propagation delay time from TP42 input to TP29, 33, 35 output when the output rises(tLH5) and falls(tHL5).	80	140	200	ns
	tHL5		80	140	200	
COM FRP propagation delay time	tLH6	SW39→ON, BRIGHT=80h. Measure the propagation delay time from TP41 input to TP39 output when the output rises(tLH6) and falls(tHL6).	400	650	900	ns
	tHL6		330	550	770	
COM BLACK propagation delay time	tLH7	SW39→ON, BRIGHT=80h, COM BLACK LEV=1Fh, TP43=SG5("Hi" level=3V). Measure the propagation delay time of TP39 output when the output rises(tLH7) and falls(tHL7).	360	730	1100	ns
	tHL7		360	730	1100	

Paramter	Symbol	Cnditions	MIN.	TYP.	MAX.	Unit
SW propagation delay time	tLH8	SW29, 33, 35→ON, TP21, 20, 19=SG10, TP22=SG5("Hi" level=3V). Measure the propagation delay time of TP29, 33, 35 output when the output rises(tLH8) and falls(tHL8).	70	130	190	ns
	tHL8		70	130	190	
HFILTER propagation delay time	tLH9	SW9→OFF, TP47=SG1("Lo" level=2.8V). Measure the propagation delay time of TP46 output when the output rises(tLH9) and falls(tHL9).	190	520	850	ns
	tHL9		180	330	480	
Sync separator propagation delay time	tLH10	TP47=SG1("Lo" level=2.8V). Measure the propagation delay time of TP10 output when the output rises(tLH10) and falls(tHL10).	500	1000	1500	ns
	tHL10		130	190	260	
Differential non linear error 1	DNL1	Apply to a DAC of lower 7 bit resolution.	-0.8		0.8	LSB
Differential non linear error 2	DNL2	Apply to a DAC of 8 bit resolution.	-1.5		1.5	LSB

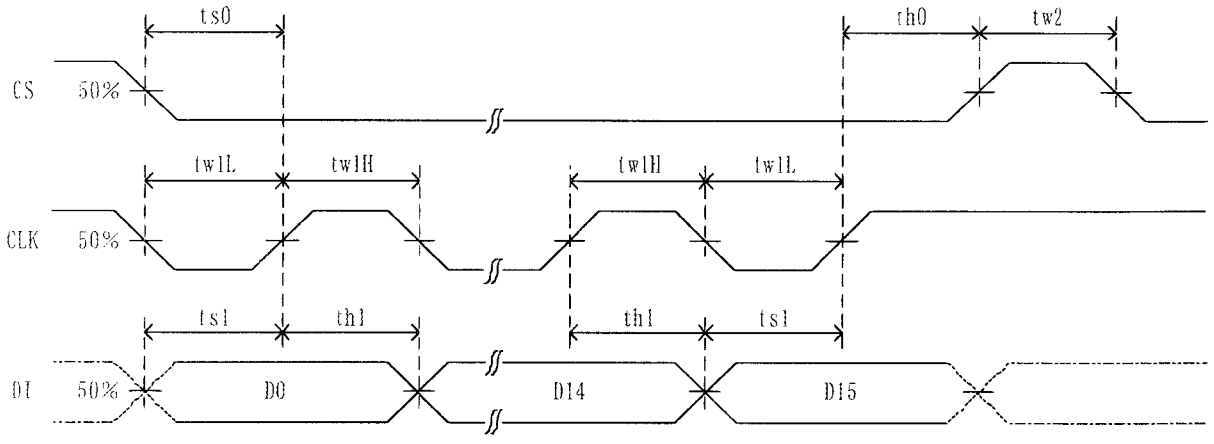
*The propagation delay time is measured by referring the 50% point of the input and the output. (As shown in the figure below.)

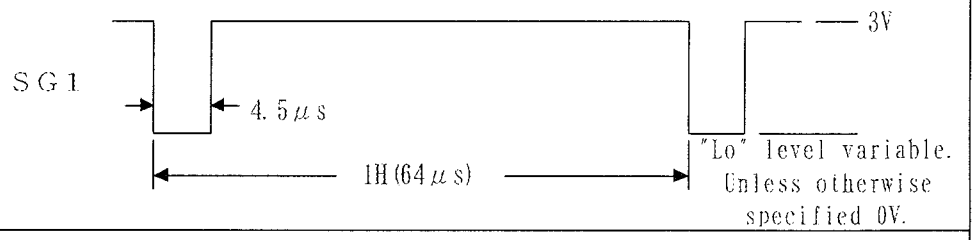
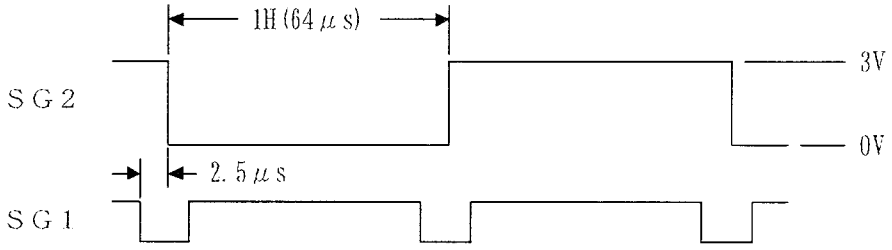
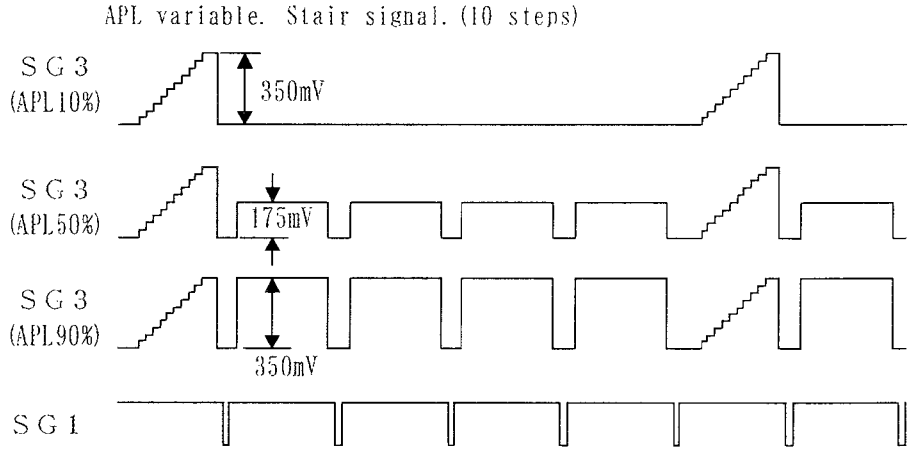
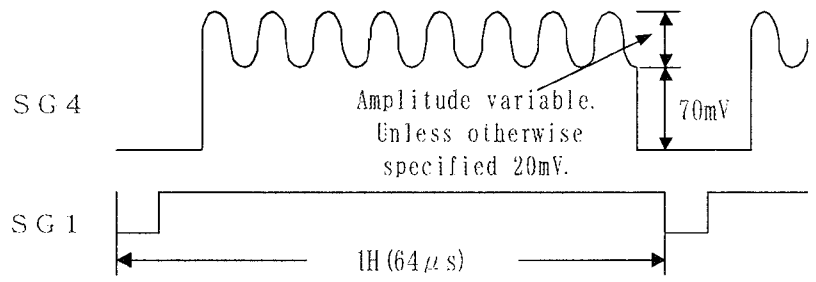
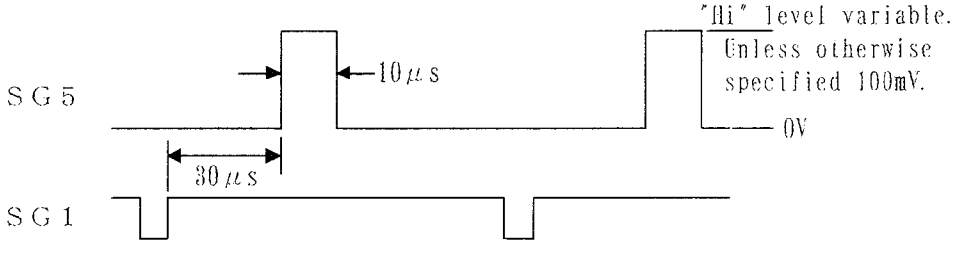


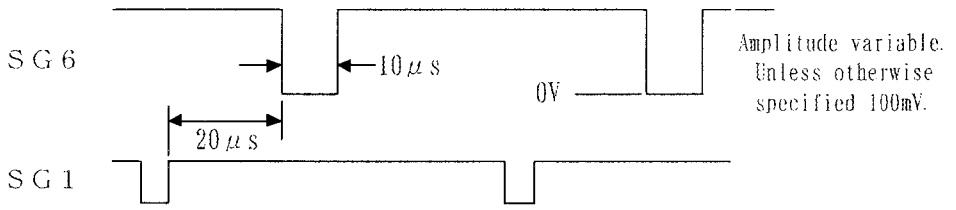
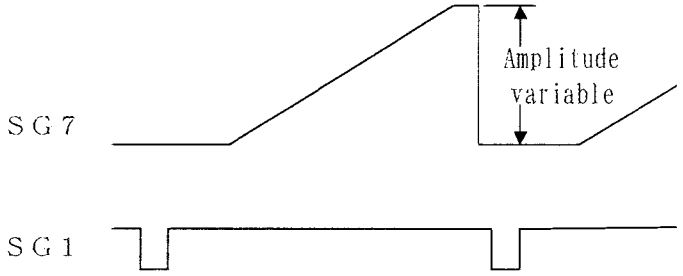
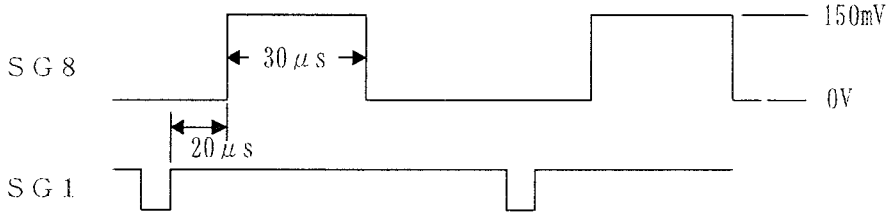
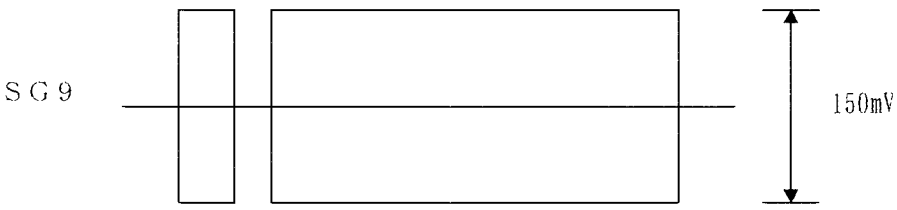
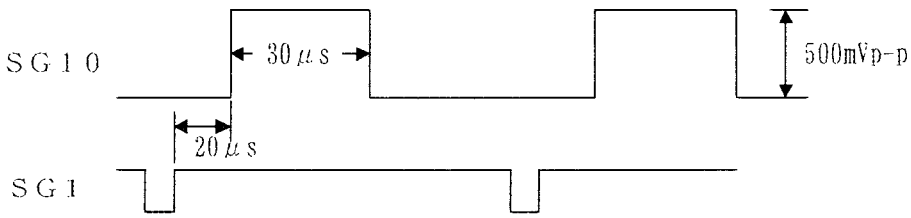
Serial I/O AC characteristics

Ta=-30～85℃, Vcc1=2.7～3.6V, Vcc2=Vcc4=4.5～5.5V, Vcc3=11～15.5V

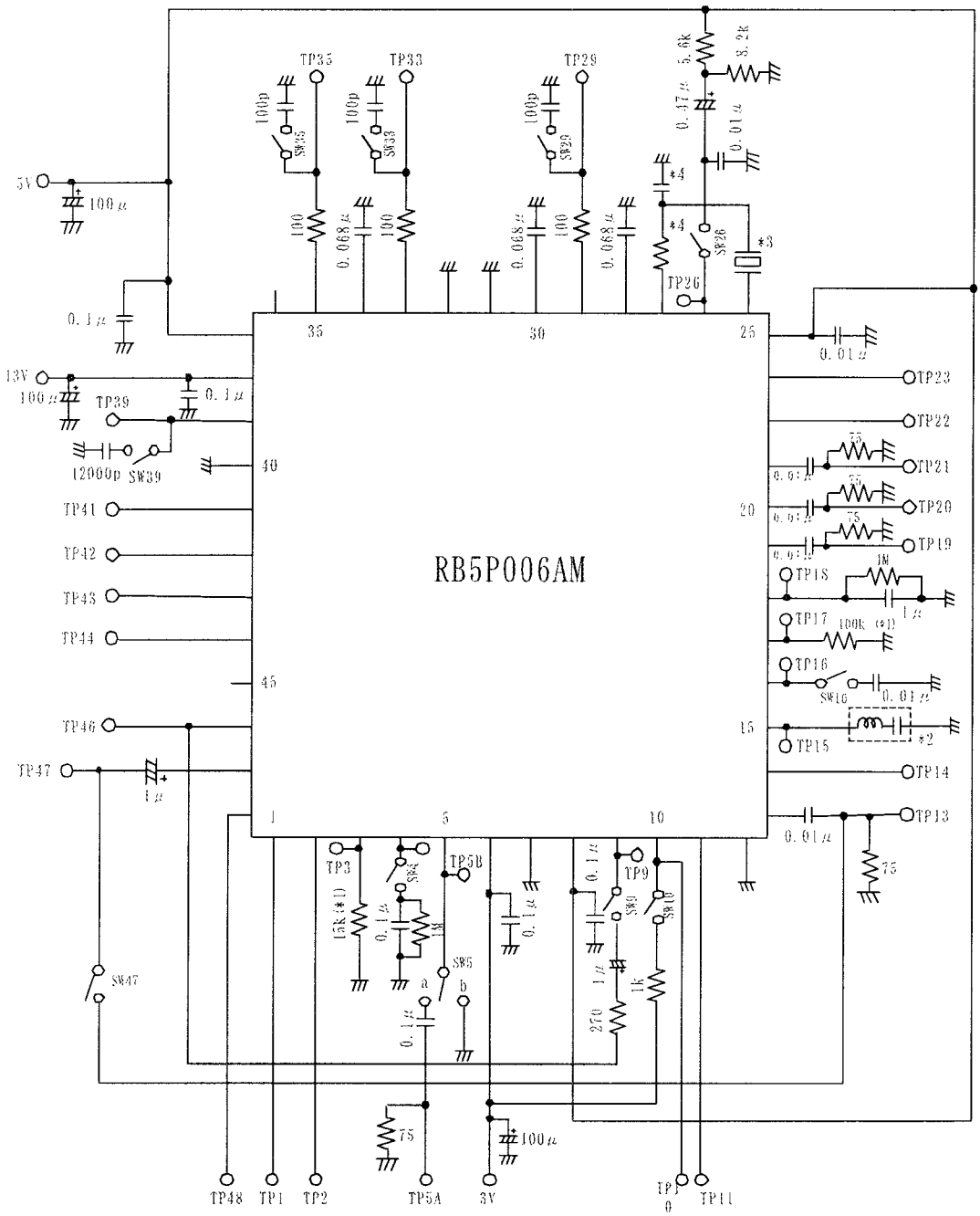
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
CS setup time based on CLK rise	ts0	330			ns
DI setup time based on CLK rise	ts1	220			ns
CS hold time based on CLK rise	th0	330			ns
DI hold time based on CLK rise	th1	220			ns
CLK pulse width ("Lo" level period)	tw1L	330			ns
CLK pulse width ("Hi" level period)	tw1H	330			ns
CS pulse width ("Hi" level period)	tw2	330			ns



SG No.	Wave form
SG1	
SG2	
SG3	
SG4	
SG5	

SG No.	Wave form
SG6	
SG7	
SG8	
SG9	Unless otherwise specified: Burst and chroma amplitude 150mVp-p Burst and chroma frequency 3.579545MHz (NTSC) / 4.433619MHz (PAL) Burst/chroma phase 180° (NTSC) / ±135° (PAL) 
SG10	

11. Test Circuit



Notes

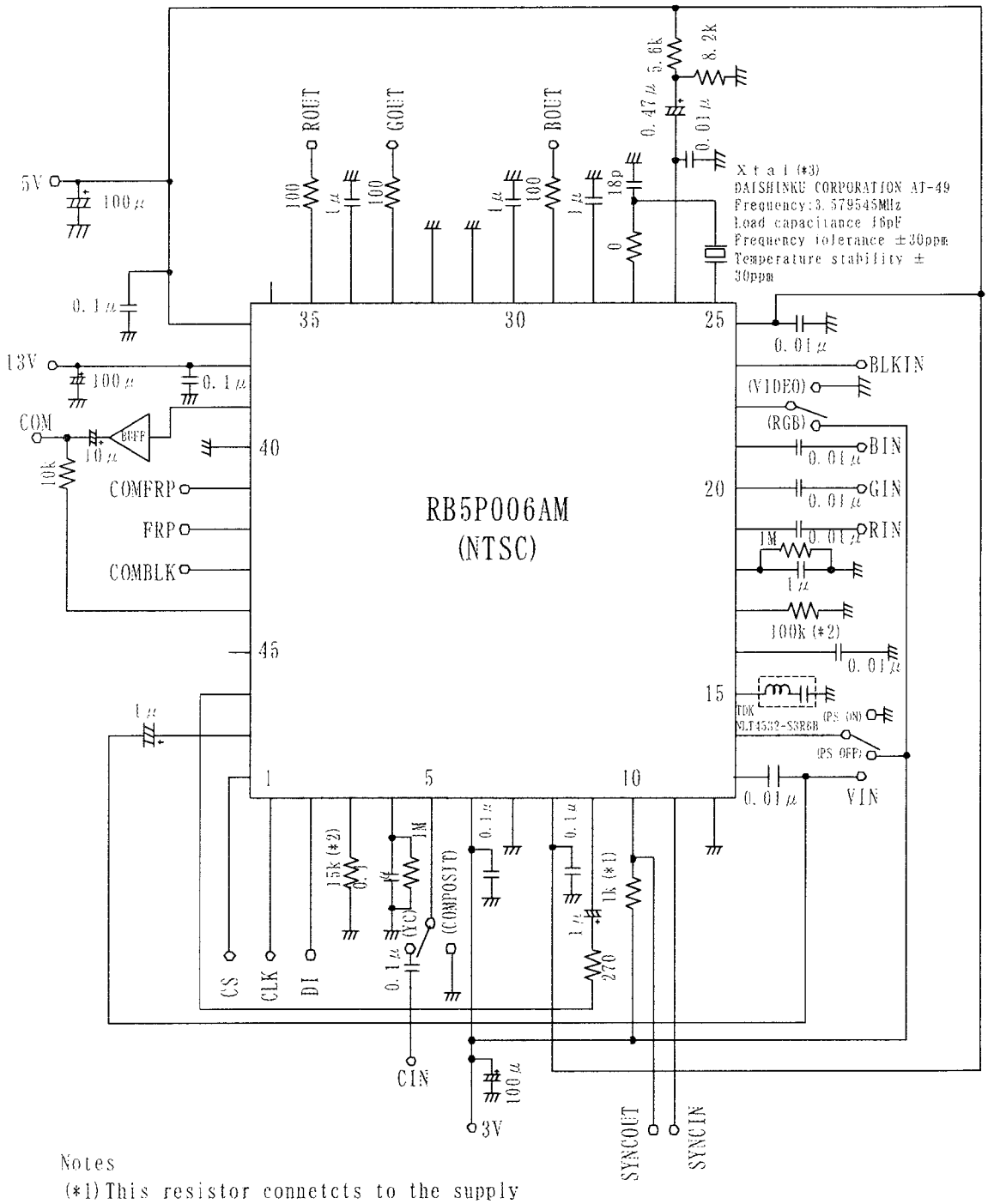
*1 Resistance accuracy ±2%, Temperature stability ±200ppm/℃

*2 TDK NLT4532-S3R6B (NTSC mode)
TDK NLT4532-S4R4 (PAL mode)

*3 Xtal
DAISHINKU CORPORATION AT-49
Frequency:3.579545MHz (NTSC mode) Name-of-article Code:1AF7294CLA
4.433619MHz (PAL mode) Name-of-article Code:1AF021SCL
Load capacitance 16pF
Frequency tolerance ±30ppm
Temperature stability ±30ppm

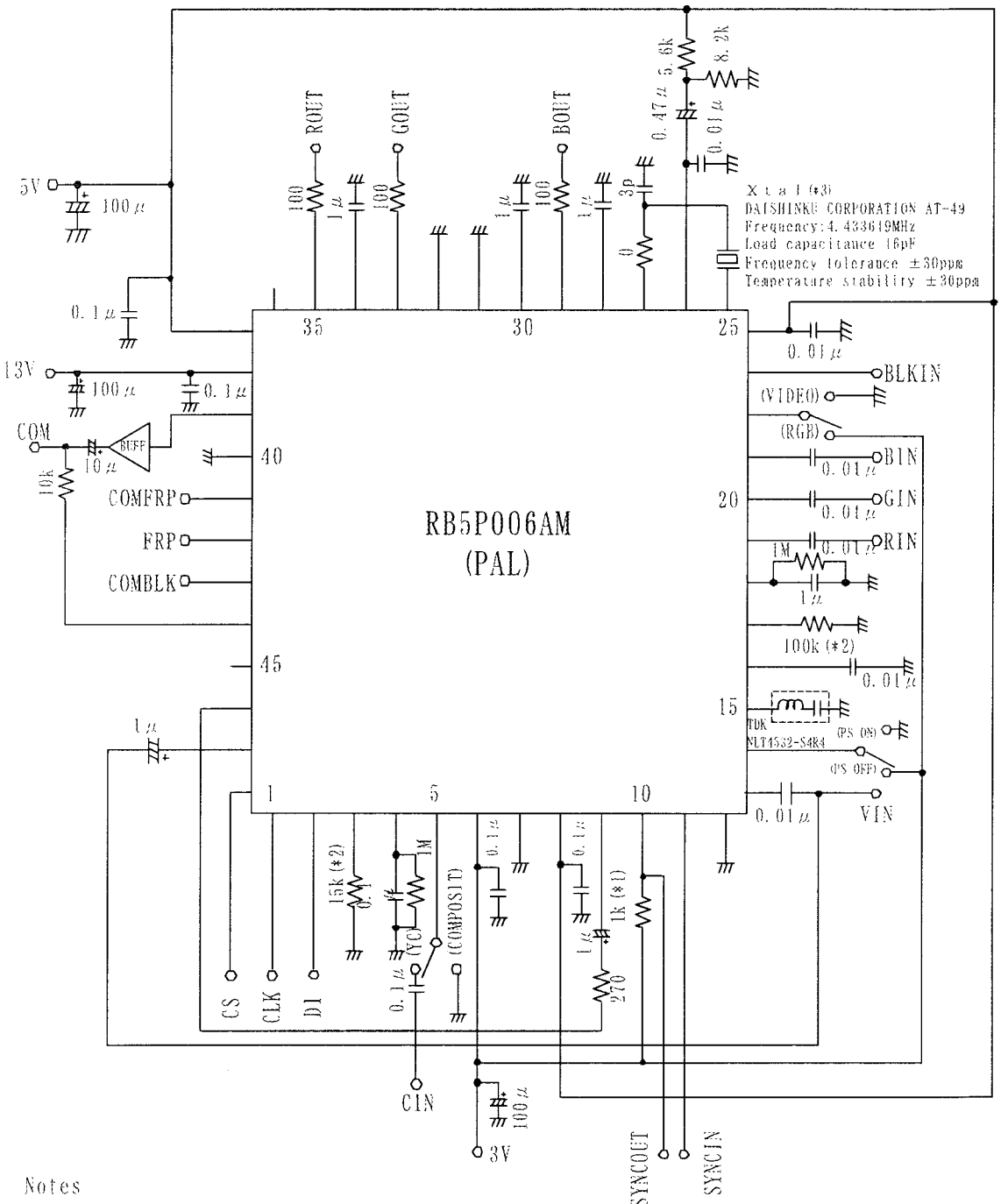
*4 0Ω, 18pF (NTSC mode)
0Ω, 3pF (PAL mode)

12. Application circuit example
(NTSC mode)



Notes
(*1) This resistor connetcts to the supply voltage of the timing generator.
(*2) Resistance accuracy ±2%,
Temperature stability ±200ppm/℃
(*3) Name-of-article Code: Please use 1AF7294CLA equivalent article.

PAL mode



Notes

(*1) This resistor connetcts to the supply voltage of the timing generator.

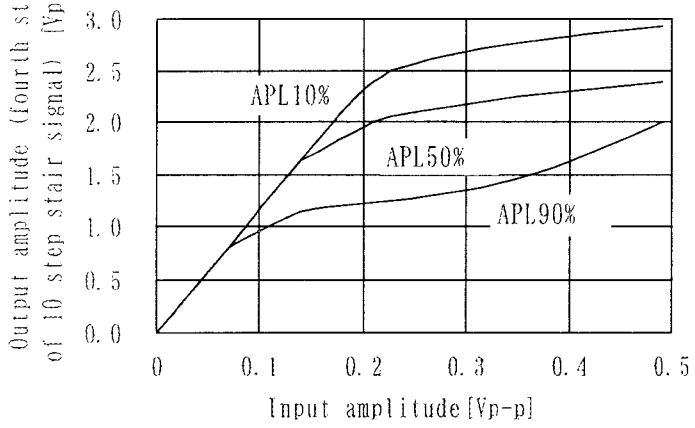
(*2) Resistance accuracy ±2%,
Temperature stability ±200ppm/℃

(*3) Name-of-article Code: Please use 1AF0218CL equivalent article.

13. Typical Characteristics

The conditions are the same as AC Characteristics.

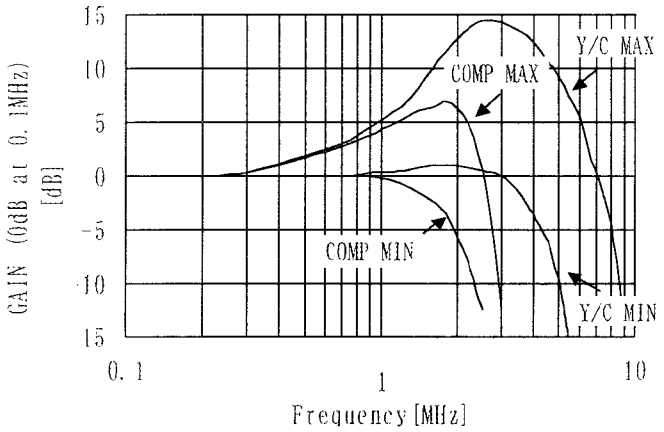
AGC amplitude characteristics



AGC LEVEL 1
Constants of AGC filter
1MΩ
1μF

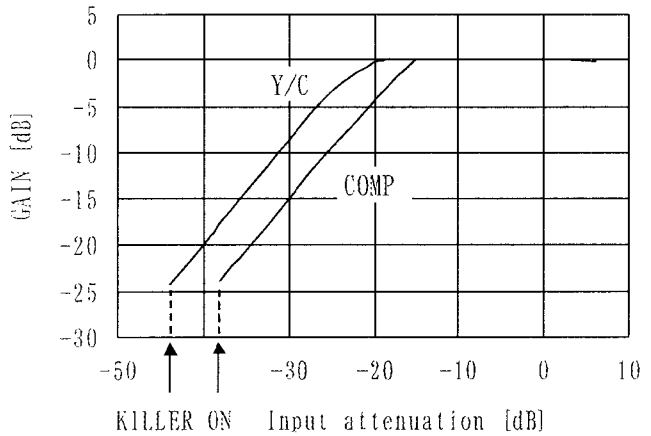
Measure the fourth step of 10 step stair signal.

PICTURE characteristics



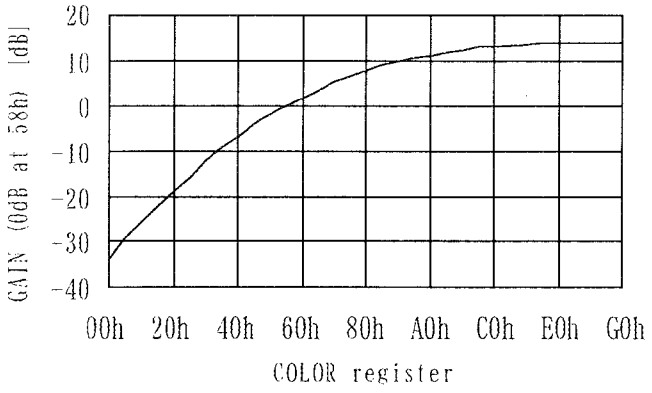
The gain at 0.1MHz frequency is 0dB.
NTSC mode.

ACC characteristics



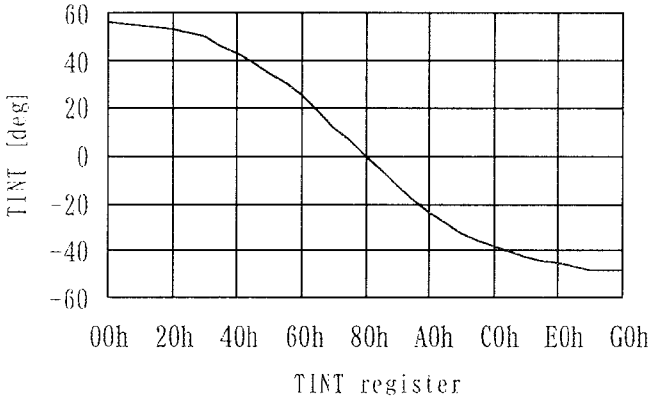
NTSC mode.

COLOR adjustment characteristics



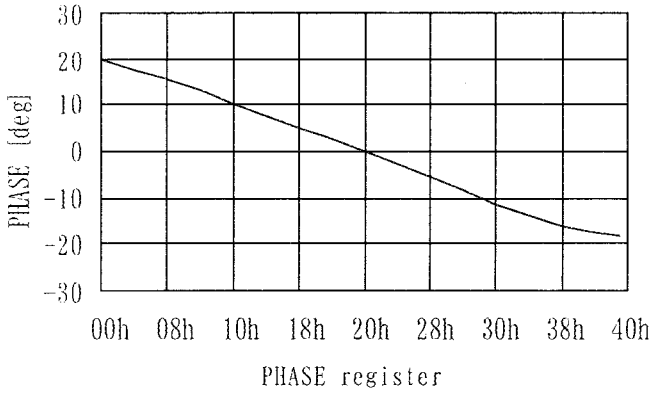
The gain at COLOR register = 58h is 0dB.

TINT adjustment characteristics



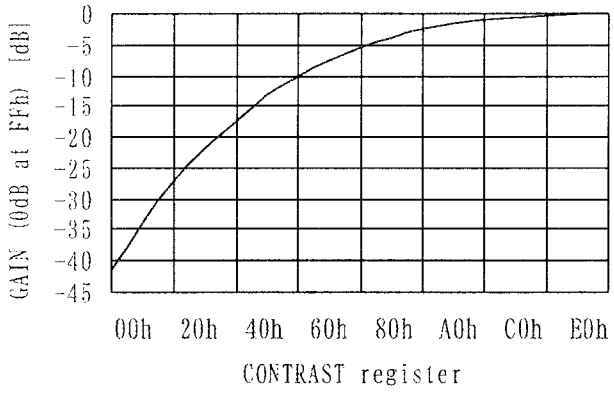
The degree at TINT register=80h (preset value) is 0deg.

PHASE adjustment characteristics



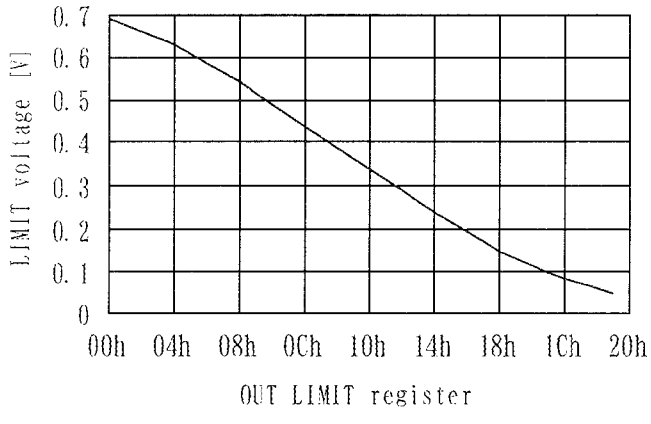
The degree at PHASE register=20h (preset value) is 0deg.

CONTRAST adjustment characteristics



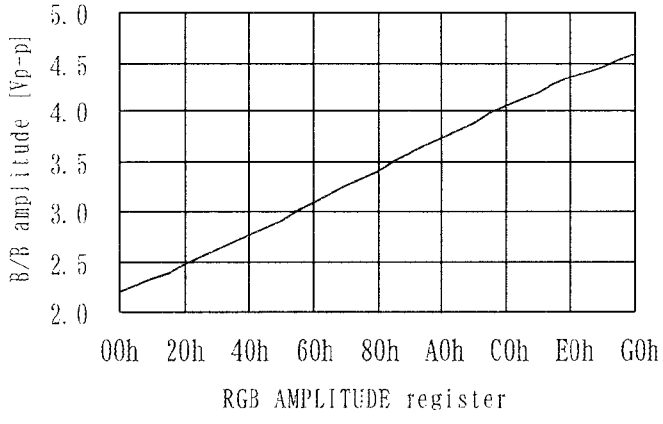
The gain at CONTRAST register = FFh is 0dB.

OUT LIMIT adjustment characteristics



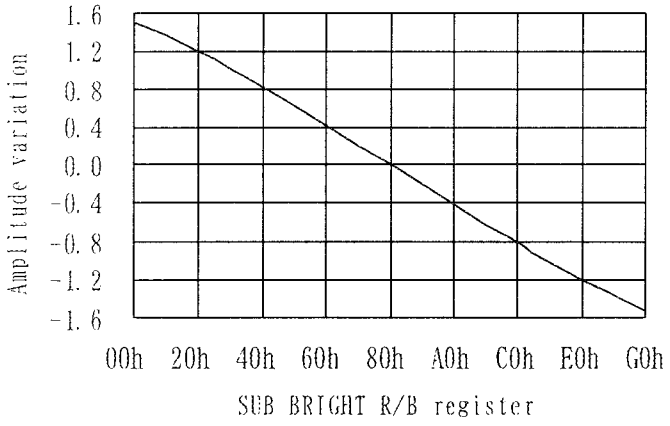
Limit voltage :
The potential between pedestal level (non-inverted output) and black limit level.

RGB AMPLITUDE adjustment characteristics



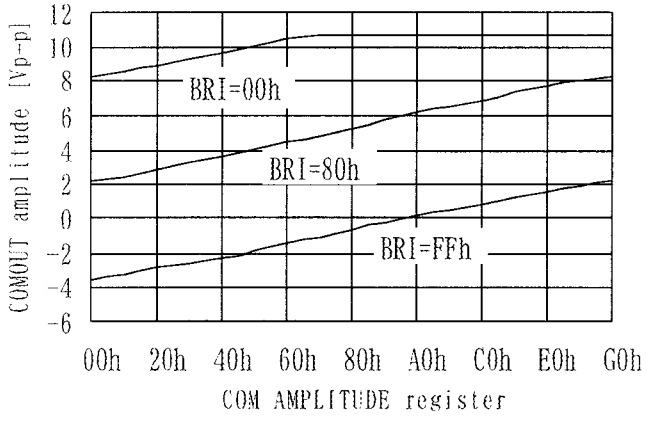
B/B amplitude :
The amplitude of the black level between inverted and non-inverted output.

SUB-BRIGHT adjustment characteristics



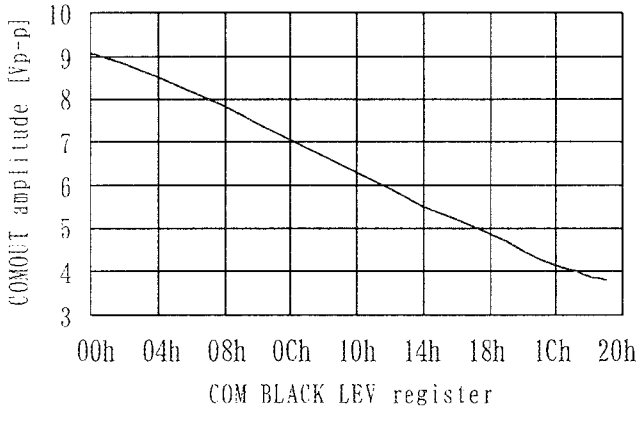
The amplitude at SUB-BRIGHT register =80h (preset value) is 0.

COM AMPLITUDE adjustment characteristics

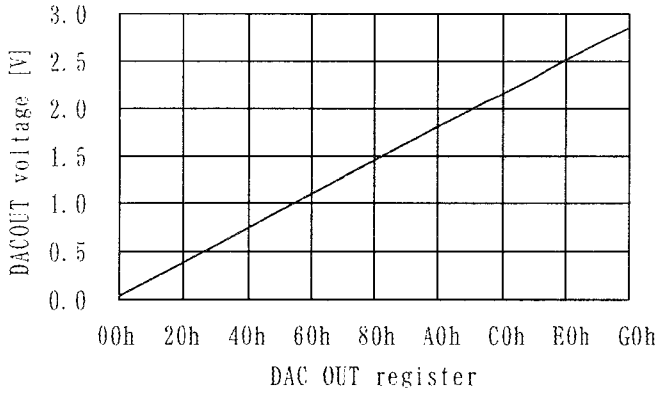


A COMOUT amplitude depends on both BRIGHT register and COM AMPLITUDE register.

COM BLACK LEV adjustment characteristics



DAC OUT adjustment characteristics



DACOUT terminal is open.

14 Package and packing specification

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80% R.H. max.

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1, V.P.S., or Manual soldering.)

- Temperature : 5～25℃
- Humidity : 60% R.H. max.
- Period : 96 hours max. after opening.

(2) Storage conditions for one-time soldering . (Solder dipping .)

- Temperature : 5～25℃
- Humidity : 60% R.H. Max.
- Period : 96 hours max. after opening.

(3) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃。
- Humidity : 60% R.H. max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃。
- Humidity : 60% R.H. max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

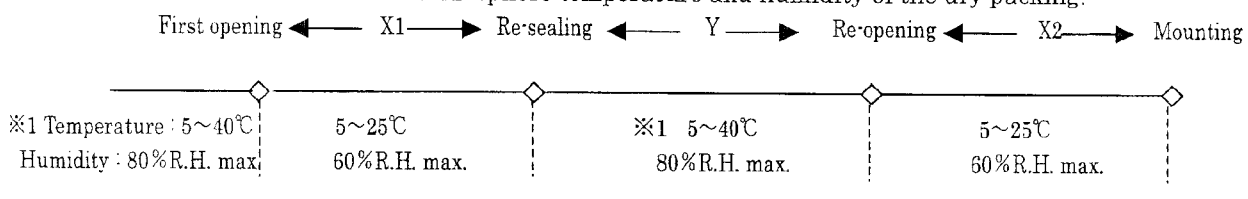
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1＋X2 : Refer to Section 1-2(1),(2), and (3)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.
  (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period :
  120℃ for 16～24 hours.
- The above baking conditions apply since the trays are heat-resistant.

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

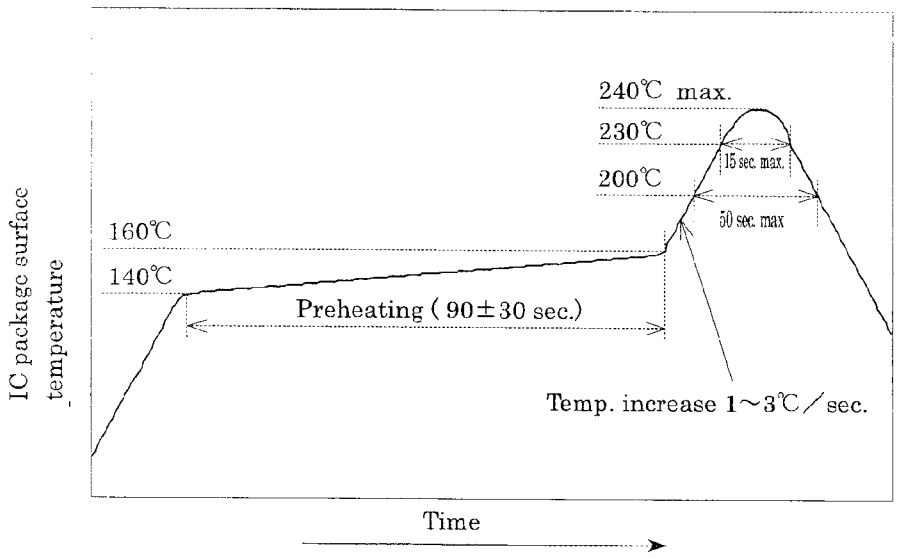
3.Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1.Soldering.

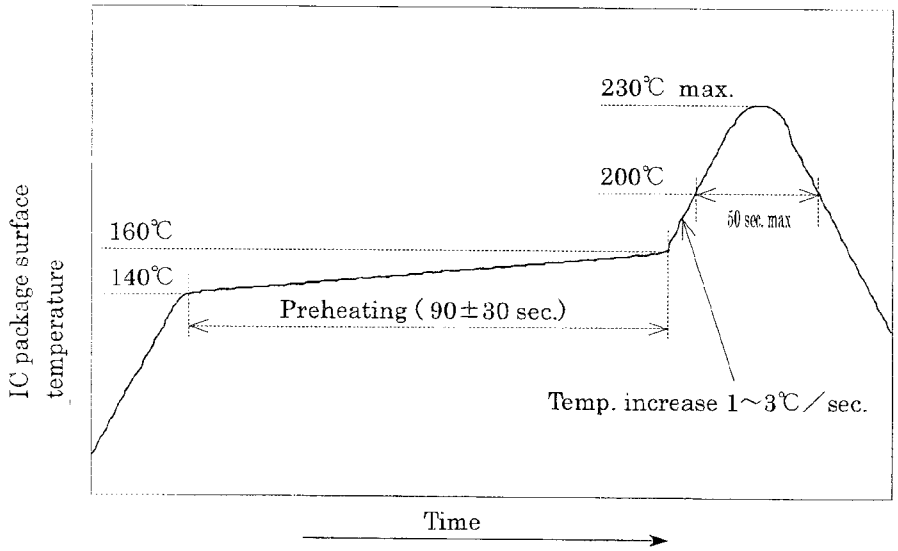
(1) Convection reflow or IR/Convection. (one-time soldering only in air or nitrogen environment)

- Temperature and period :
  Peak temperature of 240℃ max., above 230℃ for 15 sec. max.
  Above 200℃ for 50 sec. max.
  Preheat temperature of 140～160℃ for 90±30 sec.
  Temperature increase rate of 1～3℃／sec.
- Measuring point : IC package surface.
- Temperature profile :



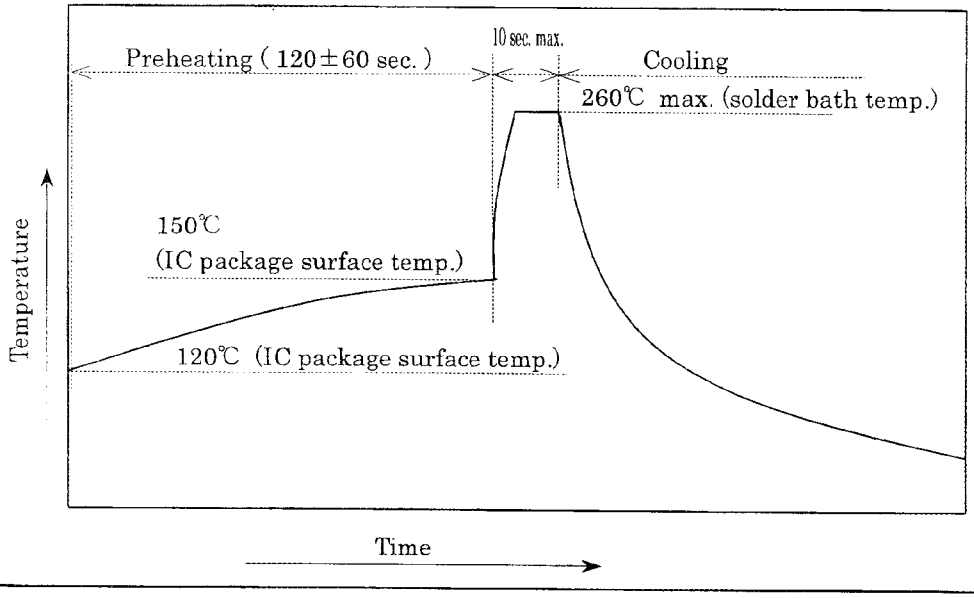
(2) Convection reflow or IR/Convection. (two-time soldering only in air or nitrogen environment)

- Temperature and period :
  Peak temperature of 230℃ max.
  Above 200℃ for 50 sec. max.
  Preheat temperature of 140～160℃ for 90±30 sec.
  Temperature increase rate of 1～3℃／sec.
- Measuring point : IC package surface.
- Temperature profile :



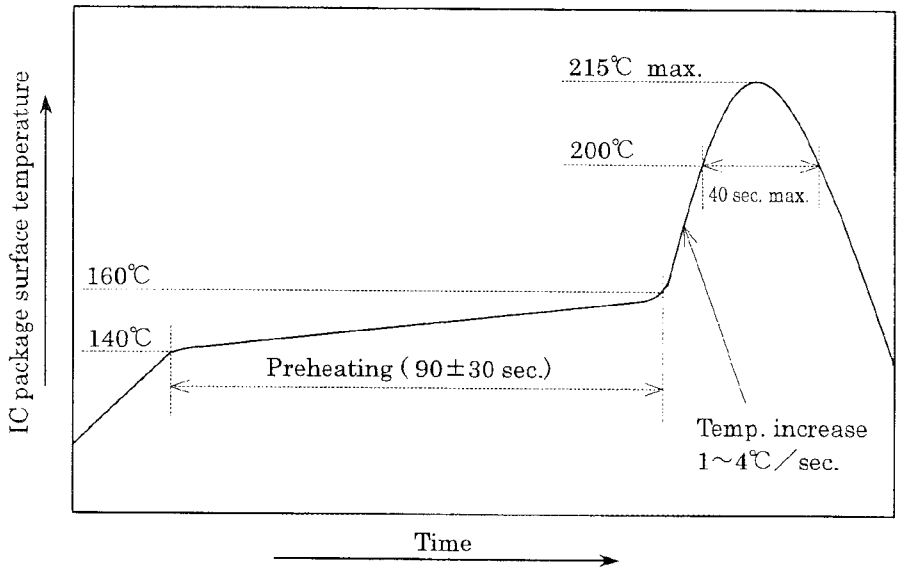
(3) Solder dipping. (one-time dipping only)

- Temperature and period :
  260℃ max. for 10 sec. max.
  Preheat temperature of 120～150℃ for 120±60 sec.
  Measuring point : IC package surface and solder bath.
- Temperature profile :



(3) V.P.S.(one-time soldering only)

- Temperature and period :
  Peak temperature of 215℃ max., above 200℃ for 40 sec. max.
  Preheat temperature of 140～160℃ for 90±30 sec.
  Temperature increase rate of 1～4℃／sec.
- Measuring point : IC package surface.
- Temperature profile



(4) Manual soldering (soldering iron) (one-time soldering only)

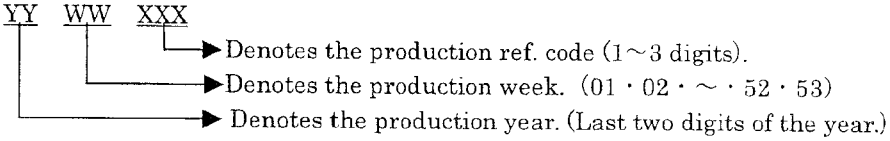
Soldering iron should only touch the IC's outer leads.

- Temperature and period :
  350℃ max. for 3 sec. / pin max., or 260℃ max. for 10 sec. / pin max.
  (Soldering iron should only touch the IC's outer leads.)
- Measuring point : Soldering iron tip.

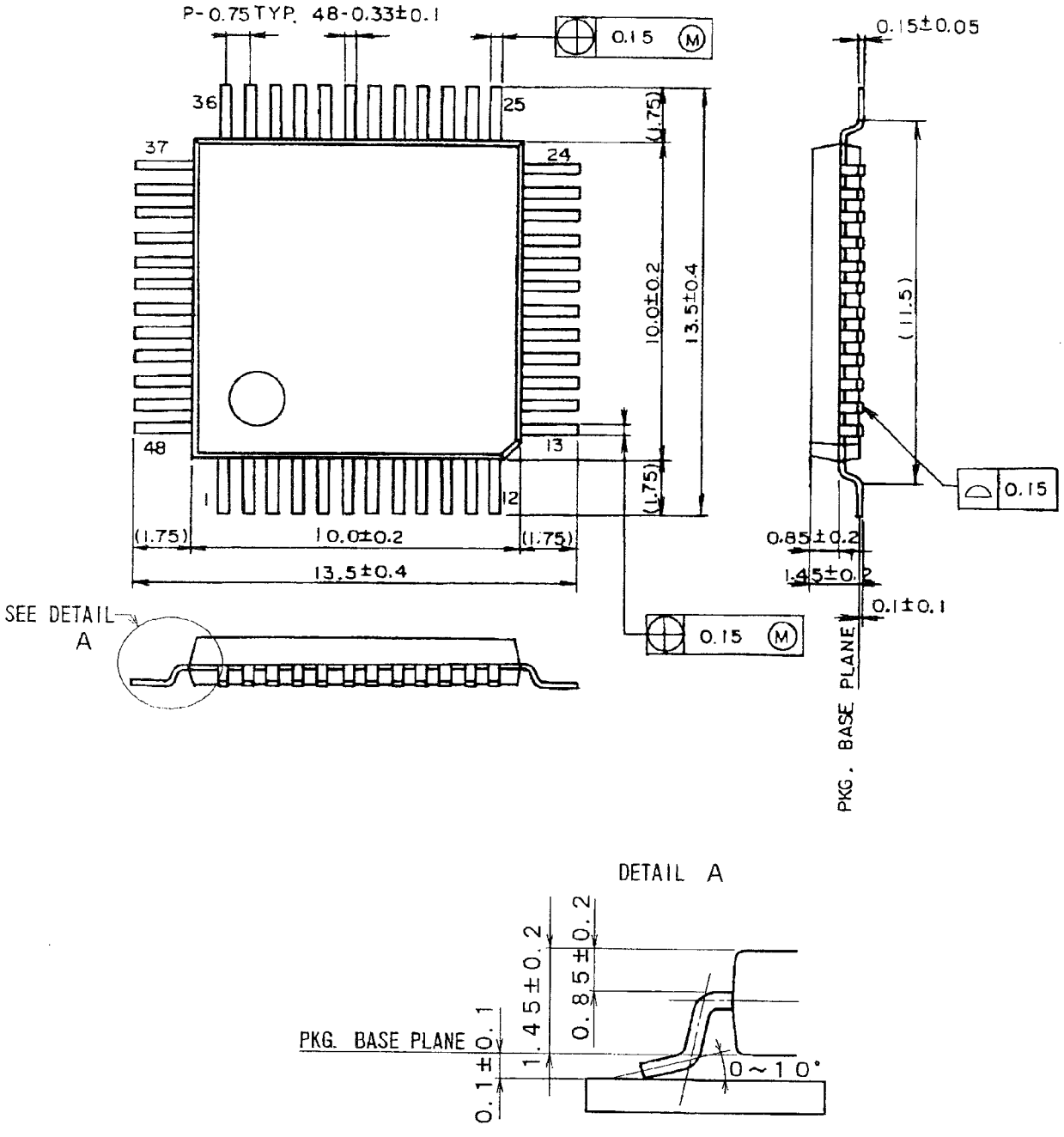
4. Condition for removal of residual flax.

(1) Ultrasonic washing power : 25 watts / liter max.
(2) Washing time : Total 1 minute max.
(3) Solvent temperature : 15～40℃

5. Package outline specification.
Refer to the attached drawing.

6. Markings.
6-1.Marking details. (The information on the package should be given as follows.)
(1) Product name : RB5P006AM
(2) Company name : SHARP
(3) Date code
(Example) YY WW XXX


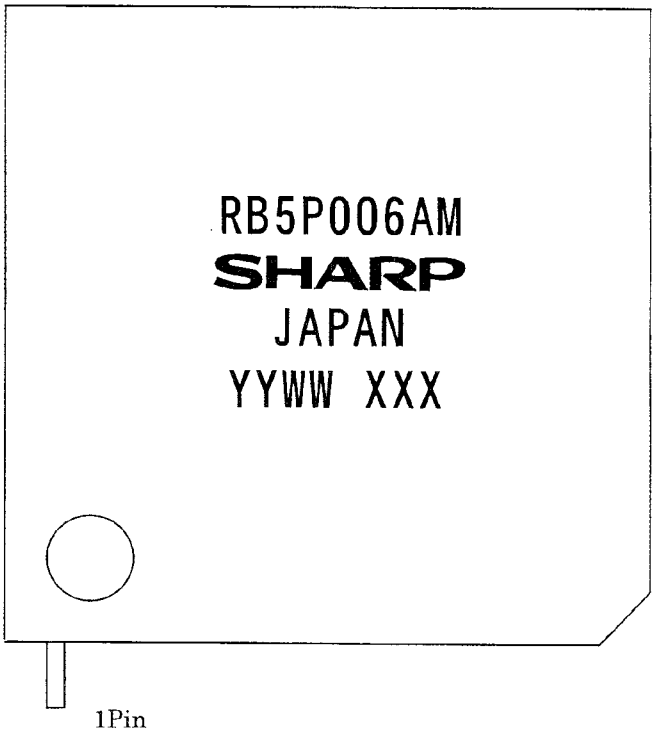
(4) "JAPAN" indicates the country of origin.
6-2.Marking layout.
The layout is shown in the attached drawing.
(However, this layout does not specify the size of the marking character and marking position.)



リード表面処理 LEAD FINISH	ハンダメッキ TIN-LEAD PLATING	リード材質 LEAD MATERIAL	42ALLOY
名称 NAME	QFP48-P-1010	備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.	
DRAWING NO. AA873	単位 UNIT mm		

20010611

マークレイアウト図
Marking layout



20010611

7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (800 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (80 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (3200 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2.Outline dimension of tray.

Refer to the attached drawing.

7-3.Outline dimension of carton.

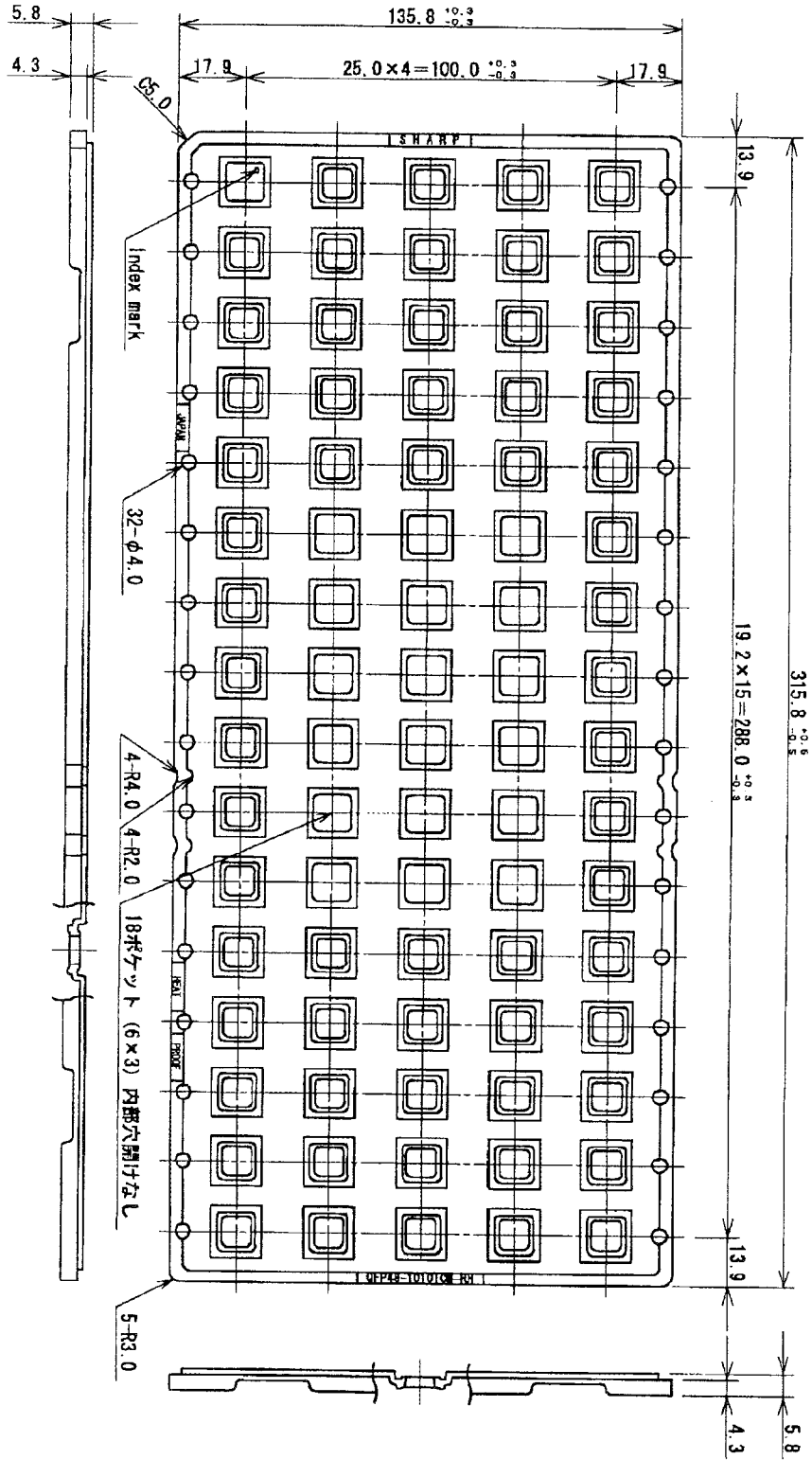
Refer to the attached drawing.

8. Precautions for use.

(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.

(3) The devices should be mounted the devices within one year of the date of delivery.



名称 NAME	QFP48-1010TCM-RH			備考 NOTE
DRAWING NO.	CV741	単位 UNIT	mm	

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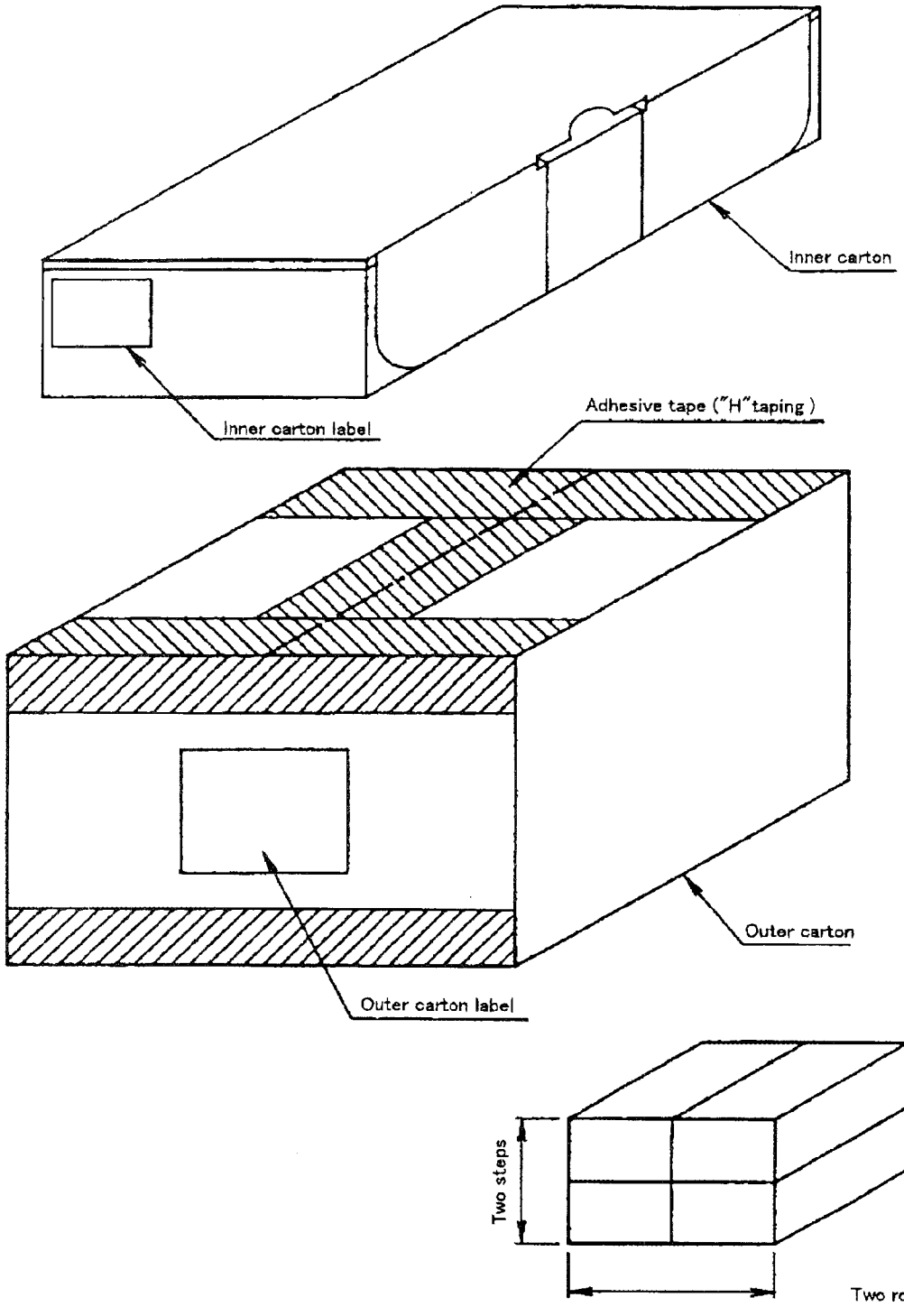


L × W× H

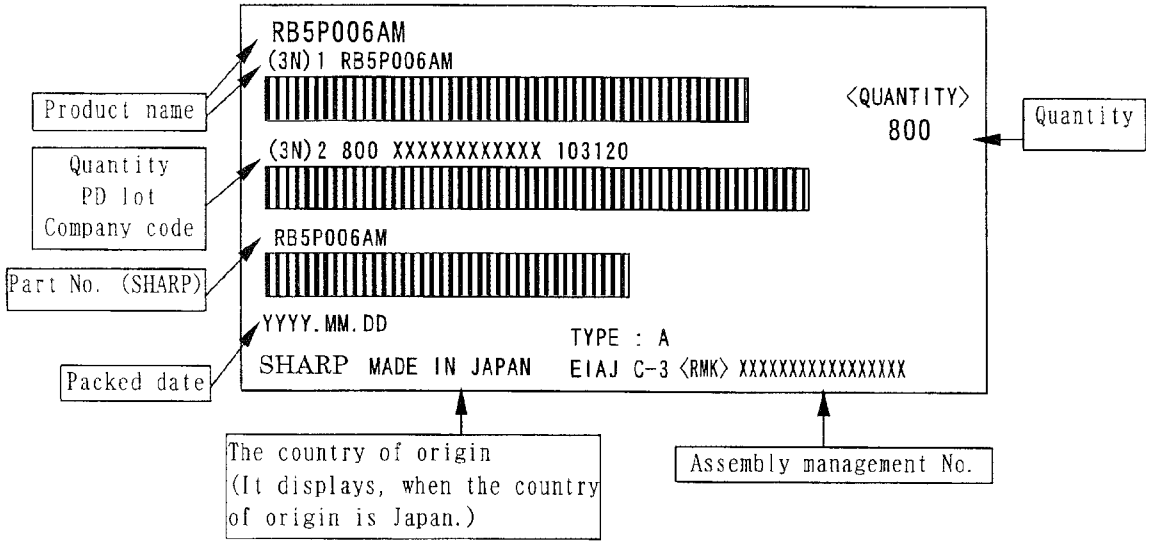
Inner carton - Outer dimensions : 335×150×80

Outer carton - Outer dimensions : 340×310×175

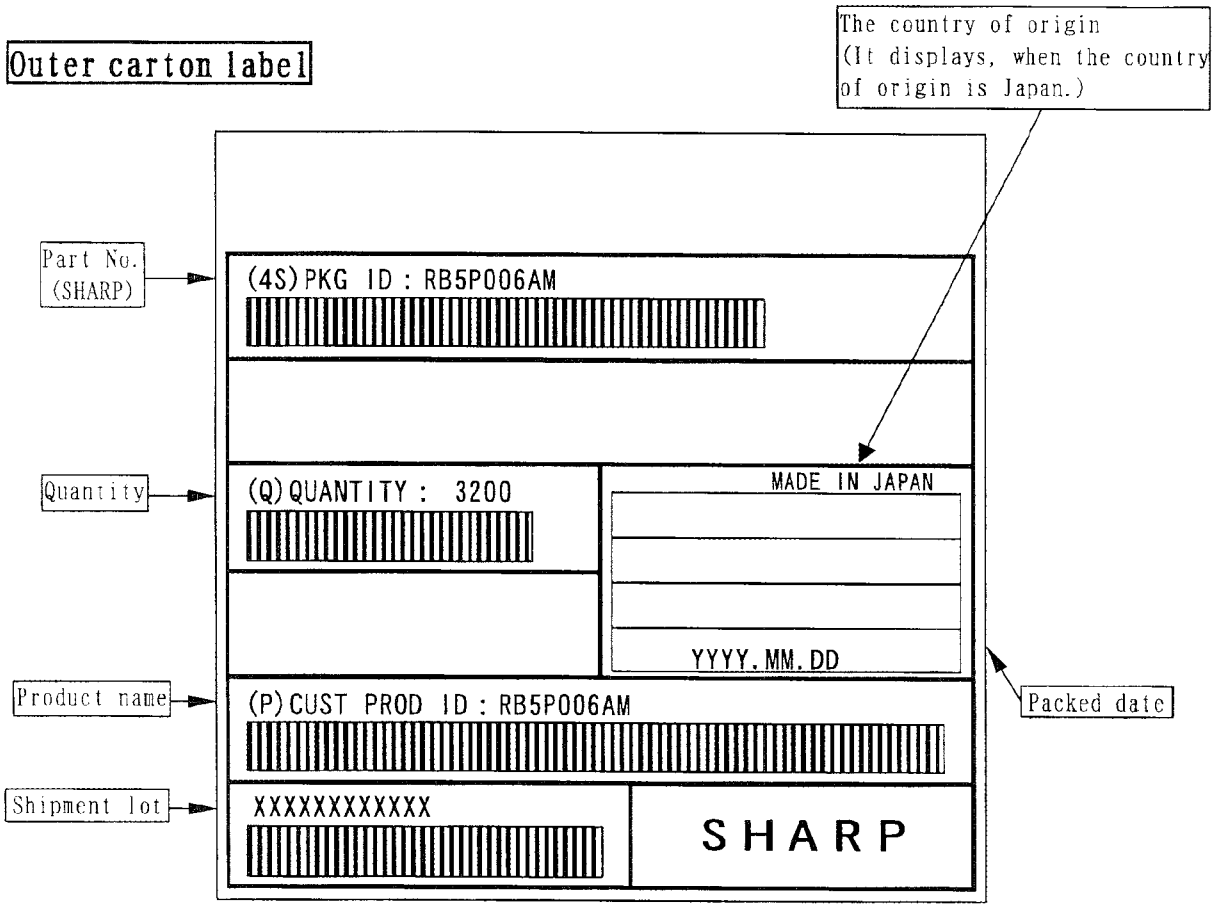
名称 NAME	トレイ品 包装仕様 Packing specifications			備考 出荷数量が端数の場合、本仕様と異なることがあります。 NOTE There is a possibility different from this specification when the number of shipments is fractions.
DRAWING NO.	BJ433	単位 UNIT	mm	

20010611

Inner carton label



Outer carton label



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