

RC210xxA

VersaClock 7 Programmable Clock Generator Family

The RC210xxA (RC21012A, RC21008A, and RC21005A) are high-performance programmable clock generators for compute, data-communications, and industrial applications.

Applications

- High-performance computing
- Data center accelerators
- Enterprise storage
- Switches and routers
- Industrial

Features

- 169fs RMS phase jitter (10kHz - 20MHz, 156.25MHz)
- PCIe® Gen6 Common Clock (CC) 27fs RMS
- PCIe SRIS and SRNS support
- 1kHz to 650MHz LVDS/LP-HCSL outputs
- 1kHz to 200MHz LVCMOS outputs

- Simple AC-coupling to LVPECL and CML
- LP-HCSL integrates 100Ω or 85Ω terminations
- Programmable General Purpose Inputs (GPI × 4) and General Purpose Input/Outputs (GPIO × 5)
- 1MHz I<sup>2</sup>C, 400kHz SMBus or 20MHz SPI Support
- Configuration via internal One-Time Programmable (OTP) memory (up to 27 different configurations), serial interface, or external I<sup>2</sup>C EEPROM.
- Factory programmable internal OTP
- 1.8V, 2.5V, 3.3V, -40° to +85°C operation
- RC21012A - 12 differential/24 single-ended outputs
  - 6 × 6 mm 48-QFN package
- RC21008A - 8 differential/16 single-ended outputs
  - 5 × 5 mm 40-QFN package with optional integrated crystal
- RC21005A - 5 differential/10 single-ended outputs
  - 4 × 4 mm 32-LGA package with integrated crystal

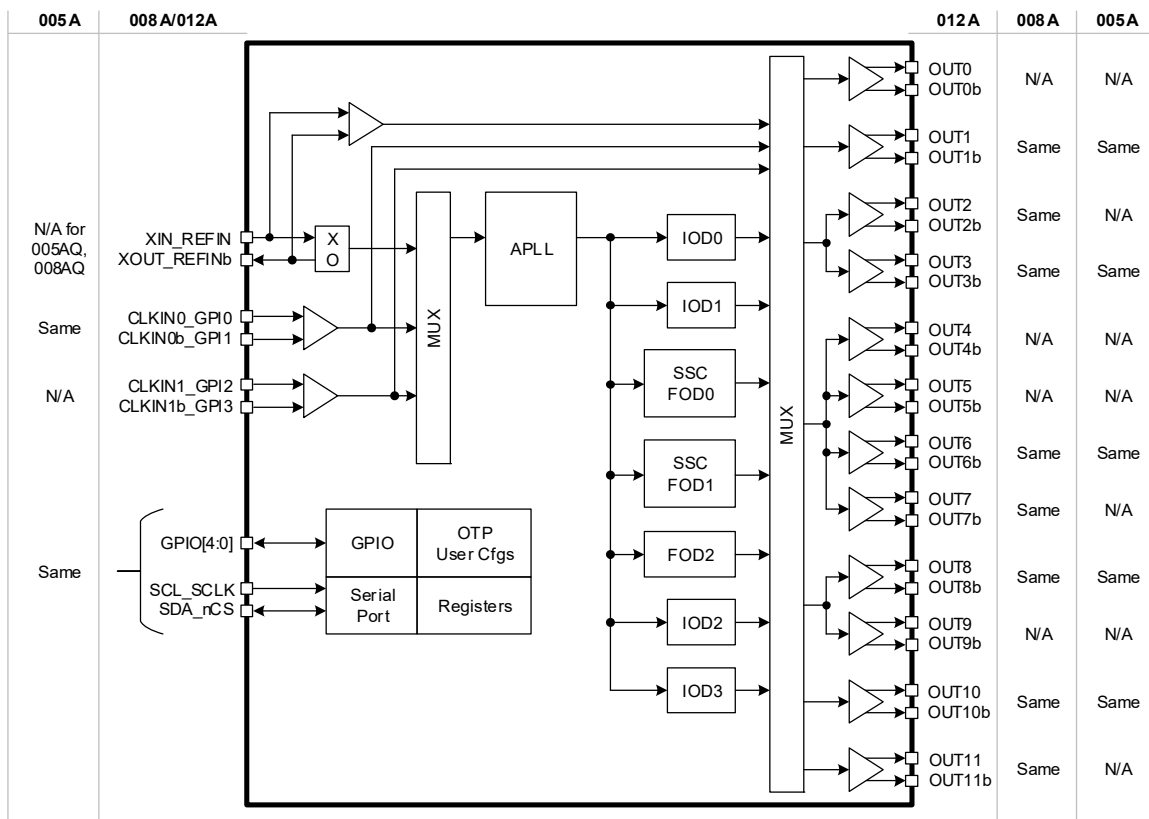


Figure 1. RC210xxA Block Diagram

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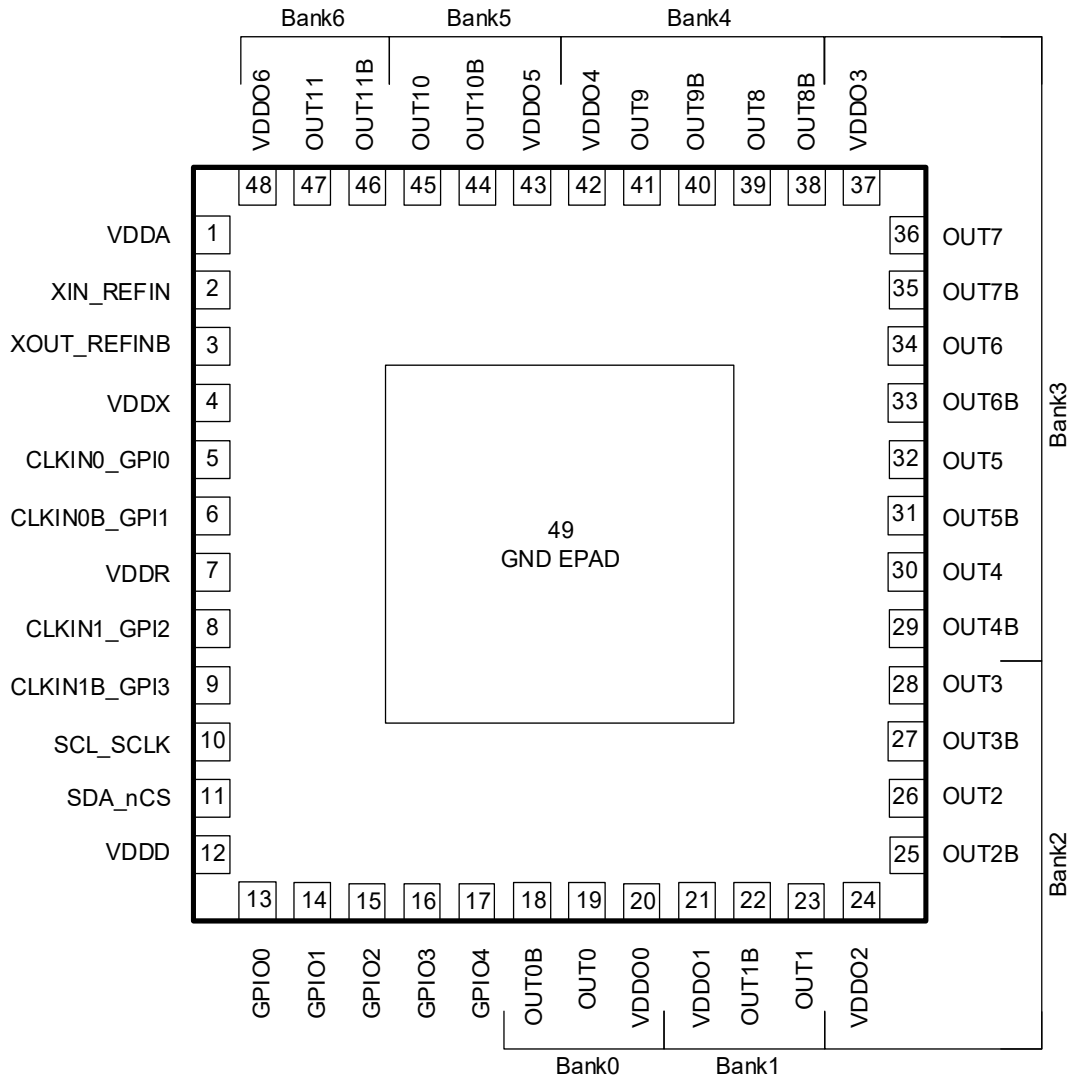
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# 1. Pin Information

## 1.1 Pin Assignments – RCxx012A



## 1.2 Pin Descriptions – RCxx012A

Table 1. RCxx012A Pin Descriptions

Number	Name	Type	Description
1	VDDA	Power	Power supply for analog, 1.8/2.5/3.3V supported.
2	XIN_REFIN	I	Crystal Input or differential reference clock positive input / CMOS single-ended reference clock input.
3	XOUT_REFINb	I/O	Crystal Output or differential reference clock negative input. This pin should be connected to a crystal. If an oscillator is connected to XIN_REFIN, then this pin must be left unconnected.
4	VDDX	Power	Power supply for Crystal oscillator. 1.8/2.5/3.3V supported.
5	CLKIN0_GPI0	I	Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPIO.

Table 1. RCxx012A Pin Descriptions (Cont.)

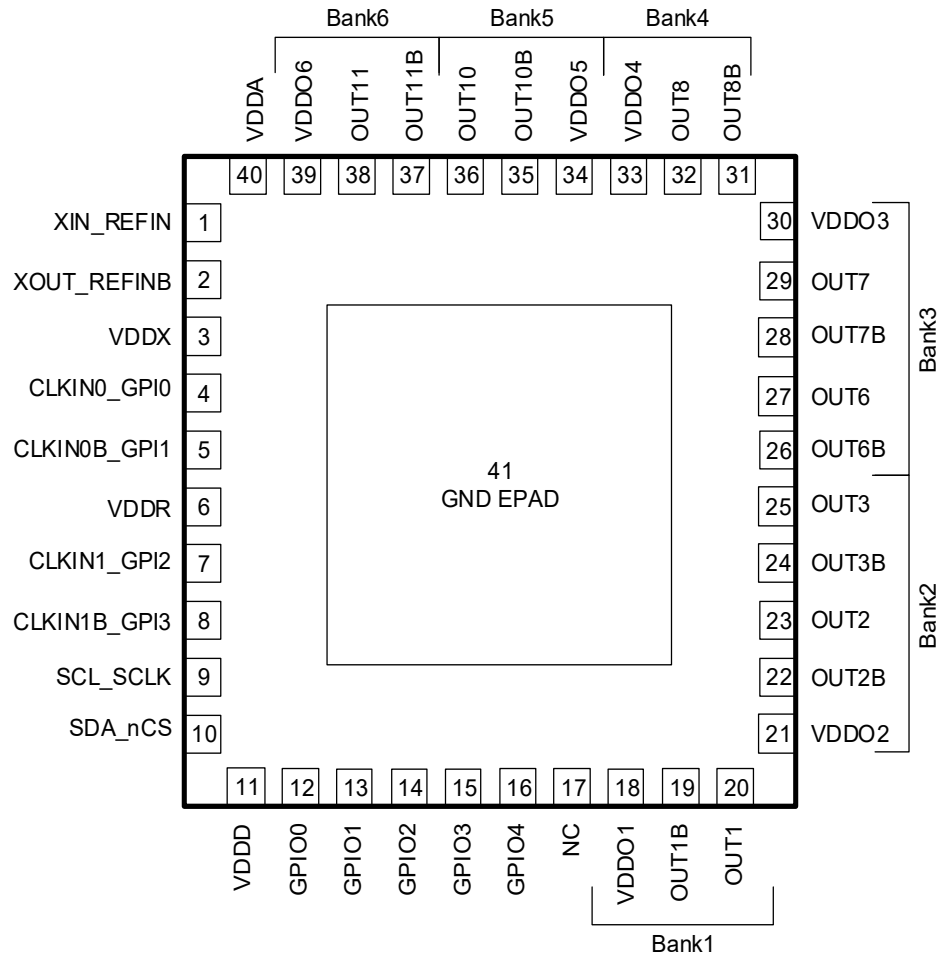
Number	Name	Type	Description
6	CLKIN0b_GPI1	I	Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1.
7	VDDR	Power	Reference input supply. 1.8/2.5/3.3V supported.
8	CLKIN1_GPI2	I	Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI2.
9	CLKIN1b_GPI3	I	Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI3.
10	SCL_SCLK	I	I2C Mode: I <sup>2</sup> C interface bi-directional clock. This pin is 3.3V tolerant.
11	SDA_nCS	I	I2C Mode: I <sup>2</sup> C interface bi-directional data in open-drain mode. This pin is 3.3V tolerant.
12	VDDD	Power	Power supply for digital core. 1.8/2.5/3.3V supported. When programming the OTP, this supply must be 2.5V or 3.3V.
13	GPIO0	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
14	GPIO1	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
15	GPIO2	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
16	GPIO3	I/O	General purpose input/output.
17	GPIO4	I/O	General purpose input/output.
18	nOUT0b	O	Output Clock 0 negative.
19	OUT0	O	Output Clock 0 positive.
20	VDDO0	Power	Supply voltage for output bank 0 and IOD 0. 1.8/2.5/3.3V supported.
21	VDDO1	Power	Supply voltage for output bank 1 and IOD 1. 1.8/2.5/3.3V supported.
22	OUT1b	O	Output Clock 1 negative.
23	OUT1	O	Output Clock 1 positive.
24	VDDO2	Power	Supply voltage for output bank 2 and FOD 0. 1.8/2.5/3.3V supported.
25	OUT2b	O	Output Clock 2 negative.
26	OUT2	O	Output Clock 2 positive.
27	OUT3b	O	Output Clock 3 negative.
28	OUT3	O	Output Clock 3 positive.
29	OUT4b	O	Output Clock 4 negative.
30	OUT4	O	Output Clock 4 positive.
31	OUT5b	O	Output Clock 5 negative.
32	OUT5	O	Output Clock 5 positive.
33	OUT6b	O	Output Clock 6 negative.
34	OUT6	O	Output Clock 6 positive.
35	OUT7b	O	Output Clock 7 negative.
36	OUT7	O	Output Clock 7 positive.

Table 1. RCxx012A Pin Descriptions (Cont.)

Number	Name	Type	Description
37	VDDO3	Power	Supply voltage for output bank 3 and FOD 1. 1.8/2.5/3.3V supported.
38	OUT8b	O	Output Clock 8 negative.
39	OUT8	O	Output Clock 8 positive.
40	OUT9b	O	Output Clock 9 negative.
41	OUT9	O	Output Clock 9 positive.
42	VDDO4	Power	Supply voltage for output bank 4 and FOD 2. 1.8/2.5/3.3V supported.
43	VDDO5	Power	Supply voltage for output bank 5 and IOD 2. 1.8/2.5/3.3V supported.
44	OUT10b	O	Output Clock 10 negative.
45	OUT10	O	Output Clock 10 positive.
46	OUT11b	O	Output Clock 11 negative.
47	OUT11	O	Output Clock 11 positive.
48	VDDO6	Power	Supply voltage for output bank 6 and IOD 3. 1.8/2.5/3.3V supported.
EPAD	GND	Power	Ground. ePad must be connected to ground before any VDD is applied.



### 1.3 Pin Assignments – RCxx008A



### 1.4 Pin Descriptions – RCxx008A

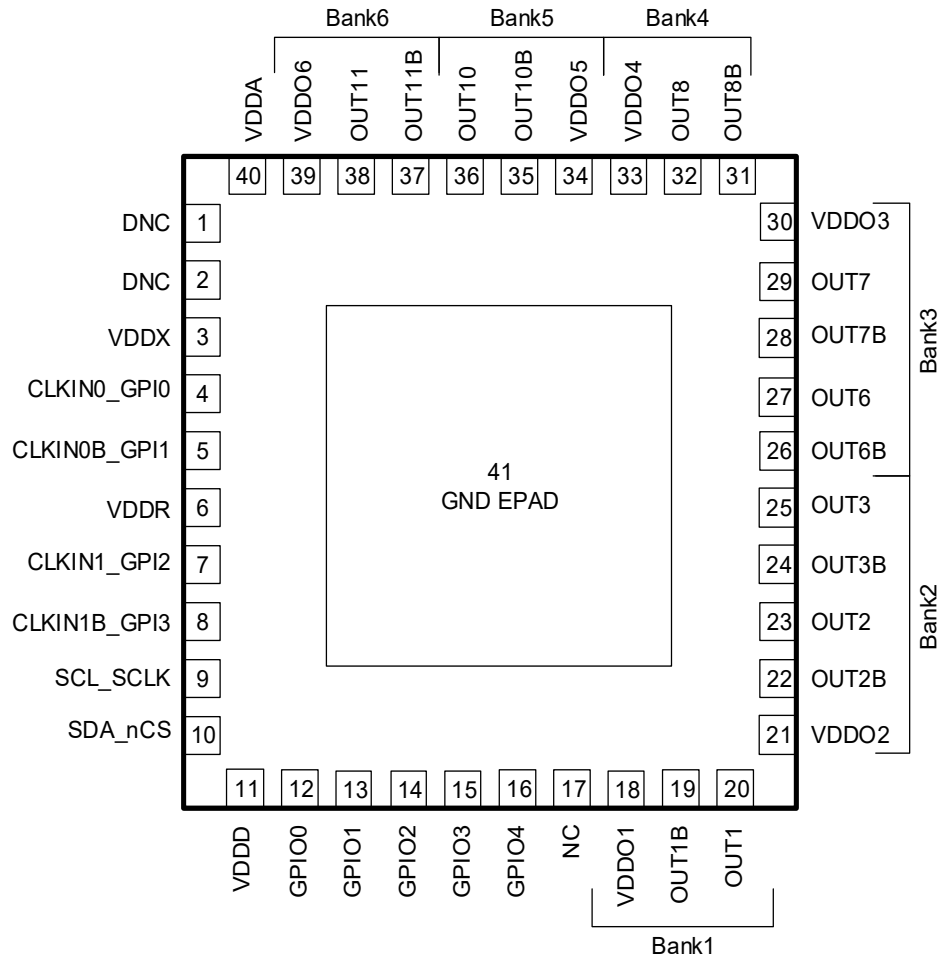
Table 2. RCxx008A Pin Descriptions

Number	Name	Type	Description
1	XIN_REFIN	I	Crystal Input or differential reference clock positive input / CMOS single-ended reference clock input.
2	XOUT_REFINb	I/O	Crystal Output or differential reference clock negative input. This pin should be connected to a crystal. If an oscillator is connected to XIN_REFIN, then this pin must be left unconnected.
3	VDDX	Power	Power supply for Crystal oscillator. 1.8/2.5/3.3V supported.
4	CLKIN0_GPI0	I	differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPIO.
5	CLKIN0b_GPI1	I	differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1.
6	VDDR	Power	Reference input supply. 1.8/2.5/3.3V supported.
7	CLKIN1_GPI2	I	Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI2.
8	CLKIN1b_GPI3	I	Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI3.

Table 2. RCxx008A Pin Descriptions (Cont.)

Number	Name	Type	Description
9	SCL_SCLK	I	I2C Mode: I <sup>2</sup> C interface bi-directional clock. SPI Mode: Serial Clock This pin is 3.3V tolerant.
10	SDA_nCS	I/O	I2C Mode: I <sup>2</sup> C interface bi-directional data in open-drain mode. SPI Mode: Chip Select (active low) This pin is 3.3V tolerant.
11	VDDD	Power	Power supply for digital core. 1.8/2.5/3.3V supported. When programming the OTP, this supply must be 2.5V or 3.3V.
12	GPIO0	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
13	GPIO1	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
14	GPIO2	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
15	GPIO3	I/O	General purpose input/output.
16	GPIO4	I/O	General purpose input/output.
17	NC	I	Not connected.
18	VDDO1	Power	Supply voltage for output bank 1 and IOD 1. 1.8/2.5/3.3V supported.
19	OUT1b	O	Output Clock 1 negative.
20	OUT1	O	Output Clock 1 positive
21	VDDO2	Power	Supply voltage for output bank 2 and FOD 0. 1.8/2.5/3.3V supported.
22	OUT2b	O	Output Clock 2 negative.
23	OUT2	O	Output Clock 2 positive.
24	OUT3b	O	Output Clock 3 negative.
25	OUT3	O	Output Clock 3 positive.
26	OUT6b	O	Output Clock 6 negative.
27	OUT6	O	Output Clock 6 positive.
28	OUT7b	O	Output Clock 7 negative.
29	OUT7	O	Output Clock 7 positive.
30	VDDO3	Power	Supply voltage for output bank 3 and FOD 1. 1.8/2.5/3.3V supported.
31	OUT8b	O	Output Clock 8 negative.
32	OUT8	O	Output Clock 8 positive.
33	VDDO4	Power	Supply voltage for output bank 4 and FOD 2. 1.8/2.5/3.3V supported.
34	VDDO5	Power	Supply voltage for output bank 5 and IOD 2. 1.8/2.5/3.3V supported.
35	OUT10b	O	Output Clock 10 negative.
36	OUT10	O	Output Clock 10 positive.
37	OUT11b	O	Output Clock 11 negative.
38	OUT11	O	Output Clock 11 positive.
39	VDDO6	Power	Supply voltage for output bank 6 and IOD 3. 1.8/2.5/3.3V supported.
40	VDDA	Power	Power supply for analog, 1.8/2.5/3.3V supported.
EPAD	GND	Power	Ground. ePad must be connected to ground before any VDD is applied.

## 1.5 Pin Assignments – RCxx008AQ



## 1.6 Pin Descriptions – RCxx008AQ

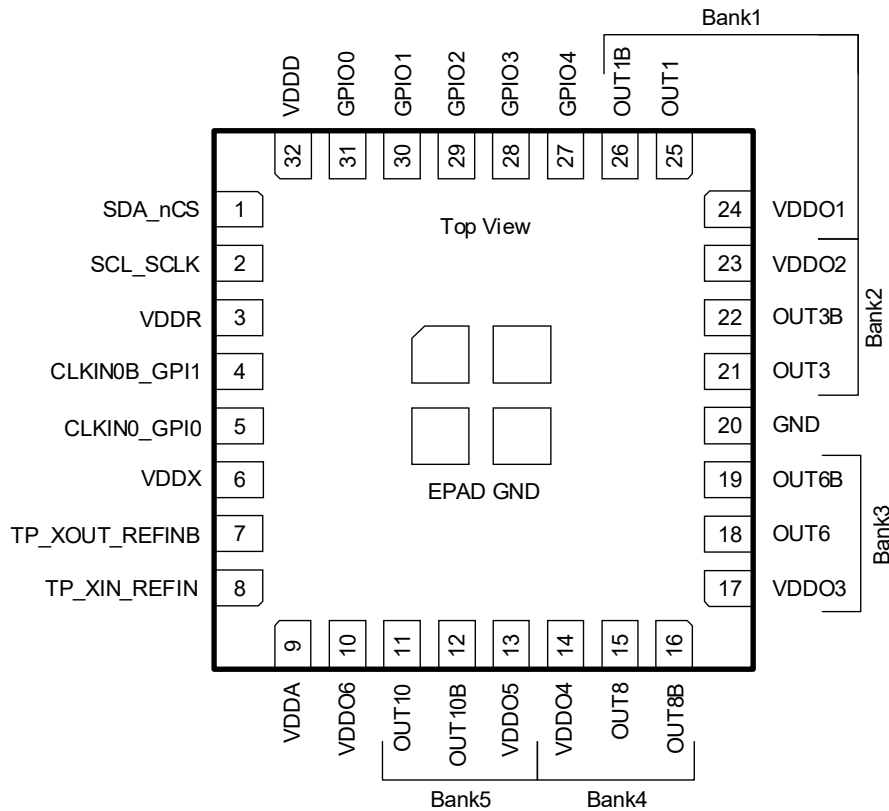
Table 3. RCxx008AQ Pin Descriptions

Number	Name	Type	Description
1	DNC	N/A	Do not connect. This pin should have no stubs.
2	DNC	N/A	Do not connect. This pin should have no stubs.
3	VDDX	Power	Power supply for Crystal oscillator. 1.8/2.5/3.3V supported.
4	CLKIN0_GPIO	I	Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPIO.
5	CLKIN0b_GPIO1	I	Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1.
6	VDDR	Power	Reference input supply. 1.8/2.5/3.3V supported.
7	CLKIN1_GPIO2	I	Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPIO2.
8	CLKIN1b_GPIO3	I	Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI3.
9	SCL_SCLK	I	I <sup>2</sup> C Mode: I <sup>2</sup> C interface bi-directional clock. SPI Mode: Serial Clock This pin is 3.3V tolerant.

Table 3. RCxx008AQ Pin Descriptions (Cont.)

Number	Name	Type	Description
10	SDA_nCS	I/O	I <sup>2</sup> C Mode: I <sup>2</sup> C interface bi-directional data in open-drain mode. SPI Mode: Chip Select (active low) This pin is 3.3V tolerant.
11	VDDD	Power	Power supply for digital core. 1.8/2.5/3.3V supported. When programming the OTP, this supply must be 2.5V or 3.3V.
12	GPIO0	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
13	GPIO1	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
14	GPIO2	I/O	General purpose input/output. 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
15	GPIO3	I/O	General purpose input/output.
16	GPIO4	I/O	General purpose input/output.
17	NC	I	Not connected.
18	VDDO1	Power	Supply voltage for output bank 1 and IOD 1. 1.8/2.5/3.3V supported.
19	OUT1b	O	Output Clock 1 negative.
20	OUT1	O	Output Clock 1 positive
21	VDDO2	Power	Supply voltage for output bank 2 and FOD 0. 1.8/2.5/3.3V supported.
22	OUT2b	O	Output Clock 2 negative.
23	OUT2	O	Output Clock 2 positive.
24	OUT3b	O	Output Clock 3 negative.
25	OUT3	O	Output Clock 3 positive.
26	OUT6b	O	Output Clock 6 negative.
27	OUT6	O	Output Clock 6 positive.
28	OUT7b	O	Output Clock 7 negative.
29	OUT7	O	Output Clock 7 positive.
30	VDDO3	Power	Supply voltage for output bank 3 and FOD 1. 1.8/2.5/3.3V supported.
31	OUT8b	O	Output Clock 8 negative.
32	OUT8	O	Output Clock 8 positive.
33	VDDO4	Power	Supply voltage for output bank 4 and FOD 2. 1.8/2.5/3.3V supported.
34	VDDO5	Power	Supply voltage for output bank 5 and IOD 2. 1.8/2.5/3.3V supported.
35	OUT10b	O	Output Clock 10 negative.
36	OUT10	O	Output Clock 10 positive.
37	OUT11b	O	Output Clock 11 negative.
38	OUT11	O	Output Clock 11 positive.
39	VDDO6	Power	Supply voltage for output bank 6 and IOD 3. 1.8/2.5/3.3V supported.
40	VDDA	Power	Power supply for analog, 1.8/2.5/3.3V supported.
EPAD	GND	Power	Ground. ePad must be connected to ground before any VDD is applied.

## 1.7 Pin Assignments – RCxx005AQ



## 1.8 Pin Descriptions – RCxx005AQ

Table 4. RCxx005AQ Pin Descriptions

Number	Name	Type	Description
1	SDA_nCS	I/O	I2C Mode: I <sup>2</sup> C interface bi-directional data in open-drain mode. SPI Mode: Chip Select (active low) This pin is 3.3V tolerant.
2	SCL_SCLK	I	I2C Mode: I <sup>2</sup> C interface bi-directional clock. SPI Mode: Serial Clock This pin is 3.3V tolerant.
3	VDDR	Power	Reference input supply. 1.8/2.5/3.3V supported
4	CLKIN0b_GPI1	I	Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1
5	CLKIN0_GPI0	I	Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPIO
6	VDDX	Power	Power supply for Crystal oscillator. 1.8/2.5/3.3V supported
7	TP_XOUT_REFINb	Do Not Connect	Crystal Output Test Point. This device is shipped with an internal crystal and this pin is a test point. It should not be connected and must not have any stubs.
8	TP_XIN_REFIN	Do Not Connect	Crystal Input Test Point. This device is shipped with an internal crystal and this pin is a test point. It should not be connected and must not have any stubs.
9	VDDA	Power	Power supply for analog, 1.8/2.5/3.3V supported

Table 4. RCxx005AQ Pin Descriptions (Cont.)

Number	Name	Type	Description
10	VDDO6	Power	Supply voltage for output bank 6 and IOD 3. 1.8/2.5/3.3V supported
11	OUT10	O	Output Clock 10 positive.
12	OUT10b	O	Output Clock 10 negative.
13	VDDO5	Power	Supply voltage for output bank 5 and IOD 2. 1.8/2.5/3.3V supported
14	VDDO4	Power	Supply voltage for output bank 4 and FOD 2. 1.8/2.5/3.3V supported
15	OUT8	O	Output Clock 8 positive.
16	OUT8b	O	Output Clock 8 negative.
17	VDDO3	Power	Supply voltage for output bank 3 and FOD 1. 1.8/2.5/3.3V supported
18	OUT6	O	Output Clock 6 positive.
19	OUT6b	O	Output Clock 6 negative.
20	GND	Power	Ground
21	OUT3	O	Output Clock 3 positive.
22	OUT3b	O	Output Clock 3 negative.
23	VDDO2	Power	Supply voltage for output bank 2 and FOD 0. 1.8/2.5/3.3V supported
24	VDDO1	Power	Supply voltage for output bank 1 and IOD 1. 1.8/2.5/3.3V supported.
25	OUT1	O	Output Clock 1 positive
26	OUT1b	O	Output Clock 1 negative.
27	GPIO4	I/O	General purpose input/output
28	GPIO3	I/O	General purpose input/output
29	GPIO2	I/O	General purpose input/output 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
30	GPIO1	I/O	General purpose input/output 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
31	GPIO0	I/O	General purpose input/output 3-level logic input during power-up and CMOS level logic after unless set to 3-level.
32	VDDD	Power	Power supply for digital core. 1.8/2.5/3.3V supported When programming the OTP, this supply must be 2.5V or 3.3V.
EPAD	GND	Power	Ground. ePad must be connected to ground before any VDD is applied.

## 1.9 Pin Characteristics

Table 5. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$C_{IN}$	Input Capacitance	CLKIN[1:0], CLKIN[1:0]b, GPI[0:3]	-	2	-	pF
		SCL_SCLK, SDA_nCS	-	3	-	
		XIN_REFIN [1]	-	5	-	
		XOUT_REFINb [1]	-	4	-	
		GPIO[0:4]	-	5	-	
$R_{PULLUP}$	Input Pull-Up Resistor	All pins with internal pull up capability	-	52.6	-	k $\Omega$
$R_{PULLDOWN}$	Input Pull-Down Resistor	All pins with internal pull down capability	-	52.6	-	
$Z_{OUTDC}$	Single-ended LP-HCSL Output Impedance	50 $\Omega$ single-ended (100 $\Omega$ differential).	-	51	-	40 to 60 $\Omega$
		42.5 $\Omega$ single-ended (85 $\Omega$ differential).	-	44	-	34 to 51 $\Omega$
	LVCMOS Output Impedance	VDDO = 3.3V	-	17.3	-	$\Omega$
		VDDO = 2.5V.	-	19.5	-	
		VDDO = 1.8V	-	17.6	-	

1. When used as clock input.

## 2. Specifications

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RC210xxA at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

### 2.1 Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
$V_{DD}$	Supply Voltage with respect to Ground	Any VDD pin	-0.5	3.63	V
$V_{IN}$	Input Voltage [1]	XIN_REFIN, XOUT_REFINb [2]	-0.5	$V_{DD} + 0.3$	V
		CLKIN[1:0]_GPI[1:0], CLKIN[1:0]b_GPI[3:2]	-0.5	$V_{DD} + 0.3$	V
		GPIO[4:0] used as inputs	-0.5	$V_{DD} + 0.3$	V
		SCL_SCLK, SDA_nCS	-0.5	3.63	V
$I_{IN}$	Input Current	CLKIN[1:0]_GPI[1:0], CLKIN[1:0]b_GPI[3:2]	-	±50	mA
$I_{OUT}$	Output Current - Continuous	OUT[11:0], OUT[11:0]b	-	30	mA
		GPIO[4:0] used as outputs, SDA_nCS	-	25	mA
	Output Current - Surge	OUT[11:0], OUT[11:0]b	-	60	mA
		GPIO[4:0] used as outputs, SDA_nCS	-	50	mA
$T_J$	Maximum Junction Temperature		-	150	°C
$T_S$	Storage Temperature	Storage Temperature	-65	150	°C

1. VDD refers to the VDD pin that supplies the particular input. To determine to which VDD pin the specification applies, see [Table 40](#).
2. This limit only applies when XIN\_REFIN/XOUT\_REFINb are configured as an "Input Buffer" for use with an external oscillator. No limit is implied when connected directly to a crystal.

### 2.2 ESD Ratings

Table 7. ESD Ratings

Symbol	Parameter	Conditions	Rating	Unit
ESD	Human Body Model	JESD22-A114 (JS-001) Classification	2000	V
	Charged Device Model	JESD22-C101 Classification	500	V



## 2.3 Recommended Operating Conditions

Table 8. Recommended Operating Conditions [1][2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T <sub>J</sub>	Maximum Junction Temperature		-	-	125	°C
T <sub>A</sub>	Ambient Operating temperature		-40	-	85	°C
V <sub>DDx</sub>	Supply Voltage with respect to Ground	Any VDD pin, 1.8V supply	1.71	1.8	1.89	V
		Any VDD pin, 2.5V supply	2.375	2.5	2.625	V
		Any VDD pin, 3.3V supply	3.135	3.3	3.465	V
t <sub>PU</sub>	Power up time for all VDDs to reach minimum specified voltage.	Power ramps must be monotonic. See the applications section for additional considerations.	0.05	-	5	ms

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.

## 2.4 Electrical Characteristics

Table 9. PCIe Refclk Jitter for VDDO = 1.8V [1][2]

Symbol	Parameter	Conditions	Typical	Maximum	PCIe Limit	Unit
t <sub>jphPCIeG1-CC</sub>	PCIe Refclk Jitter in Clock Generator Mode (Common Clocked Architecture, SSC = 0%, -0.3%, -0.5%)	PCIe Gen 1 (2.5 GT/s)	4330	8622	86,000	fs pk-pk
t <sub>jphPCIeG2-CC</sub>		PCIe Gen 2 Hi Band (5 GT/s)	265	547	3000	fs RMS
t <sub>jphPCIeG3-CC</sub>		PCIe Gen 2 Lo Band (5 GT/s)	76	210	3100	
t <sub>jphPCIeG4-CC</sub>		PCIe Gen 3 (8 GT/s)	126	246	1000	
t <sub>jphPCIeG5-CC</sub>		PCIe Gen 4 (16 GT/s) [3][4]	126	246	500	
t <sub>jphPCIeG6-CC</sub>		PCIe Gen 5 (32 GT/s) [3][5]	49	95	150	
		PCIe Gen 6 (64 GT/s) [3][6]	29	59	100	
t <sub>jphPCIeG2-SRIS</sub>	PCIe Refclk Jitter Clock Generator Mode (SRIS Architecture, SSC = -0.5%)	PCIe Gen 2 (5 GT/s)	1342	1474	N/A [7]	fs RMS
t <sub>jphPCIeG3-SRIS</sub>		PCIe Gen 3 (8 GT/s)	313	355		
t <sub>jphPCIeG4-SRIS</sub>		PCIe Gen 4 (16 GT/s)	137	178		
t <sub>jphPCIeG5-SRIS</sub>	PCIe Refclk Jitter Clock Generator Mode (SRIS Architecture, SSC = -0.3%)	PCIe Gen 5 (32 GT/s)	104	146		
t <sub>jphPCIeG6-SRIS</sub>	PCIe Gen 6 (64 GT/s)	115	174			
t <sub>jphPCIeG2-SRNS</sub>	PCIe Refclk Jitter in Clock Generator Mode (SRNS Architecture, SSC = 0%)	PCIe Gen 2 (5 GT/s)	137	277	N/A [7]	fs RMS
t <sub>jphPCIeG3-SRNS</sub>		PCIe Gen 3 (8 GT/s)	61	131		
t <sub>jphPCIeG4-SRNS</sub>		PCIe Gen 4 (16 GT/s)	61	131		
t <sub>jphPCIeG5-SRNS</sub>		PCIe Gen 5 (32 GT/s)	24	52		
t <sub>jphPCIeG6-SRNS</sub>		PCIe Gen 6 (64 GT/s)	15	31		

Table 9. PCIe Refclk Jitter for VDDO = 1.8V [1][2] (Cont.)

Symbol	Parameter	Conditions	Typical	Maximum	PCIe Limit	Unit
t <sub>jph</sub> PCIeG1-CC	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (CC Architecture, SSC = 0%, -0.3%, -0.5%)	PCIe Gen 1 (2.5 GT/s)	3242	10190	N/A [7][8]	fs pk-pk
t <sub>jph</sub> PCIeG2-CC		PCIe Gen 2 Hi Band (5 GT/s)	201	656		fs RMS
t <sub>jph</sub> PCIeG3-CC		PCIe Gen 2 Lo Band (5 GT/s)	44	160		
t <sub>jph</sub> PCIeG4-CC		PCIe Gen 3 (8 GT/s)	88	268		
t <sub>jph</sub> PCIeG5-CC		PCIe Gen 4 (16 GT/s) [3][4]	88	268		
t <sub>jph</sub> PCIeG6-CC		PCIe Gen 5 (32 GT/s) [3][5]	34	102		
		PCIe Gen 6 (64 GT/s) [3][6]	22	67		
t <sub>jph</sub> PCIeG2-SRIS	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = -0.5%)	PCIe Gen 2 (5 GT/s)	252	833	N/A [7][8]	fs RMS
t <sub>jph</sub> PCIeG3-SRIS		PCIe Gen 3 (8 GT/s)	65	210		
t <sub>jph</sub> PCIeG4-SRIS		PCIe Gen 4 (16 GT/s)	67	217		
t <sub>jph</sub> PCIeG5-SRIS	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = -0.3%)	PCIe Gen 5 (32 GT/s)	58	192		
t <sub>jph</sub> PCIeG6-SRIS		PCIe Gen 6 (64 GT/s)	76	257		
t <sub>jph</sub> PCIeG2-SRNS	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRNS Architecture, SSC = 0%)	PCIe Gen 2 (5 GT/s)	244	843	N/A [7][8]	fs RMS
t <sub>jph</sub> PCIeG3-SRNS		PCIe Gen 3 (8 GT/s)	63	212		
t <sub>jph</sub> PCIeG4-SRNS		PCIe Gen 4 (16 GT/s)	65	219		
t <sub>jph</sub> PCIeG5-SRNS		PCIe Gen 5 (32 GT/s)	57	194		
t <sub>jph</sub> PCIeG6-SRNS		PCIe Gen 6 (64 GT/s)	74	264		

- The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 6.0, Revision 0.9*. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
- SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
- Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 0.15 ps RMS is to be used in channel simulations to account for additional noise in a real system.
- The *PCI Express Base Specification 6.0, Revision 0.9* provides the filters necessary to calculate SRIS and SRNS jitter values; it does not provide specification limits, hence the N/A in the Limit column. SRIS and SRNS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
- The RMS sum of the source jitter and the additive jitter must be less than the jitter specification listed for the clock generator operating mode.

Table 10. PCIe Refclk Jitter for VDDO = 2.5V [1][2]

Symbol	Parameter	Conditions	Typical	Maximum	PCIe Limit	Unit
$t_{jphPCIeG1-CC}$	PCIe Refclk Jitter in Clock Generator Mode (Common Clocked Architecture, SSC = 0%, -0.3%, -0.5%)	PCIe Gen 1 (2.5 GT/s)	4054	5248	86,000	fs pk-pk
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Hi Band (5 GT/s)	241	322	3000	fs RMS
$t_{jphPCIeG3-CC}$		PCIe Gen 2 Lo Band (5 GT/s)	67	142	3100	
$t_{jphPCIeG4-CC}$		PCIe Gen 3 (8 GT/s)	118	150	1000	
$t_{jphPCIeG5-CC}$		PCIe Gen 4 (16 GT/s) [3][4]	118	150	500	
$t_{jphPCIeG6-CC}$		PCIe Gen 5 (32 GT/s) [3][5]	46	60	150	
		PCIe Gen 6 (64 GT/s) [3][6]	28	35	100	
$t_{jphPCIeG2-SRIS}$	PCIe Refclk Jitter Clock Generator Mode (SRIS Architecture, SSC = -0.5%)	PCIe Gen 2 (5 GT/s)	1328	1366	N/A [7]	fs RMS
$t_{jphPCIeG3-SRIS}$		PCIe Gen 3 (8 GT/s)	309	323		
$t_{jphPCIeG4-SRIS}$		PCIe Gen 4 (16 GT/s)	133	142		
$t_{jphPCIeG5-SRIS}$	PCIe Refclk Jitter Clock Generator Mode (SRIS Architecture, SSC = -0.3%)	PCIe Gen 5 (32 GT/s)	99	115		
$t_{jphPCIeG6-SRIS}$		PCIe Gen 6 (64 GT/s)	106	132		
$t_{jphPCIeG2-SRNS}$	PCIe Refclk Jitter in Clock Generator Mode (SRNS Architecture, SSC = 0%)	PCIe Gen 2 (5 GT/s)	125	215	N/A [7]	fs RMS
$t_{jphPCIeG3-SRNS}$		PCIe Gen 3 (8 GT/s)	55	81		
$t_{jphPCIeG4-SRNS}$		PCIe Gen 4 (16 GT/s)	55	81		
$t_{jphPCIeG5-SRNS}$		PCIe Gen 5 (32 GT/s)	21	33		
$t_{jphPCIeG6-SRNS}$		PCIe Gen 6 (64 GT/s)	13	19		
$t_{jphPCIeG1-CC}$	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (CC Architecture, SSC = 0%, -0.3%, -0.5%)	PCIe Gen 1 (2.5 GT/s)	2032	5139	N/A [7][8]	fs pk-pk
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Hi Band (5 GT/s)	122	277		fs RMS
$t_{jphPCIeG3-CC}$		PCIe Gen 2 Lo Band (5 GT/s)	34	65		
$t_{jphPCIeG4-CC}$		PCIe Gen 3 (8 GT/s)	57	137		
$t_{jphPCIeG5-CC}$		PCIe Gen 4 (16 GT/s) [3][4]	55	137		
$t_{jphPCIeG6-CC}$		PCIe Gen 5 (32 GT/s) [3][5]	23	56		
		PCIe Gen 6 (64 GT/s) [3][6]	14	33		
$t_{jphPCIeG2-SRIS}$	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = -0.5%)	PCIe Gen 2 (5 GT/s)	152	310	N/A [7][8]	fs RMS
$t_{jphPCIeG3-SRIS}$		PCIe Gen 3 (8 GT/s)	40	84		
$t_{jphPCIeG4-SRIS}$		PCIe Gen 4 (16 GT/s)	41	86		
$t_{jphPCIeG5-SRIS}$	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = -0.3%)	PCIe Gen 5 (32 GT/s)	36	94		
$t_{jphPCIeG6-SRIS}$		PCIe Gen 6 (64 GT/s)	46	108		

Table 10. PCIe Refclk Jitter for VDDO = 2.5V [1][2] (Cont.)

Symbol	Parameter	Conditions	Typical	Maximum	PCIe Limit	Unit
t <sub>jphPCIeG2-SRNS</sub>	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRNS Architecture, SSC = 0%)	PCIe Gen 2 (5 GT/s)	164	348	N/A [7][8]	fs RMS
t <sub>jphPCIeG3-SRNS</sub>		PCIe Gen 3 (8 GT/s)	43	94		
t <sub>jphPCIeG4-SRNS</sub>		PCIe Gen 4 (16 GT/s)	45	97		
t <sub>jphPCIeG5-SRNS</sub>		PCIe Gen 5 (32 GT/s)	39	102		
t <sub>jphPCIeG6-SRNS</sub>		PCIe Gen 6 (64 GT/s)	49	116		

- The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 6.0, Revision 0.9*. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
- SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
- Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 0.15 ps RMS is to be used in channel simulations to account for additional noise in a real system.
- The *PCI Express Base Specification 6.0, Revision 0.9* provides the filters necessary to calculate SRIS and SRNS jitter values; it does not provide specification limits, hence the N/A in the Limit column. SRIS and SRNS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
- The RMS sum of the source jitter and the additive jitter must be less than the jitter specification listed for the clock generator operating mode.

Table 11. PCIe Refclk Jitter for VDDO = 3.3V [1][2]

Symbol	Parameter	Conditions	Typical	Maximum	PCIe Limit	Unit
t <sub>jphPCIeG1-CC</sub>	PCIe Refclk Jitter in Clock Generator Mode (Common Clocked Architecture, SSC = 0%, -0.3%, -0.5%)	PCIe Gen 1 (2.5 GT/s)	4042	5554	86,000	fs pk-pk
t <sub>jphPCIeG2-CC</sub>		PCIe Gen 2 Hi Band (5 GT/s)	241	332	3000	fs RMS
		PCIe Gen 2 Lo Band (5 GT/s)	65	146	3100	
t <sub>jphPCIeG3-CC</sub>		PCIe Gen 3 (8 GT/s)	118	164	1000	
t <sub>jphPCIeG4-CC</sub>		PCIe Gen 4 (16 GT/s) [3][4]	118	164	500	
t <sub>jphPCIeG5-CC</sub>		PCIe Gen 5 (32 GT/s) [3][5]	46	65	150	
t <sub>jphPCIeG6-CC</sub>		PCIe Gen 6 (64 GT/s) [3][6]	27	37	100	

Table 11. PCIe Refclk Jitter for VDDO = 3.3V [1][2] (Cont.)

Symbol	Parameter	Conditions	Typical	Maximum	PCIe Limit	Unit
t <sub>jph</sub> PCleG2-SRIS	PCIe Refclk Jitter Clock Generator Mode (SRIS Architecture, SSC = -0.5%)	PCIe Gen 2 (5 GT/s)	1329	1392	N/A [7]	fs RMS
t <sub>jph</sub> PCleG3-SRIS		PCIe Gen 3 (8 GT/s)	309	328		
t <sub>jph</sub> PCleG4-SRIS		PCIe Gen 4 (16 GT/s)	133	145		
t <sub>jph</sub> PCleG5-SRIS	PCIe Refclk Jitter Clock Generator Mode (SRIS Architecture, SSC = -0.3%)	PCIe Gen 5 (32 GT/s)	99	114		
t <sub>jph</sub> PCleG6-SRIS		PCIe Gen 6 (64 GT/s)	106	132		
t <sub>jph</sub> PCleG2-SRNS	PCIe Refclk Jitter in Clock Generator Mode (SRNS Architecture, SSC = 0%)	PCIe Gen 2 (5 GT/s)	125	208	N/A [7]	fs RMS
t <sub>jph</sub> PCleG3-SRNS		PCIe Gen 3 (8 GT/s)	56	81		
t <sub>jph</sub> PCleG4-SRNS		PCIe Gen 4 (16 GT/s)	56	81		
t <sub>jph</sub> PCleG5-SRNS		PCIe Gen 5 (32 GT/s)	22	32		
t <sub>jph</sub> PCleG6-SRNS		PCIe Gen 6 (64 GT/s)	13	19		
t <sub>jph</sub> PCleG1-CC	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (CC Architecture, SSC = 0%, -0.3%, -0.5%)	PCIe Gen 1 (2.5 GT/s)	2256	4829	N/A [7][8]	fs RMS
t <sub>jph</sub> PCleG2-CC		PCIe Gen 2 Hi Band (5 GT/s)	132	241		
		PCIe Gen 2 Lo Band (5 GT/s)	35	51		
t <sub>jph</sub> PCleG3-CC		PCIe Gen 3 (8 GT/s)	63	122		
t <sub>jph</sub> PCleG4-CC		PCIe Gen 4 (16 GT/s) [3][4]	63	122		
t <sub>jph</sub> PCleG5-CC		PCIe Gen 5 (32 GT/s) [3][5]	25	50		
t <sub>jph</sub> PCleG6-CC		PCIe Gen 6 (64 GT/s) [3][6]	15	29		
t <sub>jph</sub> PCleG2-SRIS	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = -0.5%)	PCIe Gen 2 (5 GT/s)	139	301	N/A [7][8]	fs RMS
t <sub>jph</sub> PCleG3-SRIS		PCIe Gen 3 (8 GT/s)	36	80		
t <sub>jph</sub> PCleG4-SRIS		PCIe Gen 4 (16 GT/s)	38	83		
t <sub>jph</sub> PCleG5-SRIS	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = -0.3%)	PCIe Gen 5 (32 GT/s)	31	81		
t <sub>jph</sub> PCleG6-SRIS		PCIe Gen 6 (64 GT/s)	40	97		
t <sub>jph</sub> PCleG2-SRNS	Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRNS Architecture, SSC = 0%)	PCIe Gen 2 (5 GT/s)	148	286	N/A [7][8]	fs RMS
t <sub>jph</sub> PCleG3-SRNS		PCIe Gen 3 (8 GT/s)	39	77		
t <sub>jph</sub> PCleG4-SRNS		PCIe Gen 4 (16 GT/s)	40	79		
t <sub>jph</sub> PCleG5-SRNS		PCIe Gen 5 (32 GT/s)	34	83		
t <sub>jph</sub> PCleG6-SRNS		PCIe Gen 6 (64 GT/s)	44	95		

1. The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 6.0, Revision 0.9*. See the "Test Loads" section of the datasheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.

3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. The *PCI Express Base Specification 6.0, Revision 0.9* provides the filters necessary to calculate SRIS and SRNS jitter values; it does not provide specification limits, hence the N/A in the Limit column. SRIS and SRNS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. The RMS sum of the source jitter and the additive jitter must be less than the jitter specification listed for the clock generator operating mode.

**Table 12. Phase Jitter and Phase Noise – 1.8V VDDO [1][2]**

Symbol	Parameter	Conditions	Typical	Maximum	Unit
tjit( $\Phi$ )	Random Phase Jitter, 10kHz to 20MHz (78.125MHz XTAL, Synthesizer Mode) [2]	122.88MHz (VCO: 9.8304GHz, FOD 0, 1 or 2)	166	212	fs (RMS)
		156.25MHz (VCO: 10GHz, FOD 0, 1 or 2)	160	265	
		245.76MHz (VCO: 9.8304GHz, FOD 0, 1 or 2)	190	261	
		312.5MHz (VCO: 10GHz, FOD 0, 1 or 2)	137	227	
		322.265625MHz (VCO: 10.3125GHz, FOD 0, 1 or 2)	138	173	
		644.53125MHz (VCO: 10.3125GHz, FOD 0, 1 or 2)	125	155	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface.

**Table 13. Phase Jitter and Phase Noise – 2.5V VDDO [1][2]**

Symbol	Parameter	Conditions	Typical	Maximum	Unit
tjit( $\Phi$ )	Random Phase Jitter, 10kHz to 20MHz (78.125MHz XTAL, Synthesizer Mode) [2]	122.88MHz (VCO: 9.8304GHz, FOD 0, 1 or 2)	178	227	fs (RMS)
		156.25MHz (VCO: 10GHz, FOD 0, 1 or 2)	169	247	
		245.76MHz (VCO: 9.8304GHz, FOD 0, 1 or 2)	209	228	
		312.5MHz (VCO: 10GHz, FOD 0, 1 or 2)	149	166	
		322.265625MHz (VCO: 10.3125GHz, FOD 0, 1 or 2)	156	278	
		644.53125MHz (VCO: 10.3125GHz, FOD 0, 1 or 2)	155	250	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface.

**Table 14. Phase Jitter and Phase Noise – 3.3V VDDO [1][2]**

Symbol	Parameter	Conditions	Typical	Maximum	Unit
t <sub>jitter</sub> (Φ)	Random Phase Jitter, 10kHz to 20MHz (78.125MHz XTAL, Synthesizer Mode) [2]	122.88MHz (VCO: 9.8304GHz, FOD 0, 1 or 2)	168	218	fs (RMS)
		156.25MHz (VCO: 10GHz, FOD 0, 1 or 2)	164	226	
		245.76MHz (VCO: 9.8304GHz, FOD 0, 1 or 2)	206	234	
		312.5MHz (VCO: 10GHz, FOD 0, 1 or 2)	145	192	
		322.265625MHz (VCO: 10.3125GHz, FOD 0, 1 or 2)	154	188	
		644.53125MHz (VCO: 10.3125GHz, FOD 0, 1 or 2)	141	162	

- Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface.

**Table 15. Clock Input Frequencies [1]**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f <sub>INAPLL</sub>	APLL Input Frequency for clock generation.	Over-driving Crystal Input, Doubler Logic Disabled	1	-	650	MHz
		Over-driving Crystal Input, Doubler Logic Enabled	1	-	250	
		CLKIN[1:0] Differential Mode	1	-	650	
		CLKIN[1:0] Single-ended Mode	1	-	250	

- For crystal characteristics, see [Table 16](#).

**Table 16. External Crystal Characteristics**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
-	Resonance Mode	-	Fundamental			-
f <sub>INXTAL</sub> [1]	Crystal input frequency	Fundamental mode	8	-	80	MHz
ESR [1]	Equivalent Series Resistance	8MHz ≤ f <sub>INXTAL</sub> ≤ 12MHz, C <sub>L</sub> = 12pF	-	-	120	Ω
		12MHz < f <sub>INXTAL</sub> ≤ 28MHz, C <sub>L</sub> = 12pF	-	-	80	
		28MHz < f <sub>INXTAL</sub> ≤ 54MHz, C <sub>L</sub> = 12pF	-	-	50	
		54MHz < f <sub>INXTAL</sub> ≤ 80MHz, C <sub>L</sub> = 8pF	-	-	50	
C <sub>O</sub> [1]	Shunt Capacitance	-	-	7	-	pF
C <sub>L</sub> [1]	Load Capacitance	-	6	8	12	
Drive [1]	Drive Level	-	-	-	100	μW
F <sub>TOL</sub>	Frequency Tolerance	Center frequency at 25°C	-	-	[2]	ppm
F <sub>STAB</sub>	Frequency Stability	Over Operating Temperature Range with respect to F <sub>TOL</sub>	-	-		
Aging	Per Year	-	-	-		

- These parameters are required, regardless of crystal used.
- These parameters are customer/application dependent. Common maximum values are F<sub>TOL</sub> = ±20ppm, F<sub>STAB</sub> = ±20ppm, and Aging = ±5ppm/10years. The customer is free to adjust these parameters to their particular requirements.

Table 17. Internal Crystal Characteristics (AQ Versions Only)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
-	Resonance Mode	-	Fundamental			-
$f_{\text{INTAL}}$	Crystal frequency	Fundamental mode	-	78.125	-	MHz
$F_{\text{STAB}}$	Frequency Stability	Includes both initial accuracy and variation over temperature.	-	-	$\pm 30$	ppm
-	Aging	Over the first ten years	-	-	$\pm 5$	

Table 18. Output Frequencies and Startup Times [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$f_{\text{OUT}}$	Output Frequency	Differential Output.	0.001	-	650	MHz
		LVC MOS Output.	0.001	-	200	
$f_{\text{MON}}$	Reference Monitor Operating Frequency	-	-	-	40	MHz
$f_{\text{VCO}}$	VCO (APLL) Operating Frequency	-	9.5	-	10.7	GHz
$t_{\text{STARTUP}}$	Start-up Time [2][3]	Synthesizer mode.	-	6	10	ms

- Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected. Includes time needed to load a configuration from internal OTP. For important additional power supply sequencing considerations, see [Power Considerations](#).
- Start-up time will depend on the actual configuration used. For more information, please contact Renesas technical support

Table 19. Output-to-Output, Input-to-Output Skew – LP-HCSL Outputs 1.8V/2.5V/3.3V VDDO [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$t_{\text{SK}}$	Output-to-Output Skew [2][3]	FOD1 driving output banks [2:4]	-	18	90	ps
		FOD1 driving all output banks	-	39	124	
		FOD1 driving Bank2	-	21	63	
		IOD1 driving bank 2	-	22	65	
$t_{\text{PD}}$	Input-to-Output Delay [3][4]	Fanout buffer path to any output	1.2	2	2.6	ns
$\Delta t_{\text{PD}}$	Input-to-Output Delay Variation [3][4]	Fanout buffer, single device, at a fixed voltage, over temperature	-	2	4	ps/°C

- Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
- This parameter is defined in accordance with JEDEC Standard 65
- Defined as the time between to output rising edge and the input rising edge that caused it.



Table 20. Output-to-Output, Input-to-Output Skew – LVDS Outputs 1.8V/2.5V/3.3V VDDO [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$t_{SK}$	Output-to-Output Skew [2][3]	FOD1 driving output banks [2:4]	-	16	93	ps
		FOD1 driving all output banks	-	44	101	
		FOD1 driving Bank2	-	14	53	
		IOD1 driving bank 2	-	20	67	
$t_{PD}$	Input-to-Output Delay [3][4]	Fanout buffer path to any output	1.3	2	2.8	ns

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65
4. Defined as the time between to output rising edge and the input rising edge that caused it.

Table 21. Output-to-Output, Input-to-Output Skew – LVCMOS Outputs 1.8V/2.5V/3.3V VDDO [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$t_{SK}$	Output-to-Output Skew [2][3]	FOD1 driving output banks [2:4]	-	50	130	ps
		FOD1 driving all output banks	-	76	180	
		FOD1 driving Bank2	-	22	64	
		IOD1 driving bank 2	-	29	79	
$t_{PD}$	Input-to-Output Delay [3][4]	Fanout buffer path to any output - 1.8V VDDO	2.3	3.2	4.3	ns
		Fanout buffer path to any output - 2.5V VDDO	1.7	2.4	3.4	
		Fanout buffer path to any output - 3.3V VDDO	1.6	2.2	3	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65
4. Defined as the time between to output rising edge and the input rising edge that caused it.

Table 22. LVDS AC/DC Output Characteristics – 1.8V V<sub>DDO</sub> [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>OT</sub> (+)	TRUE binary state.	out_prog = 0x00	243	346	448	mV
V <sub>OT</sub> (-)	FALSE binary state.		-462	-355	-248	
V <sub>OT</sub> (+)	TRUE binary state.	out_prog = 0x01	257	362	468	mV
V <sub>OT</sub> (-)	FALSE binary state.		-482	-372	-262	
V <sub>OT</sub> (+)	TRUE binary state.	out_prog = 0x02	219	310	400	mV
V <sub>OT</sub> (-)	FALSE binary state.		-419	-323	-227	
V <sub>OT</sub> (+)	TRUE binary state.	out_prog = 0x03	232	328	425	mV
V <sub>OT</sub> (-)	FALSE binary state.		-441	-338	-235	
ΔV <sub>OT</sub>	Change in V <sub>OT</sub> between Complimentary Output States	-	14	37	60	mV
V <sub>CMR</sub>	Output Common Mode Voltage	-	1.07	1.21	1.35	V
ΔV <sub>CMR</sub>	Change in V <sub>CMR</sub> between Complimentary Output States	-	-	25	37	mV
I <sub>OS</sub>	Output Short Circuit Current	V <sub>OUT+</sub> or V <sub>OUT-</sub> = 0V or VDD	-	7.5	-	mA
I <sub>OSD</sub>	Differential Output Short Circuit Current	V <sub>OUT+</sub> = V <sub>OUT-</sub>	-	3.3	-	
t <sub>R</sub> /t <sub>F</sub>	Rise/Fall Time [2] V <sub>T</sub> = 20% to 80% of swing.	-	138	252	365	ps
t <sub>DC</sub>	Output Duty Cycle	V <sub>T</sub> = 0V differential	43.9	49.7	54.3	%

1. See Test Loads for additional test conditions.

2. Single-ended measurement

Table 23. LVDS AC/DC Output Characteristics – 2.5V/3.3V  $V_{DDO}$  [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{OT (+)}$	TRUE binary state.	out_prog = 0x00	240	348	457	mV
$V_{OT (-)}$	FALSE binary state.		-464	-356	-247	
$V_{OT (+)}$	TRUE binary state.	out_prog = 0x01	255	366	477	mV
$V_{OT (-)}$	FALSE binary state.		-483	-372	-261	
$V_{OT (+)}$	TRUE binary state.	out_prog = 0x02	211	311	411	mV
$V_{OT (-)}$	FALSE binary state.		-427	-325	-224	
$V_{OT (+)}$	TRUE binary state.	out_prog = 0x03	225	330	434	mV
$V_{OT (-)}$	FALSE binary state.		-446	-341	-235	
$\Delta V_{OT}$	Change in $V_{OT}$ between Complimentary Output States	-	14	37	60	mV
$V_{CMR}$	Output Common Mode Voltage	-	1.16	1.21	1.32	V
$\Delta V_{CMR}$	Change in $V_{CMR}$ between Complimentary Output States	-	-	25	37	mV
$I_{OS}$	Output Short Circuit Current	$V_{OUT+}$ or $V_{OUT-} = 0V$ or $V_{DD}$	-	7.5	-	mA
$I_{OSD}$	Differential Output Short Circuit Current	$V_{OUT+} = V_{OUT-}$	-	3.3	-	
$t_R/t_F$	Rise/Fall Time [2] $V_T = 20\%$ to $80\%$ of swing.	-	138	252	365	ps
$t_{DC}$	Output Duty Cycle	$V_T = 0V$ differential	43.9	49.7	54.3	%

1. See Test Loads for additional test conditions.
2. Single-ended measurement

Table 24. LP-HCSL AC/DC Characteristics, Non-PCIe Frequencies – 1.8V V<sub>DDO</sub><sup>[1]</sup>

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit	
V <sub>OH</sub>	Output High Voltage <sup>[2]</sup> f < 400MHz	V <sub>HIGH</sub> = 800mV, Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz.	680	849	1018	mV	
	Output High Voltage <sup>[2]</sup> f ≥ 400MHz		522	657	792		
V <sub>OL</sub>	Output Low Voltage <sup>[2]</sup>		-130	-4	123		
V <sub>CROSS</sub>	Crossing Voltage (abs) <sup>[3]</sup>		166	423	680		
ΔV <sub>CROSS</sub>	Crossing Voltage (var) <sup>[3][4][5]</sup>		-	30	43		
t <sub>R</sub> /t <sub>F</sub>	Rise/Fall Time <sup>[2]</sup> V <sub>T</sub> = 20% to 80% of swing, f < 400MHz		232	392	552	ps	
	Rise/Fall Time <sup>[2]</sup> V <sub>T</sub> = 20% to 80% of swing, f ≥ 400MHz		160	300	439		
V <sub>OH</sub>	Output High Voltage <sup>[2]</sup> f < 400MHz		V <sub>HIGH</sub> = 900mV, Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz.	718	924	1130	mV
	Output High Voltage <sup>[2]</sup> f ≥ 400MHz			551	703	855	
V <sub>OL</sub>	Output Low Voltage <sup>[2]</sup>			-164	-2	160	
V <sub>CROSS</sub>	Crossing Voltage (abs) <sup>[3]</sup>	170		446	722		
ΔV <sub>CROSS</sub>	Crossing Voltage (var) <sup>[3][4][5]</sup>	-		27	41		
t <sub>R</sub> /t <sub>F</sub>	Rise/Fall Time <sup>[2]</sup> V <sub>T</sub> = 20% to 80% of swing, f < 400MHz	217		402	588	ps	
	Rise/Fall Time <sup>[2]</sup> V <sub>T</sub> = 20% to 80% of swing, f ≥ 400MHz	169		298	428		
t <sub>DC</sub>	Output Duty Cycle <sup>[6]</sup>	Across all settings, f < 400MHz V <sub>T</sub> = 0V.		47	50	53	%
		Across all settings, f ≥ 400MHz V <sub>T</sub> = 0V.		45	50	55	

- Standard high impedance load with C<sub>L</sub> = 2pF. See Test Loads
- Measured from single-ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
- Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum variance in V<sub>CROSS</sub> for any particular system.
- Measured from differential waveform.

Table 25. LP-HCSL AC/DC Characteristics, Non-PCIe Frequencies – 2.5V/3.3V V<sub>DDO</sub> [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit	
V <sub>OH</sub>	Output High Voltage [2] f < 400MHz.	V <sub>HIGH</sub> = 800mV, Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz.	667	861	1055	mV	
	Output High Voltage [2] f ≥ 400MHz.		552	717	881	mV	
V <sub>OL</sub>	Output Low Voltage [2]		-164	-4	156	mV	
V <sub>CROSS</sub>	Crossing Voltage (abs) [3]		261	384	507	mV	
ΔV <sub>CROSS</sub>	Crossing Voltage (var) [3][4][5]		-	27	42	mV	
t <sub>R</sub> /t <sub>F</sub>	Rise/Fall Time [2] V <sub>T</sub> = 20% to 80% of swing, f < 400MHz.		214	393	606	ps	
	Rise/Fall Time [2] V <sub>T</sub> = 20% to 80% of swing f ≥ 400MHz		148	302	456		
V <sub>OH</sub>	Output High Voltage [2] f < 400MHz.		V <sub>HIGH</sub> = 900mV, Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz.	694	917	1140	mV
	Output High Voltage [2] f ≥ 400MHz.			598	757	917	mV
V <sub>OL</sub>	Output Low Voltage [2]			-164	-8	148	mV
V <sub>CROSS</sub>	Crossing Voltage (abs) [3]	238		455	673	mV	
ΔV <sub>CROSS</sub>	Crossing Voltage (var) [3][4][5]	-		27	42	mV	
t <sub>R</sub> /t <sub>F</sub>	Rise/Fall Time [2] V <sub>T</sub> = 20% to 80% of swing, f < 400MHz.	218		397	581	ps	
	Rise/Fall Time [2] V <sub>T</sub> = 20% to 80% of swing f ≥ 400MHz	174		300	426		
t <sub>DC</sub>	Output Duty Cycle [6]	Across all settings, f < 400MHz V <sub>T</sub> = 0V.		48	50	52	%
		Across all settings, f ≥ 400MHz V <sub>T</sub> = 0V.		45	50	55	

- Standard high impedance load with C<sub>L</sub> = 2pF. See Test Loads.
- Measured from single-ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
- Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in V<sub>CROSS</sub> for any particular system.
- Measured from differential waveform.

Table 26. LP-HCSL AC/DC Characteristics, 100MHz PCIe – 1.8V V<sub>DDO</sub> [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Spec. Limit [2]	Unit
V <sub>MAX</sub>	Absolute Max Voltage Includes 300mV of overshoot (Vovs) [3][4]	V <sub>HIGH</sub> set to 900mV.	-	-	1103	1150	mV
V <sub>MIN</sub>	Absolute Min Voltage Includes -300mV of undershoot (Vuds) [3][5]		-152	-	-	-300	
V <sub>HIGH</sub>	Voltage High [3]	V <sub>HIGH</sub> set to 800mV.	825	886	984	-	mV
V <sub>LOW</sub>	Voltage Low [3]		-70	-15	44	-	
V <sub>CROSS</sub>	Crossing Voltage (abs) [3][6][7]	V <sub>HIGH</sub> set to 800mV, scope averaging off.	266	406	545	250 to 550	
ΔV <sub>CROSS</sub>	Crossing Voltage (var) [3][6][8]		-	27	49	140	
dv/dt	Slew rate [9][10]	V <sub>HIGH</sub> set to 800mV, Fast slew rate, scope averaging on.	1.6	2.6	3.6	1 to 4	V/ns
		V <sub>HIGH</sub> set to 800mV, Slow slew rate, scope averaging on.	1.2	1.8	2.4		
ΔT <sub>RF</sub>	Rise/fall matching [3][11]	V <sub>HIGH</sub> set to 800mV. Fast or slow slew rate.	-	7	19.3	20	%
V <sub>HIGH</sub>	Voltage High [3]	V <sub>HIGH</sub> set to 900mV.	844	940	1037	-	mV
V <sub>LOW</sub>	Voltage Low [3]		-79	-14	51	-	
V <sub>CROSS</sub>	Crossing Voltage (abs) [3][6][7]	V <sub>HIGH</sub> set to 900mV, scope averaging off.	301	451	600	300 to 600	
ΔV <sub>CROSS</sub>	Crossing Voltage (var) [3][6][8]		-	28	44	140	
dv/dt	Slew rate [9][10]	V <sub>HIGH</sub> set to 900mV, Fast slew rate, scope averaging on.	1.7	2.7	3.7	1 to 4	V/ns
		V <sub>HIGH</sub> set to 900mV, Slow slew rate, scope averaging on.	1.3	1.9	2.5		
ΔT <sub>RF</sub>	Rise/fall matching [3][11]	V <sub>HIGH</sub> set to 900mV. Fast or slow slew rate.	-	4	18.5	20	%
t <sub>DC</sub>	Output Duty Cycle [9]	V <sub>T</sub> = 0V differential.	49	50	51	45 to 55	
t <sub>jycyc-cyc</sub>	Jitter, Cycle to cycle [9]	Across all settings in this table at 100MHz.		33	49.3	50	ps

- Standard high impedance load with C<sub>L</sub> = 2pF. See Test Loads.
- The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
- Measured from single-ended waveform.
- Defined as the maximum instantaneous voltage including overshoot.
- Defined as the minimum instantaneous voltage including undershoot.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
- Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V<sub>CROSS</sub> for any particular system.

- 9. Measured from differential waveform.
- 10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
- 11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

**Table 27. LP-HCSL AC/DC Characteristics, 100MHz PCIe – 2.5V/3.3V V<sub>DDO</sub> [1]**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Spec. Limit [2]	Unit
V <sub>MAX</sub>	Absolute Max Voltage Includes 300mV of overshoot (V <sub>ovs</sub> ) [3][4]	V <sub>HIGH</sub> set to 900mV.	-	-	1088	1150	mV
V <sub>MIN</sub>	Absolute Min Voltage Includes -300mV of undershoot (V <sub>uds</sub> ) [3][5]		-174	-	-	-300	
V <sub>HIGH</sub>	Voltage High [3]	V <sub>HIGH</sub> set to 800mV.	743	869	994	-	mV
V <sub>LOW</sub>	Voltage Low [3]		-92	-7	58	-	
V <sub>CROSS</sub>	Crossing Voltage (abs) [3][6][7]	V <sub>HIGH</sub> set to 800mV, scope averaging off.	256	406	533	250 to 550	
ΔV <sub>CROSS</sub>	Crossing Voltage (var) [3][6][8]		-	27	40	140	
dv/dt	Slew rate [9][10]	V <sub>HIGH</sub> set to 800mV, Fast slew rate, scope averaging on.	1.3	2.6	3.9	1 to 4	V/ns
		V <sub>HIGH</sub> set to 800mV, Slow slew rate, scope averaging on.	1	1.7	3.1		
ΔT <sub>R/F</sub>	Rise/fall matching [3][11]	V <sub>HIGH</sub> set to 800mV. Fast or slow slew rate.	-	8	19.7	20	%
V <sub>HIGH</sub>	Voltage High [3]	V <sub>HIGH</sub> set to 900mV.	800	925	1051	-	mV
V <sub>LOW</sub>	Voltage Low [3]		-95	-2	68	-	
V <sub>CROSS</sub>	Crossing Voltage (abs) [3][6][7]	V <sub>HIGH</sub> set to 900mV, scope averaging off.	286	454	629	250 to 600	
ΔV <sub>CROSS</sub>	Crossing Voltage (var) [3][6][8]		-	27	40	140	
dv/dt	Slew rate [9][10]	V <sub>HIGH</sub> set to 900mV, Fast slew rate, scope averaging on.	1.4	2.8	4.2	1 to 4.2	V/ns
		V <sub>HIGH</sub> set to 900mV, Slow slew rate, scope averaging on.	1.2	2.0	3		
ΔT <sub>R/F</sub>	Rise/fall matching [3][11]	V <sub>HIGH</sub> set to 900mV. Fast or slow slew rate.	-	6	18.7	20	%
t <sub>DC</sub>	Output Duty Cycle [9]	V <sub>T</sub> = 0V differential.	49	50	51	45 to 55	
t <sub>jyc-cyc</sub>	Jitter, Cycle to cycle [9]	Across all settings in this table at 100MHz.	-	30	48.3	50	ps

- 1. Standard high impedance load with C<sub>L</sub> = 2pF. See Test Loads.
- 2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
- 3. Measured from single-ended waveform.

4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in  $V_{CROSS}$  for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a  $\pm 75$  mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

**Table 28. 100MHz PCIe Output Clock Accuracy and SSC**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	PCIe Limit <sup>[1]</sup>	Unit
$T_{PERIOD\_AVG\_32G\_64G\_CC}$	Average Clock Period Accuracy for devices supporting 32GT/s or 64GT/s CC mode at any speed. [2][3]	SSC $\leq$ -0.5%, includes spread-spectrum modulation, if any.	0	-	2410	-100 to +2600	ppm
$T_{PERIOD\_AVG\_32G\_64G\_SRIS}$	Average Clock Period Accuracy for devices supporting 32GT/s SRIS mode at any speed. [2][3]	SSC $\leq$ -0.3%, includes spread-spectrum modulation, if any.	0	-	1430	-100 to +1600	
$T_{PERIOD\_AVG\_32G\_64G}$	Average Clock Period Accuracy for devices supporting 32GT/s CC/SRNS mode at any speed. [2][3]	SSC = 0% (SSC Off).	0	-	0	$\pm 100$	
$T_{PERIOD\_ABS\_32G\_64G\_CC}$	Average Clock Period Accuracy for devices supporting 32GT/s CC mode at any speed. [2][4]	SSC $\leq$ -0.5%, includes jitter and spread-spectrum modulation.	10	-	10.024	9.849 to 10.201	ns
$T_{PERIOD\_ABS\_32G\_64G\_SRIS}$	Average Clock Period Accuracy for devices supporting 32GT/s SRIS mode at any speed. [2][4]	SSC $\leq$ -0.3%, includes jitter and spread-spectrum modulation.	10	-	10.014	9.849 to 10.181	
$T_{PERIOD\_ABS\_32G\_64G}$	Average Clock Period Accuracy for devices supporting 32GT/s CC/SRNS mode at any speed. [2][4]	SSC = 0% (SSC Off), includes jitter.	10	-	10	9.849 to 10.151	
$F_{REFCLK\_32G\_64G}$	Refclk Frequency for devices that support 32GT/s or 64GT/s.	SSC = 0% (SSC Off)	100	-	100	99.99 to 100.01	MHz
$F_{SSC}$	SSC Modulation Frequency		31.2	31.5	31.9	30 to 33	kHz
$T_{SSC\_FREQ\_DEV}$	SSC Deviation for all devices and architectures except 32GT/s or 64GT/s devices operating in SRIS mode.	SSC = -0.5%	-0.490	-0.488	-0.486	-0.5	%



Table 28. 100MHz PCIe Output Clock Accuracy and SSC (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	PCIe Limit <sup>[1]</sup>	Unit
T <sub>SSC_FREQ_DEV_32G_64G_SRIS</sub>	SSC Deviation for devices that support 32 or 64GT/s operating in SRIS mode, at any speeds.	SSC = -0.3%	-0.300	-0.295	-0.290	-0.3	%
T <sub>SSC_MAX_FREQ_SLEW</sub>	Max df/dt of the SSC. <sup>[5]</sup>		-	310	372	1250	ppm/ us
T <sub>TRANSPORT_DELAY</sub>	Tx-Rx transport delay used for PCIe Jitter calculations. <sup>[6]</sup>	Applies to Common Clocked architectures only.	-	-	12	12	ns

1. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
2. Measured from differential waveform.
3. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100PPM, then we have an error budget of 100Hz/PPM \* 100PPM = 10kHz. The period is to measured with a frequency counter with measurement window set to 100 ms or greater. The ±100PPM applies to systems that do not employ Spread-Spectrum Clocking, or that use common clock source. For systems employing Spread-Spectrum Clocking, there is an additional 2,500PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600PPM for Common Clock Architectures. SRIS Architectures may have a lower allowed spread percentage. Devices meeting these specifications automatically meet the less stringent -300ppm to +2800ppm tolerances for data rates ≤16GT/s. Refer to Section 8.6 of the *PCI Express Base Specification, Revision 6.0*.
4. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread-spectrum modulation. Devices meeting these specifications automatically meet the less stringent and 9.847ns to 10.203ns tolerances for data rates ≤16GT/s.
5. Measurement is made over a 0.5us time interval with a 1st order LPF with an fC of 60x the SSC modulation frequency (1.89MHz for 31.5kHz modulation frequency).
6. This is the default value used for all PCIe Common Clock architecture jitter calculations. There are form factors (for example topologies including long cables) that may exceed this limit. Contact Renesas for assistance calculating jitter if your topology exceeds 12ns.

Table 29. Spread-Spectrum Programmability

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f <sub>SSCMOD</sub>	SSC Modulation Frequency	Modulation frequency.	30	-	63	kHz
SSC%	Spread percentage <sup>[1]</sup>	Down Spread.	-1	-	-0.5	%
		Center Spread.	±0.025	-	±0.75	
f <sub>OUTSSC</sub>	Output frequency	Allowable output frequency range when SSC is enabled.	33	-	650	MHz

1. Spread off is 0%.

Table 30. GPI/GPIO Electrical Characteristics – 1.8V VDDD, VDDR, or VDDX [1][2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input High Voltage [3]	XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0].	0.65 VDD	-	VDD + 0.3	V
V <sub>IL</sub>	Input Low Voltage [3]	XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0].	-0.3	-	0.35 VDD	
V <sub>OH</sub>	Output High Voltage [3]	GPIO[4:0], IOH = -2mA.	VDD - 0.45	-	VDD + 0.3	
V <sub>OL</sub>	Output Low Voltage [3]	GPIO[4:0], IOL = 2mA.	-	-	0.45	
V <sub>IH</sub>	Input High Voltage	GPIO[2:0], when set to tri-level.	0.75 VDD	-	VDD + 0.3	
V <sub>IM</sub>	Input Mid Voltage	GPIO[2:0], when set to tri-level.	0.45 VDD	-	0.55 VDD	
V <sub>IL</sub>	Input Low Voltage	GPIO[2:0], when set to tri-level.	-0.3	-	0.25 VDD	

1. Input specifications refer to signals XIN\_REFIN, XOUT\_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 30, see GPI and GPIO VDD pin assignments in Pin Information. For SCL\_SCLK, SDA\_SDI, see the I2C/SMBus electrical characteristics Table 35 and Table 36.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8-7A. These values only apply to XIN\_REFIN and XOUT\_REFINb when "Input Buffer" mode is selected. See the Applications section for more details.

Table 31. GPI/GPIO Electrical Characteristics – 2.5V VDDD, VDDR, or VDDX [1][2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input High Voltage [3]	XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0].	1.7	-	VDD + 0.3	V
V <sub>IL</sub>	Input Low Voltage [3]	XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0].	-0.3	-	0.7	
V <sub>OH</sub>	Output High Voltage [3]	GPIO[4:0], IOH = -2mA.	1.7	-	VDD + 0.3	
V <sub>OL</sub>	Output Low Voltage [3]	GPIO[4:0], IOL = 2mA.	-	-	0.7	
V <sub>IH</sub>	Input High Voltage	GPIO[2:0], when set to tri-level.	0.75 VDD	-	VDD + 0.3	
V <sub>IM</sub>	Input Mid Voltage	GPIO[2:0], when set to tri-level.	0.45 VDD	-	0.55 VDD	
V <sub>IL</sub>	Input Low Voltage	GPIO[2:0], when set to tri-level.	-0.3	-	0.25 VDD	

1. Input specifications refer to signals XIN\_REFIN, XOUT\_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 31, see GPI and GPIO VDD pin assignments in Pin Information. For SCL\_SCLK, SDA\_SDI, see the I2C/SMBus electrical characteristics Table 35 and Table 36.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8-5A.01. These values only apply to XIN\_REFIN and XOUT\_REFINb when "Input Buffer" mode is selected. See the Applications section for more details.

**Table 32. GPI/GPIO Electrical Characteristics – 3.3V VDDD, VDDR, or VDDX [1][2]**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	Input High Voltage [3]	XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0].	2.2	-	VDD + 0.3	V
V <sub>IL</sub>	Input Low Voltage [3]	XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0].	-0.3	-	0.8	
V <sub>OH</sub>	Output High Voltage [3]	GPIO[4:0], IOH = -2mA.	2.4	-	VDD + 0.3	
V <sub>OL</sub>	Output Low Voltage [3]	GPIO[4:0], IOL = 2mA.	-	-	0.4	
V <sub>IH</sub>	Input High Voltage	GPIO[2:0], when set to tri-level.	0.75 VDD	-	VDD + 0.3	
V <sub>IM</sub>	Input Mid Voltage	GPIO[2:0], when set to tri-level.	0.45 VDD	-	0.55 VDD	
V <sub>IL</sub>	Input Low Voltage	GPIO[2:0], when set to tri-level.	-0.3	-	0.25 VDD	

1. Input specifications refer to signals XIN\_REFIN, XOUT\_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 32, see GPI and GPIO VDD pin assignments in Pin Information. For SCL\_SCLK, SDA\_SDI, see the I2C/SMBus electrical characteristics Table 35 and Table 36.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8-5A.01. These values only apply to XIN\_REFIN and XOUT\_REFINb when “Input Buffer” mode is selected. See the Applications section for more details.

**Table 33. CMOS GPI/GPIO Common Electrical Characteristics [1][2]**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I <sub>IL</sub>	Input Leakage Current	Includes input pull up/pull down resistor current. V <sub>IL</sub> = 0V, V <sub>IH</sub> = V <sub>DD</sub> .	-15	-	15	μA

1. Input specifications refer to signals XIN\_REFIN, XOUT\_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. For VDD pin mapping, see GPI and GPIO VDD pin assignments in Pin Information.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.

**Table 34. Power Supply Current [1]**

Symbol	Parameter	Conditions	Typical	Maximum	Unit
I <sub>DDR</sub>	V <sub>DDR</sub> Supply Current	CMOS inputs (per input) [2][3]	11	20	mA
		HCSL inputs (per input pair) [3]	12	15	
		LVDS inputs (per input pair) [2][3]	13	14	
		LVPECL inputs (per input pair) [3][4] V <sub>DDR</sub> = 2.5V or 3.3V,	13	15	
		CML inputs (per input pair) [3][4] V <sub>DDR</sub> = 2.5V or 3.3V, input termination disabled.	14	16	
		CML inputs (per input pair) [3][4] V <sub>DDR</sub> = 2.5V or 3.3V, input termination enabled.	33	54	
I <sub>DDRBias</sub>	Bias Supply Current	Internal DC-bias circuit when enabled for AC-coupled external clock (per input pair) [3]	13	24	mA

Table 34. Power Supply Current [1] (Cont.)

Symbol	Parameter	Conditions	Typical	Maximum	Unit
I <sub>DDX</sub>	V <sub>DDX</sub> Supply Current	Crystal oscillator supply	3.5	5	mA
I <sub>DDA</sub>	V <sub>DDA</sub> Supply Current	V <sub>DDA</sub> = any valid supply.	142	151	mA
I <sub>DDD</sub>	V <sub>DDD</sub> Supply Current	V <sub>DDD</sub> = any valid supply.	69	73	mA
I <sub>DDO_CMOS</sub>	V <sub>DDO</sub> Supply Current per output pair, CMOS mode (both OUT[x] and OUT[x]b enabled). [5][6]	V <sub>DDO</sub> = 1.8V ±5%.	13	20	mA
		V <sub>DDO</sub> = 2.5V ±5%.	18	24	
		V <sub>DDO</sub> = 3.3V ±5%.	25	33	
	V <sub>DDO</sub> Supply Current per output pair, CMOS mode (OUT[x] or OUT[x]b enabled, other output Hi-Z). [5][6]	V <sub>DDO</sub> = 1.8V ±5%.	8	16	mA
		V <sub>DDO</sub> = 2.5 ±5%.	11	17	
		V <sub>DDO</sub> = 3.3 ±5%.	15	23	
I <sub>DDO_LPHCSL</sub>	V <sub>DDO</sub> Supply Current per output pair [5][6]	LP-HCSL outputs, 85ohm impedance, fast slew rate, 650MHz. V <sub>DDO</sub> = any valid supply.	12	19	mA
		LP-HCSL outputs, 85ohm impedance, fast slew rate, 100MHz for PCIe. V <sub>DDO</sub> = any valid supply.	13	17	
I <sub>DDO_LVDS</sub>	V <sub>DDO</sub> Supply Current per output pair, LVDS mode [3][4]	V <sub>DDO</sub> = any valid supply.	8	17	mA
I <sub>DD_IOD</sub>	V <sub>DDO</sub> Divider Supply Current	Portion of VDDO used by IOD	25	28	mA
I <sub>DD_FOD</sub>	V <sub>DDO</sub> Divider Supply Current	Portion of VDDO used by FOD	38	51	mA
I <sub>DD_PD</sub>	Total Power Down Current	Power Down Mode Enabled, VDDs = 1.8V	13	16	mA
		Power Down Mode Enabled, VDDs = 2.5V	15	23	
		Power Down Mode Enabled, VDDs = 3.3V	19	38	

1. Current consumption figures represent a worst-case consumption with all functions associated with the particular voltage supply enabled and all outputs running at maximum speed, unless otherwise noted. This information is provided to allow for design of appropriate power supply circuits that will support all possible register-based configurations for the device. To determine actual consumption for the user's device configuration, see [Power Considerations](#). Outputs are not terminated. Values apply to all voltage levels unless noted.
2. Voltage of the input signal must be appropriate for the V<sub>DDR</sub> voltage supply level when using a DC-coupled connection. For example, when supplying an LVDS input signal that is referenced to a 2.5V supply at its source, the V<sub>DDR</sub> supply must also be 2.5V nominal voltage. When using a 3.3V CMOS input signal, V<sub>DDR</sub> must be 3.3V
3. There are two possible input clock pairs. If both are used, the current for each type must be added together. If the external clock(s) is/are AC-coupled, the internal DC-bias must be enabled and also added to the total I<sub>DDR</sub> current.
4. LVPECL and CML input clocks are not supported when V<sub>DDR</sub> = 1.8V.
5. I<sub>DDO\_x</sub> denotes the current consumed by each output driver and does not include output divider current. These values are measured at maximum output frequency, unless otherwise stated (200MHz for LVCMOS outputs and 650MHz for differential outputs).
6. Please refer to the Output Driver and Output Divider V<sub>DDO</sub> Pin Assignments Table to determine the allocation of I<sub>DDO\_IOD</sub>, I<sub>DDO\_FOD</sub> and I<sub>DDO\_x</sub> to each V<sub>DDO</sub> pin.

Table 35. I<sup>2</sup>C/SMBus Bus DC Electrical Characteristics [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V <sub>IH</sub>	High-level input voltage for SCL_SCLK and SDA_nCS		0.7 V <sub>DDD</sub>	-	-	V
V <sub>IL</sub>	Low-level input voltage for SCL_SCLK and SDA_nCS		-	-	0.3 V <sub>DDD</sub>	V
V <sub>HYS</sub>	Hysteresis of Schmitt trigger inputs		0.05 V <sub>DDD</sub>	-	-	V
V <sub>OL</sub>	Low-level output voltage for SCL_SCLK and SDA_nCS	I <sub>OL</sub> = 4mA	-	-	0.4	V
I <sub>IN</sub>	Input leakage current per pin		-10	-	10	μA
C <sub>B</sub>	Capacitive Load for Each Bus Line		-	-	400	pF

1. V<sub>OH</sub> is governed by the V<sub>PUP</sub>, the voltage rail to which the pull up resistors are connected.

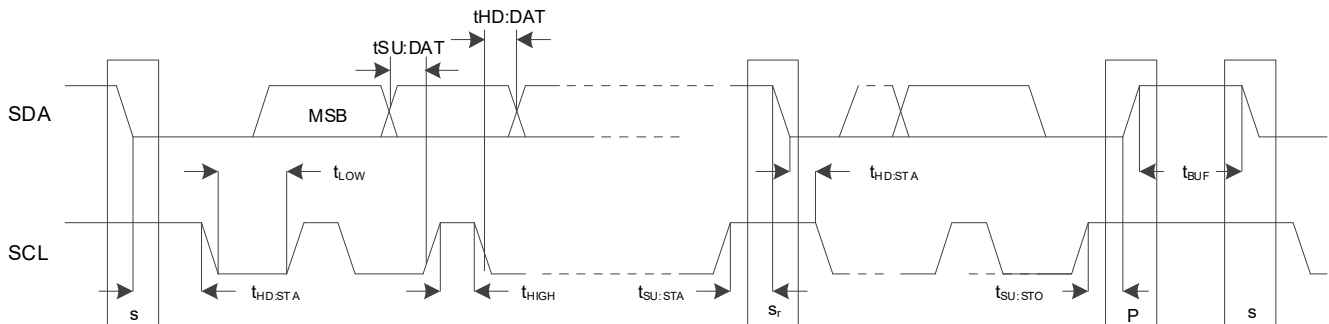


Figure 2. I<sup>2</sup>C/SMBus Slave Timing Diagram

Table 36. I<sup>2</sup>C/SMBus Bus AC Electrical Characteristics

Symbol	Parameter	Conditions	100kHz Class Minimum	100kHz Class Maximum	400kHz Class Minimum	400kHz Class Maximum	Unit
f <sub>SMB</sub>	SMBus Operating Frequency [1]	-	10	100	10	400	kHz
t <sub>BUF</sub>	Bus free time between STOP and START Condition	-	4.7	-	1.3	-	μs
t <sub>HD:STA</sub>	Hold time after (REPEATED) START Condition [2]	-	4	-	0.6	-	
t <sub>SU:STA</sub>	REPEATED START Condition setup time	-	4.7	-	0.6	-	
t <sub>SU:STO</sub>	STOP Condition setup time	-	4	-	0.6	-	
t <sub>HD:DAT</sub>	Data hold time [3]	-	300	-	300	-	ns
t <sub>SU:DAT</sub>	Data setup time	-	250	-	100	-	
t <sub>TIMEOUT</sub>	Detect SCL_SCLK low timeout [4]	-	25	35	25	35	ms
t <sub>TIMEOUT</sub>	Detect SDA_nCS low timeout [5]	-	25	35	25	35	
t <sub>LOW</sub>	Clock low period	-	4.7	-	1.3	-	μs
t <sub>HIGH</sub>	Clock high period [6]	-	4	50	0.6	50	

Table 36. I<sup>2</sup>C/SMBus Bus AC Electrical Characteristics (Cont.)

Symbol	Parameter	Conditions	100kHz Class Minimum	100kHz Class Maximum	400kHz Class Minimum	400kHz Class Maximum	Unit
t <sub>LOW:SEXT</sub>	Cumulative clock low extend time (slave device) [7]	-	N/A, the RC210xxA do not extend the clock low.				ms
t <sub>LOW:MEXT</sub>	Cumulative clock low extend time (master device) [8]	-	N/A, the RC210xxA are not bus masters.				
t <sub>F</sub>	Clock/Data Fall Time [9]	-	-	120	-	120	ns
t <sub>R</sub>	Clock/Data Rise Time [9]	-	-	120	-	120	
t <sub>SPIKE</sub>	Noise spike suppression time [10]	-	-	N/A	-	50	

1. A master shall not drive the clock at a frequency below the minimum  $f_{SMB}$ . Further, the operating clock frequency shall not be reduced below the minimum value of  $f_{SMB}$  due to periodic clock extending by slave devices as defined in Section 5.3.3 of the *SMBus 2.0 Specification*. This limit does not apply to the bus idle condition, and this limit is independent from the  $t_{LOW:SEXT}$  and  $t_{LOW:MEXT}$  limits. For example, if the SMBCLK is high for  $t_{HIGH:MAX}$ , the clock must not be periodically stretched longer than  $1/f_{SMB:MIN} - t_{HIGH:MAX}$ . This requirement does not pertain to a device that extends the SMBCLK low for data processing of a received byte, data buffering and so forth for longer than 100µs in a non-periodic way.
2. A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the  $V_{IH:MIN}$  of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
3. Slave devices may have caused other slave devices to hold SDA low. The maximum time that a device can hold SMBDAT low after the master raises SMBCLK after the last bit of a transaction. A slave device may detect how long SDA is held low and release SDA after the time out period.
4. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of  $t_{TIMEOUT:MIN}$ . After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than  $t_{TIMEOUT:MAX}$ . Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for  $t_{TIMEOUT:MAX}$  or longer.
5. The device has the option of detecting a timeout if the SDA\_nCS pin is also low for this time.
6.  $t_{HIGH:MAX}$  provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than  $t_{HIGH:MAX}$ .
7.  $t_{HIGH:MAX}$  provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than  $t_{HIGH:MAX}$ .
8.  $t_{LOW:SEXT}$  is the cumulative time a given slave device is allowed to extend the clock cycles in one message from the initial START to the STOP. It is possible that another slave device or the master will also extend the clock causing the combined clock low extend time to be greater than  $t_{LOW:SEXT}$ . Therefore, this parameter is measured with the slave device as the sole target of a full-speed master.
9. The rise and fall time measurement limits are defined as follows:  
 Rise Time Limits: ( $V_{IL:MAX} - 0.15V$ ) to ( $V_{IH:MIN} + 0.15V$ )  
 Fall Time Limits: ( $V_{IH:MIN} + 0.15V$ ) to ( $V_{IL:MAX} - 0.15V$ )
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

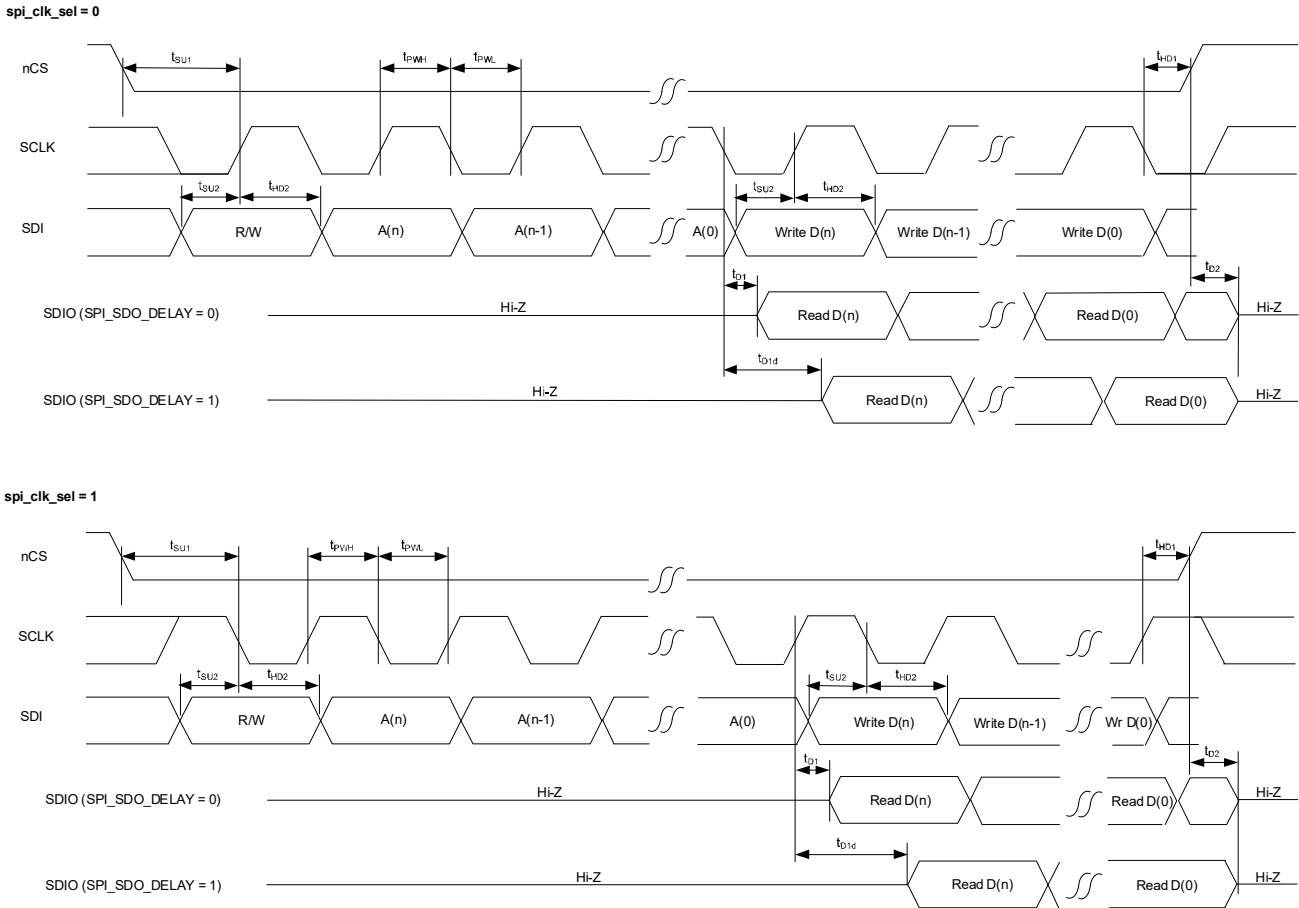


Figure 3. SPI Bus Timing

Table 37. SPI Slave Interface Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$f_{OP}$	Operating frequency	-	0.1	-	20	MHz
$t_{PWH}$	SCLK Pulse Width High	-	-	25	-	ns
$t_{PWL}$	SCLK Pulse Width Low	-	-	25	-	
$t_{SU1}$	nCS Setup Time to SCLK rising or falling edge	-	-	7	-	ns
$t_{HD1}$	nCS Hold Time from SCLK rising or falling edge	-	-	10	-	ns
$t_{SU2}$	SDIO Setup Time to SCLK rising or falling edge	-	-	4	-	ns
$t_{HD2}$	SDIO Hold Time from SCLK rising or falling edge	-	-	1	-	ns
$t_{D1}$	Read Data Valid Time from SCLK rising or falling edge with no data delay added	-	-	6	-	ns
$t_{D1d}$	Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing	[1]	-	6 + half SCLK period	-	ns
$t_{D2}$	SDIO Read Data Hi-Z Time from CS High	[2]	-	10	-	ns

1. Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.
2. This is the time until the device releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

Table 38. Power Supply Noise Rejection

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
PSNR	Power Supply Noise Rejection [1][2][3][4] 1.8V operation	$f_{\text{NOISE}} \leq 1\text{MHz}$ , VDDO[0:6] [5]	-146	-112	-	dBc
		$f_{\text{NOISE}} \leq 1\text{MHz}$	-76	-69	-	
		$f_{\text{NOISE}} \leq 100\text{kHz}$	-138	-135	-	
		$f_{\text{NOISE}} \leq 100\text{kHz}$	-97	-85	-	
		$100\text{kHz} \leq f_{\text{NOISE}} \leq 500\text{kHz}$	-140	-139	-	
		$100\text{kHz} \leq f_{\text{NOISE}} \leq 500\text{kHz}$	-138	-105	-	
		$500\text{kHz} \leq f_{\text{NOISE}} \leq 1\text{MHz}$	-144	-143	-	
		$500\text{kHz} \leq f_{\text{NOISE}} \leq 1\text{MHz}$	-93	-90	-	
PSNR	Power Supply Noise Rejection [1][3][4][6] 2.5V or 3.3V operation	$f_{\text{NOISE}} \leq 1\text{MHz}$ , VDDO[0:6] [5]	-146	-112	-	dBc
		$f_{\text{NOISE}} \leq 1\text{MHz}$	-76	-69	-	
		$f_{\text{NOISE}} \leq 100\text{kHz}$	-138	-135	-	
		$f_{\text{NOISE}} \leq 100\text{kHz}$	-94	-85	-	
		$100\text{kHz} \leq f_{\text{NOISE}} \leq 500\text{kHz}$	-140	-139	-	
		$100\text{kHz} \leq f_{\text{NOISE}} \leq 500\text{kHz}$	-138	-105	-	
		$500\text{kHz} \leq f_{\text{NOISE}} \leq 1\text{MHz}$	-144	-143	-	
		$500\text{kHz} \leq f_{\text{NOISE}} \leq 1\text{MHz}$	-93	-90	-	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. VDDX = VDDR = VDDR2 = VDDA = VDD[0:6] = 1.8V ±5%, VSS = 0V, TA = -40°C to 85°C.
3. 50mV peak-to-peak sine wave applied injected on indicated power supply pin(s).
4. Noise spur amplitude measured relative to 156.25MHz carrier frequency.
5. Excluding VDDOx of the output being measured.
6. VDDX = VDDR = VDDR2 = VDDA = VDD[0:6] = 2.5V or 3.3V ±5%, VSS = 0V, TA = -40°C to 85°C.



## 3. Functional Description

The RC210xxA is a small-form factor, fully integrated, low-power, high performance frequency synthesizer providing excellent phase jitter on reference clocks for PCI express and Ethernet, while covering a wide range of output frequencies up to 650MHz. It can simultaneously provide low phase jitter non-spreading clocks for Ethernet and storage applications, while providing spread-spectrum PCIe Gen6 clocks.

The following sections provide an overview of the RC210xxA.

### 3.1 Power-Up, Configuration, and Serial Interfaces

The RC210xxA can be powered up and configured in three ways:

1. From 1 of 27 internal non-volatile memory using OTP user configurations (UserCfgs)
2. From its slave serial interface
3. From an external I2C EEPROM

The RC210xxA supports three slave serial interfaces (I2C, SPI, and SMBUS), and one serial master interface (I2C). These interfaces share the same pins, so only one is available at a time.

### 3.2 Input Clocks

The RC210xxA supports one crystal/reference input and up to two differential or four single-ended clock inputs.

#### 3.2.1 Crystal/Reference Input

The crystal input supports crystal frequencies of 8MHz to 80MHz. It has programmable internal load capacitors to support crystals with CL = 6pF to 12pF. Internal crystal variants of RC210xxA support a trim value in OTP that can be set during ATE to compensate for initial frequency offset of the internal crystal.

The crystal input may be over-driven with differential or single-ended inputs with proper external terminations. It also supports being over-driven with a clipped sine-wave TCXO with a 0.8V<sub>PP</sub> signal.

The supported frequency range is same as reference clock inputs: 1kHz to 650MHz in differential mode, and 1kHz to 200MHz in single-ended mode.

An available LOS monitor detects the loss of signal on crystal input.

#### 3.2.2 Clock Inputs

There are two differential clock inputs that support LVDS, HCSL, or single-ended CMOS logic levels without external terminations. LVPECL or CML clock inputs may be supported with external terminations and/or AC coupling. Internal terminations are available for both HCSL and LVDS logic levels. Additionally, HCSL input terminations support both 100ohm and 85ohm operating environments.

If set to single-ended type, the differential inputs turn into two single-ended inputs. CLKIN0 drives clkin0 internally, CLKIN0b drives clkin1 internally, CLKIN1 drives clkin2 internally, and CLKIN1b drives clkin3 internally. If set to differential type, CLKIN0/CLKIN0b pair drives clkin0 while CLKIN1/CLKIN1b pair drives clkin2. Internal biasing is available for AC-coupled applications. The two clock inputs can be left floating when unused. An available LOS monitor detects the loss of signal on crystal input.

### 3.3 Clock Input Monitor

The APLL input is monitored for Loss of Signal (LOS).

The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least 8 times that of the measuring clock period.

## 3.4 APLL

The APLL is fractional LC-VCO based PLL with an operating range from 9.5GHz to 10.7GHz. Any of the available input clocks can be selected to drive the APLL, and the input clock can be frequency doubled for increased performance. The APLL is temperature compensated for the utmost frequency stability. For synchronous, deterministic requirements, the APLL also supports ZDB mode where CLKIN0 is used for the feedback input.

### 3.4.1 APLL Lock Detector

The APLL lock detector indicates whether the APLL is locked to a functioning crystal or reference input by monitoring the phase errors. Lock status can be sent on to a GPIO pin or in the register map.

## 3.5 Output Dividers

The RC210xxA provides four integer and three fractional output dividers.

### 3.5.1 Integer Output Dividers

All four Integer Output Dividers (IOD) are identical. They use a 25-bit divider to provide output frequencies of 1kHz to 650MHz from the VCO clock. Changing IOD values results in an immediate change to the new frequency. Glitch-less squelch and release of the IOD clock is supported. When enabled, this mimics a gapped clock behavior when an IOD frequency is changed.

### 3.5.2 Fractional Output Dividers

There are three Fractional Output Dividers (FOD). Each FOD can divide down the VCO clock to provide frequencies from 1kHz to 650MHz. Each FOD is implemented in two stages. The first stage is an 8-bit fractional divider with Digital Control Delay (DCD) correction. The DCD FOD allows a divide down of the VCO clock to 30MHz to 650MHz. A 17-bit second-stage integer divider with minimum divide ratio of 4 and a maximum ratio of  $2^{(2^{17}-1)}$  allows output frequencies lower than 30MHz. For output frequencies above 30MHz, this second-stage divider may be bypassed.

#### 3.5.2.1 Spread-Spectrum Clocking

FOD0 and FOD1 support Spread-Spectrum Clocking (SSC).

When SSC is enabled, the spread spectrum engine modulates the FOD divider ratio with a triangular modulation pattern. The modulation can be programmed for either down-spread or center-spread. The SSC modulation frequency can be programmed to a value between 30kHz to 63kHz. The SSC amplitude can be programmed in 0.05% steps to -1.5% for down spread, or  $\pm 1.5\%$  for center spread. When turning off SSC, the current modulation cycle completes, returning the output to the non-spreading frequency before the SSC stops.

#### 3.5.2.2 Sync and Phase Adjustment

Each FOD can adjust its output clock phase with a step size of 1/4 VCO period up to about  $\pm 20$ ns. The adjustment can be of either positive or negative directions.

IOD phase adjustment is same as FOD phase adjustment but with a step size of one VCO period.

## 3.6 Clock Outputs

The RC210xxA supports up to 12 differential or 24 single-ended clock outputs or any combination of differential and single-ended clock outputs. Every differential clock output can be programmed as two single-ended clock outputs.

### 3.6.1 Output Types

The RC210xxA outputs drive HCSL inputs (such as those used in PCIe applications) directly. They use Low-Power HCSL (LP-HCSL) driver technology to eliminate external termination resistors. The LP-HCSL outputs can

be set to 85ohm or 100ohm differential output impedance. The LP-HCSL outputs have selectable output swing and slew rate settings.

The RC210xxA outputs may also be set to LVDS. LVDS outputs require only a 100ohm resistor between the true and complement inputs of the receiver clock input. LVDS outputs have selectable amplitude. Both LVDS and LP-HCSL outputs provide LVPECL and CML-compatible output swing levels by using external AC coupling.

If set to single-ended mode, the output pair can drive either pin or both pins. If both pins are enabled, they can be in phase, or inverted phase. The single-ended outputs support CMOS swings of 1.8V, 2.5V, or 3.3V as determined by their VDDO voltage.

### 3.6.2 Output Banks

The RC210xxA maps the internal and external frequency sources to output banks, that can be programmed in register `output_bank_src`, according to [Table 39](#). There are up to 12 clock outputs arranged in seven output banks. Each bank sits on its own VDDO (each VDDO also supplies an IOD or FOD according to [Table 40](#)).

**Table 39. Output Bank Source Mapping**

output_bank_src	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6
	OUT0	OUT1	OUT[2:3]	OUT[4:7]	OUT[8:9]	OUT10	OUT11
0x0	IOD0		N/A		CLKIN1		
0x1	IOD1			N/A		XIN_REFIN	N/A
0x2	N/A				IOD2		
0x3	N/A					IOD3	
0x4	FOD0				N/A		
0x5	FOD1						
0x6	N/A			FOD2			
0x7	N/A				CLKIN0		

**Table 40. VDD Pin Assignments for Outputs, Integer Output Dividers, and Fractional Output Dividers**

VDDO0	VDDO1	VDDO2	VDDO3	VDDO4	VDDO5	VDDO6	VDDX	VDDR	VDDD	VDDA
IOD0, OUT0	IOD1, OUT1	FOD0, OUT[2:3]	FOD1, OUT[4:7]	FOD2, OUT[8:9]	IOD2, OUT10	IOD3, OUT11	XO, XIN_REFIN, XOUT_REFI Nb	GPI[3:0]	SCL_SCLK, SDA_nCS, GPIO[4:0]	PLL

## 4. Application Information

### 4.1 Recommendations for Unused Input and Output Pins

#### 4.1.1 CLKIN/CLKINb [1:0] Inputs

For applications that do not require the use of reference clock inputs, both CLKIN and CLKINb should be left floating. If the CLKIN/CLKINb inputs are connected but not used by the device, Renesas recommends that CLKIN and CLKINb be connected to static signals, not active signals.

#### 4.1.2 LVCMOS Control Pins

LVCMOS control pins have selectable internal pull-ups and/or pull-downs. Additional resistance is not required but may be added for additional protection. A 10kΩ resistor can be used.

#### 4.1.3 LVCMOS Outputs

Any LVCMOS output may be left floating if unused. There should be no trace attached. The mode of the output buffer should be set to high impedance state to avoid unnecessary noise generation.

#### 4.1.4 Differential Outputs

All unused differential outputs may be left floating. There should be no trace attached. Both sides of the differential output pair should be treated the same, either left floating or terminated.

### 4.2 CLKIN/CLKINb Clock Input Interface

The RC210xxA provides a programmable input buffer for reference clock inputs, as shown in Figure 4. This programmable buffer supports most standard signaling protocols with no need for external termination components at the receiver end of the transmission line.

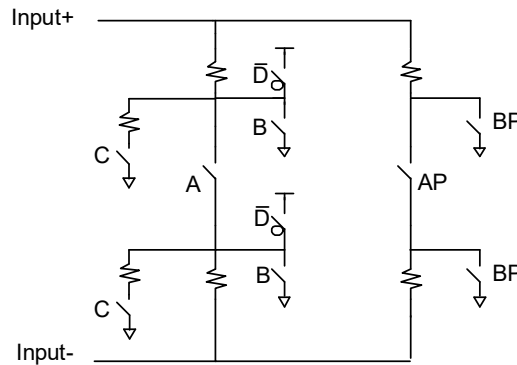


Figure 4. Programmable Input Buffer Logical Diagram

By making appropriate register selections, the switches labeled in Figure 4 can be closed as shown in Table 41 to support the indicated protocols. With the switches closed as indicated, the input buffer will operate as shown in Figure 5 for the various input reference signal protocols. Note that HCSL is used in both 100ohm and 85ohm transmission line environments and this input buffer supports both with no external terminations required.

Table 41. Input Buffer Programming Options for Specific Signaling Protocols

Input Signaling Protocol	Switches Closed	V <sub>DDR</sub> Voltage Required
2.5V LVPECL	A, C	2.5V
3.3V LVPECL	A, C	3.3V
LVDS (85 ohms)	A, AP	1.8V / 2.5V / 3.3V
LVDS (100 ohms)	A	1.8V / 2.5V / 3.3V
1.8V LVCMOS	-	1.8V
2.5V LVCMOS	-	2.5V
3.3V LVCMOS	-	3.3V
CML	D	3.3V
HCSL (42.5 ohms)	B, BP	1.8V / 2.5V / 3.3V
HCSL(42 ohms)	B	1.8V / 2.5V / 3.3V
Externally AC-coupled <sup>[1]</sup>	-	1.8V / 2.5V / 3.3V

1. In this mode of operation, AC-coupling capacitors must be used to isolate the voltage level of the transmitter from the receiver. The signal must be properly terminated on the transmitter side of the AC-coupling capacitors. Bias terminations are needed between the AC-coupling capacitors and the RC210xxA.

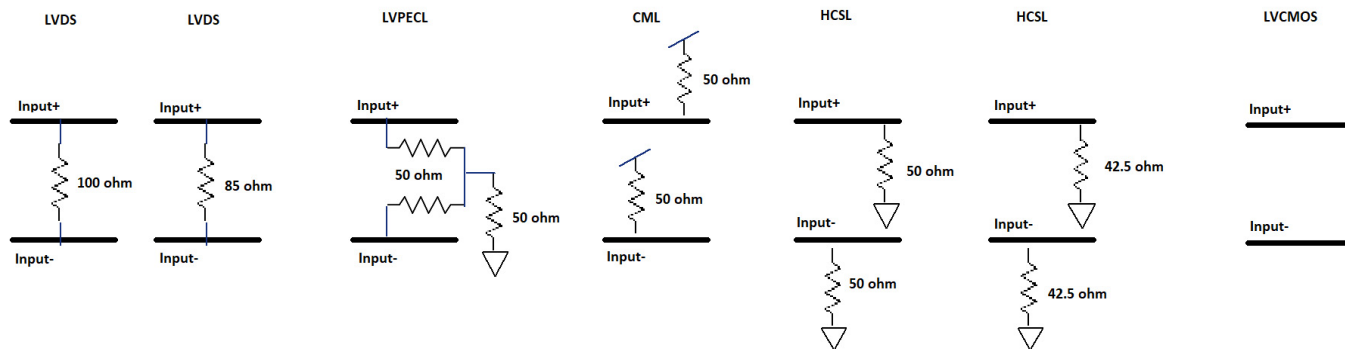


Figure 5. Input Buffer Behavior by Protocol

### 4.3 Overdriving the XTAL Interface

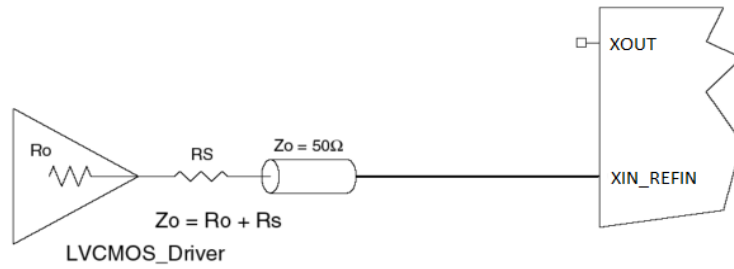
#### 4.3.1 Input Buffer Mode Selected

The RC210xxA has two bits to disconnect the internal XO and enable input buffer mode on the XIN\_REFIN pin. First, setting `sel_ib_xo = 0`, disconnects the internal XO. Next, setting `xo_ib_cmos_sel = 1` enables the LVCMOS input clock path. Setting these two bits as indicated removes any AC-coupling or input voltage requirements for overdriving the XTAL interface. Note that the maximum input swing is still governed by the VDDX supply rail.

#### 4.3.2 Input Buffer Mode Not Selected

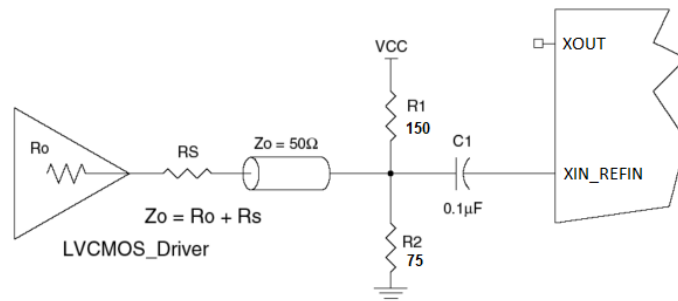
If the two bits mentioned above are not set as indicated, then there is a limitation of 1.2V on the XIN\_REFIN pin.

The XIN\_REFIN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V, and the slew rate must be  $\geq 0.2V/ns$ . For 1.2V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 6. For LVCMOS drivers with > 1.2V swing, the amplitude must be reduced from full swing to at least 1.2V in order to prevent signal interference with the power rail. The sum of the driver output impedance and  $R_s$  must equal the transmission line impedance to prevent overshoot and undershoot.



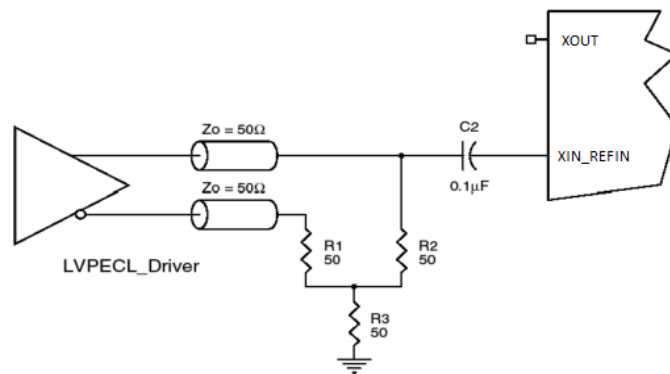
**Figure 6. 1.2V LVCMOS Driver to XTAL Input Interface**

Figure 7 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equal the transmission line impedance. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. We also need to scale the 3.3V LVCMOS swing to 1.2V (~1/3 of the swing). This yields  $R_1 = 2 \times R_2$  while  $R_1 \parallel R_2 = 50\Omega$ . Solving for a 50Ω ohm system gives  $R_1 = 150\Omega$  and  $R_2 = 75\Omega$ . The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Different scaling factors are required for 2.5V and 1.8V LVCMOS drivers.



**Figure 7. LVCMOS Driver to XTAL Input Interface**

Figure 8 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN\_REFIN input. Renesas recommends that all components in the schematics be placed in the layout. Though some components may not be used by the application, they can be used for debugging purposes.



**Figure 8. LVPECL Driver to XTAL Input Interface**

## 4.4 Differential Output Terminations

### 4.4.1 Direct-Coupled LP-HCSL Termination

For the LP-HCSL differential protocol, the following termination scheme is recommended (see Figure 9). The RC210xxA supports internal source terminations (see Figure 9) for 85 ohm or 100 ohm differential transmission lines. No external components are needed.

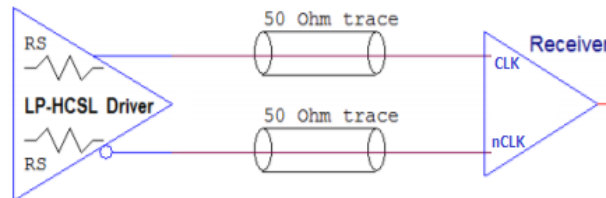


Figure 9. Standard HCSL Termination

### 4.4.2 Direct-Coupled LVDS Termination

For LVDS differential protocol, the following termination scheme is recommended (see Figure 10). The recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of the transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver in a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, any external components should be surface-mounted and must be placed as close to the receiver as possible.

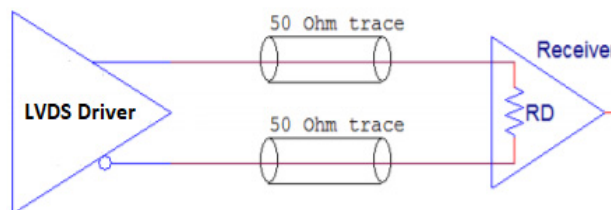


Figure 10. Standard LVDS Termination

### 4.4.3 AC-Coupled Differential Terminations for Other Protocols

Alternate differential protocols including LVPECL, CML and SSTL can be supported with AC-coupled LP-HCSL outputs. Figure 11 shows a typical AC-coupled termination scheme for a  $100\Omega$  differential transmission-line environment. The RC210xxA supports a differential swing of 1.6V or 1.8V in LP-HCSL mode.

No terminations are needed between the RC210xxA and the AC-coupling capacitors. The resistors on the receiver side of the AC-coupling capacitors provide an appropriate voltage bias for the particular receiver. Finally, a  $100\Omega$  resistor across the differential pair (located near the receiver) attenuates reflections that may corrupt the clock signal integrity.

Often, receivers used with a high-performance device like the RC210xxA are equipped with internal terminations, voltage biasing, and even AC-coupling. Please consult your particular the receiver specification to determine if any or all of the indicated external components in Figure 11 are needed.

Refer to *Driving LVPECL, LVDS, CML, and SSTL Logic with Renesas' "Universal" Low-Power HCSL Outputs* (AN-891) on the RC210xxA product page for additional information on both re-biasing and amplitude attenuation.

If a smaller differential swing is desired as a starting point, refer to "LVDS Termination" in *Quick Guide - Output Terminations* (AN-953) located on the RC210xxA product page.

Please contact Renesas for additional support, if necessary.

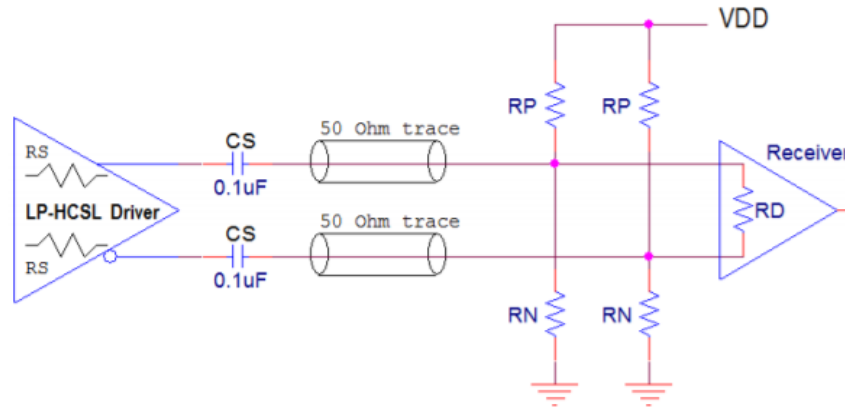


Figure 11. AC-Coupling Termination

## 4.5 Crystal Recommendations

For the latest vendor / frequency recommendations, please contact Renesas.

## 4.6 External I<sup>2</sup>C Serial EEPROM Recommendations

An external I<sup>2</sup>C EEPROM can be used to store configuration data, please contact Renesas for specific recommendations. A specific configuration code is required for the devices to access an external I<sup>2</sup>C serial EEPROM at power up. See the ordering information.

## 4.7 Power Considerations

The electrical characteristics tables provide current consumption values for various blocks and output configurations, and can be used to estimate total current consumption for a particular design. The Renesas IC Toolbox, available on the Renesas website, can also be used to estimate current consumption.

### 4.7.1 Power Sequencing Considerations

There are power sequencing considerations that must be followed to ensure robust operation of the RC210xxA. The basic rule is to have the output supply pins (VDDOs) reach 1.62V within 4mS of all other voltage supply pins (VDDA, VDDD, etc.) reaching 1.62V. Note that 1.62V is a constant specification, regardless of the power supply voltage connected to the pin (1.8V, 2.5V, or 3.3V). When the entire RC210xxA is powered from a single voltage, this requirement is easy to meet. For applications where multiple supply voltages are used, meeting this requirement can be more complex. The RC210xxA has a GPIO function called PWRGD/PWRDN# which can simplify power supply sequencing in multi-voltage environments.

There are two scenarios to consider. The first does not use the PWRGD/PWRDN# GPIO function (pin). The second uses the PWRGD/PWRDN# pin.

#### 4.7.1.1 Power Up Operation without PWRGD/PWRDN#

Figure 12 shows the power supply sequencing requirements for operation without the PWRGD/PWRDN# pin. The last VDDO to ramp must reach 1.62V within 4mS of the last of these voltages - VDDA, VDDX, VDDR, VDDD - to reach 1.62V.



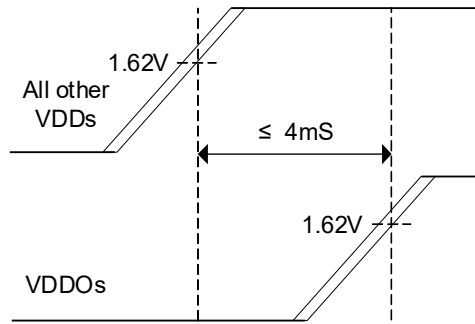


Figure 12. Power Supply Sequencing Recommendations – Power Up without PWRGD/PWRDN#

4.7.1.2 Power Up Using PWRGD/PWRDN# (GPIO4)

When GPIO4 is configured as PWRGD/PWRDN#, power supply sequencing requirements are relaxed.

Figure 13 shows use of the PWRGD\PWRDN# input to hold the entire RC210xxA in power-down until all power supply rails reach 1.62V. The PWRGD\PWRDN# pin must be held low for at least 200 $\mu$ S before the last VDD pin reaches 1.62V. It may be held longer. Using PWRGD/PWRDN# is recommended, since it isolates the RC210xxA from changes to power supply sequencing that may be caused by other devices in the system.

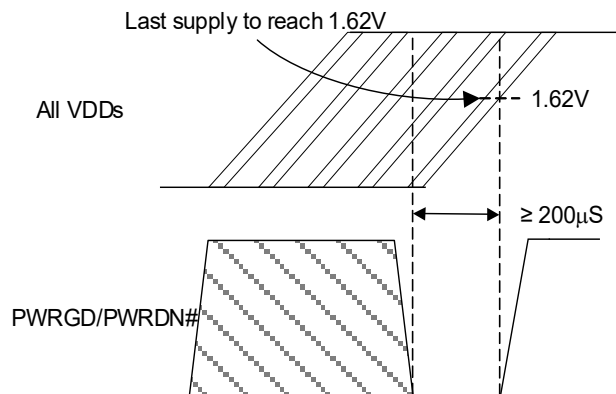


Figure 13. Power Supply Sequencing Recommendations – Power Up Using PWRGD/PWRDN#

## 5. Thermal Information

### 5.1 VFQFPN ePad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 14. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

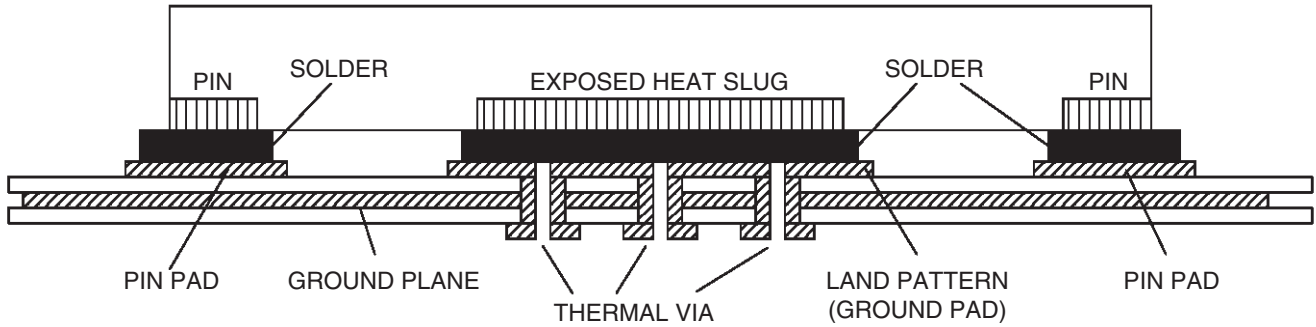


Figure 14. P.C. Assembly for Exposed Pad Thermal Release Path – Side View

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes.” The number of vias (i.e., “heat pipes”) are application specific and dependent on the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33 mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

### 5.2 Thermal Characteristics

Table 42. Thermal Characteristics (48-pin) [1]

Symbol	Parameter	Value	Unit
$\theta_{JC}$	Theta J <sub>C</sub> . Junction to Device Case Thermal Coefficient [2]	20.1	°C/W
$\theta_{JB}$	Theta J <sub>B</sub> . Junction to Board Thermal Coefficient [2]	1.9	
$\theta_{JA}$	Junction to Ambient Air Thermal Coefficient (still air)	25.8	
	Junction to Ambient Air Thermal Coefficient 1 m/s air flow	21.5	
	Junction to Ambient Air Thermal Coefficient 3 m/s air flow	18.8	
	Junction to Ambient Air Thermal Coefficient 5 m/s air flow	17.9	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	N/A

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 25 thermal vias.

Table 43. Thermal Characteristics (40-pin with External Crystal) [1]

Symbol	Parameter	Value	Unit
$\theta_{JC}$	Theta $J_C$ . Junction to Device Case Thermal Coefficient [2]	35.7	°C/W
$\theta_{JB}$	Theta $J_B$ . Junction to Board Thermal Coefficient [2]	1.9	
$\theta_{JA}$	Junction to Ambient Air Thermal Coefficient (still air)	28.9	
	Junction to Ambient Air Thermal Coefficient 1 m/s air flow	25.6	
	Junction to Ambient Air Thermal Coefficient 3 m/s air flow	23	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	N/A

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 16 thermal vias.

Table 44. Thermal Characteristics (40-pin with Internal Crystal) [1]

Symbol	Parameter	Value	Unit
$\theta_{JC}$	Theta $J_C$ . Junction to Device Case Thermal Coefficient [2]	35	°C/W
$\theta_{JB}$	Theta $J_B$ . Junction to Board Thermal Coefficient [2]	52.4	
$\theta_{JA}$	Junction to Ambient Air Thermal Coefficient (still air)	70.7	
	Junction to Ambient Air Thermal Coefficient 1 m/s air flow	65.9	
	Junction to Ambient Air Thermal Coefficient 3 m/s air flow	62.5	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	N/A

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 16 thermal vias.

Table 45. Thermal Characteristics (32-pin with Internal Crystal) [1]

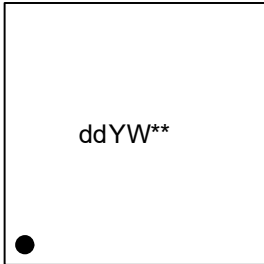
Symbol	Parameter	Value	Unit
$\theta_{JC}$	Theta $J_C$ . Junction to Device Case Thermal Coefficient [2]	61.2	°C/W
$\theta_{JB}$	Theta $J_B$ . Junction to Board Thermal Coefficient [2]	7.4	
$\theta_{JA}$	Junction to Ambient Air Thermal Coefficient (still air)	40.3	
	Junction to Ambient Air Thermal Coefficient 1 m/s air flow	37.4	
	Junction to Ambient Air Thermal Coefficient 3 m/s air flow	34.8	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	N/A

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 4 thermal vias.

## 6. Package Outline Drawings

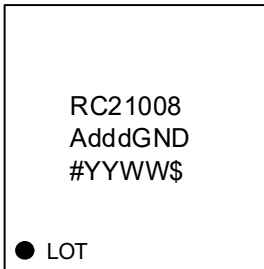
The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

## 7. Marking Diagrams



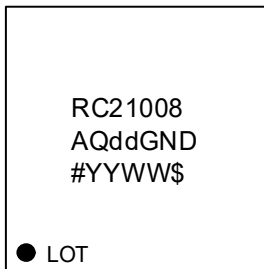
**RC21005AQdd**

- Line 1:
  - “dd” indicates preprogrammed device custom configuration dash code.
  - “YW” indicates the last digit of the year and work week the part was assembled.
  - “\*\*” indicates the lot sequence.



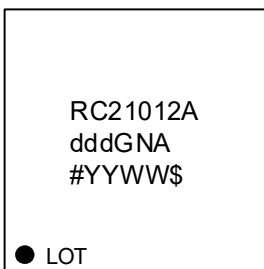
**RC21008Add**

- Lines 1 and 2: part number.
  - “ddd” indicates preprogrammed device custom configuration dash code.
- Line 3:
  - “#” indicates the stepping number.
  - “YYWW” indicates the last two digits of the year and work week the part was assembled.
  - “\$” indicates the mark code.



**RC21008AQdd**

- Lines 1 and 2: part number.
  - “dd” indicates preprogrammed device custom configuration dash code.
- Line 3:
  - “#” indicates the stepping number.
  - “YYWW” indicates the last two digits of the year and work week the part was assembled.
  - “\$” indicates the mark code.



**RC21012Add**

- Lines 1 and 2: part number.
  - “ddd” indicates preprogrammed device custom configuration dash code.
- Line 3:
  - “#” indicates the stepping number.
  - “YYWW” indicates the last two digits of the year and work week the part was assembled.
  - “\$” indicates the mark code.

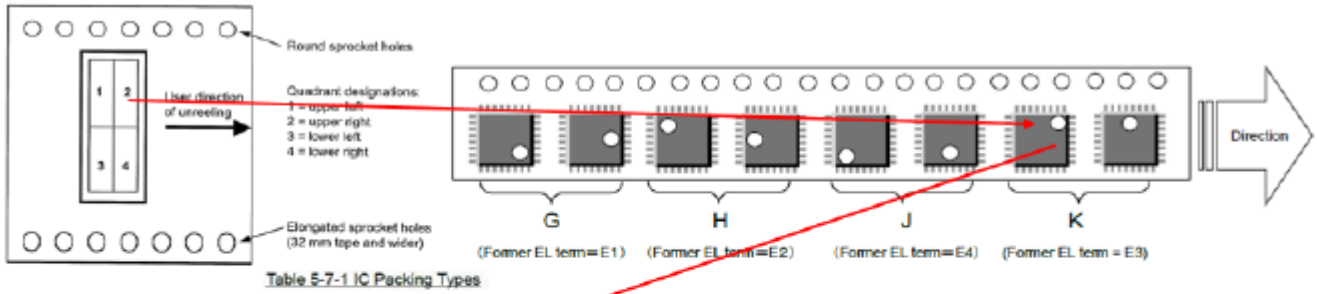


Figure 15. Pin 1 Orientation in Tape and Reel Packaging

## 8. Ordering Information

Part Number [1]	Description	Carrier Type	Pkg. Description	Temp. Range		
RC21005AQ00GL2#BB0	5-output un-programmed part with internal crystal. I2C address is 0x09.	Tray	4 × 4 × 1.2 mm, 32-LGA	-40° to +85°C		
RC21005AQ00GL2#KB0		Tape and Reel, Pin 1 Orientation: EIA-481-D				
RC21005AQ01GL2#BB0	5-output un-programmed part with internal crystal for use with external I2C EEPROM. I2C address is 0x09 after I2C EEPROM is loaded.	Tray				
RC21005AQ01GL2#KB0		Tape and Reel, Pin 1 Orientation: EIA-481-D				
RC21005AQddGL2#BB [2]	5-output pre-programmed part with internal crystal	Tray				
RC21005AQddGL2#KB0 [2]		Tape and Reel, Pin 1 Orientation: EIA-481-D				
RC21008AQ00GL2#BD0	8-output un-programmed part with internal crystal. I2C address is 0x09.	Tray			5 × 5 × 1.7 mm, 40-LGA	-40° to +85°C
RC21008AQ00GL2#KD0		Tape and Reel, Pin 1 Orientation: EIA-481-D				
RC21008AQ01GL2#BD0	8-output un-programmed part with internal crystal for use with external I2C EEPROM. I2C address is 0x09 after I2C EEPROM is loaded.	Tray				
RC21008AQ01GL2#KD0		Tape and Reel, Pin 1 Orientation: EIA-481-D				
RC21008AQddGL2#BD0 [2]	8-output pre-programmed part with internal crystal	Tray				
RC21008AQddGL2#KD0 [2]		Tape and Reel, Pin 1 Orientation: EIA-481-D				

Part Number [1]	Description	Carrier Type	Pkg. Description	Temp. Range
RC21008A000GND#BB0	8-output un-programmed part with external crystal. I2C address is 0x09.	Tray	5 × 5 × 0.9 mm, 40-VFQFPN	-40° to +85°C
RC21008A000GND#KB0		Tape and Reel, Pin 1 Orientation: EIA-481-D		
RC21008A001GND#BB0	Tray			
RC21008A001GND#KB0	Tape and Reel, Pin 1 Orientation: EIA-481-D			
RC21008AdddGND#BB0 [2]	8-output pre-programmed part with external crystal.	Tray	6 × 6 × 0.9 mm, 48-VFQFPN	-40° to +85°C
RC21008AdddGND#KB0 [2]		Tape and Reel, Pin 1 Orientation: EIA-481-D		
RC21012A000GNA#BB0	12-output un-programmed part with external crystal. I2C address is 0x09.	Tray		
RC21012A000GNA#KB0		Tape and Reel, Pin 1 Orientation: EIA-481-D		
RC21012AdddGNA#BB0 [2]	12-output pre-programmed part with external crystal	Tray		
RC21012AdddGNA#KB0 [2]		Tape and Reel, Pin 1 Orientation: EIA-481-D		

1. The “00”, “000”, “01”, and “001” dash codes support for any mix of 1.8V and 3.3V power supplies. For configurations that require 2.5V power supplies, please contact Renesas.
2. Replace “ddd” or “dd” with the pre-programmed configuration code provided by Renesas in response to a custom configuration request.

## 9. Revision History

Revision	Date	Description
1.03	Sep 19, 2022	<ul style="list-style-type: none"> <li>Updated the <a href="#">Marking Diagrams</a> and <a href="#">Ordering Information</a>, added 01 and 001 dash codes to indicate configurations that load from external I2C EEPROMs. Updated footnotes.</li> <li>Updated <a href="#">Power Sequencing Considerations</a></li> </ul>
1.02	Aug 31, 2022	<ul style="list-style-type: none"> <li>Completed minor updates to various <a href="#">Electrical Characteristics</a> values</li> </ul>
1.01	Aug 9, 2022	<ul style="list-style-type: none"> <li>Corrected a typo in <a href="#">Pin Assignments – RCxx012A</a></li> <li>Completed minor updates to various <a href="#">Electrical Characteristics</a> values</li> <li>Completed other minor changes</li> </ul>
1.00	Jul 22, 2022	Initial release.