Rockwell

RC2424DP/DS 2400 bps Full-Duplex Modem Data Pump Device Set

1

INTRODUCTION

The Rockwell RC2424DP/DS is a 2400 bps, full-duplex, OEM, data pump modem device set. The RC2424DP/DS operates over the public switched telephone network (PSTN), as well as on point-to-point leased lines.

The set consists of two CMOS VLSI components—a digital signal processor (DSP) device and an integrated analog (IA) device. The DSP is available in a 64-pin quad in-line package (QUIP) or a 68-pin plastic leaded chip carrier (PLCC) package. The IA device is available in a 40-pin dual in-line package (DIP) or a 44-pin PLCC package.

The RC2424DP/DS modem meets the requirements specified in CCITT V.22 bis, V.22 A/B, and V.21, as well as Bell 212A and Bell 103.

Full compatibility with V.23 is realized with the addition of an external FSK demodulator. The V.23 capability allows asynchronous operation at 1200 bps with backward channel operation to 75 bps. RC2424DP/DS DSP firmware, in conjunction with a fully compatible hardware interface, directly configures and controls the V.23 FSK demodulator device. Moreover, the centralized transmitter function in the RC2424DP/DS allows "clean" soft turn-offs in V.23 mode.

In addition, the SDLC/HDLC support eliminates the cost of an external serial input/output (SIO) device in products incorporating error correction protocols.

FEATURES

- CMOS DSP and IA devices
- 2-wire full-duplex operation
- Compatible configurations:
  - –CCITT V.22 bis, V.22A/B
  - –CCITT V.21 and V.23
  - –Bell 212A and 103
- Receive dynamic range: –9 dBm to –43 dBm
- Maximum transmit level: 0.0 dBm ±1.0 dB, programmable in 1 dB steps
- Multi-modem detection support
  - –Programmable tone detect bandpass filters
  - –Zero-crossing detector
- V.22 bis fallback/fall-forward – 2400/1200 bps
- Synchronous serial data
  - –2400, 1200, 600 bps ± 0.01% (PSK modulation)
    Internal/external/slave clock selection
- Parallel data both synchronous and asynchronous
  - –Synchronous:
    Normal sync: 8-bit data for transmit and receive
  - –SDLC/HDLC support:
    Transmitter: Flag generation, 0 bit stuffing, CCITT CRC generation
    Receiver: Flag detection, 0 bit un-stuffing, CCITT CRC checking
  - –Asynchronous:
    5, 6, 7, or 8 data bits per character
    Odd/even parity generation/checking (or 9th data bit)
    2400, 1200, 600 bps +1% or (2.3%), –2.5% (PSK modulation)
    75, 300, 600, 1200 bps (FSK modulation)
- Programmable ring detect
  - –Min and max frequency range
- Programmable dialer
  - –Make/break times for pulse dialling
  - –DTMF on time for touch-tone dialling
  - –Interdigit times for both pulse and tone dialling
  - –DTMF Level: 0.0 dBm ± 1.0 dB (high tone level is 2.0 dB ± 0.5 dB above low tone level)

- Diagnostics
  - –Read/write RAM
  - –Serial eye pattern output
  - –EQM value in RAM
- Host bus interface memory for configuration, control, and parallel data; compatible with either 8086 or 6502 microprocessor bus
- RS-232C (TTL compatible) interface for RTS control and serial data
- Adaptive and fixed compromise equalization
- Test Configurations:
  - –Local analog loopback
  - –Local digital loopback
  - –Remote digital loopback
- Answer and originate handshake
- Leased line operation
- Power requirements:
  - –± 5 Vdc ± 5%
  - –500 mW typical

R2424 COMPATIBILITY

A high performance modem engine, the RC2424DP/DS is the functional and performance equivalent of Rockwell's R2424DS modem with the following enhancements:

- –2-device implementation in CMOS
- –V.21 and V.23 interface
- –Asynchronous/synchronous parallel data transfer over the microprocessor bus interface
- –Extended 2.3% overspeed in asynchronous, DPSK/QAM modes
- –SDLC/HDLC framing in parallel data mode
- –Additional configuration and control capabilities

These options and enhancements, combined with a user accessible, dual port interface memory (RAM) in the DSP, offer maximum flexibility in customizing the RC2424DP/DS to meet a wide variety of functional requirements.

The RC2424DP/DS device set, with the addition of a few external filter components, interfaces easily to a data access arrangement (DAA). The RC2424DP/DS general interface is illustrated in Figure 1.

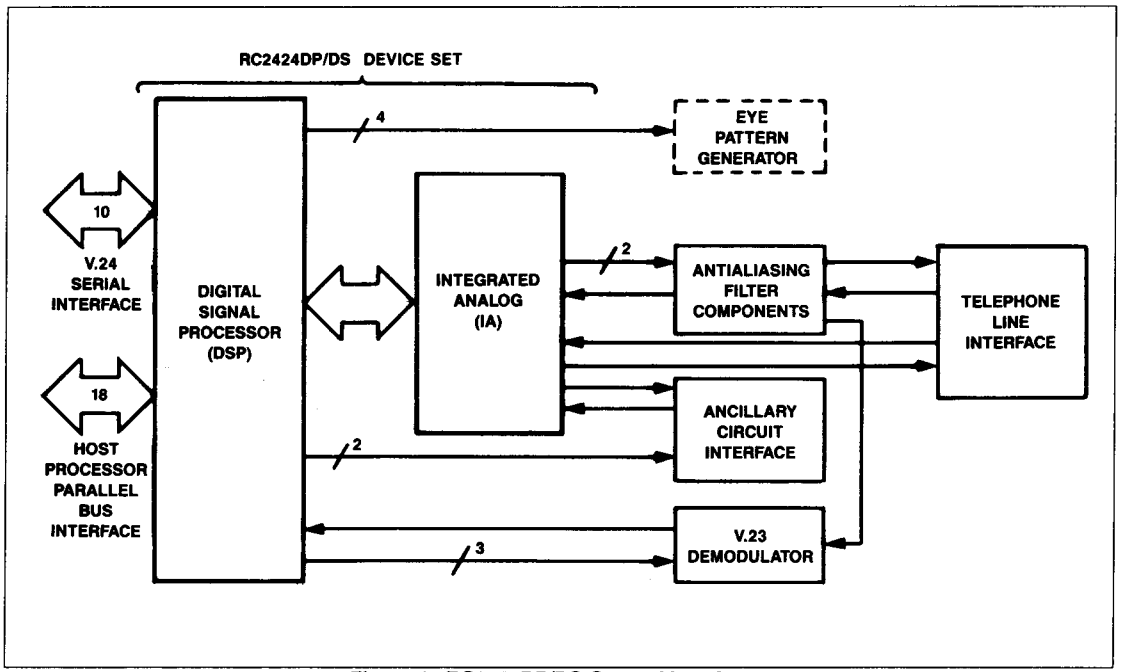


Figure 1. RC2424DP/DS General Interfaces

TECHNICAL SPECIFICATIONS

CONFIGURATIONS, SIGNALING RATES, AND DATA RATES

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1. The modem configuration is established by the CONF bits.

Note: Bit names refer to control bits in DSP Interface Memory which are set or reset by the host processor (see Software Interface Section, Figure 7 and Table 11).

TONE GENERATION

Answer Tone: A CCITT (2100 ± 15 Hz) or Bell (2225 ± 10 Hz) answer tone is generated depending on the selected configuration.

Guard Tone: A guard tone of 1800 ± 20 Hz (GTS bit = 0) or 550 ± 20 Hz (GTS bit = 1) can be generated (enabled by the GTE bit). The level of transmitted power is 6 ± 1 dB or 3 ± 1 dB below the level of the data power in the main channel for the 1800 Hz or 550 Hz guard tone, respectively. The total power transmitted to the line is the same whether or not a guard tone is enabled. When a guard tone is generated, the main channel transmit path gain is reduced by 0.97 dB or 1.76 dB for the 1800 Hz or 550 Hz guard tone, respectively.

Guard tone on/off must be controlled by the host depending on the state of the handshake sequence, i.e., the host should enable guard tone when DSR is turned on.

DTMF Tones: When Dial/Call Progress configuration is selected (CONF bits = 81) and the DTMF bit is set to a 1, dual tone multi-frequency (DTMF) tones can be generated. The specific DTMF tone generated is specified by the host loading the Transmitter Data Buffer (TBUFFER) with the appropriate digit code shown in Table 2.

User Defined Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), a user-defined single or dual tone can be generated. In this mode, the transmitter immediately begins sending the frequencies specified in DSP RAM. The tones will remain on as long as Tone Generator/Tone Detector configuration is selected and the tone amplitudes are greater than zero. Setting one of the two amplitudes to zero selects single tone frequency.

Note: Frequencies from 0 to 1675 Hz can be sent when the ORG bit is set, or frequencies from 1925 Hz to 2875 Hz can be sent when the ORG bit is cleared. 1800 Hz frequency can be sent by setting the GTE bit with GTS = 0 and ORG = 0.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Transmitter Carrier Frequency (Hz) ±0.01%		Data Rate (bps)	Baud	Bits Per	Constellation
		Answer[2]	Originate[2]	± 0.01%	(Symbols/Sec.)	Symbol	Points
V.22 bis	QAM	2400	1200	2400[3]	600	4	16
V.22A/B	DPSK	2400	1200	1200[3]	600	2	4
		2400	1200	600[3]	600	1	2
Bell 212A	DPSK	2400	1200	1200[3]	600	2	4
Bell 103	FSK	2225 M 2025 S	1270 M 1070 S	300[4]	300[4]	1	1
V.21	FSK	1650 M 1850 S	980 M 1180 S	300[4]	300[4]	1	1
V.23 Forward Channel	FSK	1300 M 2100 S	1300 M 2100 S	1200[4]	1200[4]	1	1
V.23 Forward Channel	FSK	1700 M 2100 S	1700 M 2100 S	600[4]	600[4]	1	1
V.23 Backward Channel	FSK	390 M 450 S	390 M 450 S	75[4]	75[4]	1	1

Notes:
1. Modulation legend: QAM Quadrature Amplitude Modulation; DPSK Differential Phase Shift Keying; FSK Frequency Shift Keying
2. M indicates a mark condition; S indicates a space condition.
3. Synchronous accuracy = ±0.01%; asynchronous accuracy = –2.5% to +1.0% (+2.3% if extended overspeed is selected).
4. Value is upper limit for serial (e.g., 0-300).

TONE DETECTION

Answer Tone and Call Progress Tones: When Dial/Call Progress configuration is selected (CONF bits = 81), tones can be detected as follows:

Call progress frequency range: 340 ± 5 Hz to 640 ± 5 Hz

Status Bit: TONEA

Answer tones (2100 ± 15 Hz or 2225 ± 10 Hz) or Bell FSK originate tone (1270 ± 10 Hz)

Detection level:0 dBm to –43 dBm

Default detection level: –43 dBm

Response time: 25 ± 2 ms

Status Bits: ATV25, ATBELL (ORG=1), BEL103 (ORG=0)

Tones are detected as energy above a certain threshold within a digital bandpass filter. The pass band of the dual bi-quad infinite impulse response (IIR) filter (Call Progress) or the single bi-quad IIR filter (answer tone or Bell FSK originate) can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in DSP RAM.

V.23 and V.21 Tones: When Tone Generator/Tone Detector configuration is selected (CONF bits = 80), tones can be detected as follows:

V.23 forward channel mark: 1300 ± 10 Hz

Status Bit: TONEA

V.23 backward channel mark: 390 ± 10 Hz

Status Bit: TONEB

V.21 high band mark (1650 ± 10 Hz) or low band mark (980 ± 10 Hz)

Table 2. Dial Digits/Tone Pairs

Hex Code	Dial Digit	Tone Pair (Hz)	(Hz)
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

Status Bit: TONEC

Detection level: 0 dBm to –43 dBm

Default detection level: –43 dBm

Response time: 25 ± 2 ms

Tones are detected as energy above the threshold within a digital bandpass filter. These filters are single bi-quad IIR filters*. The pass bands can be changed by writing new coefficients to DSP RAM. The tone detect threshold can also be changed in the DSP RAM.

*Except the filter represented by TONEA in Dial/Call Progress configuration, which is a dual biquad IIR filter.

Zero Crossing Detector: A zero crossing detector is always available. The detector can measure tone frequencies between 100 Hz and 3000 Hz. The zero crossing counter increments for both positive and negative zero crossings.

DATA ENCODING

The data encoding conforms to CCITT Recommendations V.22 bis, V.22A/B, V.23, or V.21, or to Bell 212A or 103, depending on the selected configuration.

EQUALIZERS

Equalization functions are incorporated that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer. A 13-tap automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations. Updating of the taps can be enabled or disabled (EQFZ). The equalizer taps can also be reset (EQRES).

Fixed Compromise Equalizer. A fixed compromise equalizer is provided in the transmitter. The equalizer can be enabled or disabled (CEQ bit).

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by a square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ± 150 microseconds over

Table 3. RTS - CTS Response Time

CTS Transition	Configuration	Constant Carrier	Controlled Carrier
OFF to ON	V.22 bis	≤2 ms	270 ms
	V.22	≤2 ms	270 ms
	Bell 212A	≤2 ms	270 ms
	V.21	2-5 ms	2-5 ms
	Bell 103	2-5 ms	2-5 ms
	V.23	5-20 ms	5-20 ms
ON to OFF	All	≤2 ms	≤2 ms

Note: The CTS OFF to ON response time is host programmable in DSP RAM for some configurations.

the frequency range 900 Hz to 1500 Hz (low channel) and 2100 Hz to 2700 Hz (high channel).

TRANSMIT LEVEL

The default transmitter output level is –6.0 dBm ±1.0 dB. The output level can be selected from 0 dBm to –15 dBm in 1 dB steps (TLVL bits).

TRANSMIT TIMING

Transmitter timing is selectable between internal (±0.01%), external , or loopback (TXCLK bits). When external clock is selected, the external clock rate must equal the desired data rate ±0.01% with a duty cycle of 50 ± 20%.

SCRAMBLER/DESCRAMBLER

A self-synchronizing scrambler/descrambler satisfying the applicable CCITT recommendation or Bell specification is incorporated. The scrambler and descrambler can be enabled or disabled (SDIS and DDIS bits, respectively)

RECEIVE LEVEL

The receiver satisfies performance requirements for received line signals from –9 dBm to –43 dBm. The received line signal is measured at the Receiver Analog (RXA) input.

RECEIVER TIMING

A ± 0.01% frequency error in the associated transmit timing source can be tracked.

CARRIER RECOVERY

A ± 7 Hz frequency offset in the received carrier can be tracked with less than a 0.2 dB degradation in bit error rate (BER).

CLAMPING

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (RLSD) output is off.

RTS - CTS RESPONSE TIME

The response times of CTS relative to a corresponding transition of RTS are listed in Table 3. The response time depends on the receiver operating in either constant carrier or controlled carrier mode (CC bit).

ASYNC/SYNC, SYNC/ASYNC CONVERSION

For parallel asynchronous data transfer, an asynchronous-to-synchronous converter is provided in the transmitter, and a synchronous-to-asynchronous converter is provided in the receiver. Asynchronous or synchronous mode is selected by the ASYNC bit. The asynchronous character format is 1 start bit, 5 to 8 data bits (WDSZ bits), an optional parity bit (PARSL and PEN bits), and 1 or 2 stop bits (STB bit). Valid character sizes, including all bits, are 7, 8, 9, 10 or 11 bits per character.

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters.

Two ranges of signaling rates are provided (selectable by the EXOS bit):

Basic range: +1% to –2.5%

Extended overspeed range: +2.3% to –2.5%

Break is handled in the transmitter and receiver as described in V.22 bis. If the RC2424DP/DS transmitter detects M to 2M + 3 bits of "start" polarity from the DTE, where M is the number of bits per character, the RC2424DP/DS will transmit 2M + 3 bits of start polarity. If the modem detects more then 2M +3 bits of start polarity, it will transmit all these bits as start polarity.

The RC2424DP/DS receiver will output the 2M + 3 or more bits of start polarity on RXD and will set the BRKD bit.

PIN ASSIGNMENTS

The RC2424DP/DS pin assignments are shown in Figure 2. The pin assigments are listed by pin number in Tables 4 and 5 for the DSP and IA devices, respectively.

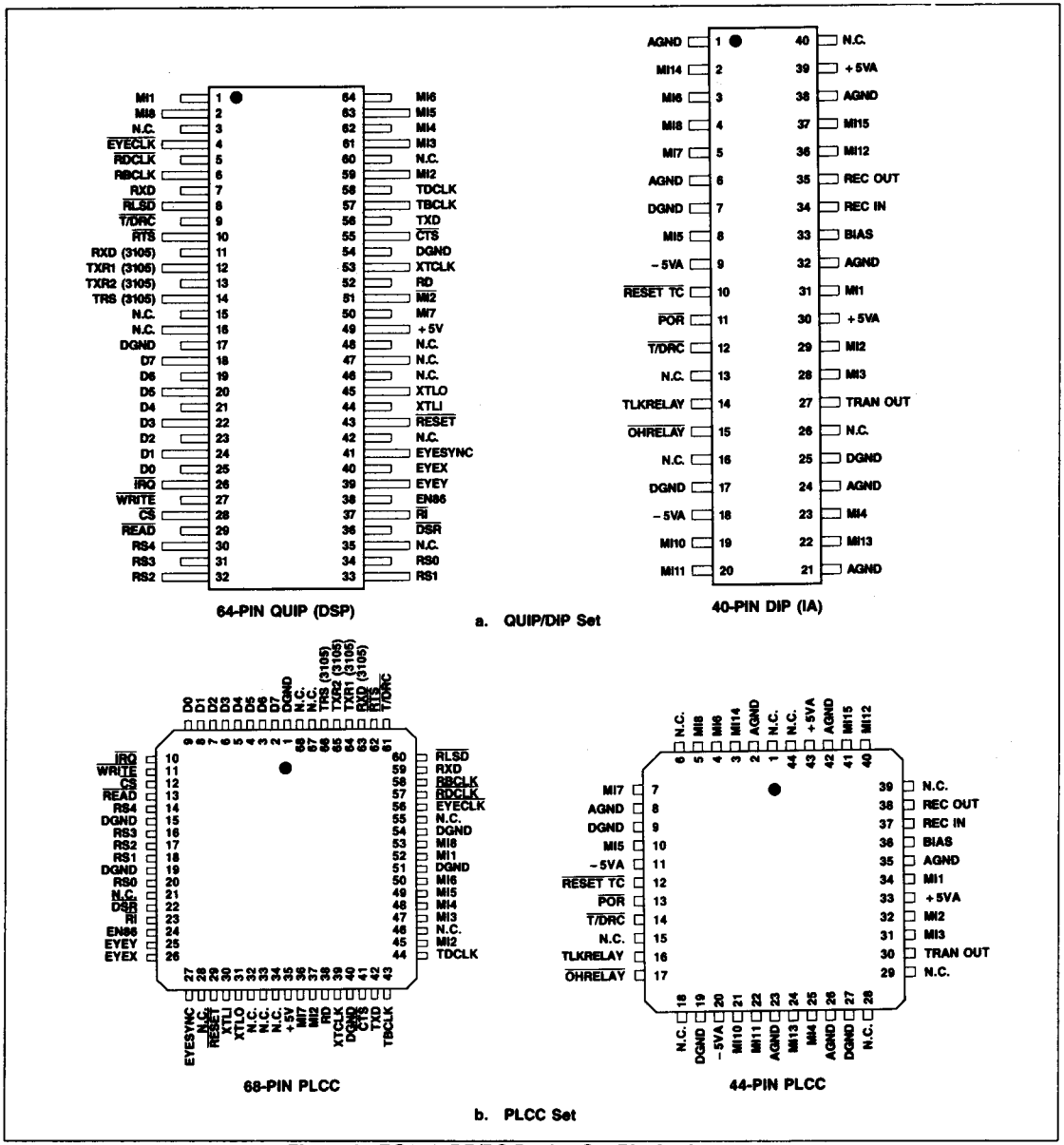


Figure 2. RC2424DP/DS Device Set Pin Assignments

Table 4. RC2424DP/DS DSP Pin Assignments

68-Pin PLCC Pin Number	64-Pin QUIP Pin Number	Signal Name	I/O Type
52	1	MI1	
53	2	MI8	
54	–	DGND	
55	3	N.C.	
56	4	EYECLK	OA
57	5	RDCLK	OA
58	6	RBCLK	OA
59	7	RXD	OA
60	8	RLSD	OA
61	9	T/DRC	IA
62	10	RTS	IA
63	11	RXD (3105)	IA
64	12	TXR1 (3105)	OB
65	13	TXR2 (3105)	OB
66	14	TRS (3105)	OB
67	15	N.C.	
68	16	N.C.	
1	17	DGND	
2	18	D7	IA/OB
3	19	D6	IA/OB
4	20	D5	IA/OB
5	21	D4	IA/OB
6	22	D3	IA/OB
7	23	D2	IA/OB
8	24	D1	IA/OB
9	25	D0	IA/OB
10	26	IRQ	OC
11	27	WRITE	IA
12	28	CS	IA
13	29	READ	IA
14	30	RS4	IA
15	–	DGND	
16	31	RS3	IA
17	32	RS2	IA
18	33	RS1	IA
19	–	DGND	
20	34	RS0	IA
21	35	N.C.	
22	36	DSR	OB
23	37	RI	OB
24	38	EN86	IA
25	39	EYEY	OB
26	40	EYEX	OB
27	41	EYESYNC	OB
28	42	N.C.	
29	43	RESET	IA
30	44	XTLI	I
31	45	XTLO	O
32	46	N.C.	
33	47	N.C.	
34	48	N.C.	
35	49	+5V	
36	50	MI7	
37	51	MI2	
38	52	RD	IA
39	53	XTCLK	IA
40	54	DGND	
41	55	CTS	OA
42	56	TXD	IA
43	57	TBCLK	OA
44	58	TDCLK	OA
45	59	MI2	
46	60	N.C.	
47	61	MI3	
48	62	MI4	
49	63	MI5	
50	64	MI6	
51	–	DGND	

Notes:
MI = Modem Interconnection (e.g., MI7), see Figure 3.
N.C. = No Connection, leave pin disconnected (open).
I/O Type: See Table 7.

Table 5. RC2424DP/DS IA Pin Assignments

44-Pin PLCC Pin Number	40-Pin DIP Pin Number	Signal Name	I/O Type
1	–	N.C.	
2	1	AGND	
3	2	MI14	
4	3	MI6	
5	4	MI8	
6	–	N.C.	
7	5	MI7	
8	6	AGND	
9	7	DGND	
10	8	MI5	
11	9	–5VA	
12	10	RESET TC	IA
13	11	POR	IA/OA
14	12	T/DRC	IA
15	13	N.C.	
16	14	TLKRELAY	OD
17	15	OHRELAY	OD
18	16	N.C.	
19	17	DGND	
20	18	–5VA	
21	19	MI10	
22	20	MI11	
23	21	AGND	
24	22	MI13	
25	23	MI4	
26	24	AGND	
27	25	DGND	
28	–	N.C.	
29	26	N.C.	
30	27	TRAN OUT	O (DD)
31	28	MI3	
32	29	MI2	
33	30	+5VA	
34	31	MI1	
35	32	AGND	
36	33	BIAS	I
37	34	REC IN	I (DB)
38	35	REC OUT	O (DA)
39	–	N.C.	
40	36	MI12	
41	37	MI15	
42	38	AGND	
43	39	+5VA	
44	40	N.C.	

Notes:
MI = Modem Interconnection (e.g., MI7), see Figure 3.
N.C. = No Connection, leave pin disconnected (open).
I/O Type: See Tables 7 and 8.

HARDWARE INTERFACE SIGNALS

The RC2424DP/DS hardware functional interface signals are shown in Figure 3. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., IRQ). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., $\overline{RDCLK}$), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals are organized into functional groups. These signals, along with their interface circuit type codes, are listed in Table 6. The digital and analog interface characteristics are defined in Tables 7 and 8, respectively.

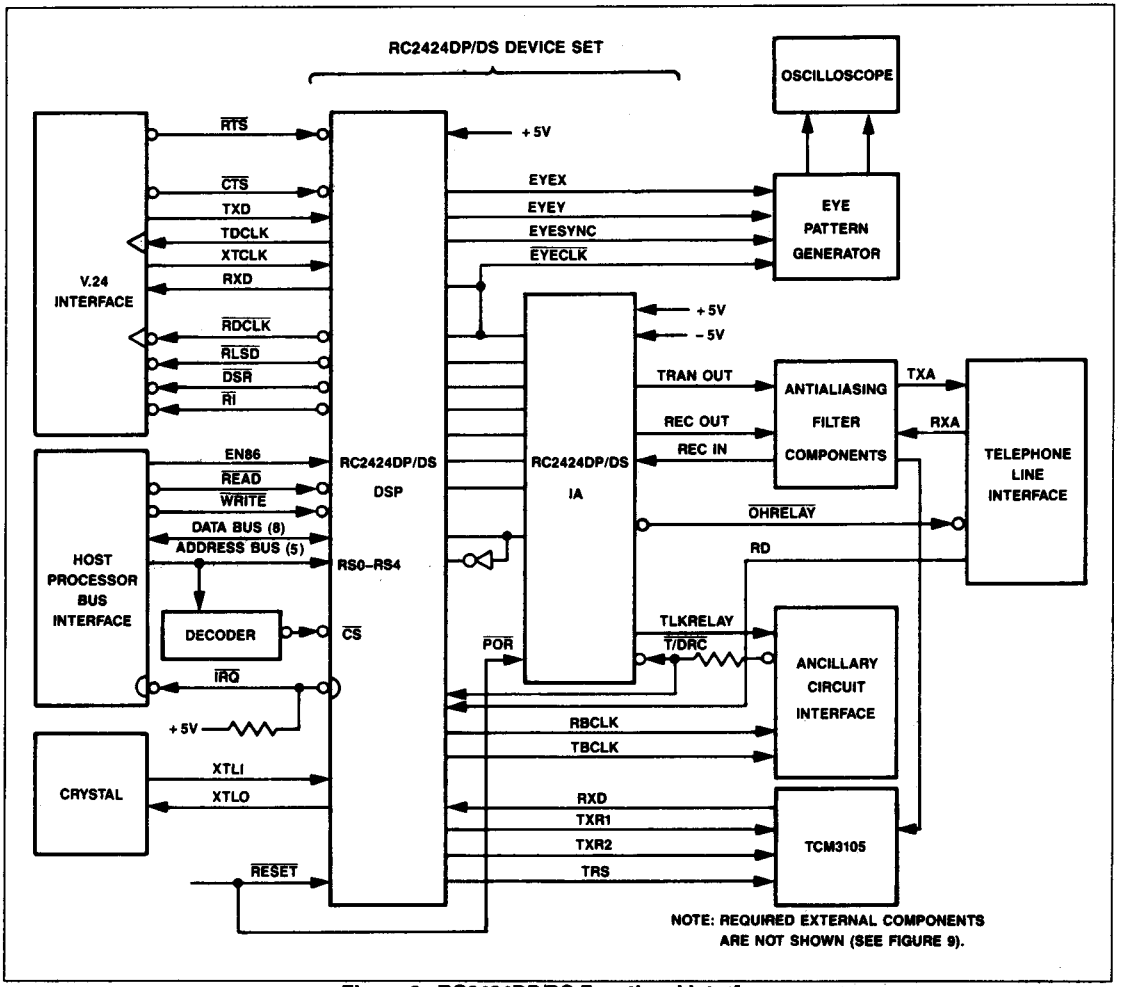


Figure 3. RC2424DP/DS Functional Interface

Table 6. RC2424DP/DS Hardware Interface Signals

Name	I/O Type	Description
DSP and IA Overhead		
AGND	GND	Analog Ground Return
DGND	GND	Digital Ground Return
+5V	PWR	+5 Volt Supply (DSP & IA)
–5V	PWR	–5 Volt Supply (IA)
RESET	IA	Reset (DSP)
POR	IA/OA	Power-On-Reset (IA)
RESET TC	IA	Reset Time Constant (IA)
XTLI	I	Crystal In
XTLO	O	Crystal Out
DSP/Host Processor Pararallel Bus Interface		
D7	IA/OB	↑
D6	IA/OB	|
D5	IA/OB	|
D4	IA/OB	Data Bus (8-Bits)
D3	IA/OB	|
D2	IA/OB	|
D1	IA/OB	|
D0	IA/OB	↓
RS4	IA	↑
RS3	IA	|
RS2	IA	Register Select (5-Bits)
RS1	IA	|
RS0	IA	↓
CS	IA	Chip Select
READ (φ2)	IA	Read Enable or φ2 Clock
WRITE (R/W)	IA	Write Enable or Read/Write
IRQ	OC	Interrupt Request
EN86	IA	Enable 8086 Bus
DSP/TCM3105 Interface		
RXD (3105)	IA	V.23 Receive Data
TXR1 (3105)	OB	V.23 TCM 3105 Control
TXR2 (3105)	OB	V.23 TCM 3105 Control
TRS (3105)	OB	V.23 TCM 3105 Control
DSP/Line Interface		
RD	IA	Ring Detect

Table 6. RC2424DP/DS Hardware Interface Signals (Cont'd)

Name	I/O Type	Description
DSP/V.24 Interface		
XTCLK	IA	External Transmit Clock
TDCLK	OA	Transmitter Data Clock
RDCLK	OA	Receiver Data Clock
RTS	IA	Request-To-Send
CTS	OA	Clear-To-Send
DSR	OB	Data Set Ready
TXD	IA	Serial Transmit Data
RXD	OA	Serial Receive Data
RLSD	OA	Received Line Signal Detector
RI	OB	Ring Indicator
IA/External Filter Components		
REC IN	DB	IA Receiver Op Amp Input
REC OUT	DA	IA Receiver Op Amp Output
TRAN OUT	DD	IA Transmitter Analog Output
External Filter Components/Line Interface		
RXA	DE	Receive Analog Input
TXA	DF	Transmit Analog Output
IA/Line Interface		
OHRELAY	OD	Off-Hook Relay Driver
DSP/Ancillary Circuits		
TBCLK	OA	Transmit Baud Clock
RBCLK	OA	Receive Baud Clock
IA/Ancillary Circuits		
T/DRC	IA	Uncommitted Relay Control
TLKRELAY	OD	Uncommitted Relay Driver
DSP/Eye Pattern Generator (Diagnostic Circuit)		
EYEX	OB	Eye Pattern Data X-Axis
EYEY	OB	Eye Pattern Data Y-Axis
EYECLK	OA	Eye Pattern Clock
EYESYNC	OB	Eye Pattern Sync

NOTES: 1. I/O types are described in Table 7 (digital signals) and Table 8 (analog signals).
2. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Table 7. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage (Types A & B)	V_{IH}	2.0	–	V_{CC}	Vdc	
Input High Current	I_{IL}	–	–	40	μA	V_{CC} = 5.25V, V_{IN} = 5.25V
Input Low Voltage (Types A & B)	V_{IL}	–0.3	–	0.8	Vdc	
Input Low Current	I_{IH}	–	–	–400	μA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}	–	–	±2.5	μA	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage	V_{OH}				Vdc	
Type A and B		3.5	–	–		I_{LOAD} = – 100 μA
Type D		–	–	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				Vdc	
Type A and C		–	–	0.4		I_{LOAD} = 1.6 mA
Type B		–	–	0.4		I_{LOAD} = 0.8 mA
Type D		–	0.75	–		I_{LOAD} = 15 mA
Three–State Input Current (Off)	I_{TSI}	–	–	±10	μA	V_{IN} = 0.4 to V_{CC} –1
Power Dissipation	P_D	–	530	850	mW	

Table 8. Analog Interface Characteristics

Name	Type	Characteristic
REC OUT	DA	1458 type op amp output Dynamic range: –9 dBm to –43 dBm
REC IN	DB	1458 type op amp input
TRAN OUT	DD	1458 type op amp output P_O (High Band) = –0.5 dBm P_O (Low Band) = –2.5 dBm
RXA	DE	Input impedance: 68.1 KΩ ± 1% Receive level: –9 dBm
TXA	DF	1458 type op amp output Output level: 0 dBm ±1 dB

OVERHEAD SIGNALS

Overhead signals include power, ground, reset, and crystal signals.

+ 5V Supply

+5V ± 5% is required by both the DSP and the IA devices.

–5V Supply

–5V ± 5% is required by the IA device.

DSP Reset ($\overline{\text{RESET}}$)

The active low $\overline{\text{RESET}}$ input resets the internal DSP logic. Upon transition of $\overline{\text{RESET}}$ from low-to-high, the DSP interface memory bits are set to the default values shown in Table 11.

During DSP power turn-on, $\overline{\text{RESET}}$ must be held low for at least 0.5 microseconds after V_{CC} operating voltage is attained for the internal clock oscillator to stabilize. The DSP $\overline{\text{RESET}}$ input is usually tied to the IA $\overline{\text{POR}}$ line to have the IA $\overline{\text{POR}}$ output initiate a reset upon RC2424DP/DS power turn-on or if the IA detects a low power condition.

Power-On-Reset ($\overline{\text{POR}}$)

The IA Power-On Reset ($\overline{\text{POR}}$) signal is a bidirectional signal that is used as an active low input to reset the IA device and as an active low output to initiate an external reset of the DSP when a low power condition is detected within the IA device.

The IA device power-on reset circuit monitors the IA +5V supply and outputs a 100 ms to 300 ms low pulse on $\overline{\text{POR}}$ upon IA +5V turn-on. This pulse is generated regardless of the IA –5V supply level. A 10 ms minimum low pulse on $\overline{\text{POR}}$ is also generated when the IA +5V supply drops below 3.5V.

When DSP $\overline{\text{RESET}}$ and IA $\overline{\text{POR}}$ are tied together, the IA devices pulses $\overline{\text{POR}}$ low upon IA power turn-on to begin the $\overline{\text{POR}}$ sequence. The modem is ready 350 ms after the low-to-high transition of $\overline{\text{POR}}$. The $\overline{\text{POR}}$ sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{\text{POR}}$ low for at least 3 µs. $\overline{\text{POR}}$ is not pulsed low by the IA device when the $\overline{\text{POR}}$ sequence is initiated externally.

NOTE: If the modem is used in applications where the supply voltage can drop below +4.75V but not low enough to cause a $\overline{\text{POR}}$ sequence (i.e., <+3.5V), the host system should assert the reset signals to the DSP and IA devices upon supply voltage recovery to ensure proper modem initialization and operation.

IA Reset Time Constant ($\overline{\text{RESET}}$ TC)

When IA $\overline{\text{POR}}$ is used as described above, an external discrete RC network must be connected to the $\overline{\text{RESET}}$ TC pin to generate the $\overline{\text{POR}}$ long time constant (see Figure 9).

In modem circuits not requiring the bidirectional $\overline{\text{POR}}$ signal, the $\overline{\text{RESET}}$ TC input can be used as the active low reset input to the IA device rather than $\overline{\text{POR}}$. In this case, the $\overline{\text{RESET}}$ TC should be connected to the DSP $\overline{\text{RESET}}$ input instead of the RC network, and the IA $\overline{\text{POR}}$ input should be left open.

Crystal In (XTLI) and Crystal Out (XTLO)

The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors (see Figure 9 and Table 19).

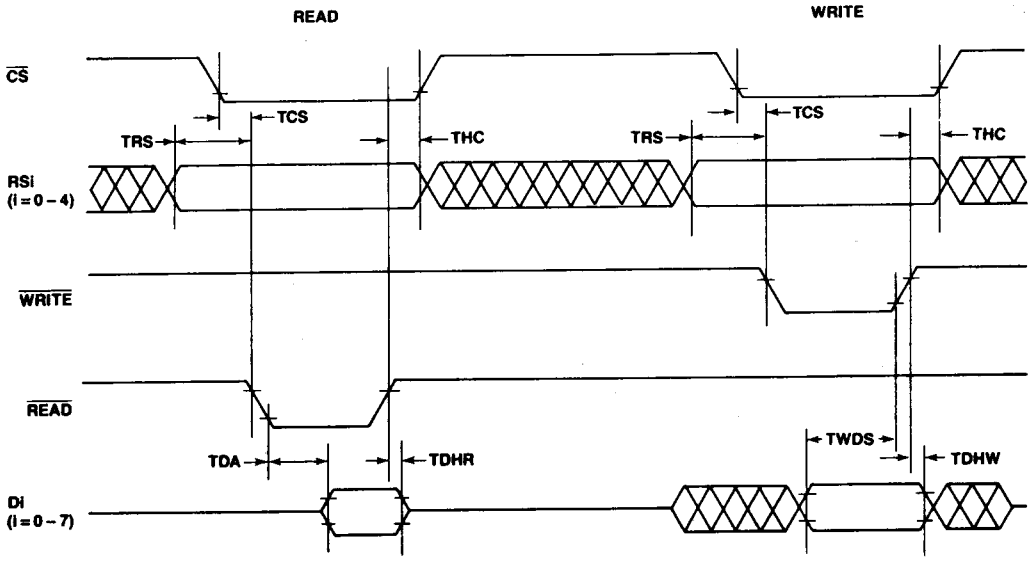
MICROPROCESSOR INTERFACE

Eighteen address, data, control and interrupt hardware interface signals implement an 8086/6502 compatible parallel microprocessor interface to a host processor. The read/write cycle timing requirements are listed in Table 9 and the timing waveforms are illustrated in Figure 4.

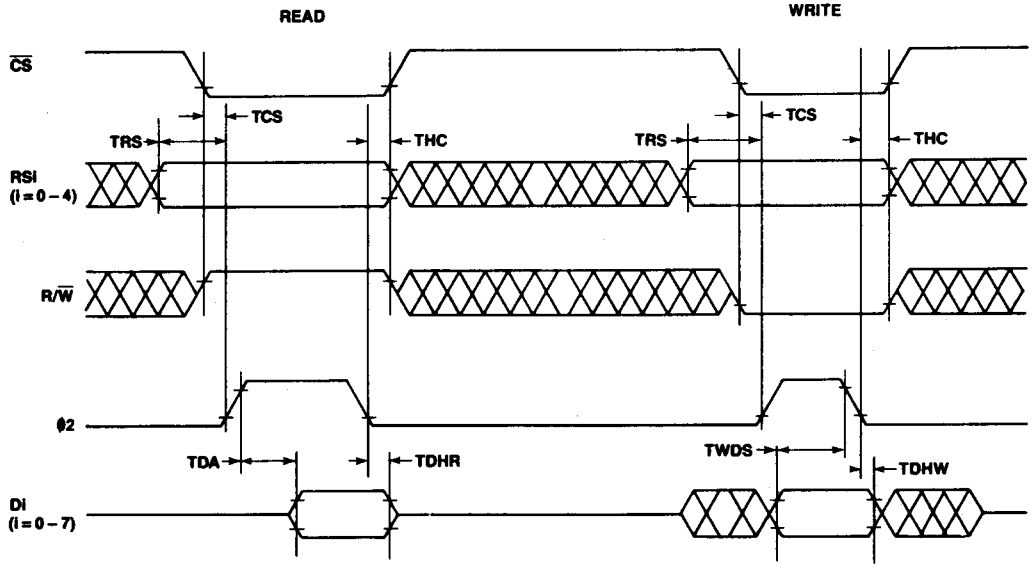
This parallel interface allows the host to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The definitions of the control and status bits, along with the methods of data interchange, are discussed in the Software Interface Section.

Table 9. Microprocessor Bus Interface Timing

Parameter	Symbol	Min.	Max.	Units
$\overline{\text{CS}}$ Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns



a. 8086 Bus Compatible (EN86 = High)



b. 6502 Bus Compatible (EN86 = Low)

Figure 4. Microprocessor Bus Interface Waveforms

Data Lines (D0–D7)

Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable (READ) and Write Enable (WRITE) signals.

Chip Select ($\overline{CS}$)

The active low Chip Select ($\overline{CS}$) input selects the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus.

Register Select Lines (RS0 - RS4)

The five active high Register Select inputs (RS0 - RS4) address interface memory registers within the DSP when $\overline{CS}$ is low. These lines are typically connected to address lines A0-A4.

When selected by $\overline{CS}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0-D7).

Read Enable ($\overline{READ}$) and Write Enable($\overline{WRITE}$)

The microprocessor bus operates with either 8086 or 6502 compatible timing as selected by the EN86 input.

When EN86 is high, 8086 timing is selected, and the read/write control signals are Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$). Reading or writing is controlled by the host pulsing either $\overline{READ}$ or $\overline{WRITE}$ input low, respectively, during the microprocessor bus access cycle (Figure 4a).

During a read cycle, data from the addressed DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.

During a write cycle, data from the data bus is copied into the addressed DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.

When EN86 is low, 6502 timing is selected, and the read/write control signals are Phase 2 Clock ($\phi 2$) and Read/Write (R/$\overline{W}$). ($\phi 2$ replaces $\overline{READ}$ and R/$\overline{W}$ replaces $\overline{WRITE}$.) Reading or writing is controlled by pulsing R/$\overline{W}$ low or leaving R/$\overline{W}$ high, respectively, during the microprocessor bus access cycle (Figure 4b).

Interrupt Request ($\overline{IRQ}$)

The modem Interrupt Request ($\overline{IRQ}$) output may be connected to the host interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in the DSP interface memory to indicate immediate change of conditions in the modem DSP device. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to the Software Considerations Section for a summary of the modem interrupt bits, interrupt conditions and interrupt clearing procedures.

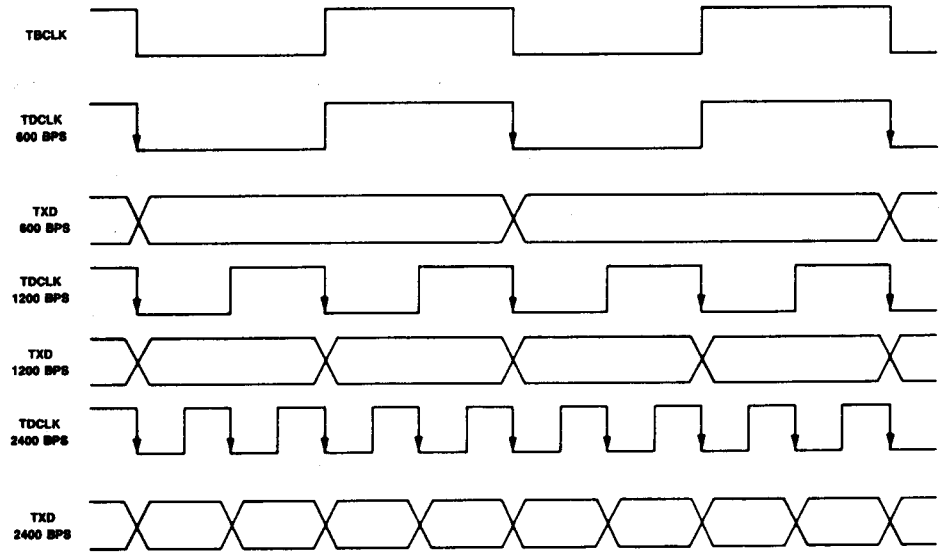
The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt request input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high).

Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25W, is sufficient.

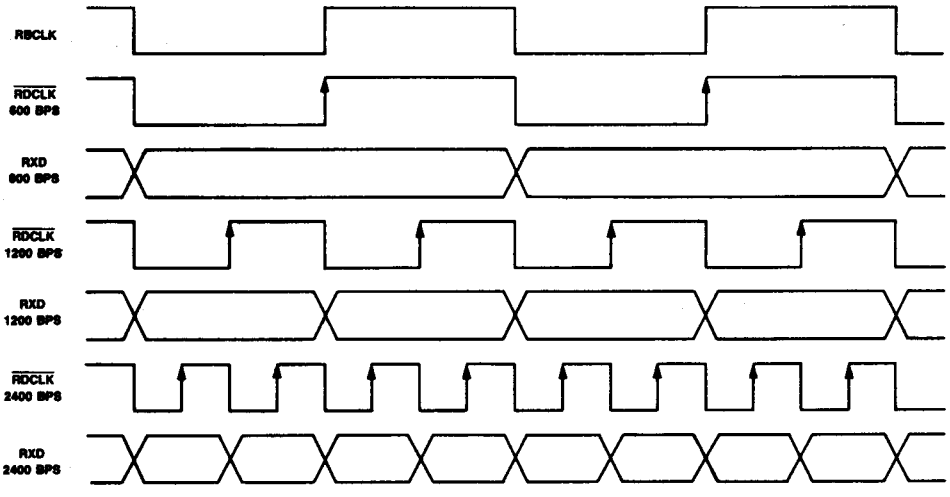
V.24 INTERFACE

Ten hardware circuits provide timing, data and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. The serial interface signals are TTL compatible and can drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to RS-232-C voltage levels using 1489 receivers and 1488 drivers, or their equivalents. The serial interface timing is illustrated in Figure 5.

The $\overline{RTS}$ hardware control input is logically ORed with its corresponding interface memory bit by the modem to form the resultant control signal. The state of each hardware status output signal ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) is also reflected in its corresponding interface memory bit. Note that the hardware interface signals are complemented with respect to their corresponding interface memory bits (e.g., $\overline{RTS}$ signal low = RTS bit set to a 1).



a. Transmit



b. Receive

Figure 5. Serial Interface Waveforms

Transmitted Data (TXD)

The modem obtains serial data to be transmitted from the host on the Transmitted Data (TXD) input in serial mode, or from the interface memory Transmit Data Register (TBUFFER) in parallel mode. (The TPDM bit in selects the serial or parallel mode.)

Received Data (RXD)

The modem presents received serial data to the host on the Received Data (RXD) output and to the interface memory Receive Data Register (RBUFFER) in both serial and parallel modes. RXD is clamped to mark in SDLC mode.

Request To Send ($\overline{RTS}$)

Request to Send ($\overline{RTS}$) input ON (low) causes the modem to transmit data on TXD when $\overline{CTS}$ becomes active.

Clear To Send ($\overline{CTS}$)

Clear to Send ($\overline{CTS}$) output ON (low) indicates that the modem will transmit any data present on TXD. $\overline{CTS}$ response times relative to $\overline{RTS}$ are shown in Table 3.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) output ON (low) indicates that the modem is in the data transfer state, i.e.:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.

$\overline{DSR}$ OFF (high) indicates that the host is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{RI}$).

Received Line Signal Detector ($\overline{RLSD}$)

$\overline{RLSD}$ ON (low) indicates that valid data is available on RXD. The $\overline{RLSD}$ thresholds are programmable in DSP RAM. The $\overline{RLSD}$ default threshold values for both high and low channels are:

$\overline{RLSD}$ ON ≥ -43 dBm
$\overline{RLSD}$ OFF ≤ -48 dBm

Ring Indicator ($\overline{RI}$)

Ring Indicator ($\overline{RI}$) output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The OFF (high) condition of the $\overline{RI}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received.

The $\overline{RI}$ frequency range is programmable in DSP RAM. $\overline{RI}$ will respond to RD input signals in the frequency range of 15.3 Hz to 68 Hz (default values).

The $\overline{RI}$ OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal on the RD input and the subsequent ON (OFF) transition of RI. The RI response times are shown in Table 10.

Table 10. RI Response Time

$\overline{RI}$ Transition	Response Time
OFF to ON	One Period *
ON to OFF	One Period

* Period of the ring frequency.

Transmit Data Clock (TDCLK)

The modem outputs a Transmit Data Clock (TDCLK) in synchronous communications. The TDCLK clock frequency is data rate ±0.01% with a duty cycle of 50 ± 1%. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding and following the rising edge of TDCLK.

In asynchronous modes, TDCLK is clamped to mark.

External Transmit Clock (XTCLK)

In synchronous communication, the host may supply the external transmit data clock input (XTCLK). The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is reflected at TDCLK if the modem is set for external clock (TXCLK = 10).

Receive Data Clock ($\overline{RDCLK}$)

The modem outputs a Receive Data Clock ($\overline{RDCLK}$) in the form of 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit can track a ±0.01% frequency error in the remote transmit timing source.

$\overline{RDCLK}$ is output in synchronous communications only. In asynchronous modes, $\overline{RDCLK}$ is clamped to mark.

DAA INTERFACE

Receive Analog (RXA)

RXA is an input to the external filter components from a data access arrangement (see Figure 9). The input impedance at RXA is determined by R13 (see Design Considerations Section). R13 is selected such that power at REC OUT is –9 dBm when the maximum signal is applied to RXA.

Transmit Analog (TXA)

The TXA output from the external filter components (see Figure 9) can drive a data access arrangement for connection to either the PSTN or a leased line. The transmitter output impedance is a 1458 type operational amplifier output. The output level is determined by R15 (see Design Considerations Section).

ANCILLARY SIGNALS

Talk/Data Relay Driver (TLKRELAY)

TLKRELAY is an open drain output which can drive a normally closed relay with greater than 360 Ω coil resistance. The TLKRELAY output is controlled by the T/DRC input. The TLKRELAY output is clamped off during power-on reset. An external discrete diode is not required across the relay coil.

In a typical application, TLKRELAY OFF opens the Talk/Data relay and disconnects the handset from the telephone line (i.e., the modem has control of the line.)

Off-Hook Relay Driver ($\overline{\text{OHRELAY}}$)

$\overline{\text{OHRELAY}}$ is an open drain output which can drive a normally open relay with greater than 360 Ω coil resistance. $\overline{\text{OHRELAY}}$ ON closes the Off-Hook relay and connects the modem to the telephone line (off-hook). The $\overline{\text{OHRELAY}}$ output is controlled by the state of the RA bit, except in pulse dial mode. $\overline{\text{OHRELAY}}$ output is clamped off during power-on reset. An external discrete diode is not required across the relay coil.

Talk/Data Relay Control ($\overline{\text{T/DRC}}$)

Talk/Data Relay Control ($\overline{\text{T/DRC}}$) is an uncommitted input that controls the state of the TLKRELAY output. $\overline{\text{T/DRC}}$ low turns the TLKRELAY output ON; $\overline{\text{T/DRC}}$ high turns the TLKRELAY output OFF.

Ring Detect (RD)

RD indicates to the modem by an ON (high) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the RD input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 Hz to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on $\overline{\text{RI}}$.

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK) outputs are provided in synchronous communication modes. TBCLK and RBCLK have no counterpart in the V.24 or RS-232-C recommendations since they mark the baud interval rather than the data rate for the transmitter and receiver, respectively. Both signals are active high. The high-to-low transition of each baud clock coincides with a high-to-low transition of the respective data clock.

DIAGNOSTIC SIGNALS

Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line distrubances can usually be identified. Timing of these signals is illustrated in Figure 6.

EYEX and EYEY

The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope horizontal (X) axis and vertical (Y) axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.

EYEX and EYEY outputs are 8-bit words, shifted out most significant bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.

$\overline{\text{EYECLK}}$

$\overline{\text{EYECLK}}$ is a clock for use by the serial-to-parallel converters. The $\overline{\text{EYECLK}}$ output is a 7200 Hz clock.

EYESYNC

EYESYNC is a strobe for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

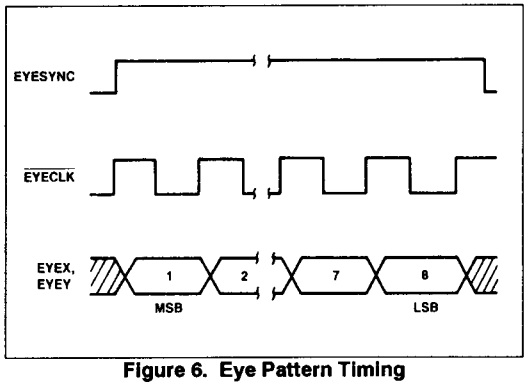


Figure 6. Eye Pattern Timing

SOFTWARE INTERFACE

Modem functions are implemented in DSP firmware.

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAP

A memory map of DSP interface memory identifying the contents of the 32 addressable registers is shown in Figure 7. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

INTERFACE MEMORY BIT DEFINITIONS

Table 11 defines the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is denoted by Z (00 through 1 F) and the bit number is located by Q (0 through 7, where 0 = LSB).

INITIALIZATION

The POR default value for each configuration/control bit is shown in Table 11. POR leaves the modem configured as follows:

- 2400 bps
- Synchronous
- Constant carrier
- Serial data mode
- Answer mode

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	XACC	—	—	—	—	—	XWT	XCR
1C	X RAM ADDRESS (XADD)							
1B	YACC	—	—	—	—	—	YWT	YCR
1A	Y RAM ADDRESS (YADD)							
19	X RAM DATA MSB (XDAM)							
18	X RAM DATA LSB (XDAL)							
17	Y RAM DATA MSB (YDAM)							
16	Y RAM DATA LSB (YDAL)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	TLVL				—	—	TXCLK	
12	CONFIGURATION (CONF)							
11	—	—	—	—	—	—	—	TXP
10	TRANSMIT DATA BUFFER (TBUFFER)							
0F	RLSD	—	CTS	DSR	RI	TM	SYNCD	FLAGS
0E	RTDET	BRKD	PE	FE	OE		SPEED	
0D	—	—	S1DET	SCR1	U1DET	SADET	—	—
0C	—	—	—	—	—	—	—	—
0B	TONEA	TONEB	TONEC	ATV25	ATBELL	—	—	BEL103
0A	—	—	—	—	—	—	—	CRCS
09	NV25	CC	DTMF	ORG	LL	DATA	—	—
08	ASYNC	TPDM	—	DDIS	TRFZ	—	RTRN	RTS
07	RDLE	RDL	L2ACT	—	L3ACT	—	RA	MHLD
06	BRKS	EXOS	PARSL		PEN	STB	WDSZ	
05	—	—	—	—	CEQ	—	—	—
04	EQRES	—	—	—	EQFZ	IFIX	—	CRFZ
03	SYNCMD		SPLIT	—	ARC	SDIS	GTE	GTS
02	—	—	—	—	—	—	—	—
01	—	—	—	—	—	—	—	RXP
00	RECEIVER DATA BUFFER (RBUFFER)							

(—) Indicates reserved for modem use only

Figure 7. RC2424DP/DS Interface Memory Map

Table 11. Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
ARC	03:3	0	**Automatic Rate Change Enable.** When control bit ARC is a 1, an automatic on-line rate change sequence is enabled. This allows on-line fallback from 2400 bps to 1200 bps per V.22 bis Section 6.6.
ASYNC	08:7	0	**Asynchronous/Synchronous.** When control bit ASYNC is a 1, asynchronous data mode is selected. When ASYNC changes from a 0 to a 1, the receiver's synchronous to asynchronous converter and the transmitter's asynchronous to synchronous converter are configured according to the EXOS, PARSL, PEN, STB and WDSZ bits at that time. ASYNC may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. Asynchronous communication is available only in parallel data mode (TPDM = 1). All clocks are clamped to mark in asynchronous mode. When ASYNC is a 0, synchronous data mode is selected. The SYNCMD bits further select one of two synchronous modes.
ATBELL	0B:3	0	**Bell Answer Tone Detected.** When set to a 1, status bit ATBELL indicates that the modem is detecting a 2225 Hz answer tone. When reset to a 0, the 2225 Hz answer tone is not being detected. ATBELL is active only in the Dial/Call Progress and originate handshake configurations.
ATV25	0B:4	0	**V25 Answer Tone Detected.** When set to a 1, status bit ATV25 signifies that the modem is detecting a 2100 Hz answer tone. When reset to a 0, the 2100 Hz answer tone is not being detected. ATV25 is only active in the Dial/Call Progress and originate handshake modes (ORG = 1).
BEL103	0B:0	0	**Bell 103 Mark Frequency Detected.** When set to a 1, status bit BEL103 indicates that the modem is detecting a Bell 103 mark frequency (1270 Hz). When reset to a 0, the mark frequency is not being detected. BEL103 is available only in Dial/Call Progress and answer handshake modes (ORG = 0).
BRKD	0E:6	0	**Break Detected.** When set to a 1, status bit BRKD indicates the modem is receiving continuous space. When reset to a 0, continuous space is not being received.
BRKS	06:7	0	**Break Sequence.** When control bit BRKS is a 1 and TPDM is a 1, the modem will send continuous space. When BRKS is a 0 and TPDM is a 1, the modem will transmit parallel data from the TBUFFER. (This bit is valid only when TPDM = 1.)
CC	09:6	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier (i.e., the carrier is controlled by $\overline{\text{RTS}}$); when 0, the modem operates in constant carrier (i.e., the carrier stays on when $\overline{\text{RTS}}$ is off). Controlled Carrier is available only in leased line (LL = 1). Controlled carrier allows the modem transmitter to be controlled by the $\overline{\text{RTS}}$ pin or the RTS bit (see Table 3). When the $\overline{\text{RTS}}$ pin goes low, or the RTS bit set to a 1, the transmitter immediately sends scrambled ones for 270 ms and then turns on the $\overline{\text{CTS}}$ signal and the CTS bit. At 2400 bps, it is recommended that a retrain be sent once in the data mode to ensure that synchronization occurs. (V.22 bis)
CEQ	05:3	0	**Compromise Equalizer Enable.** When control bit CEQ is a 1, the transmitter's passband digital compromise equalizer is inserted into the transmit path. When CEQ is a 0, the equalizer is not inserted into the transmit path.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CONF	12:0-7	84	**Modem Configuration Select.** The CONF control bits select the modem operating mode from one of the following configuration codes: Data Rate (bps) Mode / Transmit / Receive / CONF (Hex) V.22 bis 2400 2400 84 V.22 1200 1200 52 V.22 600 600 51 Bell 212A 1200 1200 62 Bell 103 0-300 0-300 60 V.21 300 300 A0 V.23 75 1200 46 V.23 1200 75 47 V.23 75 600 44 V.23 600 75 45 V.23 1200 1200 42 V.23 600 600 41 V.23 75 75 40 Tone Generator/Detector 80 Dial/Call Progress Monitor 81 **Note:** NEWC must be set to a 1 after CONF is changed.
CRCS	0A:0	0	**CRC Sending.** When set to a 1, status bit CRCS indicates that the transmitter is sending the CRC (2 bytes) in SDLC mode. A 0 indicates that the CRC is not being sent.
CRFZ	04:0	0	**Carrier Recovery Freeze.** When control bit CRFZ is a 1, updating of the receiver's carrier recovery phase lock loop (PLL) is inhibited. When reset to a 0, normal updating is enabled.
CTS	0F:5	0	**Clear to Send.** When set to a 1, status bit CTS indicates that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted (see TPDM). CTS response times from an $\overline{\text{RTS}}$ ON or OFF transition after the modem has completed a handshake are shown in Table 3. When reset to a 0, data is not being transmitted.
DATA	09:2	0	**Data Mode.** When control bit DATA is a 0, the modem is in the idle mode and data is not being transmitted. The modem is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering. When control bit DATA is a 1, the modem is in the data mode in either leased line mode (LL = 1) or handshake mode (LL = 0).
DDIS	08:4	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.
DSR	0F:4	0	**Data Set Ready.** When set to a 1 (ON), status bit DSR indicates that the modem is in the data transfer state. When reset to a 0 (OFF), DSR indicates that the DTE is to disregard all signals appearing on the interchange circuits–except RI.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DTMF	09:5	0	**DTMF Select.** When the modem is configured for dialing mode (CONF = 81), the modem will dial using DTMF tones or pulses. When control bit DTMF is a 1, the modem will dial using DTMF tones. When DTMF is a 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. Dialing mode is selected by configuration code 81 in the Configuration Register (CONF). When in dialing mode, the data placed in the Transmitter Data Buffer (TBUFFER) is treated as the digit to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the TBUFFER). Also, see TDBE bit. Dialing timing is host programmable in DSP RAM.
EQFZ	04:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited. When a 0, updating is enabled.
EQRES	04:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver adaptive equalizer taps are reset to zero. When a 0, the equalizer taps are updated normally.
EXOS	06:6	0	**Extended Overspeed.** When control bit EXOS is a 1, Extended Overspeed mode is selected in the transmitter async-to-sync converter and in the receiver sync-to-async converter. When a 0, normal overspeed mode is selected. (See SPLIT)
FE	0E:4	0	**Framing Error.** When set to a 1, status bit FE indicates that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode or an ABORT sequence was detected in SDLC/HDLC synchronous mode. When reset to a 0, no framing error is detected.
FLAGS	0F:0	0	**Flag Sequence.** When set to a 1, status bit FLAGS indicates that the transmitter is sending the Flag sequence in SDLC/HDLC mode, or a constant mark in parallel asynchronous mode. When reset to a 0, FLAGS indicates that the transmitter is sending data.
GTE	03:1	0	**Guard Tone Enable.** When control bit GTE is a 1, the specified guard tone to be transmitted is enabled (CCITT configurations only), according to the state of the GTS bit. The guard tone will be transmitted only by the answering modem. When set to a 0, guard tone transmission is disabled. (V.22 bis)
GTS	03:0	0	**Guard Tone Select.** When control bit GTS is set to a 1, the 550 Hz tone is selected; when a 0, the 1800 Hz tone is selected. The selected guard tone will be transmitted only when GTE is enabled. (V.22 bis)
IFIX	04:2	1	**Eye Fix.** When control bit IFIX is a 1, the serial diagnostic data output on the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM Address and Y RAM Address registers, respectively.
LL	09:3	0	**Leased Line.** When control bit LL is set to a 1, the modem will enter the Leased Line Data Mode (selected by the ORG bit) when the DATA bit is a 1. When a 0, the modem will enter the Handshake Mode (selected by the ORG bit) when the DATA bit is a 1.
L2ACT	07:5	0	**Loop 2 (Local Digital Loopback) Activate.** When control bit L2ACT is a 1, the receiver's digital output is internally connected to the transmitter's digital input (locally activated digital loopback) in accordance with CCITT Recommendation V.54.
L3ACT	07:3	0	**Loop 3 (Local Analog Loopback) Activate.** When control bit L3ACT is a 1, the transmitter's analog output is internally coupled to the receiver's analog input (local analog loopback) in accordance with CCITT Recommendation V.54. The modem may only be placed into loop 3 mode when in idle mode (DATA bit is a 0). After setting the L3ACT bit to a 1, the NEWC bit must also be set. The loopback is then completed when the modem sets DSR, CTS, and DCD (RLSD) bits to a 1. To terminate the loopback, reset L3ACT to a 0 and then set NEWC to a 1.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
MHLD	07:0	0	**Mark Hold.** When control bit MHLD is a 1, the transmitter sends continuous mark. When MHLD is a 0, the transmitter sends continuous flag or data from TBUFFER. This bit is valid only in SDLC/HDLC mode.
NCIA	1F:6	0	**NEWC Interrupt Active.** When the new configuration interrupt is enabled (NCIE is a 1) and a new configuration is implemented (NEWC is reset to a 0 by the DSP), $\overline{IRQ}$ is asserted and status bit NCIA is set to a 1 to indicate that NEWC being a 0 caused the interrupt. NCIA and the interrupt request due to NEWC are cleared by the host writing a 0 into NCIE. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable.** When control bit NCIE is a 1 (interrupt enabled), the modem will assert $\overline{IRQ}$ and set NCIA to a 1 when the NEWC bit is reset to a 0 by the DSP. When NCIE is a 0 (interrupt disabled), NEWC has no effect on $\overline{IRQ}$ or NCIA. (See NEWC and NCIA.)
NEWC	1F:0	0	**New Configuration.** When control bit NEWC is set to a 1, the modem will implement the new configuration. The DSP resets the NEWC bit to a 0 when the configuration change is acknowledged. A configuration change can also cause $\overline{IRQ}$ to be asserted. (See NCIE and NCIA.) **Note:** Control bit NEWC must be set to a 1 by the host after the host changes the contents of any of the following control bits: CONF Configuration SYNCMD Synchronous Mode Select GTE Guard Tone Enable GTS Guard Tone Select RDLE Remote Digital Loopback Enable RDL Remote Digital Loopback Request L2ACT Loop 2 Activate L3ACT Loop 3 Activate RA Relay Activate PARSL Parity Select PEN Parity Enable STB Stop Bit Number WDSZ Word Size ORG Originate Mode LL Leased Line Mode DATA Data ASYNC Asynchronous Mode RTRN Retrain TLVL Transmit Level EQRES Equalizer Reset
NEWS	1F:3	–	**New Status.** When set to a 1, status bit NEWS indicates that one or more status bits located in registers 0A, 0B, 0E, or 0F have changed state, or a DSP RAM read or write has been completed. This bit can be reset to a 0 only by the host. When set to a 1, this bit can cause $\overline{IRQ}$ to be asserted. (See NSIE and NSIA.)
NSIA	1F:7	0	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is a 1) and a change of status occurs (NEWS is set to a 1), $\overline{IRQ}$ is asserted and status bit NSIA is set to a 1 to indicate that NEWS being a 1 caused the interrupt. NSIA and the interrupt request due to NEWS are cleared when the host writes a 0 to NEWS. (See NEWS and NSIE.)
NSIE	1F:4	0	**NEWS Interrupt Enable.** When control bit NSIE is a 1 (interrupt enabled), $\overline{IRQ}$ will be asserted and NSIA will be set to a 1 when NEWS is set to a 1 by the DSP. When NSIE is a 0 (interrupt disabled), NEWS has no effect on $\overline{IRQ}$ or NSIA. (See NEWS and NSIA.)

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
NV25	09:7	0	**No. V.25 Answer Tone.** When control bit NV25 is a 1, the transmitter will not transmit the 2100 Hz CCITT answer tone when a handshake sequence is initiated and the modem is in answer mode. In originate mode, the receiver will not look for the 2100 Hz tone. When reset to a 0, the modem will transmit the answer tone in answer mode and will look for the answer tone in originate mode.
OE	0E:3	0	**Overrun Error.** When set to a 1, status bit OE indicates that the Receiver Data Buffer (RBUFFER) was loaded from the RXA input before the host read the old data from RBUFFER. When reset to a 0, RBUFFER was read before new receive data was loaded into RBUFFER. This is valid for both ASYNC mode and SDLC/HDLC mode.
ORG	09:4	0	**Originate.** When control bit ORG is a 1, the modem is in originate mode; when a 0, the modem is in answer mode. **Note:** The NEWC bit must be set after the ORG bit is changed.
PARSL	06:4, 5		**Parity Select.** Control bits PARSL select the method by which parity is generated and checked during the asynchronous parallel data mode (ASYNC = 1). The options are: **5 4 — Parity Selected** 0 0 — Stuff Parity ("9th Data Bit") (see TXP, RXP) 0 1 — Space Parity 1 0 — Even Parity 1 1 — Odd Parity
PE	0E:5	0	**Parity Error.** When set to a 1, status bit PE indicates that a character with bad parity was received in the asynchronous mode, or bad CRC was detected in the SDLC/HDLC synchronous mode. When a 0, a character with good parity was received.
PEN	06:3	0	**Parity Enable.** When set to a 1, control bit PEN enables parity generation and checking during asynchronous parallel data mode. When reset to a 0, parity generation and checking is disabled.
RA	07:1	0	**Off-Hook Relay Activate.** When control bit RA is set to a 1, the $\overline{\text{OHRELAY}}$ output is activated causing the relay to close (off-hook); when RA is reset to 0, the $\overline{\text{OHRELAY}}$ is turned off causing the relay to open (on-hook). **Note:** The host has exclusive control of the $\overline{\text{OHRELAY}}$ output through the RA bit except in pulse dial mode.
RBUFFER	00:0-7	0	**Receive Data Buffer.** The host obtains data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER.
RDBF	1E:0	–	**Receiver Data Buffer Full.** When set to a 1, status bit RDBF signifies that the modem wrote valid received data into register 00 (RBUFFER). This condition can also cause $\overline{\text{IRQ}}$ to be asserted. The host reading or writing register 00 resets the RDBF bit to 0. (See RDBIE and RDBIA.)
RDBIA	1E:6	0	**Receiver Data Buffer Interrupt Active.** When the receiver data buffer full interrupt is enabled (RDBIE is a 1) and register 00 is written to by the DSP (RDBF is set to a 1), the modem asserts $\overline{\text{IRQ}}$ and sets RDBIA to a 1 to indicate that RDBF being a 1 caused the interrupt. The host reading or writing register 00 resets the RDBF bit to a 0 and clears the interrupt request due to RDBF. (See RDBF and RDBIE.)
RDBIE	1E:2	0	**Receiver Data Buffer Interrupt Enable.** When control bit RDBIE is a 1 (interrupt enabled), the modem will assert $\overline{\text{IRQ}}$ and set the RDBIA bit to a 1 when RDBF is set to a 1 by the DSP. When RDBIE is a 0 (interrupt disabled), RDBF has no effect on $\overline{\text{IRQ}}$ or RDBIA. (See RDBF and RDBIA.)
RDL	07:6	0	**Remote Digital Loopback Request.** When control bit RDL is a 1, the modem initiates a request for the remote modem to go into digital loopback, RXD is clamped to a mark, and the RLSD bit and $\overline{\text{RLSD}}$ signal will be reset until the loop is established. When the host resets the RDL bit the modem sends the RDL terminating sequence.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RDLE	07:7	0	**Remote Digital Loopback Response Enable.** When set to a 1, control bit RDLE enables the modem to respond to the remote modem's digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS and RLSD bits to a 0, and turns the $\overline{CTS}$ and $\overline{DCD}$ signals OFF. The TM bit is set to a 1 to inform the host of the test status.
RI	0F:3	0	**Ring Indicator.** When set to a 1, status bit RI indicates that a valid ringing signal is being detected. Ringing is detected if pulses are present on the $\overline{RD}$ input in the 15 Hz - 68 Hz frequency range (default frequency range). The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with $\overline{RI}$ output signal. The minimum and maximum valid ring frequencies are host programmable in DSP RAM. If the maximum value is set to zero, the RI bit will go on and off with each half of the ring frequency sine wave.
RLSD	0F:7	0	**Received Line Signal Detector.** When status bit RLSD is set to a 1, the carrier is being detected and receive data is valid. When a 0, the carrier is not being detected and RXD output is clamped to mark. **Note:** RXD is also clamped to mark during retrain while the RLSD bit remains on.
RTDET	0E:7	0	**Retrain Detected.** When set to a 1, status bit RTDET indicates that a retrain request sequence has been detected.
RTRN	08:1	0	**Retrain.** When control bit RTRN set to a 1 and the modem is in data mode, the modem requests retrain (or automatic rate change - see ARC) from the remote modem. RTRN is set to 0 when the previous retrain is completed. **Note:** If retrain is not completed successfully, the host must clear the RTRN bit. Fallback from 2400 bps to 1200 bps per CCITT V.22 bis may be accomplished as follows: 1. Set the ARC bit to a 1 in both modems. 2. Set the RTRN bit to a 1 in either modem. 3. Set the NEWC bit to a 1. Fall forward from 1200 bps to 2400 may be accomplished as follows: 1. Reset the ARC bit (with the remote modem having the ARC bit set). 2. Set the RTRN bit. 3. Set the NEWC bit. If the remote modem can operate at the requested rate, the SPEED bits will be changed by the modem to reflect the new rate after the retrain is completed. If the remote modem cannot operate at the new rate, then no rate change will take place during the retrain. In this case, the host must clear the RTRN bit.
RTS	08:0	0	**Request to Send.** When control bit RTS is a 1 or the $\overline{RTS}$ input is ON, the CTS bit is set to a 1 and the $\overline{CTS}$ output is turned ON. When the RTS bit is reset to 0 and the RTS input is OFF, the CTS bit is reset to a 0 and the $\overline{CTS}$ output is turned OFF.
RXP	01:0	0	**Received Parity bit.** This bit is only valid when parity is enabled (PEN = 1), and word size is set for 8 bits per character (WDSZ = 11). In this case, the parity bit received (or ninth data bit) will be available at this location. The host must read this bit before reading the received data buffer (RBUFFER).
S1DET	0D:5	0	**S1 Sequence Detected.** Status bit S1DET is set to a 1 when the S1 sequence is being detected. This bit is reset to a 0 when the S1 sequence is not being detected.
SADET	0D:2	0	**Scrambled Alternating Ones Sequence Detected.** Status bit SADET is set to a 1 when the Scrambled Alternating Ones sequence is being detected. This bit is reset to a 0 when the Scrambled Alternating Ones sequence is not being detected. **Note:** SADET is used to indicate the response of the remote modem to a V.22 bis rate change request or a remote digital loopback request.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
SCR1	0D:4	0	**Scrambled Ones Sequence Detected.** Status bit SCR1 is set to a 1 when Scrambled Ones is being detected during handshake. This bit is reset to 0 when Scrambled Ones is not being detected.
SDIS	03:2	0	**Scrambler Disable.** When control bit SDIS is a 1, the transmitter scrambler is disabled; when SDIS is a 0, the scrambler is enabled.
SPEED	0E:0-2	0	**Speed Indication.** The SPEED status bits indicate the data rate at the completion of a handshake: **2 1 0 — Data Rate (bps)** 0 0 0 — 300 0 0 1 — 600 0 1 0 — 1200 0 1 1 — 2400
SPLIT	03:5	0	**Parallel Async Extended Overspeed TX/RX Split.** When SPLIT is set to a 1 and EXOS is set, the transmitter will transmit at the basic overspeed while the receiver receives at the extended overspeed rate.
STB	06:2	0	**Stop Bit Number.** When control bit STB is a 0, one stop bit is selected in asynchronous mode; when a 1, two stop bits are selected.
SYNCD	0F:1	0	**Sync Pattern Detected.** When set to a 1, status bit SYNCD indicates that SDLC/HDLC flags (7E pattern) are being detected. When reset to a 0, the 7E pattern is not being detected.
SYNCMD	03:6,7	0	**Synchronous Mode.** Configuration bits SYNCMD select the synchronous mode (ASYNC = 0) from the following: **7 6 — Synchronous Mode** 0 0 — Normal Sync 0 1 — SDLC/HDLC Sync
TBUFFER	10:0-7	00	**Transmitter Data Buffer.** The host conveys output data to the transmitter in the parallel mode (TPDM = 1) by writing a data byte to the TBUFFER when the TDBE bit is a 1. The data is transmitted bit 0 first.
TDBE	1E:3	–	**Transmitter Data Buffer Empty.** When set to a 1, status bit TDBE signifies that the modem has read transmit data from register 10 (TBUFFER) and the host can write new data into register 10. This condition can also cause IRQ to be asserted. The host reading or writing register 10 resets the TDBE bit to 0. (See TDBIE and TDBIA.)
TDBIA	1E:7	0	**Transmitter Data Buffer Interrupt Active.** When the transmitter data buffer empty interrupt is enabled (TDBIE is a 1) and register 10 is empty (TDBE is set to a 1), the modem asserts IRQ and sets status bit TDBIA to a 1 to indicate that TDBE being a 1 caused the interrupt. The host reading or writing register 10 resets the TDBIA bit to a 0 and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmitter Data Buffer Interrupt Enable.** When control bit TDBIE is a 1 (interrupt enabled), the modem will assert IRQ and set the TDBIA bit to a 1 when TDBE is set to 1 by the DSP. When TDBIE is a 0 (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TLVL	13:4-7	6	**Transmit Level Attenuation Select.** The TLVL control code selects the transmitter analog output level attenuation at the TXA pin as follows: **7 6 5 4 — Transmit Level Attenuation (dB ±0.5 dB)** 0 0 0 0 — 0 dB 0 0 0 1 — 1 dB 0 0 1 0 — 2 dB 0 0 1 1 — 3 dB 0 1 0 0 — 4 dB 0 1 0 1 — 5 dB 0 1 1 0 — 6 dB 0 1 1 1 — 7 dB 1 0 0 0 — 8 dB 1 0 0 1 — 9 dB 1 0 1 0 — 10 dB 1 0 1 1 — 11 dB 1 1 0 0 — 12 dB 1 1 0 1 — 13 dB 1 1 1 0 — 14 dB 1 1 1 1 — 15 dB The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM.
TM	0F:2	0	**Test Mode.** When set to a 1, status bit TM indicates that the selected test mode is active. When TM is reset to a 0, no test mode is active.
TONEA	0B:7	0	**Tone Filter A Energy Detected.** When set to a 1, status bit TONEA indicates that energy above the threshold is being detected by the Call Progress Monitor filter in the Dial Configuration (CONF = 81) or that 1300 Hz FSK tone energy is being detected by the Tone A bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	0B:6	0	**Tone Filter B Energy Detected.** When set to a 1, status bit TONEB indicates that 390 Hz FSK tone energy is being detected by the Tone B bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	0B:5	0	**Tone Filter C Energy Detected.** When set to a 1, status bit TONEC indicates that either 1650 Hz (ORG = 1) or 980 Hz (ORG = 0) FSK tone energy is being detected by the Tone C bandpass filter in the Tone Detector configuration (CONF = 80). When reset to a 0, energy is not being detected. The bandpass filter coefficients are host programmable in DSP RAM.
TPDM	08:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts parallel data from the host microprocessor interface via the TBUFFER register for transmission rather than serial data from the TXD input pin. When TPDM is a 0, serial data from the TXD input pin is accepted for transmission rather than parallel data from TBUFFER.
TRFZ	08:3	0	**Timing Recovery Freeze.** When control bit TRFZ is a 1, the updating of the receiver's timing recovery algorithm is inhibited. When TRFZ is a 0, normal updating occurs.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TXCLK	13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock: **1 0 — Transmit Clock** 0 0 — Internal 0 1 — Not Used (Internal) 1 0 — External (XTCLK input) 1 1 — Slave (RDCLK output) When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin. The external clock will then be reflected at the TDCLK output pin. When the slave clock is chosen, the transmitter clock output (TDCLK) is phase locked to the receiver clock output (RDCLK).
TXP	11:0	0	**Transmit Parity bit.** This bit is only active when parity is enabled (PEN = 1), stuff parity is selected (PARSL = 00) and word size is set for 8 bits per character. The host must load the stuffed parity bit (or ninth data bit) in this location before loading the other 8 bits of data in TBUFFER.
U1DET	0D:3	0	**Unscrambled Ones Detected.** When set to a 1, status bit U1DET indicates that V.22 bis Unscrambled Ones sequence has been detected. This bit is reset to a 0 by the modem at the end of the Unscrambled Ones sequence. (V.22 bis)
WDSZ	06:0,1	0	**Data Word Size.** The WDSZ control field sets the number of data bits per character in asynchronous mode as follows: **1 0 — Data Bits/Character** 0 0 — 5 0 1 — 6 1 0 — 7 1 1 — 8
XACC	1D:7	0	**X RAM Access Enable.** When control bit XACC is a 1, the DSP accesses the X RAM associated with the address in XADD and the XCR bit. XWT determines if a read or write is performed. The DSP resets XACC to a 0 upon RAM access completion.
XADD	1C:0-7	00	**X RAM Address.** XADD contains the X RAM address used to access the DSP's X Data RAM (XCR = 0) or X Coefficient RAM (XCR = 1) via the X RAM Data LSB and MSB registers (addresses 18 and 19, respectively). (See Table 12.)
XCR	1D:0	0	**X Coefficient RAM Select.** When control bit XCR is a 1, XADD applies to the X Coefficient RAM. When XCR is a 0, XADD applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 12).
XDAL	18:0-7	00	**X RAM Data LSB.** XDAL is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XDAM	19:0-7	00	**X RAM Data MSB.** XDAM is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XWT	1D:1	0	**X RAM Write.** When XWT is a 1 and XACC is set to a 1, the DSP copies data from the X RAM Data registers (18 and 19) into the X RAM location addressed by XADD and XCR. When control bit XWT is a 0 and XACC is set to a 1, DSP reads X RAM at the location addressed by XADD and XCR and stores the data into the X RAM Data registers (18 and 19)
YACC	1B:7	0	**Y RAM Access Enable.** When control bit YACC is a 1, the DSP accesses the Y RAM associated with the address in YADD and the YCR bit. YWT determines if a read or write is performed. The DSP resets YACC to a 0 upon RAM access completion.

Table 11. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description (Cont'd)
YADD	1A:0-7	00	**Y RAM Address.** YADD contains the Y RAM address used to access the DSP's Y Data RAM (YCR = 0) or Y Coefficient RAM (YCR = 1) via the Y RAM Data LSB and MSB registers (adresses 16 and 17, respectively). (See Table 12.)
YCR	1B:0	0	**Y Coefficient RAM Select.** When control bit YCR is a 1, YADD applies to the DSP's Y Coefficient RAM. When YCR is a 0, YADD applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 12).
YDAL	16:0-7	00	**Y RAM Data LSB.** YDAL is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YDAM	17:0-7	00	**Y RAM Data MSB.** YDAM is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YWT	1B:1	0	**Y RAM Write.** When YWT is a 1 and YACC is set to a 1, the DSP copies data from the Y RAM Data registers (16 and 17) into the Y RAM location addressed by YADD and YCR. When control bit YWT is a 0 and YACC is set to a 1, the DSP reads Y RAM at the location addressed by YADD and YCR and stores the data into the Y RAM Data registers (16 and 17).

DSP RAM ACCESS

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in DSP interface memory RAM Address registers (i. e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i. e., XCR and YCR) determine the DSP RAM addresses for data access.

One or two 16-bit words are transferred between DSP RAM and DSP interface memory once each internal DSP cycle. The transmitter and the receiver sample rate functions operate at the 7200 Hz sample rate. The receiver baud rate function operates at the 600 Hz.

Two RAM access bits (XACC and YACC) in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The DSP tests these bits each sample period.

HOST PROGRAMMABLE DATA

The parameters available in DSP RAM are listed in Table 12 along with the X RAM or Y RAM address and corresponding XCR or YCR bit value.

HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

1. Before writing to DSP interface memory, verify that XACC and YACC are reset to 0.
2. Load the RAM address into XRAM address (XADD) and/or YRAM address (YADD).
3. Write the desired data to the RAM data registers (XDAM, XDAL, YDAM, or YDAL).
4. Set the coressponding coefficient RAM select bits (XCR, YCR) as necessary.

Table 12. DSP RAM Parameters

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	0	–	1st Equalizer Tap, Real
1	1	11	–	Last Equalizer Tap, Real
2	1	–	0	1st Equalizer Tap, Imaginary
2	1	–	11	Last Equalizer Tap, Imaginary
3	0	16	–	Rotated Error, Real
4	0	–	16	Rotated Error, Imaginary
5	0	3F	–	Max AGC Gain Word
6	0	71	–	Pulse Dial Interdigit Time
7	0	7C	–	Tone Dial Interdigit Time
8	0	72	–	Pulse Dial Relay Make Time
9	0	7D	–	Pulse Dial Relay Break Time
10	0	7E	–	DTMF Duration
11	0	6D	–	Tone 1 Angle Increment Per Sample
12	0	–	6D	Tone 2 Angle Increment Per Sample
13	0	6F	–	Tone 1 Amplitude
14	0	–	6F	Tone 2 Amplitude
15	0	73	–	Max Samples Per Ring Frequency Period
16	0	74	–	Min Samples Per Ring Frequency Period
17	1	12	–	Real Part of Error
18	1	–	12	Imaginary Part of Error
19	1	–	14	Rotation Angle for Carrier Recovery
20	1	15	–	Rotated Equalizer Output, Real
21	1	–	15	Rotated Equalizer Output, Imaginary
22	1	16	–	Lower Part of Phase Error
23	1	–	16	Upper Part of Phase Error
24	1	3F	–	Upper Part of AGC Gain Word
25	1	–	3F	Lower Part of AGC Gain Word
26	1	1F	–	Average Power
27	1	2D	–	Phase Error
28	1	2F	–	Tone Power (ATBELL, BEL103 or TONEA
29	1	–	2F	Tone Detect Threshold (Call Progress Energy)
30	1	30	–	Tone Power (ATV25 or TONEB)

Table 12. DSP RAM Parameters (Cont'd)

No.	XCR/ YCR*	X RAM Addr	Y RAM Addr	Parameter
31	1	31	–	Tone Power (TONEC)
32	1	36	–	Tone Detect Threshold (ATBELL, BEL103, or TONEA)
33	1	37	–	Tone Detect Threshold (ATV25 or TONEB)
34	1	38	–	Tone Detect Threshold (TONEC)
35	1	3B	–	Zero Crossing Counter
36	1	52	–	Eye Quality Monitor (EQM)
37	1	–	31	Filter 1 Coefficient $\alpha 0$
38	1	–	32	Filter 1 Coefficient $\alpha 1$
39	1	–	33	Filter 1 Coefficient $\alpha 2$
40	1	–	34	Filter 1 Coefficient $\beta 1$
41	1	–	35	Filter 1 Coefficient $\beta 2$
42	1	–	37	Filter 2 Coefficient $\alpha 0$
43	1	–	38	Filter 2 Coefficient $\alpha 1$
44	1	–	39	Filter 2 Coefficient $\alpha 2$
45	1	–	3A	Filter 2 Coefficient $\beta 1$
46	1	–	3B	Filter 2 Coefficient $\beta 2$
47	1	–	76	Filter 3 Coefficient $\alpha 0$
48	1	–	77	Filter 3 Coefficient $\alpha 1$
49	1	–	78	Filter 3 Coefficient $\alpha 2$
50	1	–	79	Filter 3 Coefficient $\beta 1$
51	1	–	7A	Filter 3 Coefficient $\beta 2$
52	1	–	45	Filter 4 Coefficient $\alpha 0$
53	1	–	46	Filter 4 Coefficient $\alpha 1$
54	1	–	47	Filter 4 Coefficient $\alpha 2$
55	1	–	48	Filter 4 Coefficient $\beta 1$
56	1	–	49	Filter 4 Coefficient $\beta 2$
57	1	1C	–	Turn-on Threshold (PSK)
58	1	32	–	Turn-off Threshold (PSK)
59	1	–	21	RLSD Turn-off Time (PSK)
60	0	–	1C	Turn-on Threshold (FSK)
61	0	–	1D	Turn-off Threshold (FSK)

*XCR if an XRAM address is listed; YCR if a YRAM address is listed.

5. Set the appropriate RAM write bits (XWT, YWT).
6. Set the appropriate RAM access bits (XACC, YACC).
7. After the DSP has transferred the contents of the interface memory RAM data registers into DSP RAM, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 indicate DSP RAM write completion.
8. If the NSIE bit is a 1, $\overline{IRQ}$ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

Note: Steps 4 and 5 can be accomplished simultaneously.

DSP RAM Read Procedure

1. Before reading from DSP interface memory, verify that XACC and YACC are reset to a 0.
2. Load the RAM address into X RAM Address (XADD) and/or Y RAM Address (YADD) register(s).
3. Set the corresponding XCR and/or YCR bit(s) appropriately.
4. Reset XWT and/or YWT to a 0, inform the DSP that a RAM read will occur when XACC and/or YACC is set to a 1.
5. Set XACC and/or YACC to a 1 to signal the DSP to perform the RAM read.
6. After the DSP has transferred the contents of RAM into the interface memory RAM data registers, the DSP resets the XACC and/or the YACC bit to a 0, then sets the NEWS bit to a 1 to indicate DSP RAM read completion.
7. If the NSIE bit is a 1, IRQ is also asserted and NSIA is set to a 1 when NEWS is set to a 1. NSIA is cleared by writing a 0 into the NEWS bit, which also causes IRQ to return high if no other interrupt requests are pending.

Note: Steps 3 and 4 can be accomplished simultaneously.

SOFTWARE INTERFACE CONSIDERATIONS

INTERRUPT REQUEST HANDLING

DSP interface memory registers 00, 10, 1E, and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER) and register 10 is the Transmit Buffer (TBUFFER). Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits.

When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using $\overline{IRQ}$) or by being interrupted by $\overline{IRQ}$. When an interrupt enable bit and the corresponding interrupt flag are both set to a 1, $\overline{IRQ}$ is asserted and the corresponding interrupt active bit set to a 1.

The interrupt flag setting conditions are status changed detected, configuration changed acknowledged, receive buffer full and transmit buffer empty. Table 13 identifies the interrupt conditions and bits, and describes the interrupt clearing procedures.

Table 13. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
NSIA	NSIE	NEWS	New status detected (NEWS transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A, 0B, 0E, or 0F	Host writes a 0 into NEWS (Clears NSIA to a 0)
NCIA	NCIE	NEWC	New configuration acknowledged by DSP (NEWC transitioned from a 1 to a 0)	Host writes a 0 into NCIE (Clears NCIA to a 0)
TDBIA	TDBIE	TDBE	Transmitter Data Buffer is empty and can be written (TDBE transitioned from a 0 to a 1)	Host reads from or writes to register 10 (TBUFFER) (Clears TDBE and TDBIA to 0)
RDBIA	RDBIE	RDBF	Receiver Data Buffer is full and can be read (RDBF transitioned from a 0 to a 1)	Host reads from or register 00 (RBUFFER) (Clears RDBF and RDBIA to 0)

DIAL PROCEDURE

The host dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 8). The modem timing accounts for the DTMF tone duration and amplitude, pulse make/break ratio, and interdigit delay. These dialing parameters are host programmable in DSP RAM.

The level of the high DTMF tone is 2 dB greater than the level of the low DTMF tone.

The dialer default parameters are given in Table 14.

Table 14. Dial Default Parameters

Parameter	Default Value
DTMF Tone Duration	70 ms
DTMF Interdigit Delay	70 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	– 4 dBm
DTMF High Band Power Level	– 2 dBm
Pulse Relay Make Time	40 ms
Pulse Relay Break Time	60 ms
Pulse Interdigit Delay	750 ms

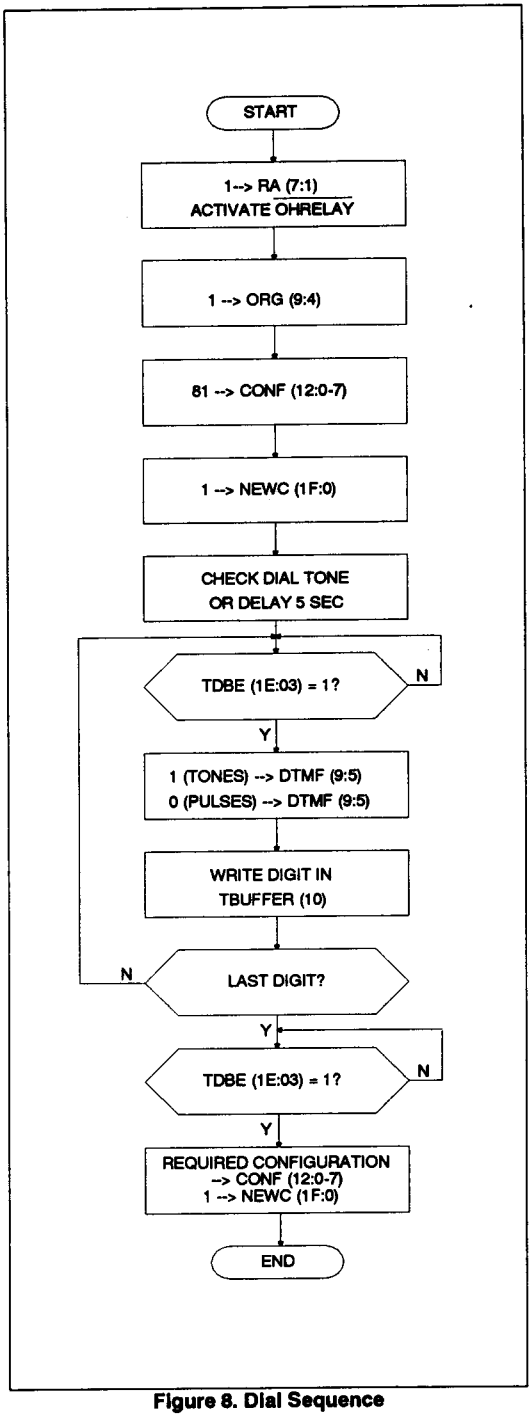


Figure 8. Dial Sequence

DESIGN CONSIDERATIONS

REQUIRED MODEM INTERFACE CIRCUIT

The RC2424DP/DS is supplied as two VLSI devices to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit (Figure 9) and parts list (Table 15) illustrate the connections and components required to connect the modem to the OEM electronics.

DAA INTERFACE

The following discussion of the interface to the integrated analog device is presented to enable designers to modify the design of the recommended line interface circuit. Also, the designer may wish to incorporate an existing line interface design with the modem device set.

Receive Input

Receive In (REC IN) and Receive Out (REC OUT) are pins associated with an integrated uncommitted operational amplifier inside the IA device. In conjunction with the three discrete components shown (R13, R14 and C11), the amplifier forms a first order lowpass antialiasing filter. This filter's function is to attenuate high frequency noise near and above the effective sampling rate of the integrated bandsplit filters (230.4 KHz).

The design of the modem requires that the pole of the anti-aliasing filter be fixed at 2337 Hz. This is calculated using the formula

$$\text{Filter Pole (Hz)} = 1/(2\pi \cdot R14 \cdot C11)$$

The recommended values of 68.1 KΩ for R14 and 1000 pF for C11 give the correct value for the filter pole. Some flexibility in choosing the component values for R14 and C11 is permissible provided that the pole of the filter is maintained within approximately ±5% of the correct value. When calculating the pole of the filter, component tolerances should be carefully considered.

Transmit Output

An external discrete smoothing filter must be added to the Transmit Output (TRAN OUT) signal to attenuate the high frequency aliases generated by the integrated switched capacitor filters. This is necessary to meet FCC requirements on transmitted high frequency energy. The pole of this filter may be calculated using the same formula as for the receiver filter, i.e.,

$$\text{Filter Pole (Hz)} = 1/(2\pi \cdot R16 \cdot C12)$$

The components values of R16 = 68.1 KΩ and C12 = 1000 pF place the pole at 2337 Hz. This may seem unusual as the response of a smoothing filter is generally designed to be flat in the band of interest, and then rolling off before the sampling rate. The bandsplit filter inside the IA is pre-distorted so that when cascaded with an external continuous first order smoothing filter, the response across the band is flat.

Some flexibility in choosing the values for R16 and C12 is permissible, provided some guidelines are followed. The choice of R16 and C12 must position the filter pole within ±5% of 2337 Hz.

The TRAN OUT integrated driver can drive a resistive load as low as 10 KΩ . This drive capability is desirable for the FCC Part 68 defined "programmable" mode.

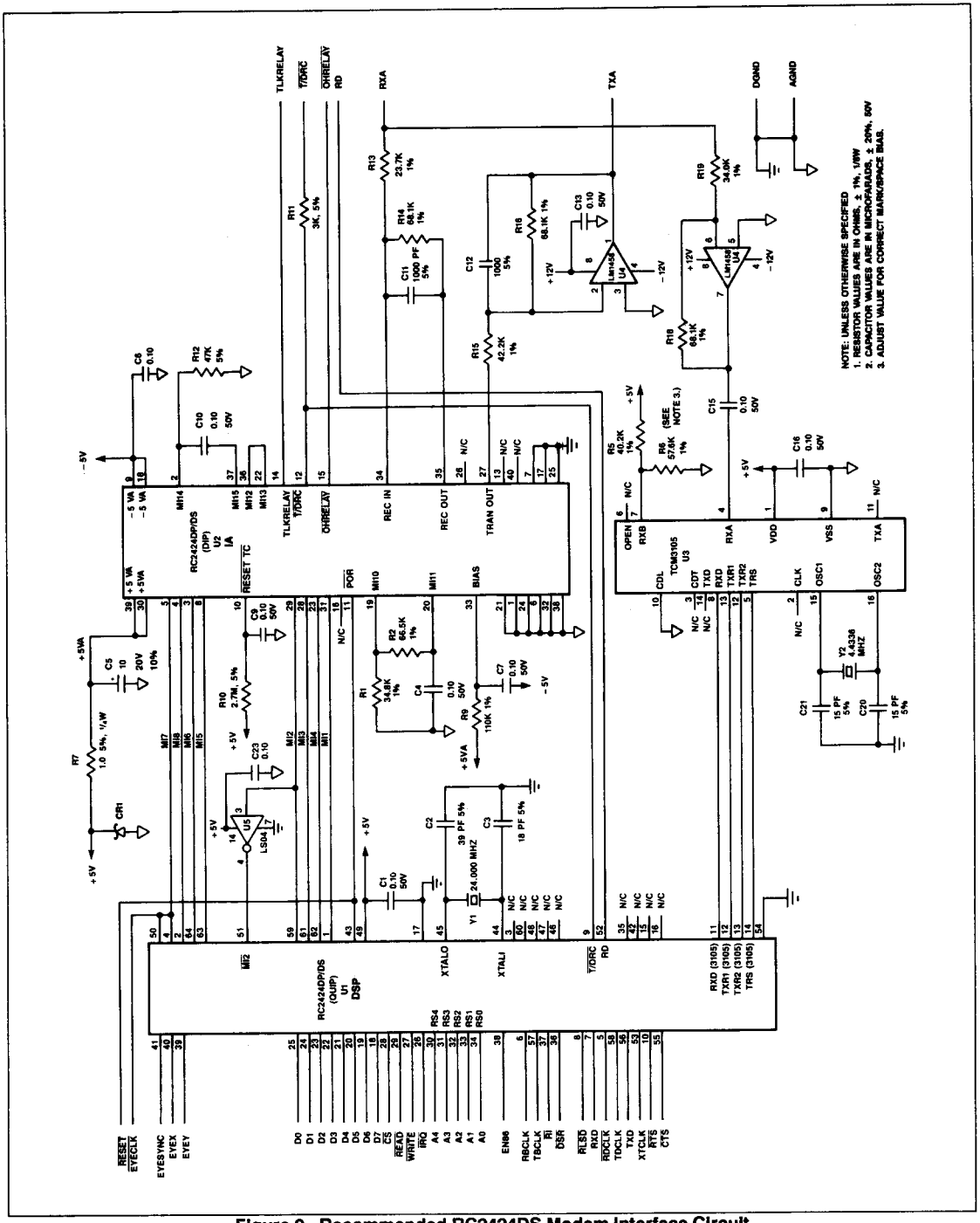


Figure 9. Recommended RC2424DS Modem Interface Circuit

Table 15. Recommended Modem Interface Circuit

Qty	Part Number	Description
1	U1	Rockwell RC2424DP/DS DSP
1	U2	Rockwell RC2424DP/DS IA
1	U3	TCM3105 FSK Modulator/ Demodulator
1	U4	1458 Dual Op
1	U5	SN74LS04 Hex Inverter
1	Y1	24.00014 MHz Crystal
1	Y2	4.4336 MHz Crystal
10	C1, C4, C6, C7, C9, C10,C13, C15, C16, C23	0.10 µF, 20%, 50V
1	C2	39 pF, 5%, 50V
1	C3	18 pF, 5%, 50V
1	C5	10 µF, 5%, 50V
2	C11, C12	1000 pF, 5%, 50V
2	C20, C21	15 pF, 5%, 50V
1	R1	34.8K Ω, 1%, 1/8 W
1	R2	66.5K Ω, 1%, 1/8 W
1	R5	40.2K Ω, 1%, 1/8 W
1	R6	57.6K Ω, 1%, 1/8 W
1	R7	1 Ω, 5%, 1/4 W
1	R9	110K Ω, 1%, 1/8W
1	R10	2.7M Ω, 5%, 1/8 W
1	R11	3K Ω, 5%, 1/8 W
1	R12	47K Ω, 5%, 1/8 W
1	R13	23.7 K Ω, 1%, 1/8 W
3	R14, R16, R18	68.1K Ω, 1%, 1/8 W
1	R15	42.2K Ω, 1%, 1/8 W
1	R19	34.0K Ω, 1%, 1/8 W
1	CR1	Schottky Diode, LL103B

PC BOARD LAYOUT GUIDELINES

The following guidelines should be adhered to when laying out a printed circuit board for the RC2424DP/DS devices. The pin numbers reflect the DSP 64-pin QUIP and the IA 40-pin DIP packages.

1. The DSP, IA and all supporting analog circuitry, including the data access arrangement should be located on the same area of printed circuit board.
2. The DSP device grounds should be routed separately from the IA device.
3. The DSP should be located on the pin 1 side of the IA device.
4. IA digital signals (pins 3, 4, 5, 8, 10, 12, 23, 28, 29, and 31) should be routed directly to the DSP, avoiding all analog components.
5. Routing of the RC2424DP/DS signals should provide maximum isolation between noise sources and noise senitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The DSP and IA noise source, neutral, and noise sensitive pins are listed in Table 16.
6. A 1.0Ω/10 µF RC network is needed to decouple the +5V supply. This must be done at the IA device to isolate it from the DSP device.
7. As a general rule, digital signals should be routed on the component side of the PCB while the analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
8. All power traces should be at least a 0.1 inch width.
9. The analog components should be located on the pin 40 side of the 40-pin IA device.
10. The IA AGND pins (1, 6, 21, 24, 32, and 38) and the DGND pins (7 and 25) should be tied together as ground directly under the device.
11. A 0.1 µF ceramic capacitor is used to decouple the –5V supply. This should be done in the immediate proximity of the IA device.
12. All circuitry connected to crystal pins 44 and 45 on the DSP device should be kept short to prevent stray capacitance from affecting the oscillator.

Table 16. RC2424DP/DS Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
DSP 64-Pin QUIP	+5V DGND Crystal Control Eye Pattern V.23 Interface Host Bus Interface Serial Interface IA Interface No Connection	 4, 41 11-13 5-7, 53, 56-58 1-2, 50-51, 59, 61-64	49, 17, 54 9, 38, 43, 52 39-40 14 18-34 8,10,36-37,55 3, 15-16, 35, 42, 46-48, 60	 44, 45
DSP 68-Pin PLCC	+5V DGND Crystal Control Eye Pattern V.23 Interface Host Bus Interface Serial Interface IA Interface No Connection	 27, 56 63, 65 39, 42-44, 57-59 36-37, 45, 47-50, 52-53	35 1, 15, 19, 40, 51, 54 24, 29, 38, 61 25-26 66 2-14, 16-18, 20, 22-23, 41, 60, 62 21, 28, 32-34, 46, 55, 67-68	 30-31
IA 40-Pin DIP	+5VA –5VA DGND AGND Control Analog DSP Interface No Connection	 3-5, 8, 23, 28-29, 31	30, 39 9, 18 7, 17, 25 1, 6, 21, 24, 32, 38 10, 14-15 12 11, 13, 16, 40	 2, 19-20, 22, 26-27, 33-37
IA 44-Pin PLCC	+5VA –5VA DGND AGND Control Analog DSP Interface No Connection	 4-5, 7, 10, 25, 31-32, 34	33, 43 11, 20 9, 19, 27 2, 8, 23, 26, 35, 42 12, 16-17 14 1, 6, 13, 15, 18, 28, 39, 44	 3, 21-22, 24, 29-30, 36-38, 40-41

GENERAL SPECIFICATIONS

Table 17. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Maximum) @ 0°C
+ 5 VDC	±5%	85 mA	130 mA
–5 VDC	±5%	20 mA	40 mA
Note: Input voltage ripple ≤1 volts peak-to-peak.			

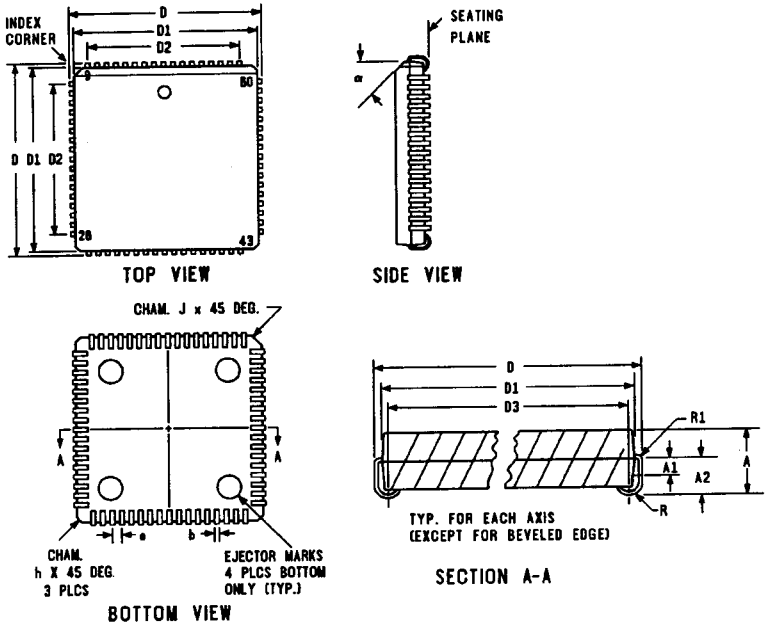
Table 18. Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to + 60°C (32°F to 140° F)
Storage	– 40°C to + 80°C (–40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	– 200 feet to + 10,000 feet

Table 19. Crystal Specifications

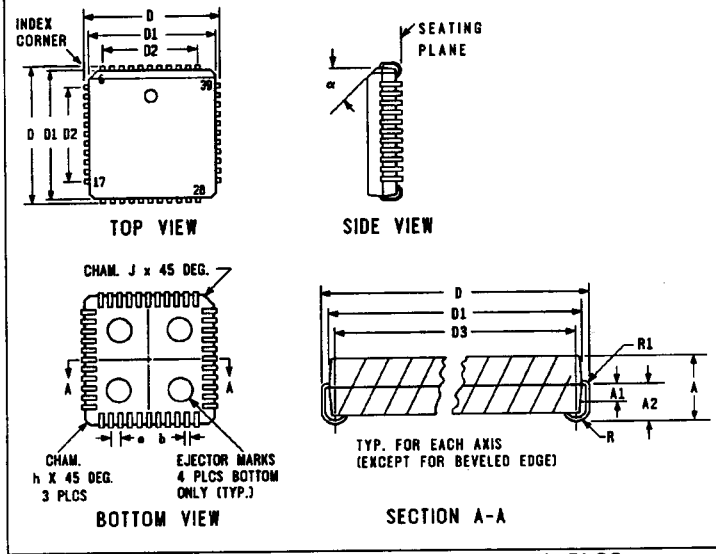
Parameter	Value
Operating Temperature	0°C to 60°C
Storage Temperature	–55°C to 85°C
Nominal Frequency @ 25°C	24.00014 MHz
Frequency Tolerance @ 25°C	±0.0015% (±15 PPM)
Temperature Stability @ T_A = 0°C to 60°C	±0.003% (±15 PPM)
Calibration Mode	Parallel resonant
Shunt Capacitance	7 pF max.
Load Capacitance	18 ±0.2 pF
Drive Level	2.5 mW max., Test at 20 nanowatts
Aging, per Year Max.	0.0005% (5PPM)
Oscillation Mode	Fundamental
Series Resistance	25 ohms max.
Max. Frequency Variation with 16.5 or 19.5 pF Load Capacitance	+0.0035% (+35 PPM)
Third Lead	Required
Sleeving	Required

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

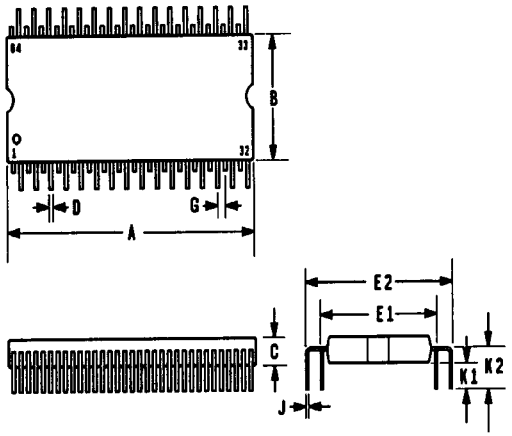
68-Pin PLCC



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	

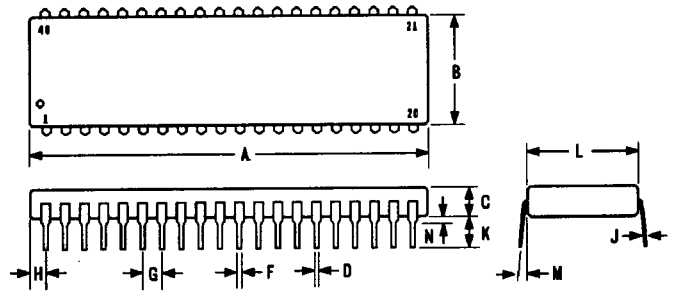
44-Pin PLCC

PACKAGE DIMENSIONS



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	41.10	41.61	1.618	1.638
B	17.02	17.23	0.670	0.690
C	3.56	4.58	0.140	0.180
D	0.46	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	2.92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0.210

64-Pin Plastic QUIP



DIM.	MILLIMETERS MIN.	MAX.	INCHES MIN.	MAX.
A	51.82	52.32	2.040	2.060
B	13.46	13.97	0.530	0.550
C	3.56	5.08	0.140	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

40-Pin Plastic DIP