

## RC4580 Dual Audio Operational Amplifier

### 1 Features

- $\pm 2\text{-V}$  to  $\pm 18\text{-V}$  Operating Voltage
- $0.8\text{-}\mu\text{V}_{\text{rms}}$  Low Noise Voltage
- 12-MHz Gain Bandwidth Product
- 0.0005% Total Harmonic Distortion
- $5\text{-V}/\mu\text{s}$  Slew Rate
- Drop-In Replacement for NJM4580
- Pin and Function Compatible with LM833, NE5532, NJM4558/9, and NJM4560/2/5 devices

### 2 Applications

- Audio Preamplifiers
- Active Filters
- Headphone Amplifiers
- Industrial Measurement Equipment

### 3 Description

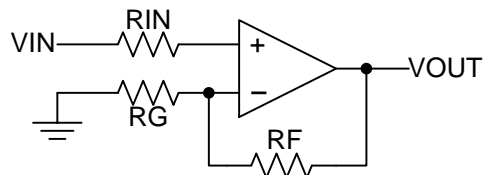
The RC4580 device is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. It offers low noise, high gain bandwidth, low harmonic distortion, and high output current, all of which make the device ideally suited for audio electronics, such as preamplifiers, active filters, and industrial measurement equipment. When high output current is required, the RC4580 device can be used as a headphone amplifier. Due to its wide operating supply voltage, the RC4580 device can also be used in low-voltage applications.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)   |
|-------------|-----------|-------------------|
| RC4580      | SOIC (8)  | 4.90 mm x 3.91 mm |
|             | TSSOP (8) | 3.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Noninverting Amplifier Schematic



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## 4 Revision History

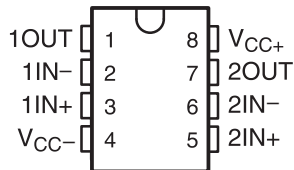
### Changes from Revision C (March 2004) to Revision D

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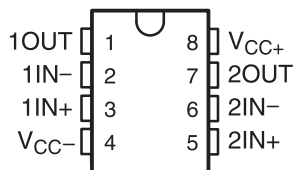
|  |          |
|--|----------|
| <ul style="list-style-type: none"> <li>Added <i>Applications</i>, <i>Device Information</i> table, <i>Pin Functions</i> table, <i>Handling Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> </ul> | <b>1</b> |
| <ul style="list-style-type: none"> <li>Removed <i>Ordering Information</i> table. ....</li> </ul>  | <b>1</b> |
| <ul style="list-style-type: none"> <li>Changed <math>T_A = 25^\circ\text{C}</math> to <math>T_A = -40^\circ\text{C}</math> to <math>125^\circ\text{C}</math> in condition statement for <i>Electrical Characteristics</i> table and <i>Operational Characteristics</i> table. ....</li> </ul>  | <b>5</b> |

## 5 Pin Configuration and Functions

**D PACKAGE  
SOIC – 8  
(TOP VIEW)**



**PW PACKAGE  
TSSOP – 8  
(TOP VIEW)**



### Pin Functions

| PIN              |     | I/O | DESCRIPTION        |
|------------------|-----|-----|--------------------|
| NAME             | NO. |     |                    |
| 1IN+             | 3   | I   | Noninverting input |
| 1IN-             | 2   | I   | Inverting Input    |
| 1OUT             | 1   | O   | Output             |
| 2IN+             | 5   | I   | Noninverting input |
| 2IN-             | 6   | I   | Inverting Input    |
| 2OUT             | 7   | O   | Output             |
| V <sub>CC+</sub> | 8   | —   | Positive Supply    |
| V <sub>CC-</sub> | 4   | —   | Negative Supply    |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|           |                            | MIN | MAX | UNIT |
|-----------|----------------------------|-----|-----|------|
| $V_{CC}$  | Supply voltage             |     | ±18 | V    |
| $V_I$     | Input voltage (any input)  |     | ±15 | V    |
| $V_{ID}$  | Differential input voltage |     | ±30 | V    |
| $I_O$     | Output current             |     | ±50 | mA   |
| $T_A$     | Ambient temperature range  | –40 | 125 | °C   |
| $T_{stg}$ | Storage temperature range  | –60 | 125 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 Handling Ratings

|             |                           | MIN  | MAX | UNIT |   |
|-------------|---------------------------|--|-----|------|---|
| $T_{stg}$   | Storage temperature range | –60  | 125 | °C   |   |
| $V_{(ESD)}$ | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 0   | 1000 | V |
|             |                           | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 0   | 1000 |   |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|           |                                 | MIN   | MAX  | UNIT |
|-----------|---------------------------------|-------|------|------|
| $V_{CC+}$ | Supply voltage                  | 2     | 16   | V    |
| $V_{CC-}$ |                                 | –2    | –16  |      |
| $V_{ICR}$ | Input common-mode voltage range | –13.5 | 13.5 | V    |
| $T_A$     | Operating free-air temperature  | –40   | 125  | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | RC4580                                       |        | UNIT |      |
|-------------------------------|--|--------|------|------|
|                               | D  | PW     |      |      |
|                               | 8 PINS                                       | 8 PINS |      |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 109    | 163  | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 55.7   | 38   |      |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 49     | 90.6 |      |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 10.6   | 1.3  |      |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 48.6   | 88.9 |      |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | —      | —    |      |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 Electrical Characteristics

$V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                                       | MIN      | TYP        | MAX | UNIT |
|--|---|----------|------------|-----|------|
| $V_{IO}$ Input offset voltage                            | $R_S = < 10\text{ k}\Omega$                           |          | 0.5        | 3   | mV   |
| $I_{IO}$ Input offset current                            |   |          | 5          | 200 | nA   |
| $I_{IB}$ Input bias current                              |   |          | 100        | 500 | nA   |
| $A_{VD}$ Large-signal differential voltage amplification | $R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$ | 90       | 110        |     | dB   |
| $V_{CM}$ Output voltage swing                            | $R_L \geq 2\text{ k}\Omega$                           | $\pm 12$ | $\pm 13.5$ |     | V    |
| $V_{ICR}$ Common-mode input voltage                      |   | $\pm 12$ | $\pm 13.5$ |     | V    |
| CMRR Common-mode rejection ratio                         | $R_S \leq 10\text{ k}\Omega$                          | 80       | 110        |     | dB   |
| $k_{SVR}$ Supply-voltage rejection ratio <sup>(1)</sup>  | $R_S \leq 10\text{ k}\Omega$                          | 80       | 110        |     | dB   |
| $I_{CC}$ Total supply current (all amplifiers)           |   |          | 6          | 9   | mA   |

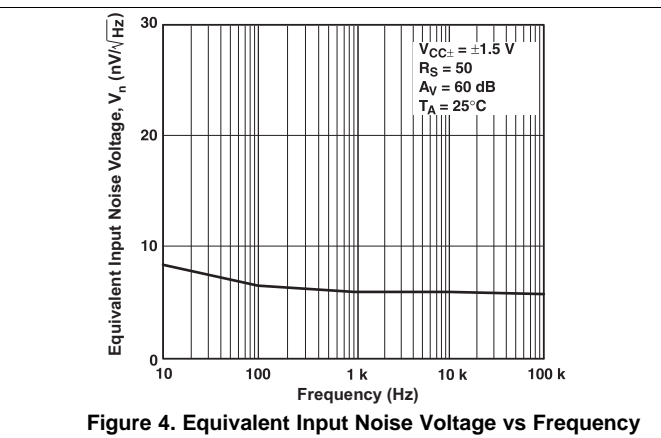
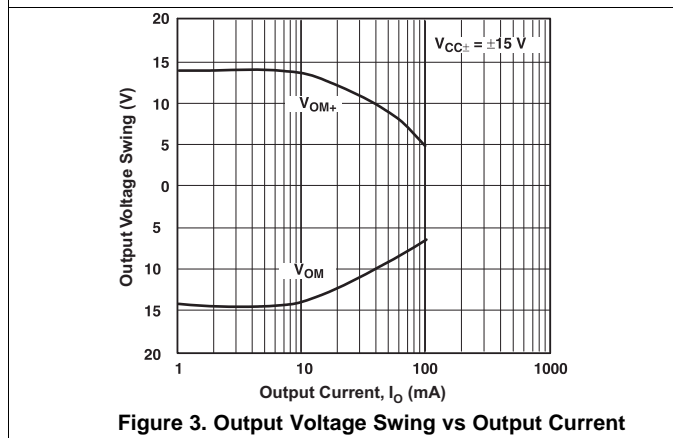
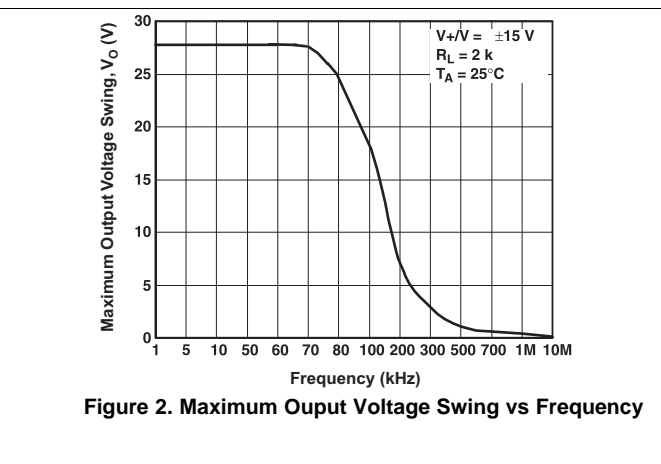
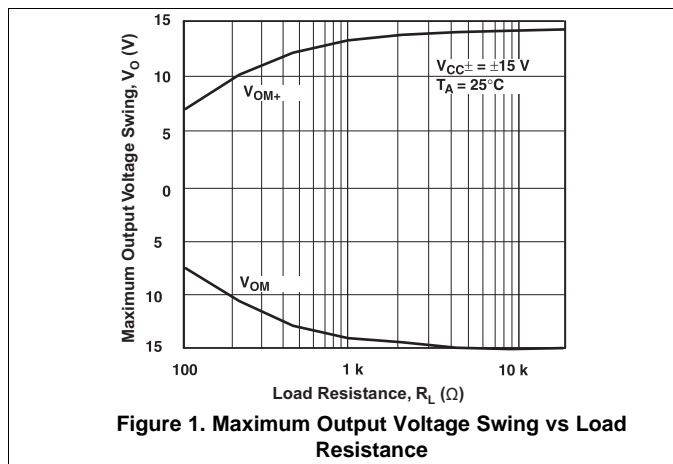
(1) Measured with  $V_{CC\pm}$  varied simultaneously

### 6.6 Operating Characteristics

$V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                            | TEST CONDITIONS  | TYP     | UNIT             |
|--------------------------------------|--|---------|------------------|
| SR Slew rate at unity gain           | $R_L \geq 2\text{ k}\Omega$  | 5       | V/ $\mu\text{s}$ |
| GBW Gain-bandwidth product           | $f = 10\text{ kHz}$  | 12      | MHz              |
| THD Total harmonic distortion        | $V_O = 5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $A_{VD} = 20\text{ dB}$ | 0.0005% |                  |
| $V_n$ Equivalent input noise voltage | RIAA, $R_S \leq 2.2\text{ k}\Omega$ , 30-kHz LPF   | 0.8     | $\mu\text{Vrms}$ |

### 6.7 Typical Characteristics



Typical Characteristics (continued)

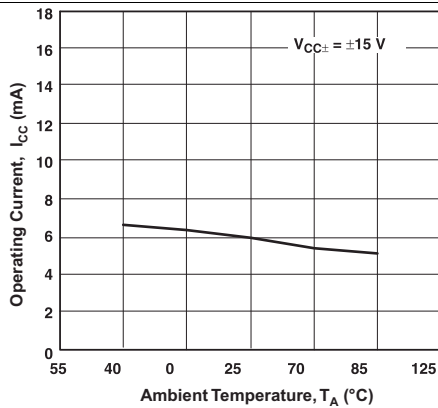


Figure 5. Operating Current vs Temperature

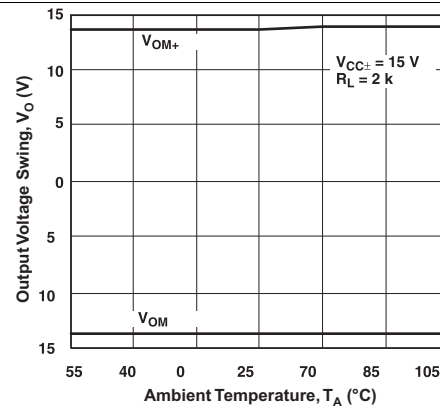


Figure 6. Output Voltage Swing vs Temperature

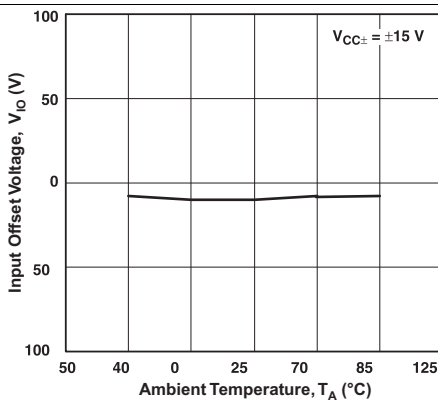


Figure 7. Input Offset Voltage vs Temperature

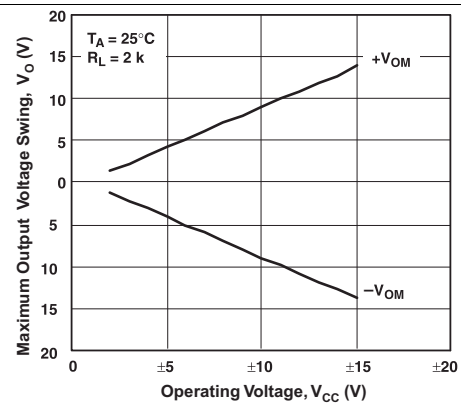


Figure 8. Input Bias Current vs Temperature

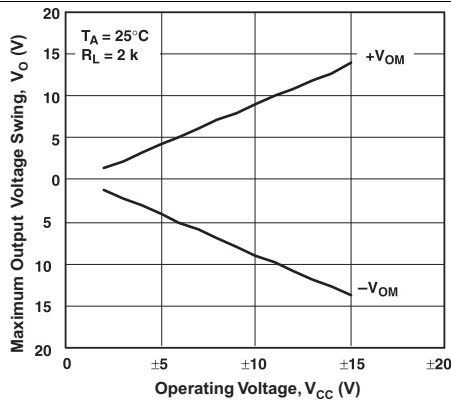


Figure 9. Maximum Output Voltage Swing vs Operating Voltage

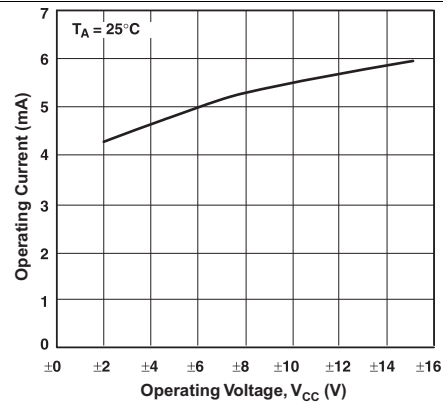


Figure 10. Operating Current vs Operating Voltage

Typical Characteristics (continued)

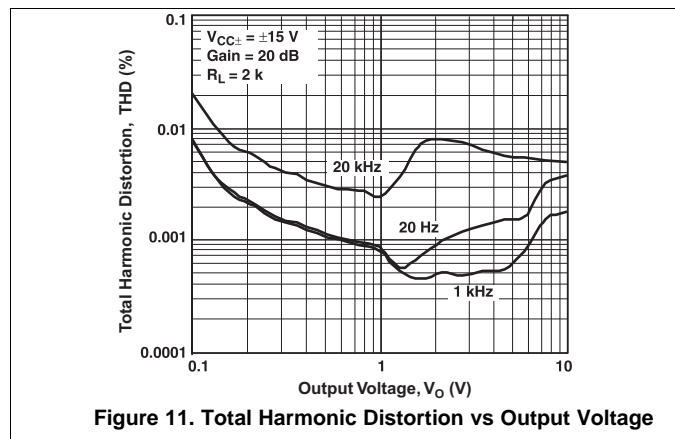


Figure 11. Total Harmonic Distortion vs Output Voltage

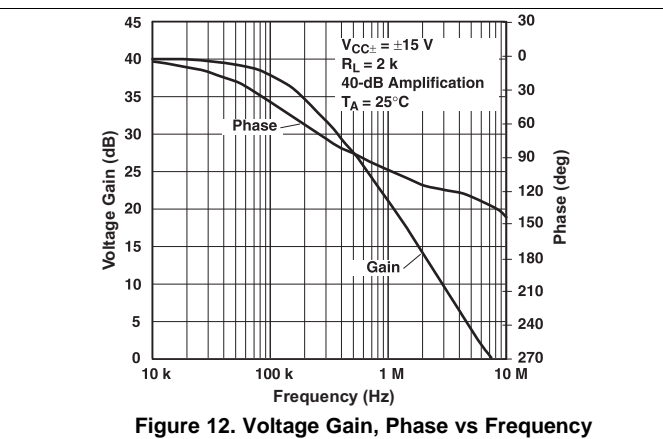


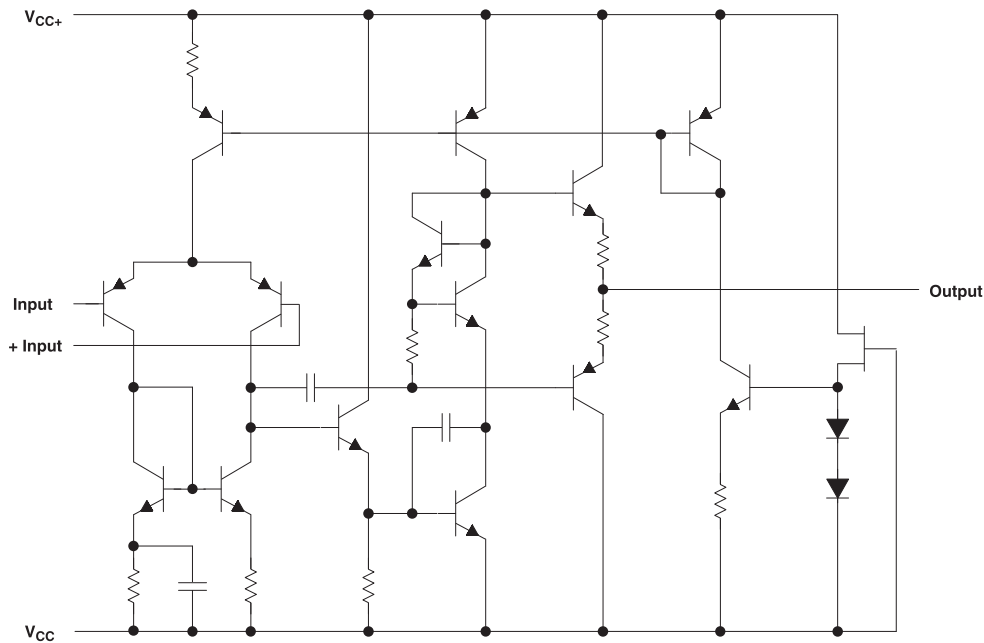
Figure 12. Voltage Gain, Phase vs Frequency

## 7 Detailed Description

### 7.1 Overview

The RC4580 device is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. It offers low noise, high gain bandwidth, low harmonic distortion, and high output current, all of which make the device ideally suited for audio electronics, such as preamplifiers, active filters, and industrial measurement equipment. When high output current is required, the RC4580 device can be used as a headphone amplifier. Due to its wide operating supply voltage, the RC4580 device can also be used in low-voltage applications.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The RC4580 device has a 12-MHz unity-gain bandwidth.

#### 7.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the RC4580 device is 110 dB.

#### 7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The RC4580 device has a 5-V/ms slew rate.

### 7.4 Device Functional Mode

The RC4580 device is powered on when the supply is connected. Each device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.



## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Typical Application

Some applications require differential signals. Figure 13 shows a simple circuit to convert a single-ended input of 2 V to 10 V into differential output of  $\pm 8$  V on a single 15-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage,  $V_{OUT+}$ . The second amplifier inverts the input and adds a reference voltage to generate  $V_{OUT-}$ . Both  $V_{OUT+}$  and  $V_{OUT-}$  range from 2 V to 10 V. The difference,  $V_{DIFF}$ , is the difference between  $V_{OUT+}$  and  $V_{OUT-}$ .

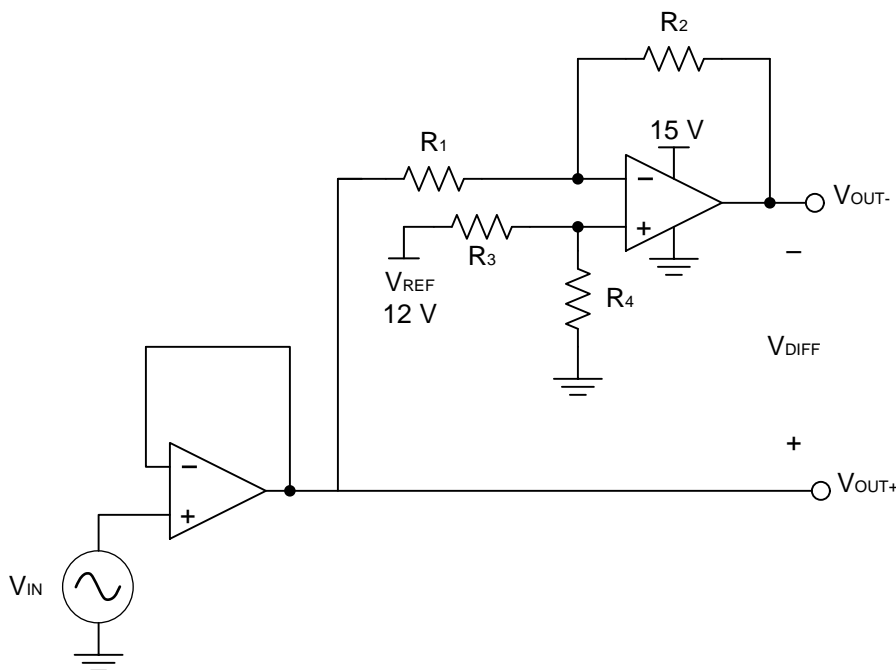


Figure 13. Schematic for Single-Ended Input to Differential Output Conversion

## Typical Application (continued)

### 8.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15 V
- Reference voltage: 12V
- Input: 2 V to 10 V
- Output differential:  $\pm 8$  V

### 8.1.2 Detailed Design Procedure

The circuit in [Figure 13](#) takes a single-ended input signal,  $V_{IN}$ , and generates two output signals,  $V_{OUT+}$  and  $V_{OUT-}$  using two amplifiers and a reference voltage,  $V_{REF}$ .  $V_{OUT+}$  is the output of the first amplifier and is a buffered version of the input signal,  $V_{IN}$  (see [Equation 1](#)).  $V_{OUT-}$  is the output of the second amplifier which uses  $V_{REF}$  to add an offset voltage to  $V_{IN}$  and feedback to add inverting gain. The transfer function for  $V_{OUT-}$  is [Equation 2](#).

$$V_{OUT+} = V_{IN} \quad (1)$$

$$V_{OUT-} = V_{REF} \times \left( \frac{R_4}{R_3 + R_4} \right) \times \left( 1 + \frac{R_2}{R_1} \right) - V_{IN} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal,  $V_{DIFF}$ , is the difference between the two single-ended output signals,  $V_{OUT+}$  and  $V_{OUT-}$ . [Equation 3](#) shows the transfer function for  $V_{DIFF}$ . By applying the conditions that  $R_1 = R_2$  and  $R_3 = R_4$ , the transfer function is simplified into [Equation 6](#). Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the  $V_{REF}$ . The differential output range is  $2 \times V_{REF}$ . Furthermore, the common mode voltage will be one half of  $V_{REF}$  (see [Equation 7](#)).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left( 1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left( \frac{R_4}{R_3 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{cm} = \left( \frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \quad (7)$$

#### 8.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because the RC4580 device has a bandwidth of 12 MHz, this circuit will only be able to process signals with frequencies of less than 12 MHz.

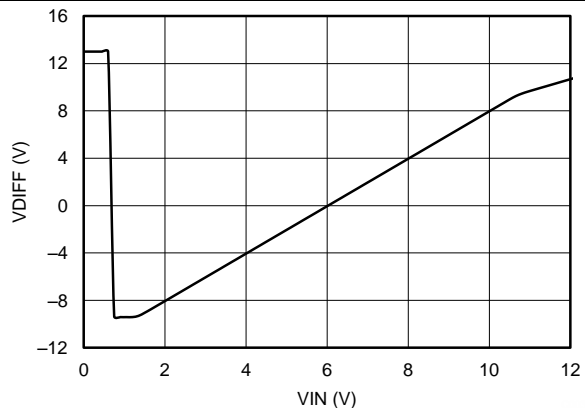
#### 8.1.2.2 Passive Component Selection

Because the transfer function of  $V_{OUT-}$  is heavily reliant on resistors ( $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$ ), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 k $\Omega$  with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6 k $\Omega$  or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

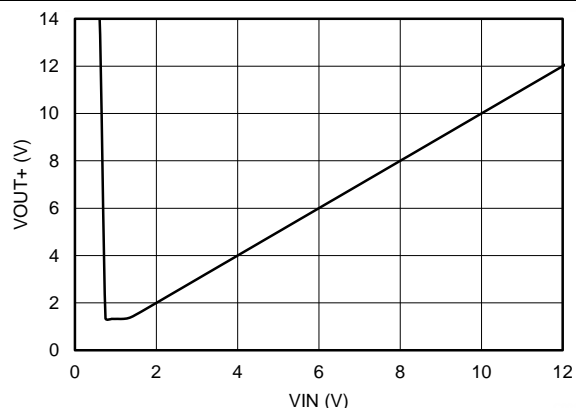
## Typical Application (continued)

### 8.1.3 Application Curves

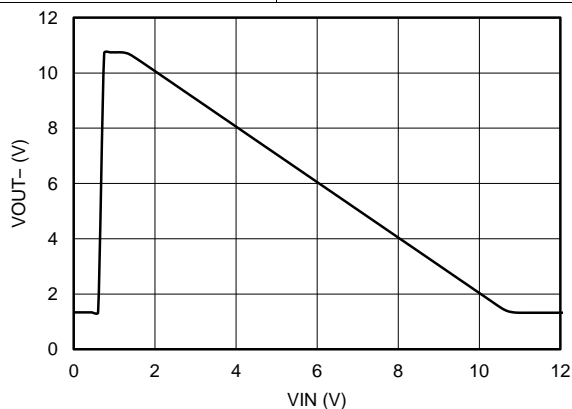
The measured transfer functions in [Figure 14](#), [Figure 15](#), and [Figure 16](#) were generated by sweeping the input voltage from 0 V to 12 V. However, this design should only be used between 2 V and 10 V for optimum linearity.



**Figure 14. Differential Output Voltage vs Input Voltage**



**Figure 15. Positive Output Voltage vs Input Voltage**



**Figure 16. Positive Output Voltage vs Input Voltage**

## 9 Power Supply Recommendations

The RC4580 device is specified for operation over the range of  $\pm 2$  to  $\pm 16$  V; many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages outside of the  $\pm 18$  V range can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 10.2 Layout Example

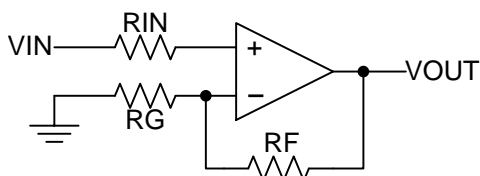


Figure 17. Operational Amplifier Schematic for Noninverting Configuration

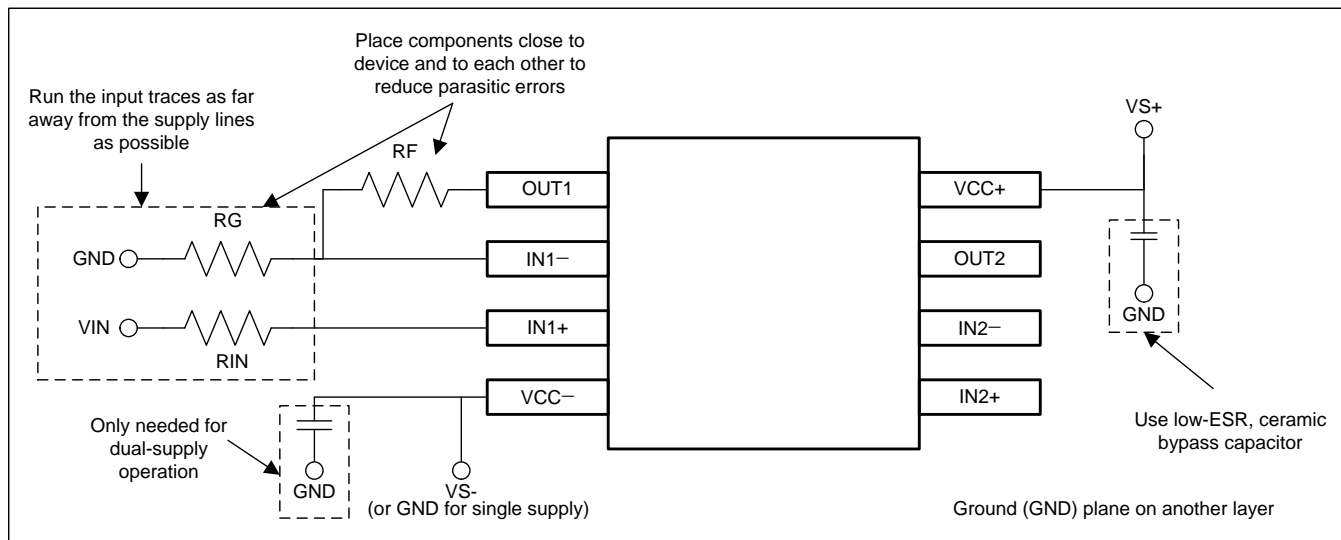


Figure 18. Operational Amplifier Board Layout for Noninverting Configuration

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| RC4580ID         | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | R4580I                  | <a href="#">Samples</a> |
| RC4580IDR        | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | R4580I                  | <a href="#">Samples</a> |
| RC4580IDRG4      | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | R4580I                  | <a href="#">Samples</a> |
| RC4580IP         | ACTIVE        | PDIP         | P               | 8    | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | RC4580IP                | <a href="#">Samples</a> |
| RC4580IPW        | ACTIVE        | TSSOP        | PW              | 8    | 150         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | R4580I                  | <a href="#">Samples</a> |
| RC4580IPWR       | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | R4580I                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF RC4580 :**

- Automotive: [RC4580-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| RC4580IDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| RC4580IDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| RC4580IPWR | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| RC4580IDR  | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| RC4580IDR  | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| RC4580IPWR | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

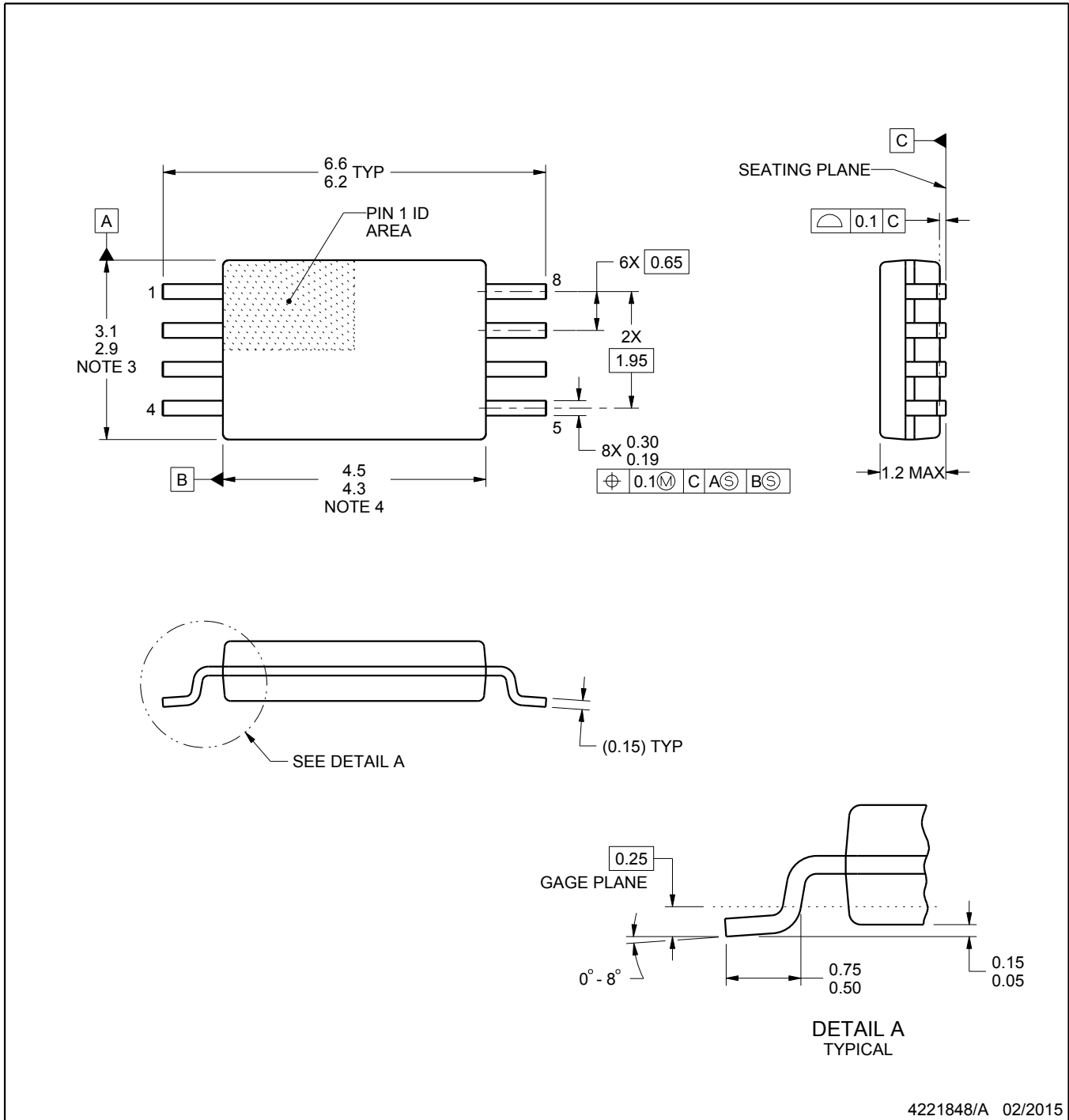
PW0008A



# PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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