RC5033

Adjustable Synchronous DC-DC Converter

Features

- >85% Efficiency
- 350uA quiescent current in shutdown
- Fast transient response
- Soft control power-up
- Over-Voltage Protection
- Output voltage range from 2.0V to 3.6V
- Factory trimmed low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFETs
- 16 pin SOIC package

Applications

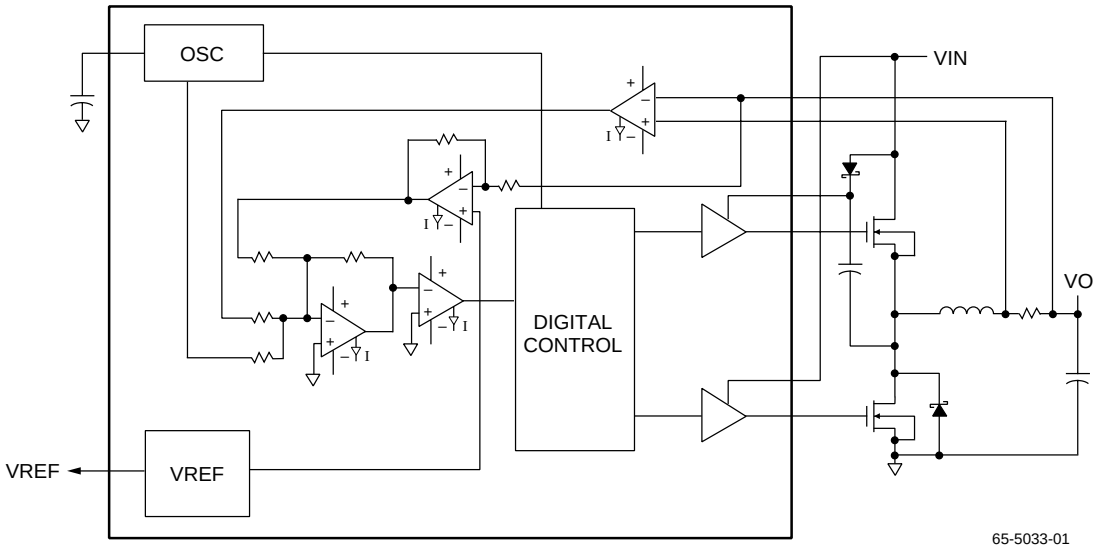
- 3.3V power supply for Pentium™ based CPU motherboards
- 3.45V power supply for AMD-K5™ CPU
- 2.5V or 3.6V power supply for PowerPC™

Preliminary Information

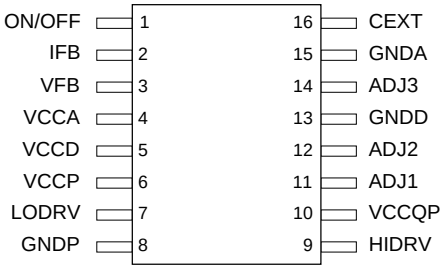
Description

The RC5033 is a synchronous mode DC-DC controller IC dedicated to providing a 5V to 2.0V up to 3.6V conversion for various types of CPU power . It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 10 Amps. The RC5033 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. Through the use of external resistors, the RC5033 can generate accurate output voltages from 2.0V up to 3.6V. An integrated Over-Voltage protection function constantly monitors the output voltage and shuts down the power to the CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

Block Diagram



Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
On/Off	1	A low level on this pin will power down; tie to VCCD if not used.
IFB	2	Current Feedback Input.
VFB	3	Voltage Feedback Input.
VCCA	4	Analog VCC.
VCCD	5	Digital VCC.
VCCP	6	VCC for synchronous FET output drivers.
LODRV	7	Synchronous FET driver output.
GNDP	8	Power ground for high current drivers.
HIDRV	9	High side FET driver output.
VCCQP	10	VCC for High side FET output driver
ADJ1	11	VREF adjust pin.[1]
ADJ2	12	VREF adjust pin.[1]
GNDD	13	Digital ground.
ADJ3	14	VREF adjust pin.[1]
GNDA	15	Analog ground.
CEXT	16	External capacitor for setting oscillator frequency.

Note:
1. See voltage adjust table for function

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Output Voltage Selection Table

VOUT	ADJ1	ADJ2	ADJ3
3.5V	N/C	N/C	N/C
3.35V	N/C	[2]	[2]
3.3V	[2]	N/C	[2]
2.9V[1]	3.9K	N/C	N/C
2.5V[1]	2K	N/C	N/C
2.0V[1]	39Ω	N/C	N/C

Note:
1. See Figure 3 for resistor connection.
2. Indicated short pins together.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Conditions	Min	Typ	Max	Units
V_{CCP}	Driver Voltage				13	V
V_{CCQP}	High Driver Supply				13	V
T_J	Junction Temperature				175	°C
T_A	Ambient Operating Temperature		0		70	°C
T_S	Storage Temperature		-65		150	°C
T_L	Lead Soldering Temperature	(10 seconds)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	7	V
V_{CCP}	Low Driver Supply		4.5	5	12	V
V_{CCQP}	High Driver Supply		9		13	V
V_{IH}	Input Voltage, Logic HIGH		2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V

DC Electrical Characteristics

(V_{CC} = 5V, fosc = 650 KHz, and T_A = +25˚C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
V_O	Output Voltage	Nominal, Pin 12 conn. Pin 14, T_A = 0–70°C	3.135	3.3	3.465	V
I_O	Output Current	See Figure for application		5		A
Vref Acc	Voltage Reference Accuracy			1		%
VTC	Output Voltage Tempco			-40		ppm
LDR	Load Regulation	0.5 to 7A		1		%Vo
LIR	Line Regulation	V_{CC} = ±5%		0.14		%Vo
V_R	Output Voltage Ripple			30		mV
Cum Acc	Cumulative Accuracy[2]	T_A = 0–70°C		3		%
Eff	Efficiency	Synchronous mode > 1A	80	85		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
PD	Power Dissipation			0.1	0.2	W

Notes:

1. Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.
2. Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

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AC Electrical Characteristics[1]

(T_A = +25˚C unless otherwise noted)

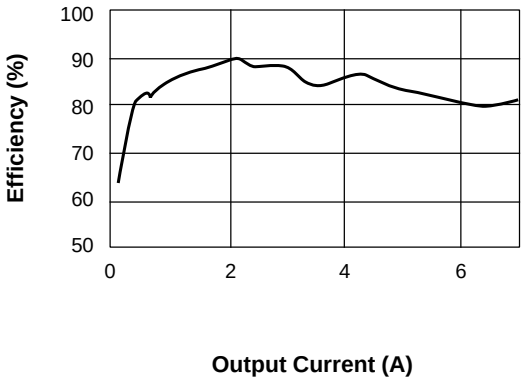
Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	Il=0.5A to 5.5A		10		µs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Imax	Imax Threshold			30		mV
Iscp	Short Circuit Prot			80		mV
Ovp	Over Voltage Prot			20		%Vo
Trimax	Response to Imax			15	30	ns
Tssp	Soft start response			10		µs

Note:

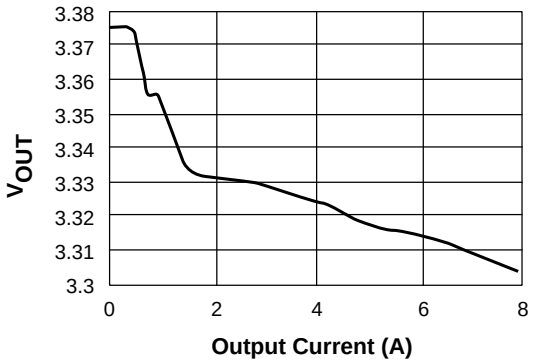
1. Guaranteed by design, not 100% total.

Typical Operating Characteristics[1]

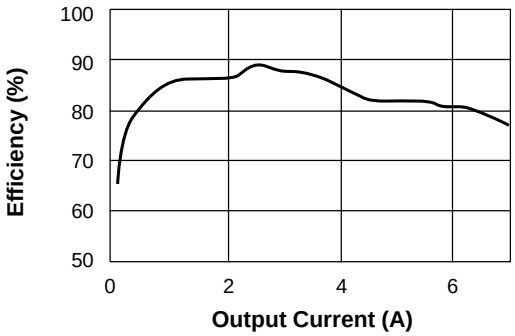
Efficiency vs Output Current (F_{OSC} = 400 KHz)



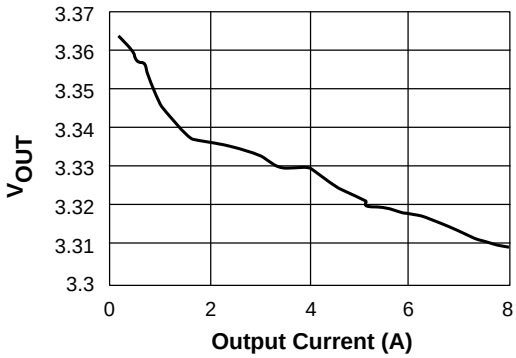
Load Regulation (F_{OSC} = 400 KHz)



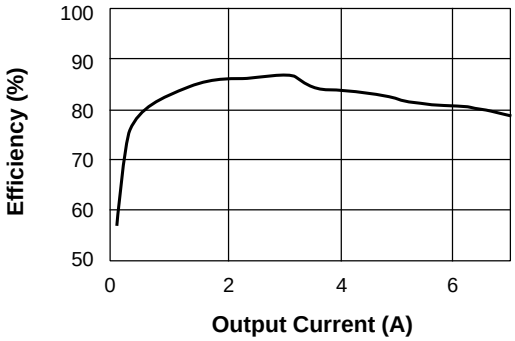
Efficiency vs Output Current (F_{OSC} = 650 KHz)



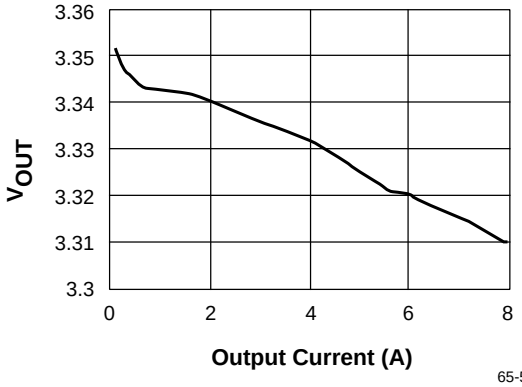
Load Regulation (F_{OSC} = 650 KHz)



Efficiency vs Output Current (F_{OSC} = 1 MHz)



Load Regulation (F_{OSC} = 1 MHz)



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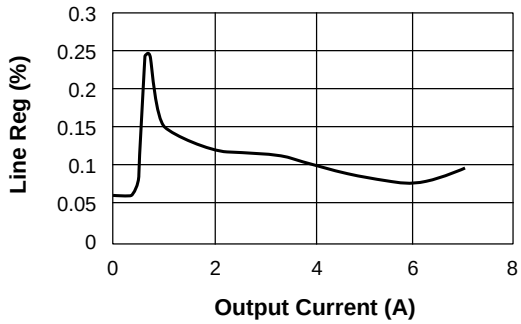
Note:

1. Data taken with circuit of Figure 1.

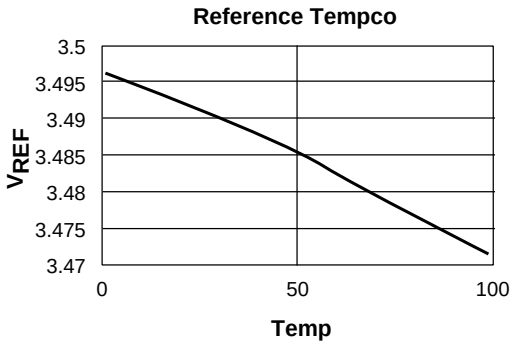
Preliminary Information

Typical Operating Characteristics (continued)

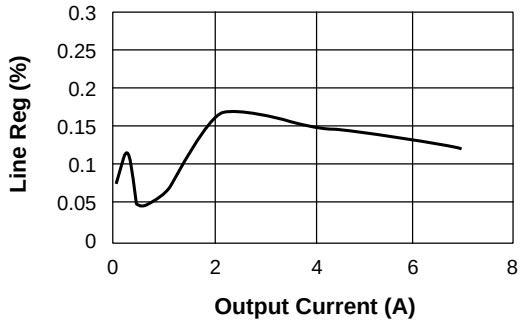
Line Regulation vs. Output Load (F_{OSC} = 400 KHz)



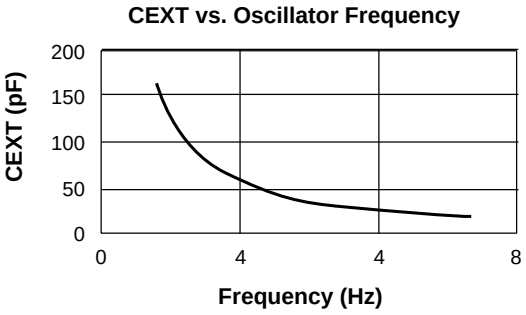
Reference Tempco



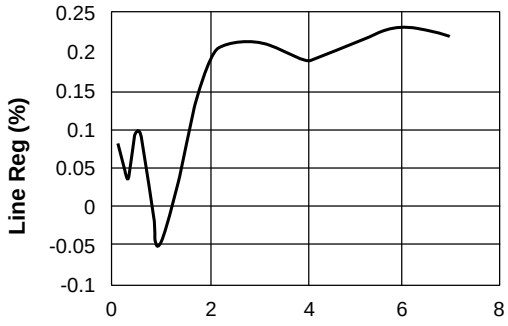
Line Regulation vs. Output Load (F_{OSC} = 650 KHz)



CEXT vs. Oscillator Frequency



Line Regulation vs. Output Load (F_{OSC} = 1 MHz)



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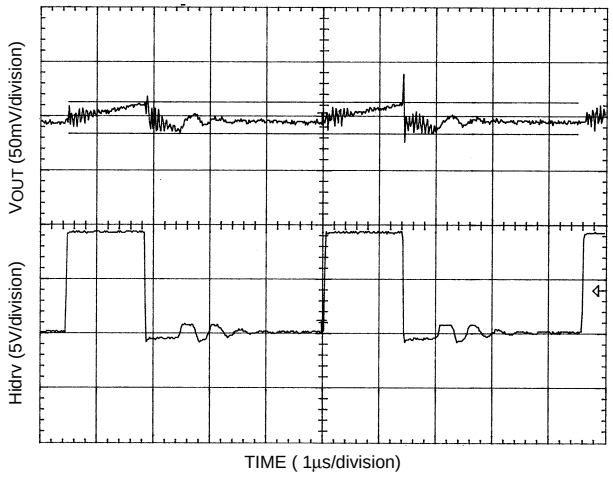
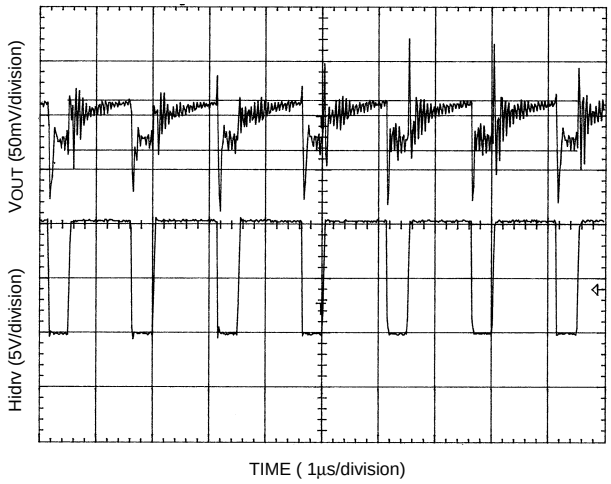
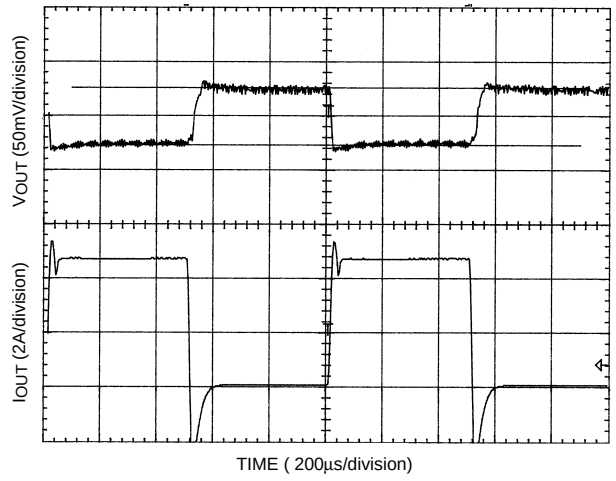
Typical Operating Characteristics (continued)



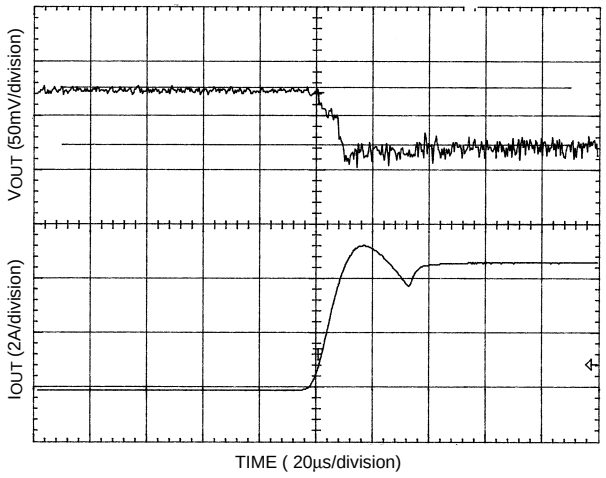
AC Ripple response .2A Load



AC Ripple response 5A Load



Transient Response .2A to 5A Load



Transient Response Magnified

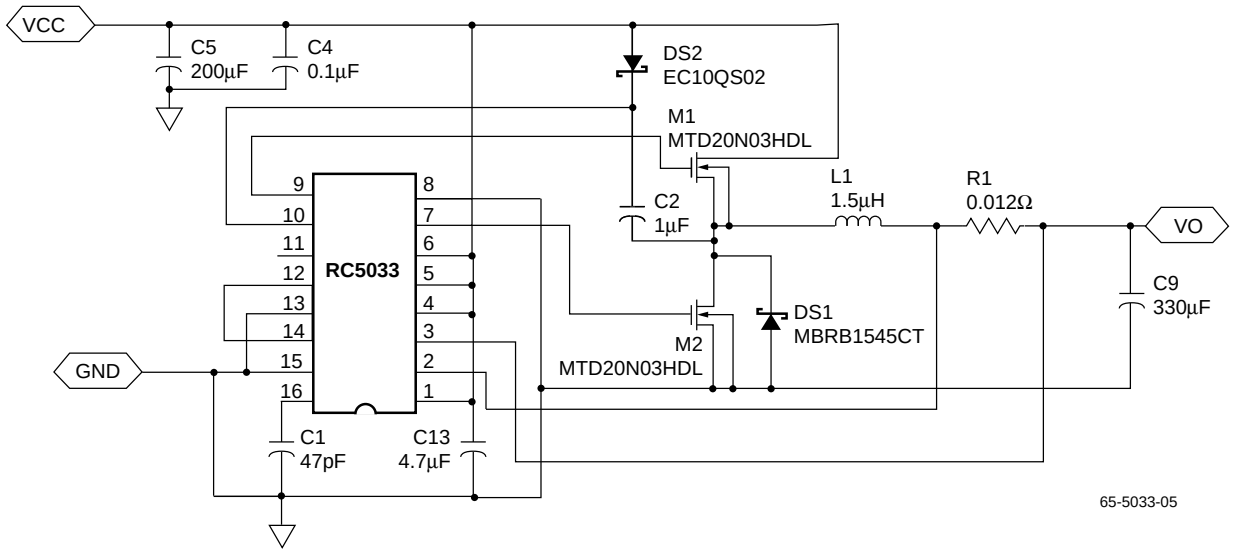


Figure 1. Standard 7A Application Schematic

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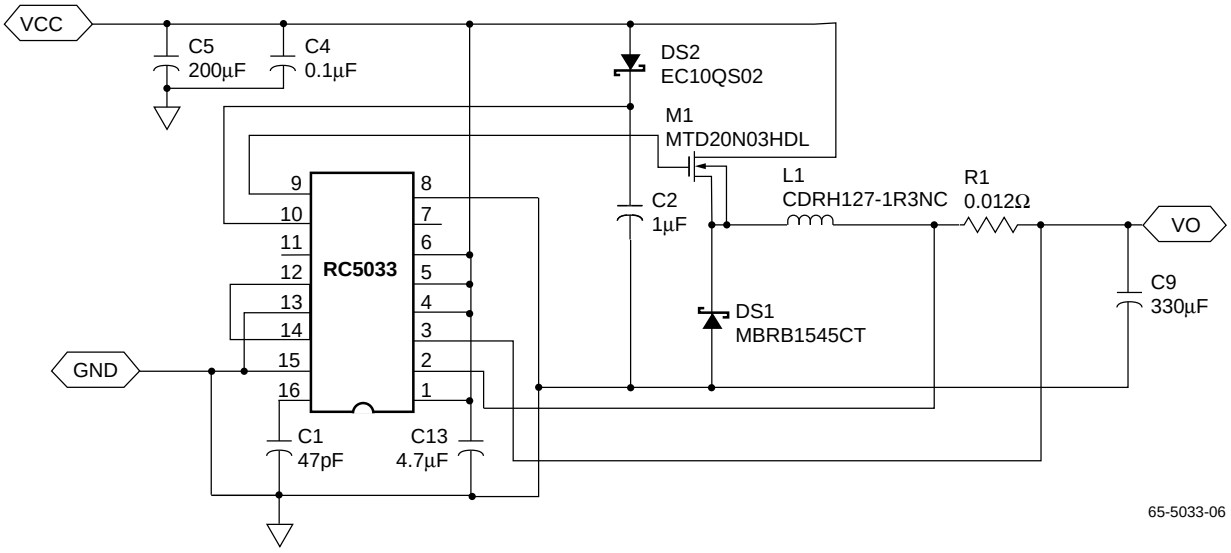

Figure 2. Non-Synchronous 7A Application Circuit

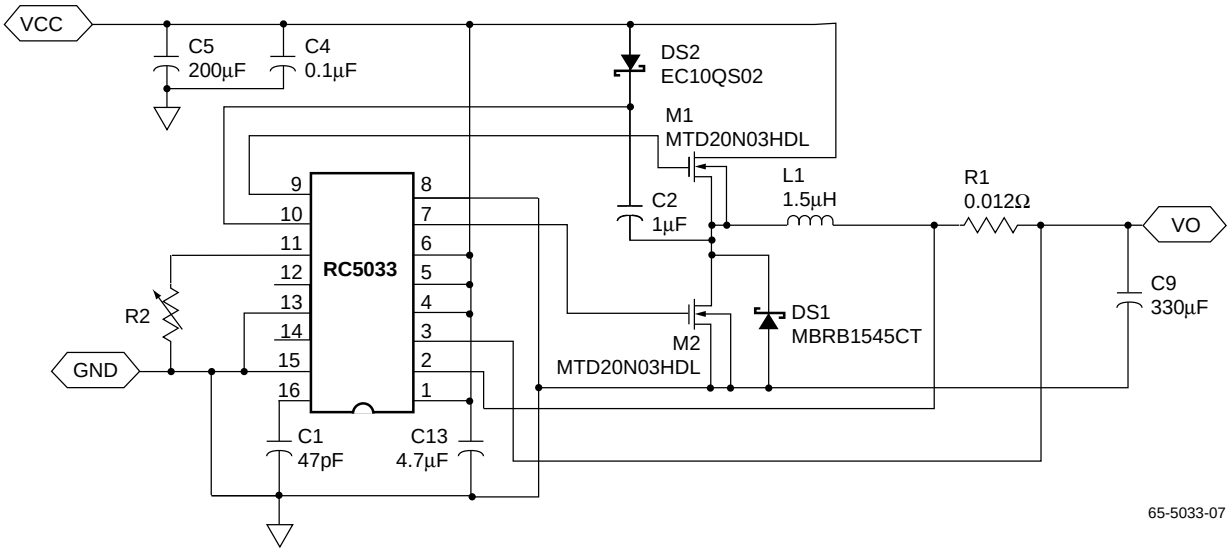

Figure 3. Adjustable Voltage DC-DC Converter

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RC5033 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	LRC-2512	IRC
C5	1	OS-CON 10SA220M	Sanyo
C9	1	OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C4	2	0.1uF	SMD Cap

Table 1. Components for RC5033

RC5033 Alternate Suppliers of Components			
Ref Designator	Quantity	Alternate Part No.	Alternate Manufacturer
L1	1	PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
		Si4410DY	Temic (Siliconix)
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	WSL-2512	DALE
C5	1		
C9	1		

Table 2. Alternate Components Selection

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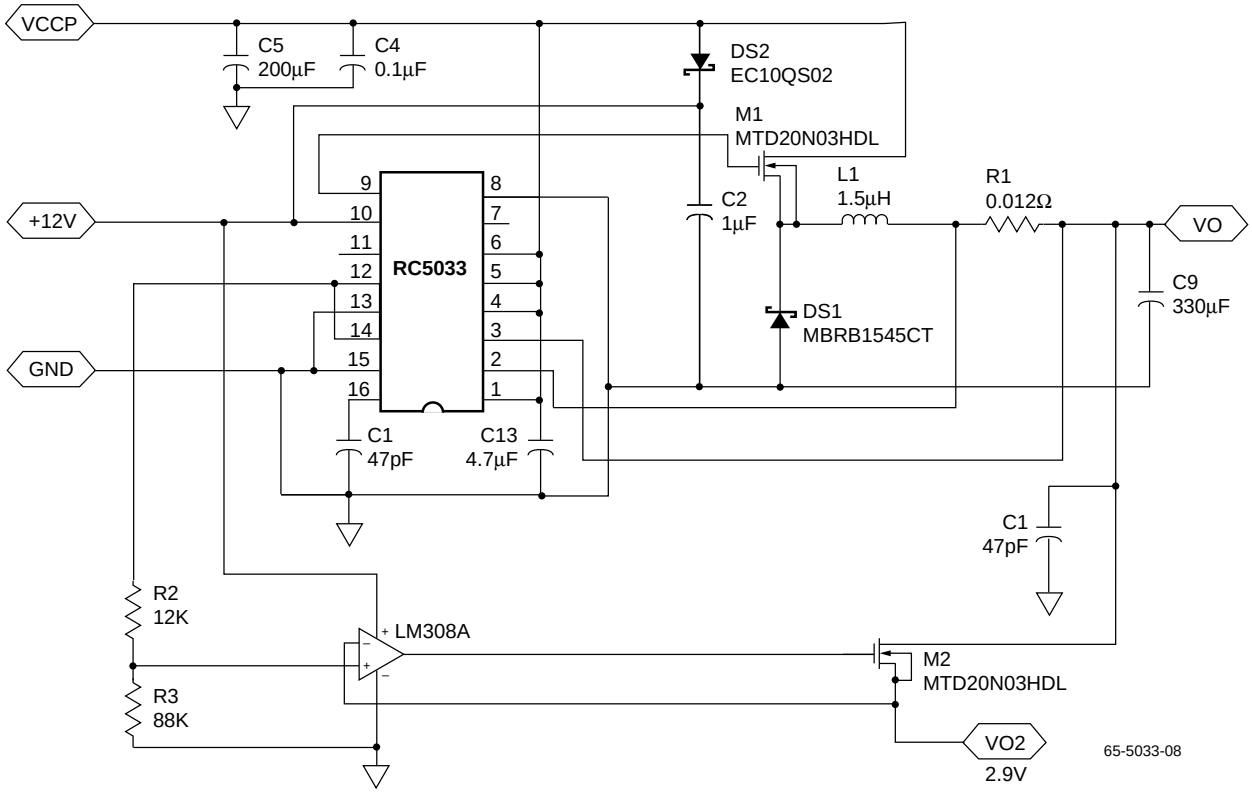
Applications Discussion



Dual Power Supply Application

In some CPU power applications there may be a need for a split voltage converter. The circuit in Figure 4 addresses this need with only minimal component count. The basic RC5033 non-synchronous DC-DC converter is augmented with an op-amp, a power MOSFET, and some 1% resistors to provide a dual power supply with one voltage set to 3.3V and the other, slaved off of the 3.3V, set to 2.9V. In this configuration, the RC5033 converts the 5V to 3..3V with high efficiency. By using the op-amp, power FET, and the resistors, a low-dropout linear regulator is realized that can be run off of the 3.3V. The 2.9V linear regulator has a relatively high efficiency just due to the fact that the ratio of 2.9V/3.3V is close to 88%. The power FET is a low Rdson n-channel MOSFET, and thus it is reasonably inexpensive. The opamp can be a garden variety, though the input bias current and output slew rate need to be considered to optimize accuracy and transient response. The overall efficiency of this power supply system will very much depend upon the percentage of power used on each power output. Overall, the efficiency of this system will be lower than if both supplies were implemented as switchers; however, the added savings of the part count reduction may more than compensate for the overall lower efficiency.

Standard Application Circuit

The circuit shown in Figure 1 along with its components and values has been designed as representative of the typical application involving the RC5033 for a Pentium™ CPU. Use of the standard application circuit will deliver the performance curves shown under the Typical Operating Characteristics section of the data sheet. Many users will want to develop their own DC-DC converter solution that is uniquely tailored to a specific application requirement. In that case, the users should review the detailed information in the Design Procedure and Applications Information section of the data sheet.

Detailed Description

The RC5033 is a programmable voltage synchronous controller. When designed around the appropriate external components, it can be configured to deliver more than 10A of output current. During heavy loading conditions the RC5033 functions as a current-mode PWM step down regulator. Under light loading conditions, the regulator functions in the PFM or pulse skipping mode, thereby increasing its efficiency under light loads.

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB(current feedback) and VFB(voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5033 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5033 to clock up to speeds greater then 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5033 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to 2*VCC - Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET that will be needed for achieving a low Rdson. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5033 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For applications that require a voltage other than the voltages provided by the fixed jumper connections, an external resistor will change the reference voltage from 2.0V up to 3.6V. For a guaranteed stable operation under all loading conditions, a 0.1µF capacitor is recommended on the VREF output pin.

Over -Voltage Protection

The RC5033 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5033 will shut down the output drive signals to the power FETs.

Oscillator

The RC5033 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5033. The oscillator frequency con be set from less than 200KHz to over 1MHz depending on the application requirements.

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 4 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5033 in Figure 1. In Figure 5, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage VB is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: IL=(VB- Vo)Ton/L; where Ton is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: IL=Vo(T – Ton)/L; where T- Ton is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: Vo= VB(Ton/T).

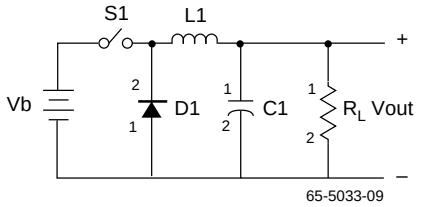


Figure 5. Simple Buck DC-DC Converter

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Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade- offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*Rl.

The value of the inductor is a function of the switching frequency (Ton) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_O T_{ON}\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} - V_D}\right) + 1}$$

Where: Fo is the desired clock frequency
Ton is the max on time of the M1 FET
Vd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN} - V_{DSON}}{I_{MAX}}(T_{ON})$$

Where: Vdson is the voltage across the drain-source of the M1 FET when switched on.
(this can be calculated by RDSon * Imax)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5033 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5033 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

R = 100 mV/ Ipeak

Where: Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the miliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5033 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 5. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5033. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low “ESR” capacitors are best suited for this application and can have an influence on the converter’s efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: ESR = Pd/2pfC. Where Pd is the capacitor’s dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C(\mu F) = \frac{T_{ON}\left(\frac{(V_{IN} - V_{OUT})I_{MAX}}{V_{OUT}} + I_L\right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5033 to be bootstrapped up to

9V by using the bootstrap capacitor C2. When the lower FET M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is Vin - Vd. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is 2Vin - Vd. The voltage then that is applied to the gate of the FET is VCCQP - Vsat, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5033. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the Rdson of M1 even lower by increasing its Vgs.

MOSFET Switches

The MOSFET switches in the RC5033 applications circuit are N-channel “logic-level” FETs. This means that they will be fully on with a Vgs of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest RDSon at the given Imax current level. The value of RDSon directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5033. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn’t necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5033.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuos ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5033 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, ADJ3, ADJ1, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 6.

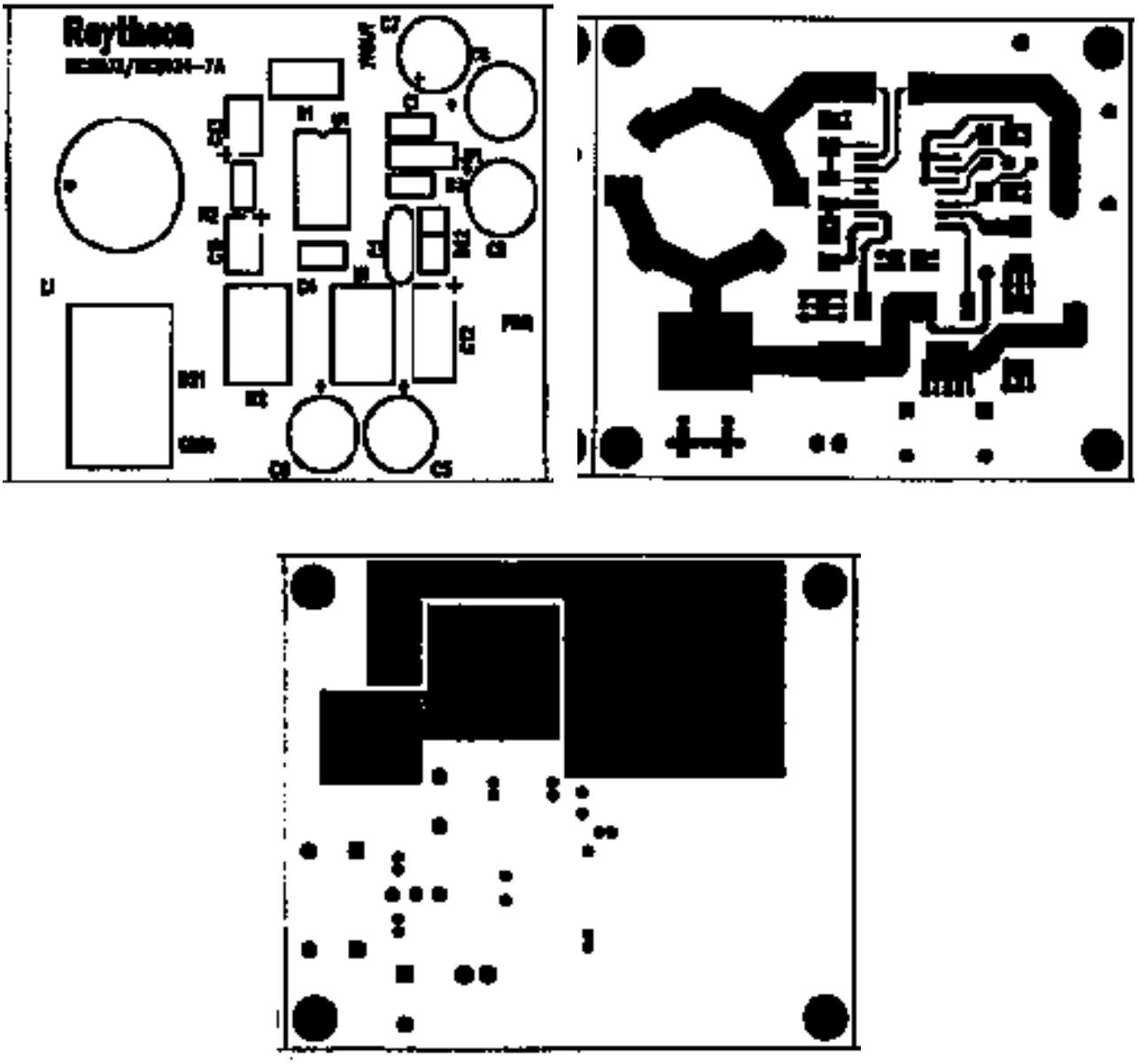


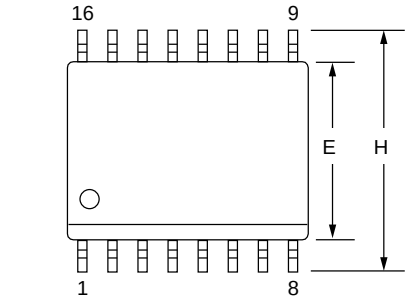
Figure 6. Sample PCB Layout

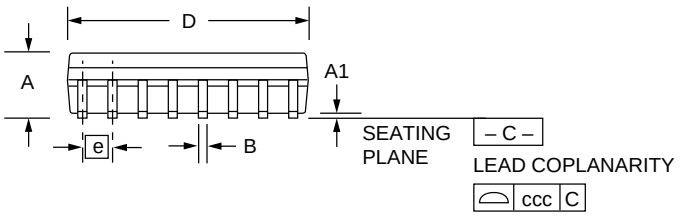
Mechanical Dimensions – 16-Lead SOIC Package

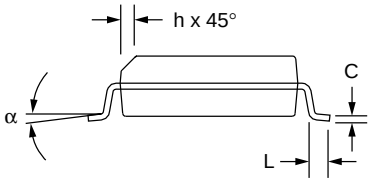
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package	θJA
RC5033M	16 SOIC	85°C/W

Preliminary Information

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