RC5042

Programmable DC-DC Converter

Features

- Programmable output from 2.1V to 3.5V using integrated 4-bit DAC
- 87% efficiency
- Oscillator frequency adjustable from 200KHz to 1MHz
- On-chip Power Good function
- Excellent transient response
- Over-Voltage Protection
- Short Circuit Protection
- Precision trimmed low TC voltage reference
- 16 pin SOIC package
- Meets Intel Pentium® Pro VRM specifications using minimum number of external components

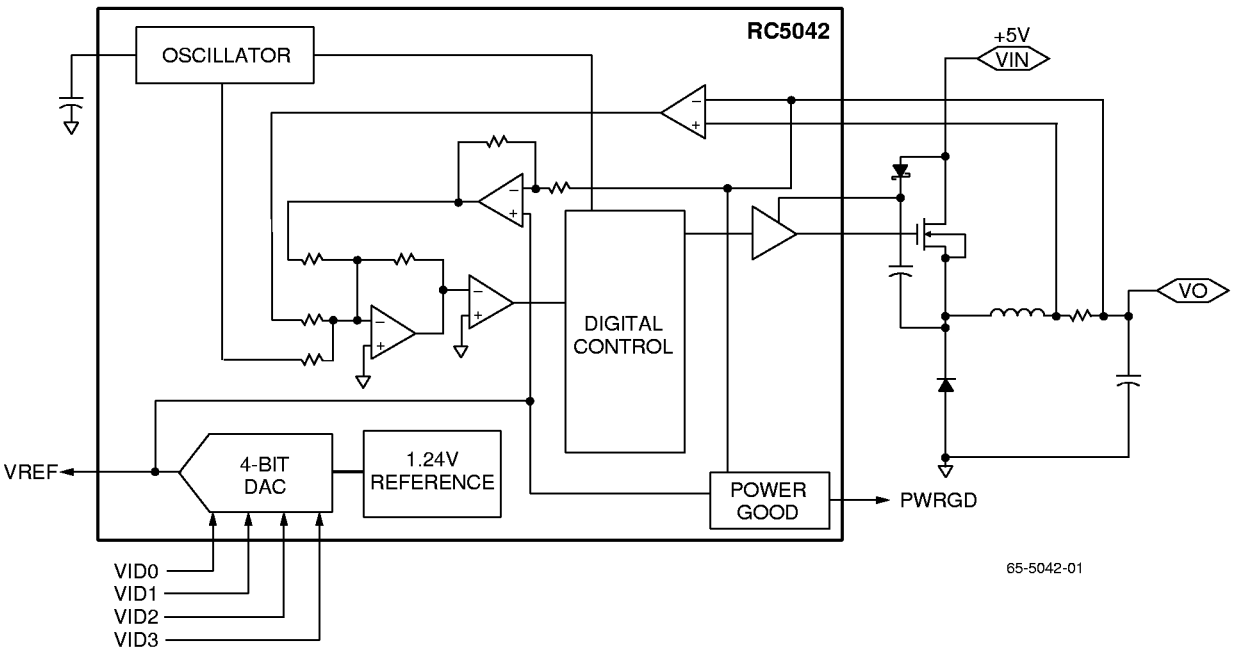
Applications

- Programmable power supply for Pentium Pro and Pentium-based CPU motherboards
- VRM module for Pentium Pro CPU
- Programmable power supply for high current microprocessors

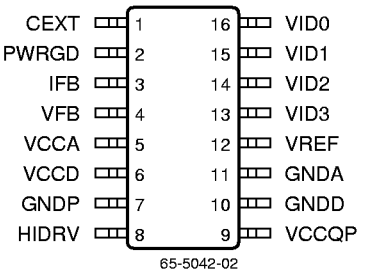
Description

The RC5042 is a non-synchronous DC-DC controller IC which provides an accurate, programmable output for Pentium Pro CPU applications. Using an integrated 4-bit DAC to accept a voltage identification (VID) code directly from the CPU, the RC5042 can generate precise output voltages between 2.1V and 3.5V in 100mV increments. Output load currents in excess of 12A can be delivered using minimal external circuitry. The RC5042 is designed to operate in a standard PWM control mode under heavy load conditions and in PFM control mode while supplying light loads for optimal efficiency. An on-board precision low TC voltage reference eliminates the requirement for external components in order to achieve tight voltage regulation. The Pentium Pro CPU is continuously protected by an integrated Power Good function, which sends an active-low interrupt signal to the CPU in the event that the output voltage is out of tolerance. The internal oscillator can be programmed to operate over a range of 200KHz to 1MHz to allow flexibility in choosing external components.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator capacitor connection.** Connecting an external capacitor to this pin sets the internal oscillator frequency from 200 KHz to 1 MHz. Layout of this pin is critical to system performance. See Application Information for details.
2	PWRGD	**Power Good output flag.** Open collector output will be at logic HIGH under normal operation. Logic LOW indicates output voltage is not within ±10% of nominal.
3	IFB	**High side current feedback.** Pins short 4 and 5 are used as the inputs for the current feedback control loop and as the short circuit current sense points. Layout of these traces is critical to system performance. See Application Information for details.
4	VFB	**Voltage feedback.** Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. Layout of this trace is critical to system performance. See Application Information for details.
5	VCCA	**Analog V_{CC}.** Connect to system 5V supply and decouple to ground with 0.1μF ceramic capacitor.
6	VCCD	**Digital V_{CC}.** Connect to system 5V supply and decouple to ground with 4.7μF tantalum capacitor.
7	GNDP	**Power ground.** Return pin for high currents flowing in pins 8 and 9 (HIDRV and VCCQP). Connect to low impedance ground. See Application Information for details.
8	HIDRV	**FET driver output.** Connect this pin to the gate of the N-channel MOSFETs M1 and M2 in Figures 1 and 2. The trace from this pin to the MOSFET gates should be kept as short as possible (less than 0.5"). See Application Information for details.
9	VCCQP	**Power V_{CC} for FET Driver.** VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (M1). See Application Information for details.
10	GNDD	**Digital ground.** Return path for digital logic. This pin should be connected to system ground so that ground loops are avoided. See Application Information for details.
11	GNDA	**Analog ground.** Return path for low power analog circuitry. Connect to system ground so that ground loops are avoided. See Application Information for details.
12	VREF	**Reference voltage test point.** This pin provides access to the DAC output and should be decoupled to ground using a 0.1μF capacitor. No load should be connected to this pin.
13–16	VID3–VID0	**Voltage identification (VID) code inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Internal 10KΩ pull-up resistors assure correct operation if pins are left unconnected.

Absolute Maximum Ratings[1]

Control Supply Voltages, VCCA and VCCD	13V
FET Supply Voltage, VCCQP	13V
Voltage Identification Code Inputs, VID3-VID0	13V
Junction Temperature, T_J	150˚C
Storage Temperature, T_S	-65 to 150˚C
Lead Soldering Temperature, 10 seconds	300˚C

Notes:

1. Functional operation under any of these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Control Supply Voltages, VCCA and VCCD		4.5	5	7	V
Driver Supply Voltage, VCCQP		9	10	12	V
VID Code Input Voltage, Logic HIGH		2			V
VID Code Input Voltage, Logic LOW				0.8	V
PWRGD HIGH Threshold				+7	%VREF
PWRGD LOW Threshold		-7			%VREF
Ambient Temperature, T_A		0		70	°C

Electrical Specifications

(V_{CCA}, V_{CCD} = 5V, f_{osc} = 650 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	T_A = 0–70°C, See Table 1.	•	2.0		3.5	V
Output Current[1]				12.5	14.5	A
Setpoint Accuracy[2]	I_{LOAD} = 5.25A			1.0	1.5	%
Output Temperature Drift	T_A = 0–70°C	•		+100		ppm/°C
Load Regulation	I_{LOAD} = 0.5 to 12.5A	•		-0.5		%Vo
Line Regulation	V_{IN} = 4.75–5.25V, I_{LOAD} = 12.5A	•		+0.14		%Vo
Output Ripple/Noise, pk-pk	V_{OUT} = 2.1–3.5V, 20MHz BW	•		30		mV
Cumulative Accuracy[3]	T_A = 0–70°C	•		±3.3	±5.0	%
Efficiency	I_{LOAD} = 12.5A, V_{OUT} = 3.3V	•	80	85		%
Short Circuit Detect Threshold	Internal comparator offset	•	100	120	140	mV
Output Current Driver			0.5	1.0		A
Power Dissipation	No load			0.1	0.2	W
Thermal Impedance, θ_{JA}				150		°C/W
Response Time, Sleep to Full Load				10		µs
Oscillator Frequency Range[4]			0.2		1	MHz
Oscillator Frequency Accuracy	Excluding tolerance of C_{EXT}			10		%
Maximum Duty Cycle in PWM Mode			90	95		%
Minimum Duty Cycle in PFM Mode					100	ns

Electrical Specifications (continued)

(V_{CCA}, V_{CCD} = 5V, f_{osc} = 650 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Response Time to Short Circuit				15	30	ns
Soft Start Duration at Power-Up				10		µs
Load Transient, 0.5A to 12.5A step	Slew rate = 30A/µs			100		mV

Notes:

1. The maximum output current is limited only by the external components used and their thermal limitations. For loads greater than 12.5A, adequate thermal management is required to achieve optimal performance and reliability.
2. Setpoint Accuracy includes Output Ripple/Noise.
3. Cumulative Accuracy is determined by Setpoint Accuracy, Line and Load Regulation, Output Ripple/Noise, Transient Performance and Temperature Drift.
4. See Typical Operating Characteristics.

Table 1. Voltage Identification Codes[1]

Pentium Pro Processor Pins				VID Setpoint	Setpoint Accuracy[2] (mV)	Cumulative Accuracy[3] (mV)
VID3	VID2	VID1	VID0			
1	1	1	1	2.0	—	—
1	1	1	0	2.1	±31	±105
1	1	0	1	2.2	±33	±110
1	1	0	0	2.3	±34	±115
1	0	1	1	2.4	±36	±120
1	0	1	0	2.5	±37	±125
1	0	0	1	2.6	±39	±130
1	0	0	0	2.7	±40	±135
0	1	1	1	2.8	±42	±140
0	1	1	0	2.9	±43	±145
0	1	0	1	3.0	±45	±150
0	1	0	0	3.1	±46	±155
0	0	1	1	3.2	±48	±160
0	0	1	0	3.3	±49	±165
0	0	0	1	3.4	±51	±170
0	0	0	0	3.5	±60	±175

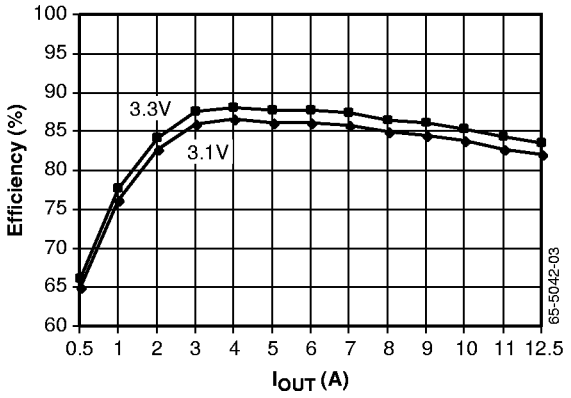
Notes:

1. 0 Indicates Processor pin is tied to V_{SS}. 1 = Open.
2. Setpoint Accuracy includes Output Ripple/Noise.
3. Cumulative Accuracy includes Setpoint Accuracy, Line & Load Regulation, Transient Effects and Temperature Drift.

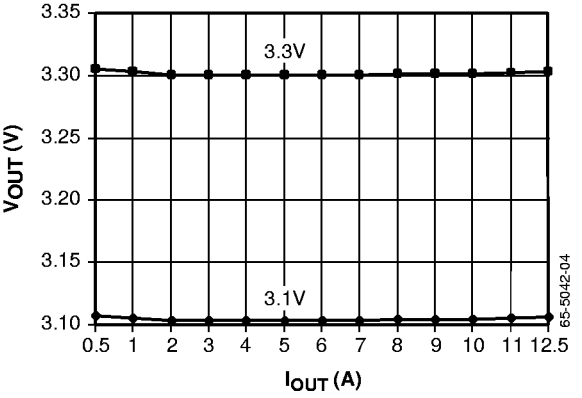
Typical Operating Characteristics

(VCCA, VCCD = 5V, f_{OSC} = 650 kHz and T_A = +25˚C using circuit in Figure 1, unless otherwise noted)

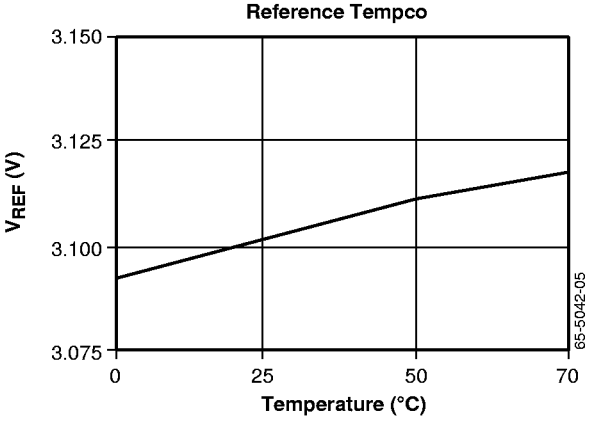
Efficiency vs. Output Current, 650 KHz



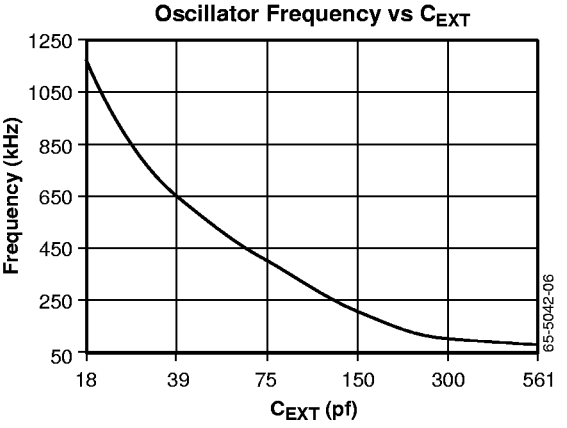
Load Regulation, 650 KHz



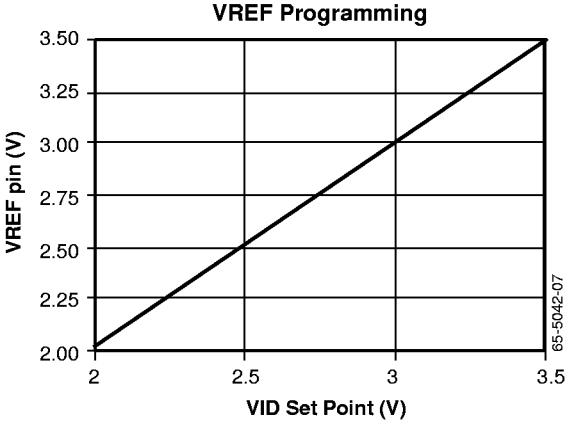
Reference Tempco



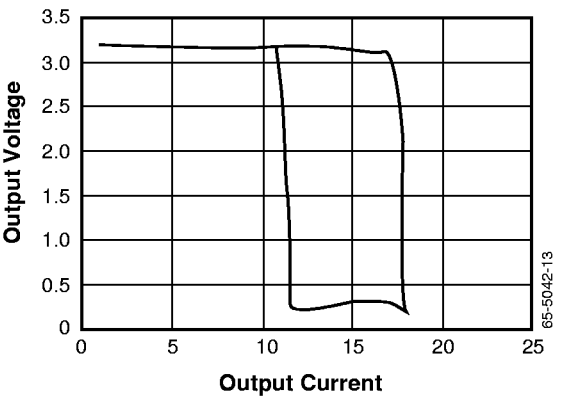
Oscillator Frequency vs C_{EXT}



VREF Programming

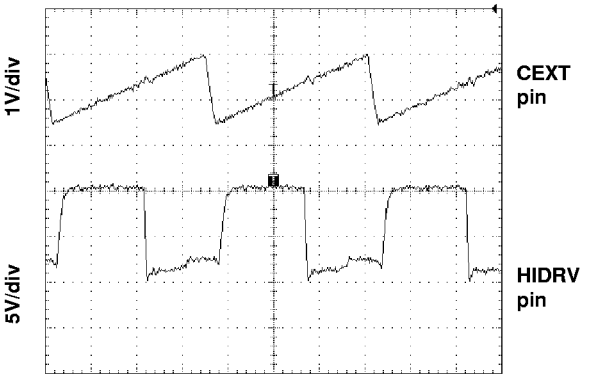


Output Voltage vs. Output Current, R_{SENSE} = 6mΩ



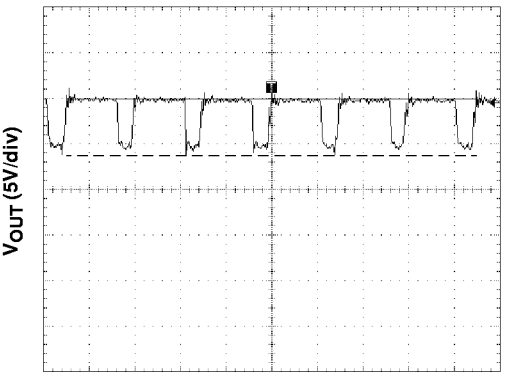
Typical Operating Characteristics (continued)

Switching Waveforms, 12.5A Load



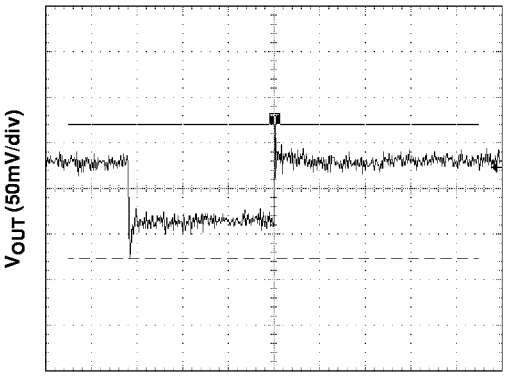
Time (500ns/division)

FET Driver Supply, VCCQP (I_{LOAD} = 12.5A using charge pump)



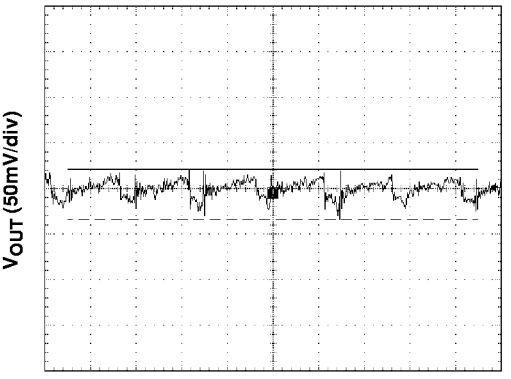
Time (1µs/division)

Transient Response, 0.5A to 12.5A Step



Time (200ns/division)

AC Ripple Response, 12.5A Load



Time (1µs/division)

65-5042-08

Test Circuits

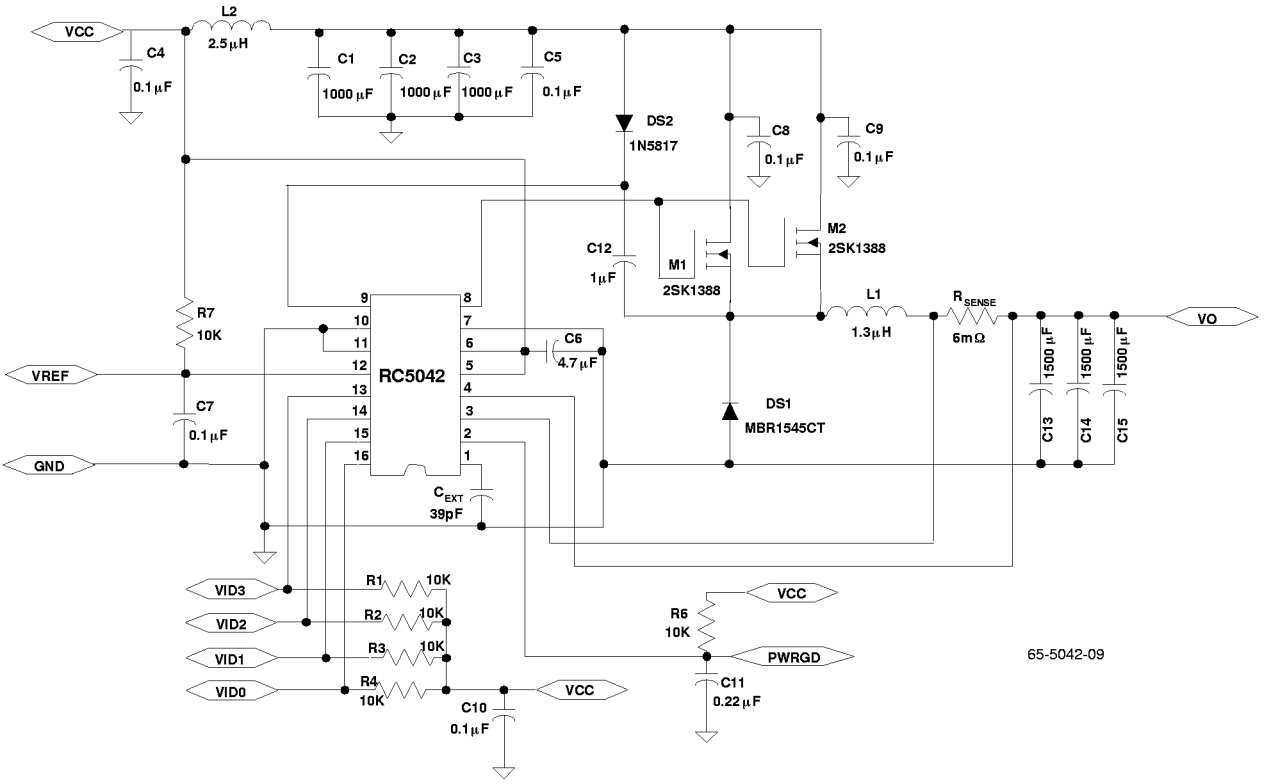


Figure 1. Standard Test or Application Schematic

Table 2. RC5042 Bill of Materials

Reference	Part Number	Description	Relevant Specification
C4, C5, C7–C10	Panasonic ECU-V1H104ZFX	0.1µF 50V capacitor	
C6	Panasonic ECSH1CY475R	4.7µF 16V capacitor	
C_{EXT}	Panasonic ECU-V1H121JCG	39pF capacitor	
C12	Panasonic ECSH1CY105R	1µF 16V capacitor	
C1, C2, C3	Sanyo 6MV1000GX	1000µF 6.3V electrolytic capacitor	
C11	Panasonic ECU-V1H224ZFX	0.22µF 50V capacitor	
C13, C14, C15	Sanyo 6MV1500GX	1500µF 6.3 electrolytic capacitor	ESR < 0.047 Ω
DS1	Motorola MBR1545CT	Schottky Diode	Vf < 0.72V @ If = 15A
DS2	General Instruments 1N5817	Schottky Diode	
L1	Skynet 320-8107	1.3µH inductor	
L2[1]	Skynet 320-6110	2.5µH inductor	
M1, M2	Fuji 2SK1388	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 37mΩ V_{GS} < 4V, I_D > 20A
R_{SENSE}	Copel AWG #18	6 mΩ CuNi Alloy Wire Resistor	
R1–R4, R6, R7	Panasonic ERJ-6ENF10.0KV	10K 5% Resistors	

Note:

1. The inductor L2 is recommended to isolate the 5V input supply from current surges caused by MOSFET switching. L2 is not required for normal operation and may be omitted if desired.

Application Information

Simple Step-Down Converter

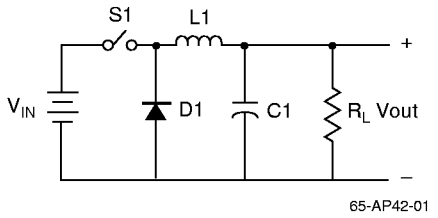


Figure 2. Simple Buck DC-DC Converter

Figure 2 illustrates a step-down DC-DC converter with no feedback control. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5042. Referring to Figure 1, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is impressed across inductor L1. The current flowing in this inductor is given by the following equation:

$$I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

Where T_{ON} is the duty cycle (the time when S1 is closed).

When S1 opens, the diode D1 will conduct the inductor current and the output current will be delivered to the load according to the equation:

$$I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

Where T_S is the overall switching period, and ($T_S - T_{ON}$) is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_S}\right)$$

In order to obtain a more accurate approximation for V_{OUT}, we must also include the forward voltage V_D across diode D1 and the switching loss, Vsw. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

Overview

The RC5042 is a programmable DC-DC controller IC. When designed around the appropriate external components, the RC5042 can be configured to deliver more than 14.5A of output current. During heavy loading conditions, the RC5042 functions as a current-mode PWM step-down regulator. Under light loads, the regulator functions in the PFM (pulse frequency modulation), or pulse skipping mode. The controller will sense the load level and switch between the two operating modes automatically, thus optimizing its efficiency under all loading conditions.

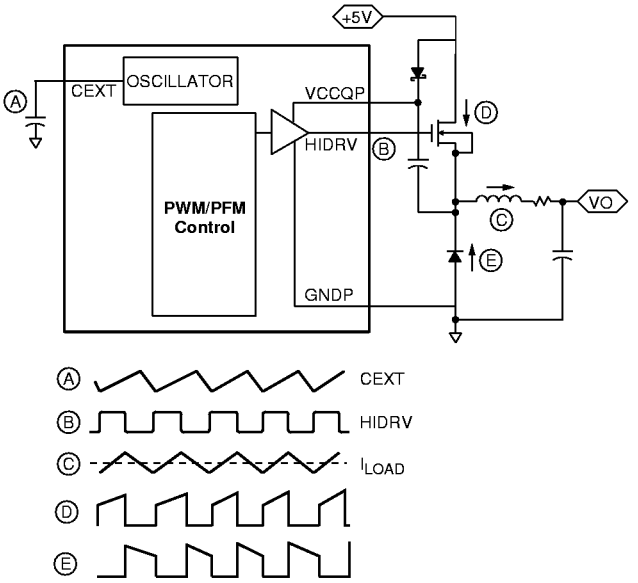


Figure 3. Typical Switching Waveforms

Main Control Loop

Refer to the Block Diagram on page 1. The control loop of the regulator contains two main sections, the analog control block and the digital control block. The analog block consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the thresholds of where the RC5042 enters its pulse skipping mode during light loads as well as the point at which the maximum current comparator disables the output drive signals to the external power MOSFETs.

The digital control block is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV output pin that controls the external power MOSFET. The digital section was designed utilizing high speed Schottky transistor logic, thus allowing the RC5042 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5042 contains two identical high current output drivers which utilize high speed bipolar transistors arranged in a push-pull configuration. Each driver is capable of delivering 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for additional switching noise immunity. The HIDRV driver has a power supply, VCCQP, which is boot-strapped from a flying capacitor as illustrated in Figure 2. Using this configuration, C12 is alternately charged from VCC via the Schottky diode DS2 and then boosted up when the FET is turned on. This scheme provides a VCCQP voltage equal to 2•VCC – VDS(DS2), or approximately 9.5V with VCC = 5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET required in order to achieve a low $R_{DS(ON)}$. Since the low side synchronous FET is referenced to ground (refer to Figure 3), there is no need to boost the gate drive voltage and its VCCP power pin can be tied to VCC. See Typical Operating Characteristics for typical full load VCCQP waveform.

Internal Voltage Reference

The reference included in the RC5042 is a 1.24V precision band-gap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference input is the resulting output from an integrated 4-bit DAC. The DAC is provided in accordance with the Pentium Pro specification guideline, which requires the DC-DC converter output to be directly programmable via a 4-bit voltage identification (VID) code. This code will scale the reference voltage from 2.0V (no CPU) to 3.5V in 100mV increments. For guaranteed stable operation under all loading conditions, a 10KΩ pull-up resistor and 0.1μF of decoupling capacitance should be connected to the VREF pin.

Power Good

The RC5042 Power Good function is designed in accordance with the Pentium Pro DC-DC converter specification and provides a constant voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed ±7% of its nominal setpoint. The Power Good flag provides no other control function to the RC5042.

Upgrade Present (UP#)

Intel's specifications state that the DC-DC converter must accept an open collector signal, used to indicate the presence of an upgrade processor. The typical state is high (standard CPU). When in the low or ground state (OverDrive processor present), the output voltage must be disabled unless the converter can supply the OverDrive processor's specifications. When disabled, the PWRGD output must be in the low state. Since the RC5042 can supply the OverDrive processor specifications, the UP# signal is not required.

Over-Voltage Protection

The RC5042 provides a constant monitor of the output voltage for protection against overvoltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an overvoltage condition will be assumed, and the RC5042 will disable the output drive signal to the MOSFET(s).

Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFET(s) when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When voltage developed across the sense resistor exceeds the comparator threshold voltage, the RC5042 will disable the output drive signal to the MOSFET(s).

The DC-DC converter returns to normal operation after the fault has been removed, for either an overvoltage or a short circuit condition.

Oscillator

The RC5042 oscillator section is implemented using a fixed current capacitor charging configuration. An external capacitor (CEXT) is used to preset the oscillator frequency between 200KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency as well as choosing external components.

In general, a lower operating frequency will increase the peak ripple current flowing in the output inductor, and thus require the use of a larger inductor value. Operation at lower frequencies also increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to the slower loop response of the controller.

As the operating frequency is increased, the user should note that the efficiency losses due to switching are relatively fixed per switching cycle. Therefore, as the switching frequency is increased, so is the contribution toward efficiency due to switching losses.

Careful analysis of the RC5042 DC-DC controller has resulted in an optimal operating frequency of 650KHz, which allows the use of smaller inductive and capacitive components while maximizing peak efficiency under all operating conditions.

Design Considerations and Component Selection

MOSFET Selection

This application requires N-channel *Logic Level* Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS(on)}$ < 37 mΩ (lower is better)
- Low gate drive voltage, V_{GS} < 4V
- Power package with low thermal resistance
- Drain current rating of 20A minimum
- Drain-Source voltage > 15V.

The on-resistance ($R_{DS(ON)}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation of the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. Table 5 presents a list of suitable MOSFETs for this application.

Table 5. MOSFET Selection Table

Manufacturer & Model #	Conditions[1]		$R_{DS,ON}$(mΩ) Typ.	$R_{DS,ON}$(mΩ) Max.	Package	Thermal Resistance
Fuji 2SK1388	V_{GS} = 4V, I_D = 17.5A	T_J = 25°C	25	37	TO-220	Φ_{JA} = 75
		T_J = 125°C	37	—		
Siliconix SI4410DY	V_{GS} = 4.5V, I_D = 5A	T_J = 25°C	16.5	20	SO-8 (SMD)	Φ_{JA} = 50
		T_J = 125°C	28	34		
National Semiconductor NDP706AL	V_{GS} = 5V, I_D = 40A	T_J = 25°C	13	15	TO-220	Φ_{JA} = 62.5 Φ_{JC} = 1.5
NDP706AEL		T_J = 125°C	20	24		
National Semiconductor NDP603AL	V_{GS} = 4.5V, I_D = 10A	T_J = 25°C	31	40	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	42	54		Φ_{JC} = 2.5
National Semiconductor NDP606AL	V_{GS} = 5V, I_D = 24A	T_J = 25°C	22	25	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	33	40		Φ_{JC} = 1.5
Motorola MTB75N03HDL	V_{GS} = 5V, I_D = 37.5A	T_J = 25°C	6	9	TO-263	Φ_{JA} = 62.5
		T_J = 125°C	9.3	14	(D_2 PAK)	Φ_{JC} = 1.0
Int. Rectifier IRLZ44	V_{GS} = 5V, I_D = 31A	T_J = 25°C	—	28	TO-220	Φ_{JA} = 62.5
		T_J = 125°C	—	46		Φ_{JC} = 1.0
Int. Rectifier IRL3103S	V_{GS} = 4.5V, I_D = 28A	T_J = 25°C	—	19	TO-220	Φ_{JA} = 62.5
		T_J = 125°C		31		Φ_{JC} = 1.0

Note:

1. $R_{DS(ON)}$ values at T_J=125°C for most devices were extrapolated from the typical operating curves supplied by the manufacturers and are approximations only. Only National Semiconductor offers maximum values at T_J = 125°C.

Two MOSFETs in Parallel

We recommend that two MOSFETs be used in parallel instead of one single MOSFET. Significant advantages are realized using two MOSFETs in parallel:

- **Significant reduction of power dissipation**.

  Maximum current of 14A with one MOSFET:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$
  $= (14)^2(0.050^*)(3.3+0.4)/(5+0.4-0.35) = 7.2\ W$

  With two MOSFETs in parallel:

  $P_{MOSFET} = (I^2 R_{DS(ON)})(\text{Duty Cycle})$
  $= (14/2)^2(0.037^*)(3.3+0.4)/(5+0.4-0.35) = 1.3W/FET$

  *Note: $R_{DS(on)}$ increases with temperature. Assume $R_{DS(on)} = 0.025$ at 25°C. $R_{DS(on)}$ can easily increase to 0.050W at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS(on)}$ to rise above the listed maximum value of 37mW.

- **Less heat sink required.** With power dissipation down to around one watt and with MOSFETs mounted flat on the motherboard, there will be considerably less heat sink required. The junction-to-case thermal resistance for the MOSFET package (TO-220) is typically at 2°C/W and the motherboard serves as an excellent heat sink.
- **Higher current capability.** With thermal management under control, this on-board DC-DC converter is able to deliver load currents up to 14.5A with no problem at all.

MOSFET Gate Bias

The MOSFET can be biased by one of two methods—Charge Pump or 12V Gate Bias.

Charge pump (or Bootstrap) method

Figure 4 employs a charge pump to provide gate bias. Capacitor CP is the charge pump deployed to boost the voltage of the RC5042 output driver. When the MOSFET switches off, the source of the MOSFET is at -0.6V. VCCQP is charged through the Schottky diode to 4.5V. Thus, the capacitor CP is charged to 5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to 10V. The Schottky is required to provide the charge path when the MOSFET is off. The Schottky reverses bias when the VCCQP goes to 10V. The charge pump capacitor, CP, needs to be a high Q and high frequency capacitor. A 1µF ceramic capacitor is recommended here.

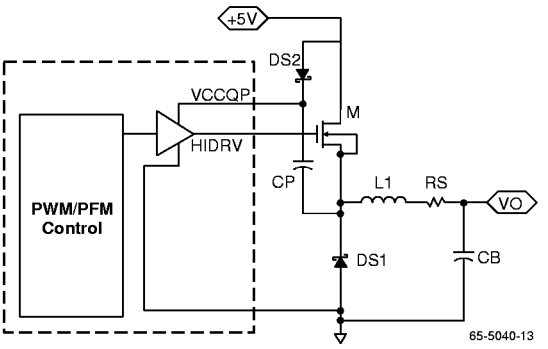


Figure 4. Charge Pump Configuration

Method 2. 12V Gate Bias

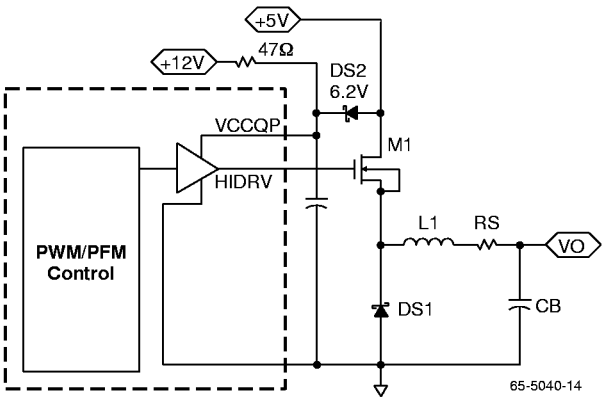


Figure 5. 12V Gate Bias Configuration

Figure 6 uses an external 12V source to bias VCCQP. A 47 Ω resistor is used to limit the transient current into the VCCQP pin. A 1µF capacitor filter is used to filter the VCCQP supply. This method provides a higher gate bias voltage to the MOSFET, and therefore reduces the $R_{SD(ON)}$ and resulting power loss within the MOSFET. Figure 7 illustrates how $R_{DS(ON)}$ decreases dramatically as V_{GS} increases. A 6.2V Zener (DS2) is used to clamp the voltage at V_{CCQP} to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

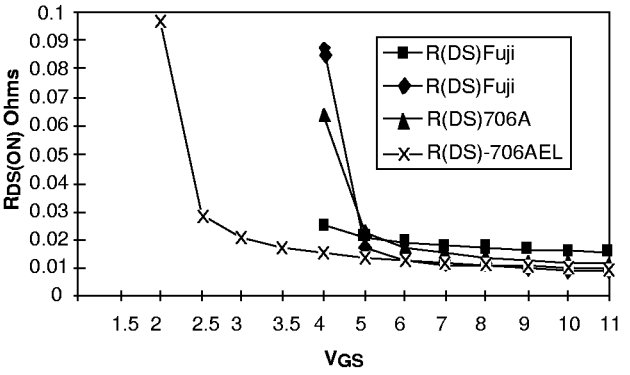


Figure 6. R(DS) vs. V_{GS} for Selected MOSFETs

Converter Efficiency

Losses due to parasitic resistance in the switches, coil, and sense resistor dominate at high load-current level. The major loss mechanisms under heavy loads, in usual order of importance, are:

- MOSFET I^2R Losses
- Inductor Coil Losses
- Sense Resistor Losses
- gate-charge losses
- diode-conduction losses
- transition losses
- Input Capacitor losses
- losses due to the operating supply current of the IC

Efficiency of the converter under heavy loads can be calculated as follows:

$$\text{Efficiency} = \frac{P_{OUT}}{p_{IN}} = \frac{I_{OUT} \times V_{OUT}}{I_{OUT} \times V_{OUT} + P_{LOSS}},$$

where $P_{LOSS} = PD_{MOSFET} + PD_{INDUCTOR} + PD_{RSENSE} + PD_{GATE} + PD_{DIODE} + PD_{TRAN} + PD_{CAP} + PD_{IC}$

Design Equations:

(1) $PD_{MOSFET} = I_{OUT}^2 \times R_{DS(ON)} \times \text{DutyCycle}$

where $\text{DutyCycle} = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}}$

(2) $PD_{INDUCTOR} = I_{OUT}^2 \times R_{INDUCTOR}$

(3) $PD_{RSENSE} = I_{OUT}^2 \times R_{SENSE}$

(4) $PD_{GATE} = q_{GATE} \times f \times 5V$, where q_{GATE} is the gate charge and f is the switching frequency

(5) $PD_{DIODE} = V_f \times I_{OUT}(1 - \text{Dutycycle})$

(6) $PD_{TRAN} = \frac{V_{IN}^2 \times C_{RSS} \times I_{LOAD} \times f}{I_{DRIVE}}$, where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET.

(7) $PD_{CAP} = I_{RMS}^2 \times ESR$

(8) $PD_{IC} = V_{CC} \times I_{CC}$

Example:

$$\text{DutyCycle} = \frac{3.3 + 0.5}{5 + 0.5 - 0.3} = 0.73$$

$$PD_{MOSFET} = 10^2 \times 0.030 \times 0.73 = 2.19W$$

$$PD_{INDUCTOR} = 10^2 \times 0.010 = 1W$$

$$PD_{RSENSE} = 10^2 \times 0.0065 = 0.65W$$

$$PD_{GATE} = CV \times f \times 5V = 1.75nf \times (9 - 1)V \times 650Khz \times 5V = 0.045W$$

$$PD_{DIODE} = 0.5 \times 10(1 - 0.73) = 1.35W$$

$$PD_{TRAN} = \frac{5^2 \times 400pf \times 10 \times 650khz}{0.7A} \sim 0.010W$$

$$PD_{CAP} = (7.5 - 2.5)^2 \times 0.015 = 0.37W$$

$$PD_{IC} = 0.2W$$

$$PD_{LOSS} = 2.19W + 1.0W + 0.65W + 0.045W + 1.35W + 0.010W + 0.37W + 0.2W = 5.815W$$

$$\therefore \text{ Efficiency} = \frac{3.3 \times 10}{3.3 \times 10 + 5.815} \sim 85\%$$

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-DC converter application.. The critical parameters are inductance (L), maximum DC current (Io) and the coil resistance (R1). The inductor core material is a crucial factor in determining the amount of current the inductor will be able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500KHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI and low hysteresis losses; however, they tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance will degrade the efficiency of the converter by the relationship: $P_{LOSS} = I_O^2$ x R1. The value of the inductor is a function of the oscillator duty cycle (T_{ON}) and the maximum inductor current (I_{PK}). I_{PK} can be calculated from the relationship:

$$I_{PK} = I_{MIN} + \left(\frac{V_{IN} - V_{SW} - V_D}{L}\right) T_{ON}$$

Where T_{ON} is the maximum duty cycle and V_D is the forward voltage of diode DS1.

Then the inductor value can be calculated using the relationship:

$$L = \left(\frac{V_{IN} - V_{SW} - V_O}{I_{PK} - I_{MIN}}\right) T_{ON}$$

Where V_{SW} (R_{DSON} x I_O) is the drain-to-source voltage of M1 when it is switched on.

Implementing Short Circuit Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Fairchild Semiconductor has implemented a current sense methodology to disable the output drive signal to the MOSFET(s) when an over current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to one terminal of an internal comparator with hysterisis. The other comparator terminal has the threshold voltage, nominally of 120mV. Table 6 states the limits for the comparator threshold of the Switching Regulator:

Table 6. RC5042 Short Circuit Comparator Threshold Voltage

	Short Circuit Comparator $V_{threshold}$ (mV)
Typical	120
Minimum	100
Maximum	140

When designing the external current sense circuitry, the designer must pay careful attention to the output limitations during normal operation and during a fault condition. If the short circuit protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFET(s) may rise to destructive levels.

The design equation used to set the short circuit threshold limit is as follows:

$$R_{SENSE} = \frac{V_{th}}{I_{SC}}, \text{ where: } I_{SC} = \text{Output short circuit current}$$

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2}$$

Where I_{pk} and I_{min} are peak ripple current and $I_{load,\,max}$ = maximum output load current.

The designer must also take into account the current ($I_{PK} - I_{min}$), or the ripple current flowing through the inductor under normal operation. Figure 7 illustrates the inductor current waveform for the RC5042/42 DC-DC converter at maximum load.

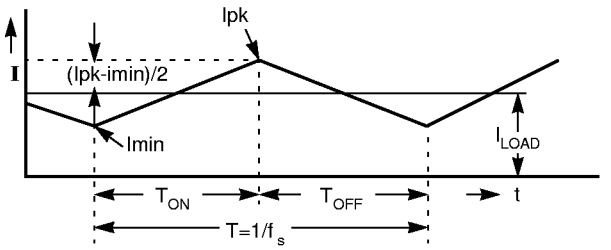


Figure 7. Typical DC-DC Converter Inductor Current Waveform

The calculation of this ripple current is as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(V_{IN} - V_{SW} - V_{OUT})}{L} \times \frac{(V_{OUT} + V_D)}{(V_{IN} - V_{SW} + V_D)} T$$

where:
- V_{in} = input voltage to Converter
- V_{SW} = voltage across Switcher (MOSFET) = I_{LOAD} x $R_{DS(ON)}$
- V_D = Forward Voltage of the Schottky diode
- T = the switching period of the converter = 1/fs, where f_S = switching frequency.

For an input voltage of 5V, an output voltage of 3.3V, an inductor value of 1.3µH and a switching frequency of 650KHz (using C_{EXT}=39pF), the inductor current can be calculated as follows:

$$\frac{(I_{pk} - I_{min})}{2} = \frac{(5.0 - 14.5 \times 0.037 - 3.3)}{1.3 \times 10^{-6}} \times$$

$$\frac{(3.3 + 0.5)}{(5.0 - 14.5 \times 0.037 + 0.5)} \times \frac{1}{650 \times 10^{3}} = 1.048A$$

Therefore, the peak current, I_{PK}, through the inductor for a 14.5A load is found to be:

$$I_{SC} \geq I_{inductor} = I_{Load,\,max} + \frac{(I_{PK} - I_{min})}{2} = 14.5 + 1 = 15.5A$$

As a result, the short circuit detection threshold must be at least 15.5A.

The next step is to determine the value of the sense resistor. Including sense resistor tolerance, the sense resistor value can be approximated as follows:

$$R_{SENSE} = \frac{V_{th,min}}{I_{SC}} \times (1 - TF) = \frac{V_{th,min}}{1.0 + I_{Load,max}} \times (1 - TF)$$

Where TF = Tolerance Factor for the sense resistor.

There are several different type of sense resistors. Table 7 describes tolerance, size, power capability, temperature coefficient and cost of various type of sense resistors:

Table 7. Comparison of Sense Resistors[1]

Description	Motherboard Trace Resistor	Discrete Iron Alloy resistor (IRC)	Discrete Metal Strip surface mount resistor (Dale)	Discrete MnCu Alloy wire resistor	Discrete CuNi Alloy wire resistor (Copel)
Tolerance Factor (TF)	±29%	±5% (±1% available)	±1%	±10%	±10%
Size (L x W x H)	2" x 0.2" x 0.001" (1 oz Cu trace)	0.45" x 0.065" x 0.200"	0.25" x 0.125" x 0.025"	0.200" x 0.04" x 0.160"	0.200" x 0.04" x 0.100"
Power capability	>50A/in	1 watt (3W and 5W available)	1 watt	1 watt	1 watt
Temperature Coefficient	+4,000 ppm	+30 ppm	±75 ppm	±30 ppm	±20 ppm
Cost @10,000 piece	Low included in motherboard	$0.31	$0.47	$0.09	$0.09

Notes:
1. Refer to Appendix A for Directory of component suppliers

Based on the Tolerance in the above table,

For Embedded PC Trace Resistor and for $I_{load,max}$ = 14.5A:

$$R_{SENSE} = \frac{V_{th,min}}{1.0A + I_{Load,\,max}} \times (1 - TF)$$

$$= \frac{100mV}{1.0A + 14.5A} \times (1 - 29\%) = 4.6m\Omega$$

For discrete resistor and $I_{load,\,max}$ = 14.5A:

$$R_{SENSE} = \frac{V_{th,min}}{1.0A + I_{Load,\,max}} \times (1 - TF)$$

$$= \frac{100mV}{1.0A + 14.5A} \times (1 - 5\%) = 6.1m\Omega$$

For user convenience, Table 8 lists recommended value for sense resistor for various load current using embedded PC trace resistor or discrete resistor.

Table 8. R_{sense} for Various Load Current

$I_{Load,max}$ (A)	R_{SENSE} PC Trace Resistor (mΩ)	R_{SENSE} Discrete Resistor (mΩ)
10.00	6.5	8.6
11.20	5.8	7.8
12.40	5.3	7.1
13.90	4.8	6.4
14.00	4.7	6.3
14.50	4.6	6.1

RC5042 Short Circuit Current Characteristics

The RC5042 has a short circuit current characteristic that includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. A typical V-I characteristic of the DC-DC converter output is presented in the Typical Operating Characteristics section, page 5. The converter performs with a normal load regulation characteristic until the voltage across the resistor reaches the internal short circuit threshold of 120mV. At this point, the internal comparator trips and sends a signal to the controller to turn off the gate drive to the power MOSFET. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit mode of control. The output voltage will not return to the normal load characteristic until the output short circuit current is reduced to within the safe range for the DC-DC converter.

Schottky Diode Selection

The application circuit diagram of Figure 1 shows two Schottky diodes, DS1 and DS2. In synchronous mode, DS1 is used in parallel with M3 to prevent the lossy diode in the FET from turning on. DS2 serves a dual purpose. As configured, it allows the VCCQP supply pin of the RC5042 to be bootstrapped up to 9V using capacitor C12. When the lower MOSFET M3 is turned on, one side of capacitor C12 is connected to ground while the other side of the capacitor is being charged up to voltage VIN – VD through DS2. The voltage that is then applied to the gate of the MOSFET is VCCQP – VSAT, or typically around 9V. A vital selection criteria for DS1 and DS2 is that they exhibit a very low forward voltage drop, as this parameter can directly affect the regulator efficiency. In non-synchronous mode, DS1 is used as a flyback diode to provide a constant current path for the inductor when M1 is turned off. Table 9 lists several suitable Schottky diodes. Note that the MBR2015CTL has a very low forward voltage drop. This diode is most ideal for application where output voltage is required to be less than 2.8V.

Table 9. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage V_F
Philips PBYR1035	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR2035CT	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR1545CT	I_F = 15A; T_j = 25°C I_F = 15A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR2015CTL	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 150°C	< 0.58V < 0.48V

Output Filter Capacitors

Optimal ripple performance and transient response are functions of the filter capacitors used. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5042.

The higher the input capacitance, the more charge storage is available for improving the current transfer through the FET. Low "ESR" capacitors are best suited for this type of application and can influence the converter's efficiency if not chosen carefully. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR or Equivalent Series Resistance, is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

Where:

- DF is the dissipation factor of the capacitor
- f is the operating frequency
- C is the capacitance in farads

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

Where ΔV is the maximum voltage deviation due load transient

ΔT is reaction time of the power source (Loop response time of the RC5042) and it is approximately 8µs

I_O is the output load current

For I_O = 10A, and ΔV = 75mV, the bulk capacitor required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{10A \times 8\mu s}{75mV - 10A \times 5m\Omega} = 3200\mu F$$

Input filter

We recommend that the design include an input inductor between the system +5V supply and the DC-DC converter input described below. This inductor will serve to isolate the +5V supply from noise occurring in the switching portion of the DC-DC converter and to also limit the inrush current into the input capacitors on power up. We recommend a value of around 2.5µH.

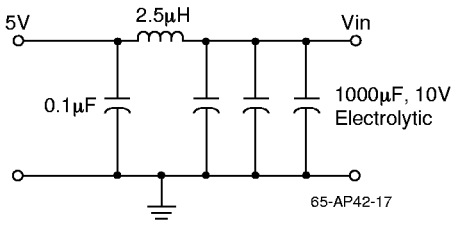


Figure 8. Input Filter

PCB Layout Guidelines and Considerations

PCB Layout Guidelines

1. Placement of the MOSFETs relative to the RC5042 is critical. The MOSFETs (M1 & M2), should be placed such that the trace length of the HIDRV pin from the RC5042 to the FET gates is minimized. A long lead length on this pin will cause high amounts of ringing due to the inductance of the trace combined with the large gate capacitance of the FET. This noise will radiate all over the board, and because it is switching at such a high voltage and frequency, it will be very difficult to suppress.

   The drawing below depicts an example of good placement for the MOSFETs in relation to the RC5042 and also an example of problematic placement for the MOSFETs.

   In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5042. That is to say, traces that connect to pins 8 and 9 (HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 4, and pin 12.

2. Place decoupling capacitors (.1µF) as close to the RC5042 pins as possible. Extra lead length on these will negate their ability to suppress noise.

3. Each VCC and GND pin should have its own via down to the appropriate plane underneath. This will help give isolation between pins.

4. Surround the CEXT timing capacitor with a ground trace as much as possible. Also be sure to keep a ground or power plane underneath the capacitor for further noise isolation. This will help to shield the oscillator pin 1 from the noise on the PCB. Place this capacitor as close to the RC5042 pin 1 as possible.

5. Place MOSFETs, inductor and Schottky as close together as possible for the same reasons as #1 above. Place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each MOSFET will help to suppress some of the high frequency switching noise on the input of the DC-DC converter.

6. The traces that run from the RC5042 IFB (pin 3) and VFB (pin 4) pins should be run together next to each other and be Kelvin connected to the sense resistor. Running these lines together will help in rejecting some of the common noise that is presented to the RC5042 feed-

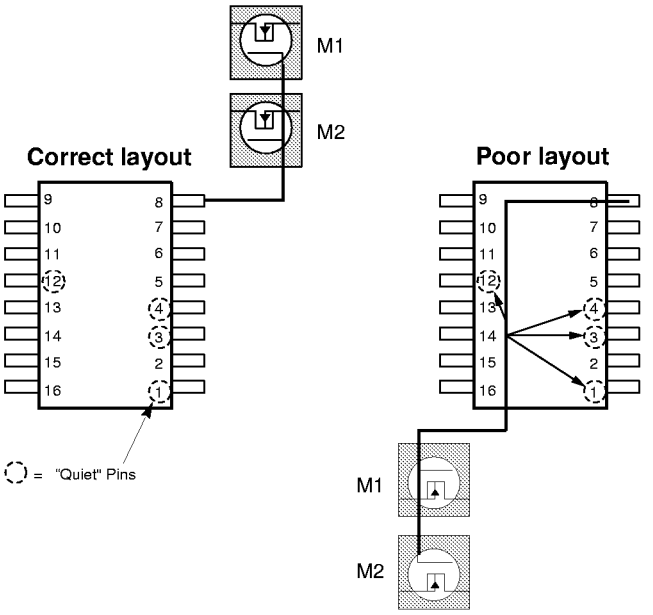
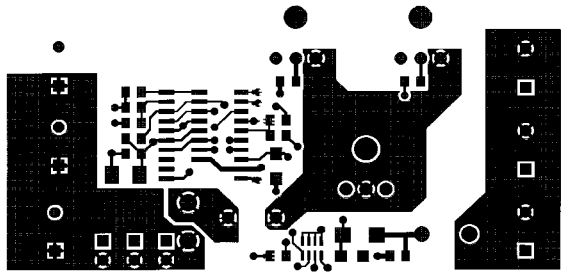


Figure 9. MOSFET Layout Guidelines

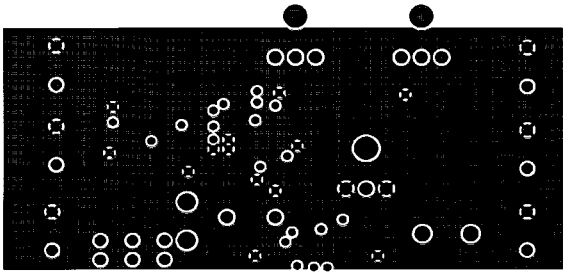
back input. Try as much as possible to run the noisy switching signals (HIDRV & VCCQP) on one layer; and use the inner layers for only power and ground. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

Example of a Layout on a PC Motherboard and Gerber File

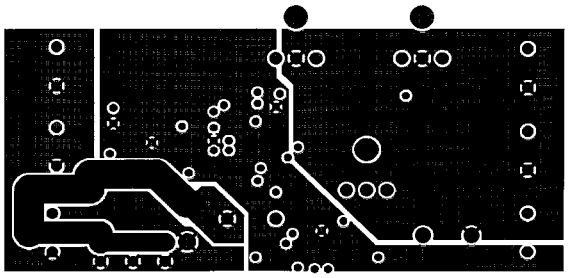
A reference design for motherboard implementation of the RC5042 along with Layout Gerber File and Silk Screen are presented here. The actual Gerber File can be obtained from a Fairchild Semiconductor local Sales Rep Office or from Fairchild Semiconductor Marketing Department at (415) 966-7819.



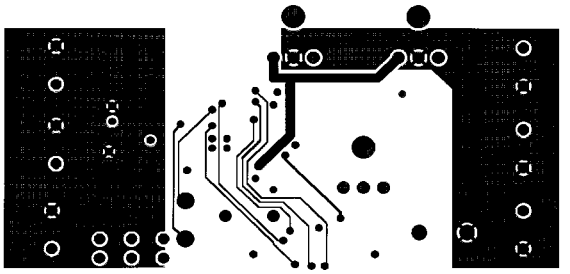
TOP



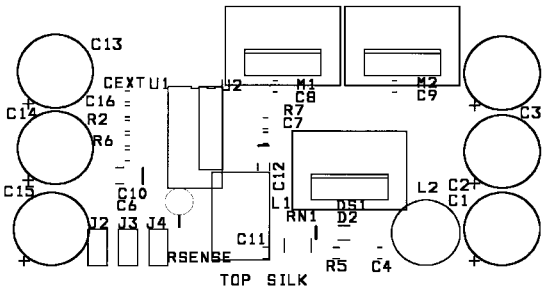
GND

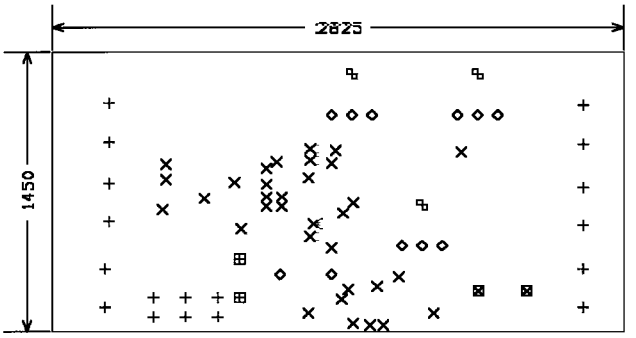


POWER



MOTTOB





RC5042 Evaluation Board

Fairchild Semiconductor provides an evaluation board for the purpose of verifying the system level performance of the RC5042. The evaluation board serves as a guide as to what can be expected in performance with the supplied external components and PCB layout. Please call your Fairchild Semiconductor local Sales Rep Office or Fairchild Semiconductor Marketing Department at (650) 966-7819 for an evaluation board.

Additional Application Information

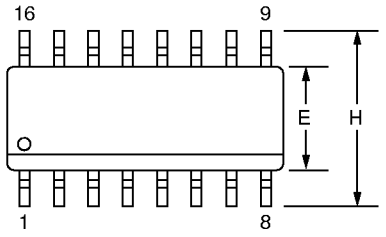
A comprehensive Application Note providing implementation guidelines for the RC5040 and RC5042 DC-DC Converters for Pentium® Pro processors (AP-42) is available from your local Fairchild Semiconductor Sales Rep or from Fairchild Semiconductor Marketing at 650-966-7819. Most application notes and data sheets can also be obtained by calling Fairchild Semiconductor's fax-on-demand system at 650-988-2123.

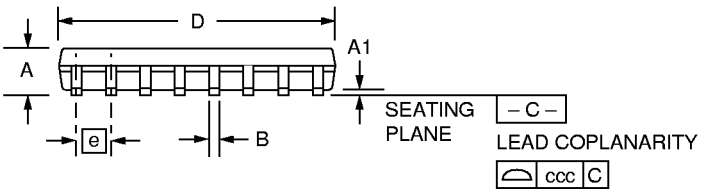
Mechanical Dimensions – 16 Lead SOIC

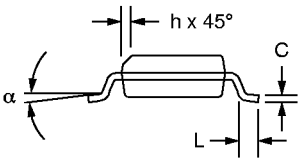
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Package
RC5042M	16 pin SOIC

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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