RC5T619-1xxx

(CSP0608-80: 0.65mm pitch)

PCB Layout Guide

Version 1.2

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Abstract

This document describes the constraints and points when designing the PCB layout with RC5T619-1xxx.
This guide provides examples to explain of how it can be done.
The PCB layout example is helpful to achieve optimal RC5T619-1xxx performance.

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1. Basic Policy and Examples of Board Pattern

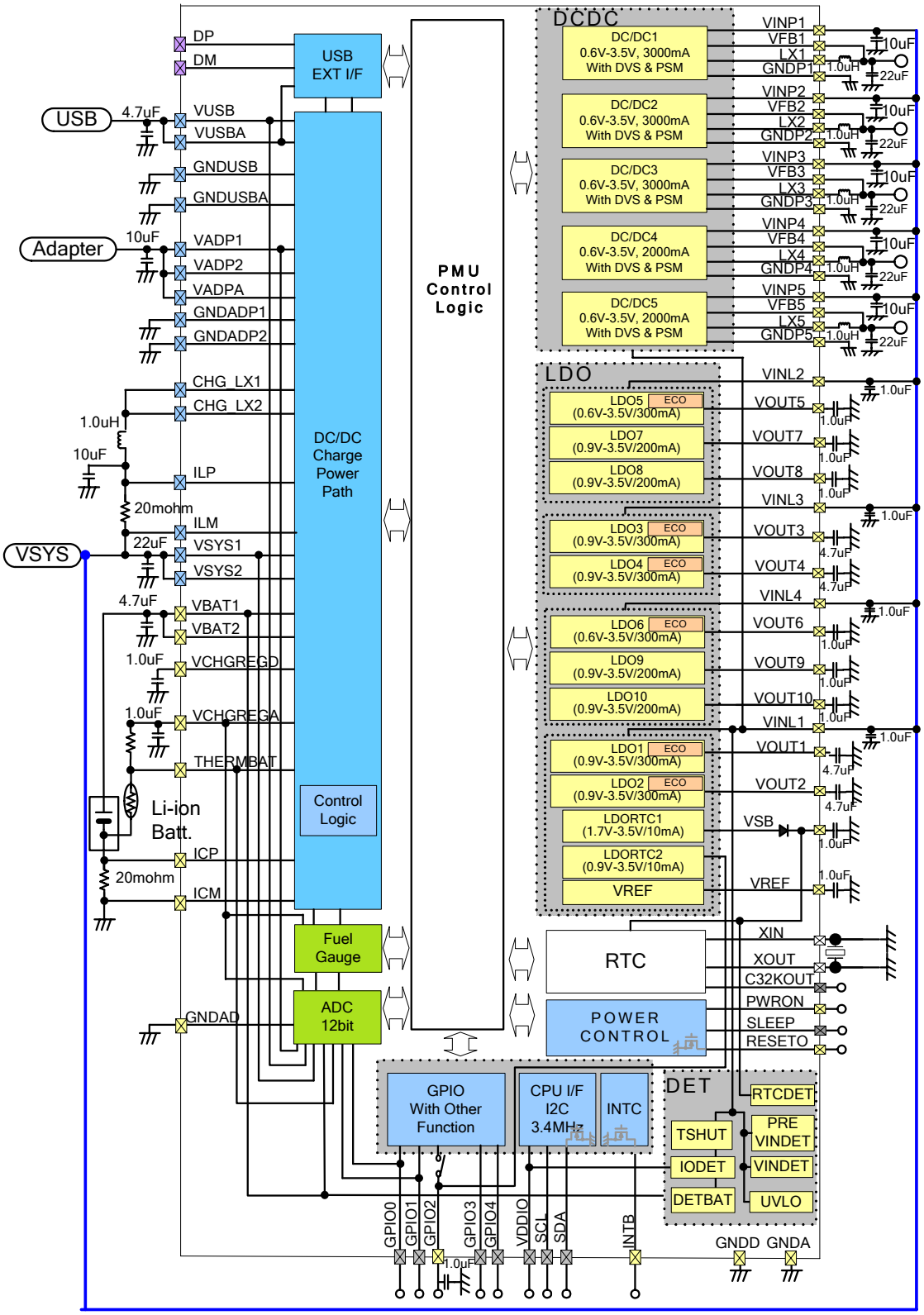


Fig. 1: RC5T619-1xxx Block Diagram

1.1 <DCDC Block>

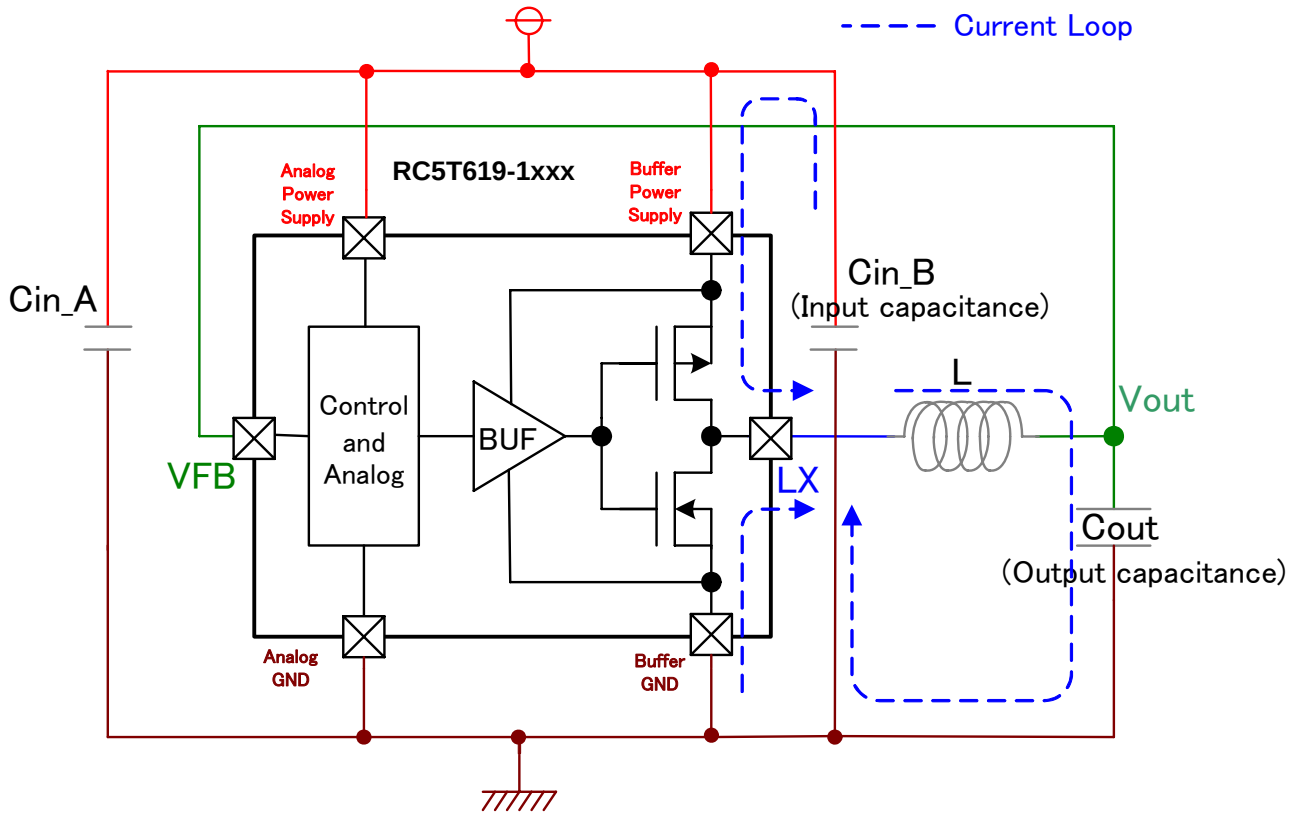


Fig. 1-1: Simplified Schematic for DCDC1, DCDC2, DCDC3, DCDC4 and DCDC5

RC5T619-1xxx Pin Names

	DCDC1	DCDC2	DCDC3	DCDC4	DCDC5
Analog Power Supply	VINL1				
Buffer Power Supply	VINP1	VINP2	VINP3	VINP4	VINP5
VFB	VFB1	VFB2	VFB3	VFB4	VFB5
LX	LX1	LX2	LX3	LX4	LX5

Table 1-1: RC5T619-1xxx Pin Names

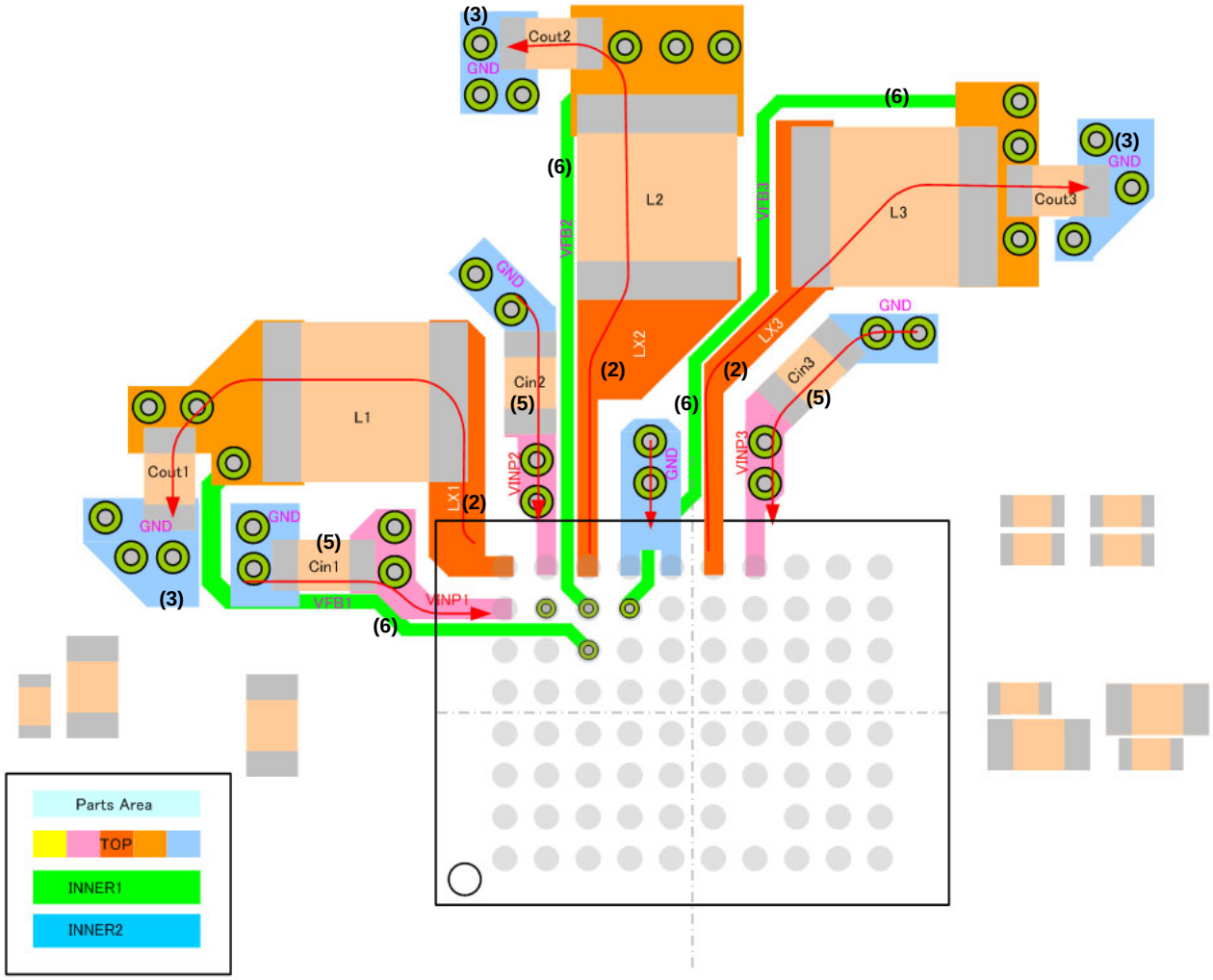


Fig. 1-2: Example of DCDC Block Board Pattern (Top Layer)

(1) Place the parts to minimize the switching current loop (Figure 1-1: blue line, Figure 1-2: red line).
(2) Route the LX line as short and wide as possible between RC5T619-1xxx and an inductor, and prohibit adding other redundant lines on it.
(3) Connect the ground line of “Cout” directly to the internal ground plane with multiple vias, in order to reduce impedance as small as possible. (Target: 50mΩ or less)
(4) Pull out the output of DCDC from near not “L” but “Cout”.
(5) Place “Cin” as close as possible to RC5T619-1xxx.
(Higher priority level is “Cin” < L < “Cout” in the close distance order with RC5T619-1xxx.)
(6) Prohibit routing the VFB line which goes back to the RC5T619-1xxx with parallel to noise source line as LX, and it's preferable to route the VFB line in the different layer from noise source.
In addition, it should not pass under the Inductors.

1.2 <Charger Block>

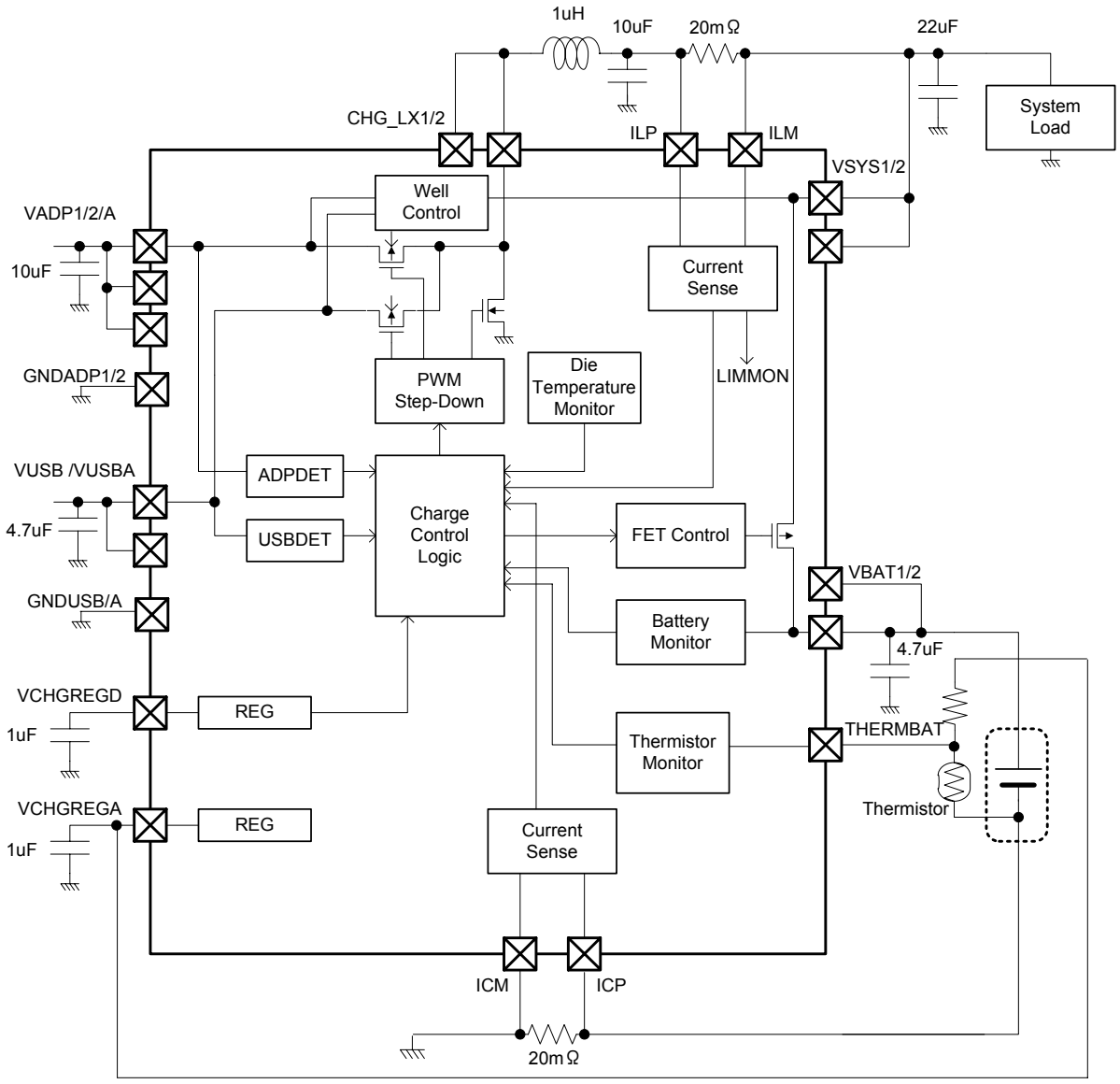


Fig. 1-3: Simplified Schematic for Charger Block

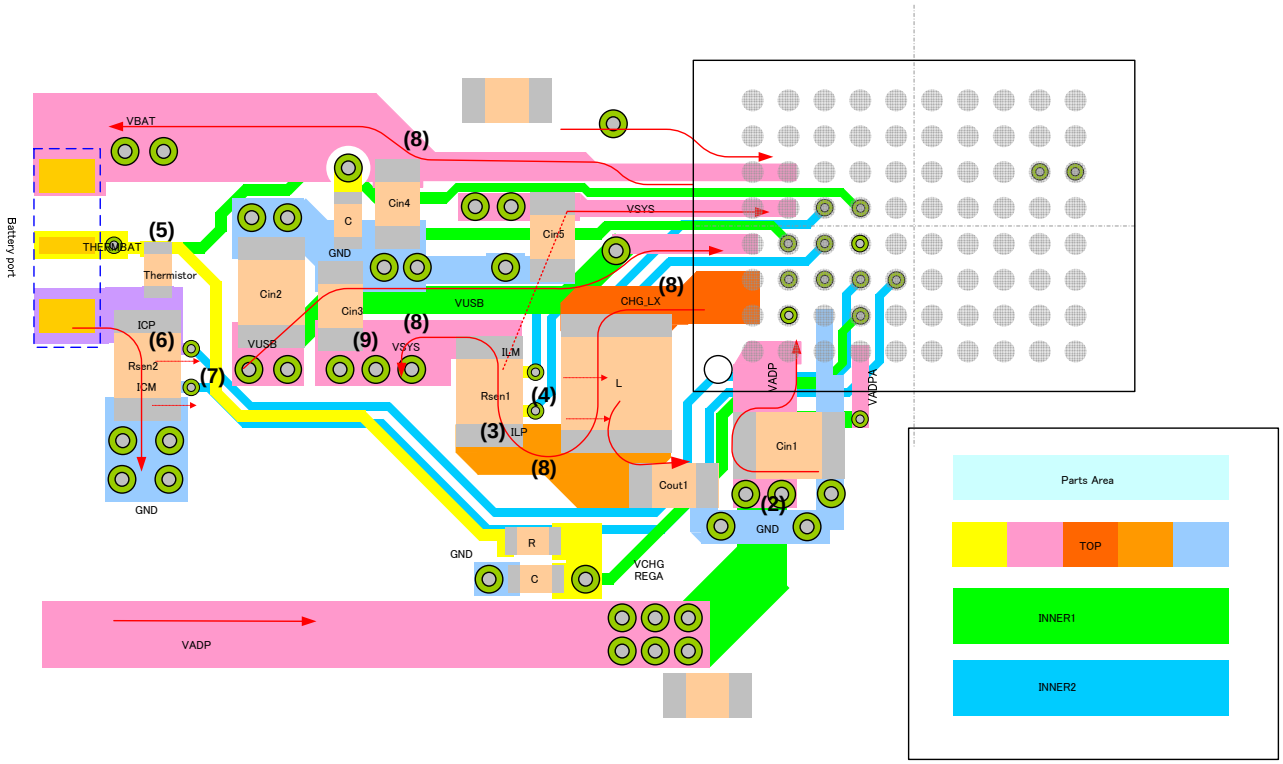


Fig. 1-4: Example of Charger Block Pattern (Top Layer)

(1) Place the parts to minimize the switching current loop. (Figure 1-4: red line)
(2) Place “VADP” capacitor as close as possible to RC5T619-1xxx, and route the line to RC5T619-1xxx short and widely in order to minimize resistance.
(3) Because “R_{SEN1}” Is the resistance which fixes accuracy of the current, use the high accuracy it as possible. (Refer to the “Recommended External Parts List” on P.11)
In addition, connect R_{SEN1} to “Cout” with very low impedance.
(4) Pull out “ILP” and “ILM” from the PAD of “R_{SEN1}”, and route the isometric lines because of the differential signal. Furthermore, prevent from routing the lines parallel to the source of noise.
(5) Connect the terminal of thermistor of battery to the port of “THERMBAT” with very low impedance to avoid reducing the accuracy of temperature detection.
(6) Because “R_{SEN2}” is the resistance which fixes the charging current, use the high accuracy it as possible. (Refer to the “Recommended External Parts List” on P.11)
In addition, connect R_{SEN2} to the minus terminal of battery with very low impedance.
(7) Pull out “ICP” and “ICM” from the PAD of “R_{SEN2}”, and route the isometric lines because of the differential signal. Furthermore, prevent from routing the lines parallel to the source of noise.
(8) Because the lines from “CHG_LX” to “VSYS”, from “VBAT” to the plus terminal of battery and from “ICP” and to the minus of battery flow large current, route them short and widely to become low impedance.
(9) Place the capacitor after passing through “R_{SEN1}” on ILM side, not “VSYS” side.

1.3 <USB External Device>

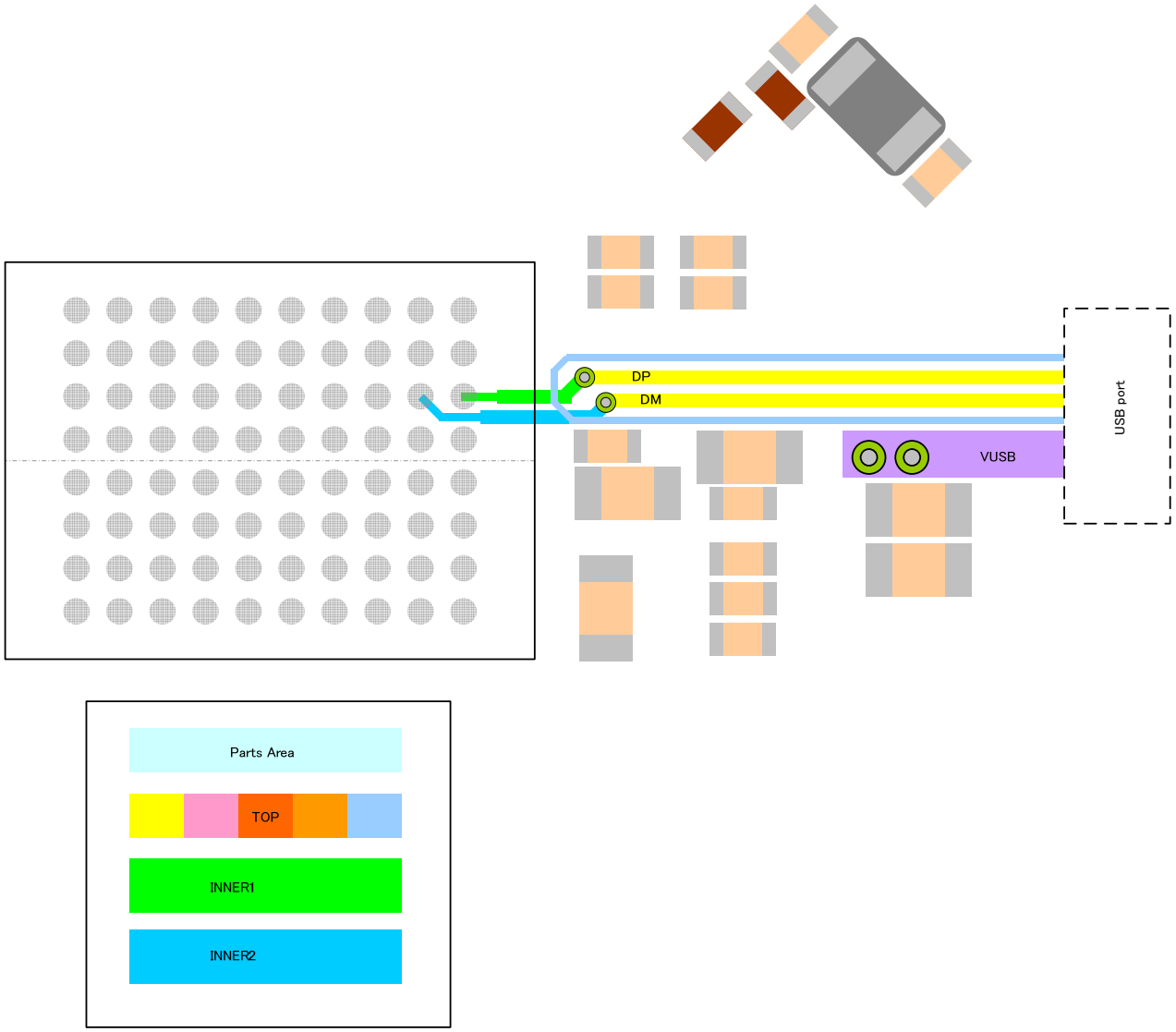


Fig. 1-5: Example of USB External Device Pattern (Top Layer)

(1) The under layer of DP and DM corresponding to the USB transmission lines should be drawn as ground plane.
(2) Wire DP and DM lines equally spaced apart and same length on the surface layer without using via. And make the differential impedance of DP and DM 90 ohms.
(3) Prohibit wiring a GND line or other signals between DP and DM lines. Place GND line around DP and DM lines (as guard ring) in order to prevent noise.
(4) Prohibit bending the DP and DM lines 90 degrees. If necessary to do so, bend them 45 degrees twice.
(5) Place DP and DM at least 50mil (1.27mm) away from high speed signals such as crystal and clock.

1.4 <RTC>

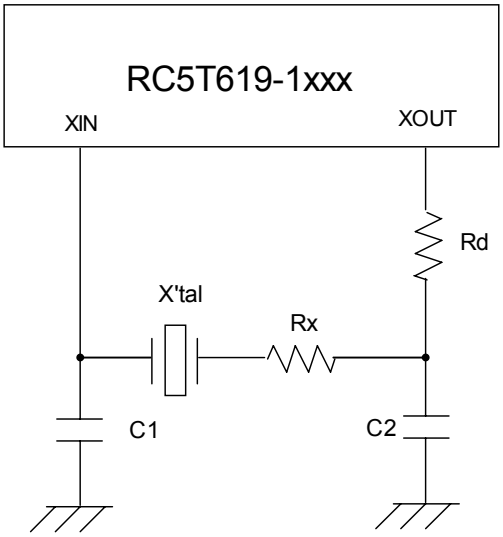


Fig. 1-6: Recommended Schematic for RTC Block.

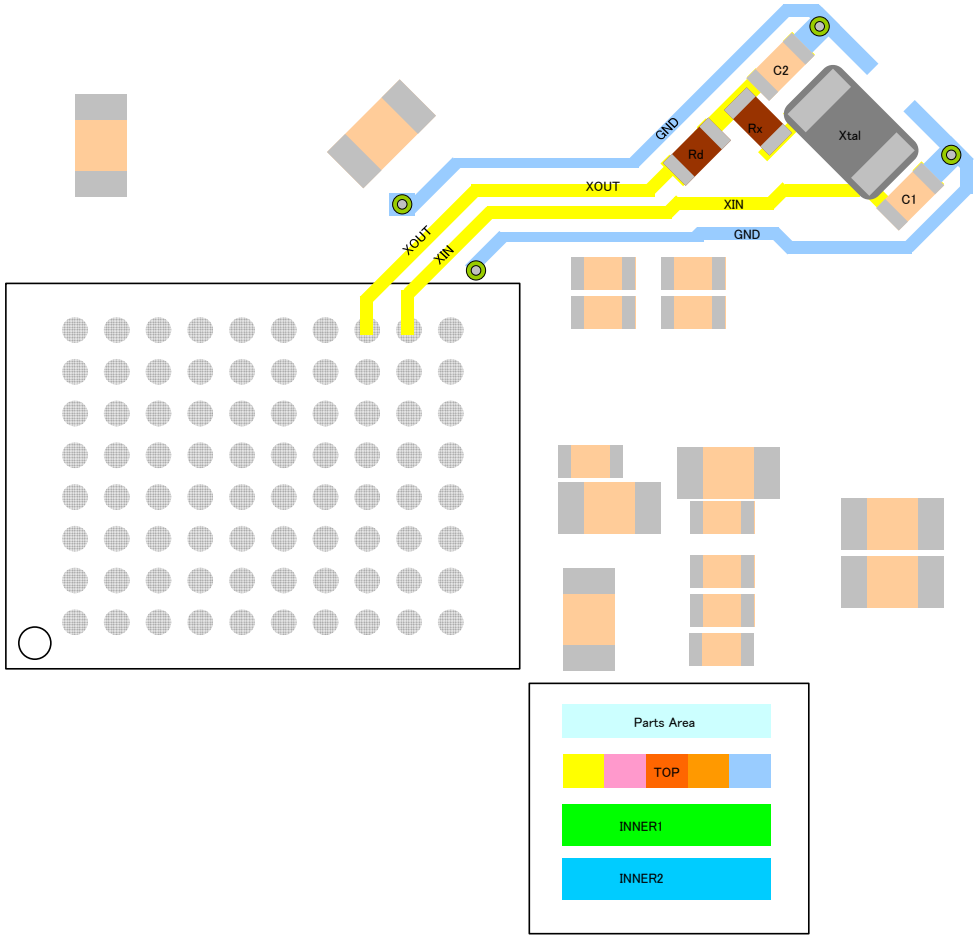


Fig. 1-7: Example of RTC Block Pattern (Top Layer)

(1) Place the crystal unit as close as possible to the RC5T619-1xxx, the route the line on the single layer without via as short as possible, and not add a redundant line like Monitoring Line.
(2) Place the input and output capacitors (C1 and C2 shown in Fig.1-7) as close as possible to the crystal unit, in order to reduce the extra parasitic resistance and capacitance.
(3) Draw Land Patterns for Rx and Rd previously, because an adjustment by adding Rx and Rd is required when the using oscillator exceeds its "Drive Level" specs.
(4) Connect the GND of the oscillation circuit with special GND plane on the component layer, and then connect with the internal GND plane by via or through hole.
Don’t route the sensitive line on the layer just under the oscillation circuit.
Also, do not place GND between pads of the oscillator to prevent a parasitic resistance.

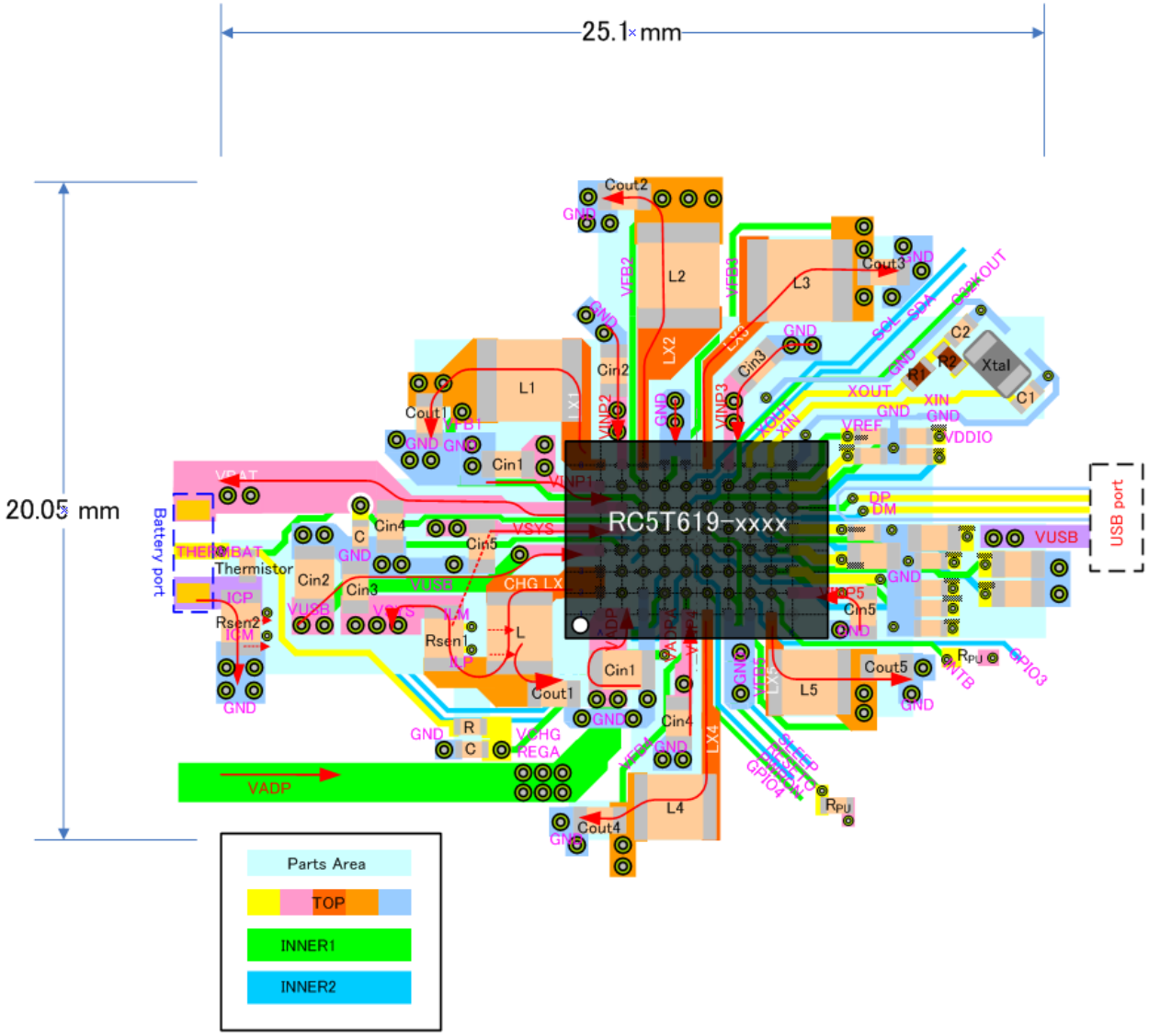
2. Recommended External Parts List

Block	Pin Name	RC5T619-1xxx External Parts								
		Parts Value	Parts No.	Model value	Vender	Num	Parts Size [mm]			
							X Size	Y Size	Z Size	[mm2]
PMU	-	-	DUT1	RC5T619	RICOH	1	6.00	8.00	0.85	48
CPU_IF	SDA	-	-	-	-	0	0.00	0.00	0.00	0
	SCL	-	-	-	-	0	0.00	0.00	0.00	0
RTC	C32KOUT	-	-	-	-	0	0.00	0.00	0.00	0
Power	PWRON	-	-	-	-	0	0.00	0.00	0.00	0
	SLEEP	-	-	-	-	0	0.00	0.00	0.00	0
	RESETO	-	-	-	-	0	0.00	0.00	0.00	0
INTC	INTB	-	-	-	-	0	0.00	0.00	0.00	0
GPIO	GPIO0	-	-	-	-	0	0.00	0.00	0.00	0
	GPIO1	-	-	-	-	0	0.00	0.00	0.00	0
	GPIO2	1.0uF	C30	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	GPIO3	-	-	-	-	0	0.00	0.00	0.00	0
	GPIO4	-	-	-	-	0	0.00	0.00	0.00	0
TEST	TESTEN	-	-	-	-	0	0.00	0.00	0.00	0
RTC	VSB	1.0uF	C61	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
		100ohm	R19	RK73H1ETTP101F	KOA	1	1.00	0.50	0.50	0.5
		-	BAT1	-	-	0	5.00	5.00	1.00	0
	XOUT	12pF	C22	C1005CH1H120J	TDK	1	1.00	0.50	0.50	0.5
		0ohm	R25	RK73Z1ETTP-RL	KOA	1	1.00	0.50	0.50	0.5
	XIN/XOUT	32.768kHz	X1	FC-12M_32.768kHz,9pF	SEIKO EPSON	1	2.05	1.20	0.60	2.46
		0ohm	R24	RMC1/16JPTP	KAMAYA	1	1.60	0.80	0.80	1.28
	XIN	12pF	C21	C1005CH1H120J	TDK	1	1.00	0.50	0.50	0.5
Power Supply	VDDIO	0.1uF	C16	GRM155R11C104KA88B	murata	1	1.00	0.50	0.50	0.5
DCDC	VINP1	10uF	C1	C1608JB0J106M	TDK	1	1.60	0.80	0.80	1.28
	LX1	1.0uH	L1	DFE322512C-1R0N	TOKO	1	3.20	2.50	1.20	8
	VFB1	22uF	C41	JMK107BJ226MA-TD	TAIYO	1	1.60	0.80	0.80	1.28
	VINP2	10uF	C2	C1608JB0J106M	TDK	1	1.60	0.80	0.80	1.28
	LX2	1.0uH	L2	DFE322512C-1R0N	TOKO	1	3.20	2.50	1.20	8
	VFB2	22uF	C42	JMK107BJ226MA-TD	TAIYO	1	1.60	0.80	0.80	1.28
	VINP3	10uF	C3	C1608JB0J106M	TDK	1	1.60	0.80	0.80	1.28
	LX3	1.0uH	L3	DFE322512C-1R0N	TOKO	1	3.20	2.50	1.20	8
	VFB3	22uF	C43	JMK107BJ226MA-TD	TAIYO	1	1.60	0.80	0.80	1.28
	VINP4	10uF	C4	C1608JB0J106M	TDK	1	1.60	0.80	0.80	1.28
	LX4	1.0uH	L4	DFE252012C-1R0M	TOKO	1	2.50	2.00	1.20	5
	VFB4	22uF	C44	JMK107BJ226MA-TD	TAIYO	1	1.60	0.80	0.80	1.28
	VINP5	10uF	C5	C1608JB0J106M	TDK	1	1.60	0.80	0.80	1.28
	LX5	1.0uH	L5	DFE252012C-1R0M	TOKO	1	2.50	2.00	1.20	5
	VFB5	22uF	C45	JMK107BJ226MA-TD	TAIYO	1	1.60	0.80	0.80	1.28
LDO	VINL1	1.0uF	C6	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VINL2	1.0uF	C7	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VINL3	1.0uF	C8	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VINL4	1.0uF	C9	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VOUT1	4.7uF	C51	C1608JB0J475K	TDK	1	1.60	0.80	0.80	1.28
	VOUT2	4.7uF	C52	C1608JB0J475K	TDK	1	1.60	0.80	0.80	1.28
	VOUT3	4.7uF	C53	C1608JB0J475K	TDK	1	1.60	0.80	0.80	1.28
	VOUT4	4.7uF	C54	C1608JB0J475K	TDK	1	1.60	0.80	0.80	1.28
	VOUT5	1.0uF	C55	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VOUT6	1.0uF	C56	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VOUT7	1.0uF	C57	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VOUT8	1.0uF	C58	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VOUT9	1.0uF	C59	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VOUT10	1.0uF	C60	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VREF	1.0uF	C63	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
EXT I/F	DP	-	-	-	-	0	0.00	0.00	0.00	0
	DM	-	-	-	-	0	0.00	0.00	0.00	0
Charger	VADP1 VADP2	10uF	C10	EMK212ABJ106KG	TAIYO	1	2.00	1.25	1.25	2.5
	VADPA	-	C12	-	-	0	1.00	0.50	0.50	0
	VUSB	4.7uF	C11	GRM21BB31E475KA75B	Murata	1	2.00	1.25	1.25	2.5
	VUSBA	-	C13	-	-	0	1.00	0.50	0.50	0
	CHG_LX1 CHG_LX2	1.0uH	L6	DFE252012C-1R0N	TOKO	1	2.50	2.00	1.20	5
	ILP	10uF	C14	LMK107BBJ106MALT	TAIYO	1	1.60	0.80	0.80	1.28
	ILP/ILM	20mohm	R6	ERJ6BWFR020V	Panasonic	1	2.00	1.25	0.60	2.5
	VSYS1 VSYS2	22uF	C15	JMK107BJ226MA-TD	TAIYO	1	1.60	0.80	0.80	1.28
	VBAT1 VBAT2	4.7uF	C17	C1608JB0J475K	TDK	1	1.60	0.80	0.80	1.28
	VCHGREGA	1.0uF	C64	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	VCHGREGD	1.0uF	C65	GRM155B31A105KE15	murata	1	1.00	0.50	0.50	0.5
	THERMBAT	10kohm	R12	RGC1/16SC103DTH	KAMAYA	1	1.00	0.50	0.35	0.5
	ICP	Thermistor	R13	TH05-3H103F	MITSUBISHI	1	1.00	0.50	0.50	0.5
	ICP/ICM	20mohm	R7	ERJ6BWFR020V	Panasonic	1	2.00	1.25	0.60	2.5
					Total Num	52			Total Parts size	133.5

dummy pattern at RC5T619 CSP Evaluation Board

Table 2-1: Recommended external parts list

3. Example of Parts Layout



Total Parts Area 269.4 mm^2

Fig. 3-1: Example PCB Parts Layout