

*POWER MANAGEMENT SYSTEM DEVICE*

# RC5T619-XXXX

*Product Brief*

**Rev3.0**

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Electronic Devices Company

This specification is subject to change without notice.

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## 1. Outline

This IC is the power management IC for GPS-PND/MID and Smart-Phone.

It integrates five high-efficiency step-down DCDC Converters, twelve low dropout regulators, power control logic, Li-ion Battery Charger, I2C-Bus Interface, voltage detections, thermal shut-down, and etc.

## 2. Feature

- System
  - ✓ I2C-Bus interface @3.4MHz and 400kHz
  - ✓ Detector Function (System/IO/Battery-Voltage-detector, UVLO)
  - ✓ Thermal Shutdown Function
  - ✓ Watchdog timer
  - ✓ Power on key input for System's power up
  - ✓ Power on reset output for CPU
  - ✓ Flexible power-on/off sequence by OTP
  - ✓ Flexible DCDCx and LDOx default-on/off control by OTP
- High Efficiency Step-down DC/DC Converters
  - ✓ DCDC1-3            0.6V-3.5V            Max 3000mA
  - ✓ DCDC4-5           0.6V-3.5V            Max 2000mA
  - ✓ Soft-start circuit
- Low Drop Voltage Regulators
  - ✓ LDO1-4 with ECO   0.9V-3.5V            Max 300mA
  - ✓ LDO5-6 with ECO   0.6V-3.5V            Max 300mA
  - ✓ LDO7-10            0.9V-3.5V            Max 200mA
  - ✓ LDORTC1            1.7-3.5V            Max 10mA (AlwaysOn, For coin battery)
  - ✓ LDORTC2            0.9-3.5V            Max 10mA (AlwaysOn)
  - ✓ Over current Protection and Short circuit Protection.
- Li-ion Battery Charger
  - ✓ Supports AC adapter charging and USB charging in an individual port.
  - ✓ With the current limit protection and charge current control.
  - ✓ The system can power on even when Li-ion Battery is low voltage or open.
  - ✓ Rapid timer and Trickle timer.
  - ✓ Power-path control.
  - ✓ Over temperature protection
- USB External device interface
- Fuel Gauge
  - ✓ 12-bit resolution.
  - ✓ 1 second integration.
- ADC
  - ✓ 12-bit resolution A/D converter
  - ✓ Eight channels: LIMMON, VADP, VUSB, VBAT, VSYS, THERMBAT and two external(GPIO) pins.
  - ✓ Single/Auto conversion mode
  - ✓ Detect high/low thresholds which can be set
- 5ch-GPIO
  - ✓ Supports interrupt function (level/edge) for input signals
  - ✓ Outputs power-on signal for external devices
  - ✓ Power on/off input for System's power up/down
  - ✓ DCDCx and LDOx can be controlled by external input
  - ✓ GPIO2 can output LDORTC2
  - ✓ GPIO0 and GPIO1 have input to ADC for voltage monitor
  - ✓ GPIO0 and GPIO1 have maximum 15mA sink for LED.
- Real-Time Clock (RTC)
  - ✓ Alarm function
  - ✓ Backup current 2.0μA (typ)
- Interrupt Controller (INTC)
- Package CSP0606-85(0.5mm pitch) or CSP0608-80(0.65mm pitch)
- Process CMOS

### 3. Block Diagram

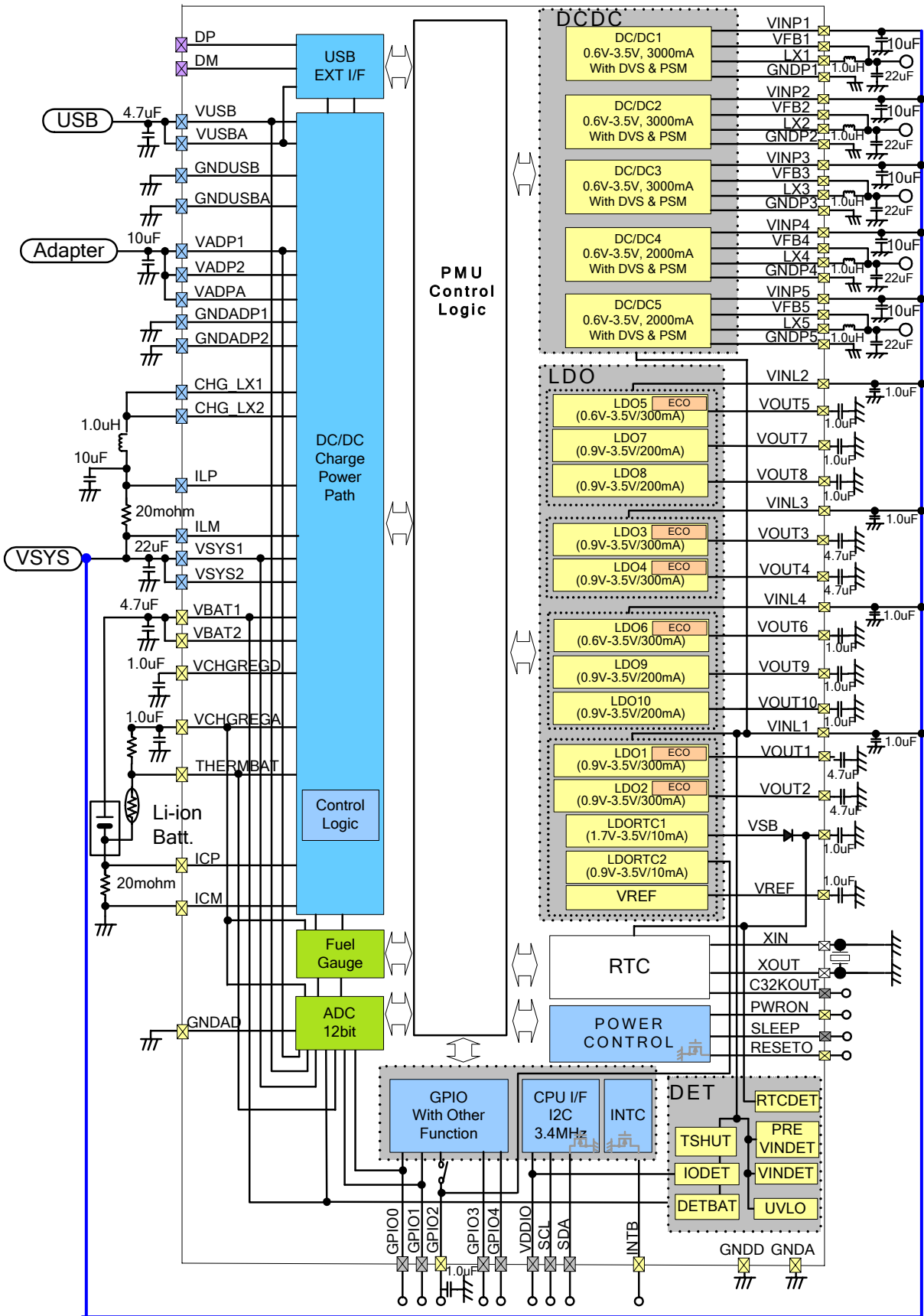


Fig 3-1 Block Diagram

## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings

Exposure to the condition exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

Symbol	Parameter	Condition	Min	Max	Units
V <sub>PS1</sub>	Power Supply Voltage 1	VADP*, VUSB* pin	-0.3	7.0	V
V <sub>PS2</sub>	Power Supply Voltage 2	VINP1-5, VINL1-4, VSYS1-2, VBAT1-2 pin	-0.3	6.0	V
V <sub>PS3</sub>	Power Supply Voltage 3	VDDIO pin	-0.3	4.5	V
V <sub>INPUT</sub>	Input Voltage Range	PWRON, RESET0, INTB, SLEEP pin	-0.3	VSYS + 0.3	V
		SDA, SCL pin	-0.3	VDDIO + 0.3	V
		GPIO0-1 pin	-0.3	VSYS + 0.3 / VDDIO + 0.3	V
		GPIO2-4 pin	-0.3	VSYS + 0.3	V
		AIN0-1(GPIO0-1) pin	-0.3	2.8	V
T <sub>stg</sub>	Storage Temperature	-	-55	125	degrees C
PD	Package Allowable Dissipation	CSP0608-80 Package T <sub>a</sub> = 25 degrees C	0	2500	mW
		CSP0606-85 Package T <sub>a</sub> = 25 degrees C	0	2200	mW

Table 4-1 Absolute Maximum Ratings

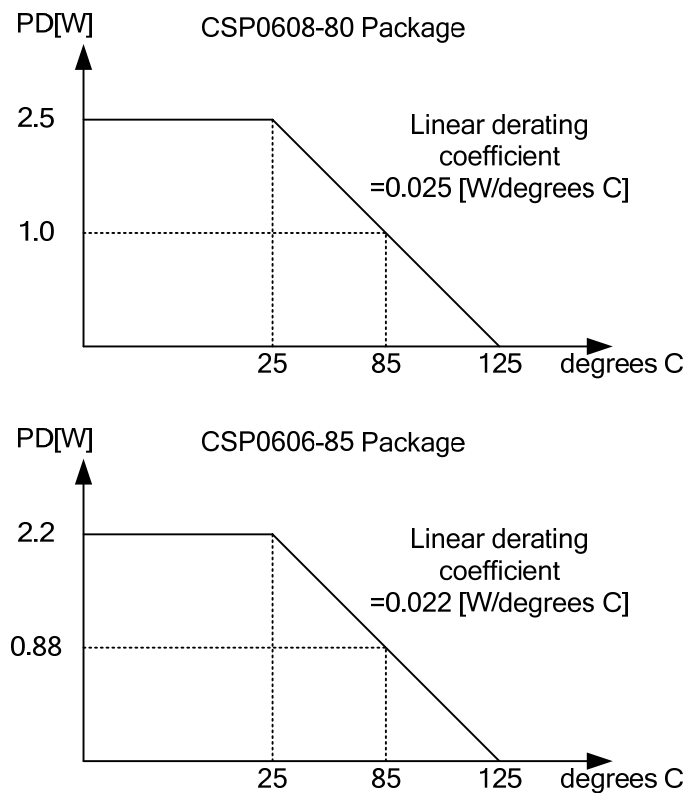


Fig 4-1 Maximum Package Allowable Dissipation

## 4.2 Recommendation of Operation Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VADP	Power Supply Voltage	VADP* pin	4.5	5.0	5.5	V
VUSB	Power Supply Voltage	VUSB* pin	4.5	5.0	5.5	V
VSYS	Power Supply Voltage	VINP1-5, VINL1,VINL3, VSYS1-2, VBAT1-2 pin	2.7	3.6	5.5	V
VINL2	Power Supply Voltage	VINL2,VINL4	1.7	3.6	5.5	V
VDDIO	Power Supply Voltage	VDDIO pin (VSYS>VDDIO)	1.7	1.8	3.4	V
VSB	Power Supply Voltage	VSB pin	1.45	3.1	3.4	V
*GND*	Ground	GND		0		V
Ta	Temperature of Operation	-	-40		85	degrees C

Table 4-2 Recommendation of Operation Conditions

### 4.3 I/O Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
<i>VSYS NMOS Input Pin: PWRON, SLEEP, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4</i>						
VIL	Low level input voltage				0.4	V
VIH	High level input voltage		1.4		VSYS	V
<i>VSYS Nch Open Drain output Pin : RESET0</i>						
VOL	Low level output voltage	Iout = 2mA			0.4	V
Vto	Tolerant				VSYS	V
<i>VSYS CMOS input/output Pin : GPIO0, GPIO1, GPIO2, GPIO3, GPIO4</i>						
VIL	Low level input voltage				VSYS*0.2	V
VIH	High level input voltage		VSYS*0.8		VSYS	V
VOL	Low level output voltage	Iout = 4mA			0.4	V
VOH	High level output voltage	Iout = -4mA	VSYS-0.4			V
<i>VSYS Nch Open Drain output Pin : INTB, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4</i>						
VOL	Low level output voltage	Iout = 4mA			0.4	V
Vto	Tolerant				VSYS	V
<i>VSYS Nch Open Drain output Pin: GPIO0, GPIO1(for LED)</i>						
VOL	Low level output voltage	Iout = 15mA			0.4	V
Vto	Tolerant				VSYS	V
Symbol	Parameter	Condition	Min	Typ	Max	Units
<i>VDDIO CMOS input Pin (Schmitt Input): SCL</i>						
VIL	Low level input voltage				VDDIO*0.3	V
VIH	High level input voltage		VDDIO*0.7		3.4	V
ΔVI	Hysteresis		VDDIO*0.1			V
<i>VDDIO CMOS input/output Pin(Schmitt Input / Nch Open Drain output) : SDA</i>						
VIL	Low level input voltage				VDDIO*0.3	V
VIH	High level input voltage		VDDIO*0.7		3.4	V
ΔVI	Hysteresis		VDDIO*0.1			V
VOL	Low level output voltage	Iout = 3mA			0.4	V
<i>VDDIO CMOS input/output Pin : GPIO0, GPIO1</i>						
VIL	Low level input voltage				VDDIO*0.2	V
VIH	High level input voltage		VDDIO*0.8		VDDIO	V
VOL	Low level output voltage	Iout = 4mA			0.4	V
VOH	High level output voltage	Iout = -4mA	VDDIO-0.4			V
<i>VDDIO CMOS output Pin : C32KOUT</i>						
VOL	Low level output voltage	Iout = 2mA			0.4	V
VOH	High level output voltage	Iout = -2mA	VDDIO-0.4			V

Table 4-3 I/O Electrical Characteristics

## 4.4 Consumption Current

Operating Conditions (unless otherwise specified)  $T_a = 25$  degrees C,  $V_{IN} = 3.6V$ , No-load

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{ST}$	Standby current	PowerOff (Note*1)		23		$\mu A$
$I_{OP}$	Operating current	PowerOn (Note*1)		560		$\mu A$
$I_{SLP}$	Sleep current	Sleep (Note*1)		138		$\mu A$

Table 4-4 Consumption Current

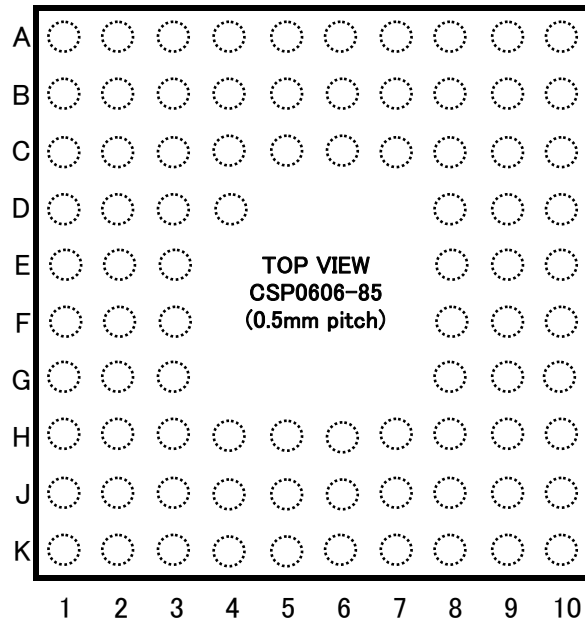
Note\*1) Each condition is below (Not include the current of thermistor)

	Power-Off	Power-On	Sleep
LDO1	-	○	-
LDO2	-	○	-
LDO3	-	○	○(ECO)
LDO4	-	○	○(ECO)
LDO5	-	○	-
LDO6	-	-	-
LDO7	-	-	-
LDO8	-	-	-
LDO9	-	-	-
LDO10	-	-	-
LDORTC1	○	○	○
LDORTC2	-	-	-
VREF	○	○	○
DCDC1	-	○	-
DCDC2	-	○	○(ECO)
DCDC3	-	-	-
DCDC4	-	-	-
DCDC5	-	-	-
UVLO	○	○	○
VINDET	○	○	○
IODET	○	○	○
PREVINDET	-	○	○
TSHUT	-	○	○
ADC	-	-	-
FuelGauge	-	○	○
VCHGREGD	○	○	○
VCHGREGA	-	○	○
CHG_DCDC	-	-	-
Internal Logic	○	○	○



## 5. Pin Configuration

### 5.1 CSP0606-85 Package

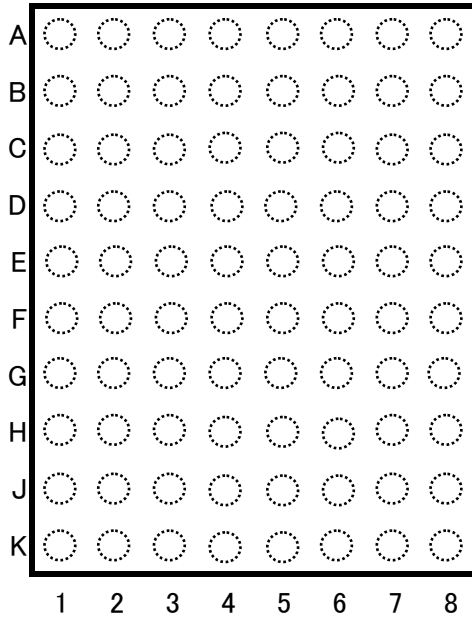


A	NC	CHG_LX1	CHG_LX2	VUSB	GNDUSBA	VSYS1	VBAT1	VINP1	LX1	LX1		
B	VADP1	VADP2	VUSBA	GNDUSB	VCHGREGD	VSYS2	VBAT2	GNDP1	GNDP1	VINP2		
C	GNDADP1	GNDADP2	ICP	ILP	ILM	THERMBAT	VFB1	VFB2	LX2	LX2		
D	VADPA	VCHGREGA	ICM	GNDAD	TOP VIEW CSP0606-85 (0.5mm pitch)			GPIO0	VFB3	GNDP2		
E	VINP4	VFB4	GNDA	GNDP3				GNDP3	GNDP3	GNDD	GPIO1	GNDP3
F	LX4	INTB	PWRON	SCL				LX3	LX3	SCL	LX3	LX3
G	GNDP4	GPIO3	SLEEP	SDA				C32KOUT	VINP3	SDA	C32KOUT	VINP3
H	GNDP5	VFB5	RESETO	VINL4	VINL3	VINL1	VINL2	VDDIO	VREF	XOUT		
J	LX5	GPIO4	VOUT9	VOUT4	VOUT1	VOUT2	VOUT8	DM	VS	XIN		
K	NC	VINP5	VOUT10	VOUT6	VOUT3	VOUT5	VOUT7	DP	GPIO2	TESTEN		
	1	2	3	4	5	6	7	8	9	10		

Fig 5-1 Package Information (CSP0606-85pin, 0.5mm pitch)

5.2 CSP0608-80 Package

TOP VIEW (CSP0608-80 : 0.65mm pitch)



TOP VIEW (CSP0608-80 : 0.65mm pitch)

A	VADP2	CHG_LX2	CHG_LX1	VUSB	VSYS1	VBAT1	VINP1	LX1
B	VADP1	GNDUSB	GNDUSBA	VCHGREGD	VSYS2	VBAT2	GNDP1	VINP2
C	GNDADP1	GNDADP2	VUSBA	ILP	ILM	VFB1	VFB2	LX2
D	VADPA	VCHGREGA	ICM	GNDAD	THERMBAT	GPIO0	VFB3	GNDP2
E	VINP4	VFB4	ICP	PWRON	GPIO1	SDA	SCL	GNDP3
F	LX4	GPIO4	GND	SLEEP	RESETO	VDDIO	GNDD	LX3
G	GNDP4	VFB5	VINL4	VINL3	VINL1	GPIO2	C32KOUT	VINP3
H	GNDP5	GPIO3	VOUT9	VOUT1	VINL2	VOUT7	VREF	XOUT
J	LX5	INTB	VOUT10	VOUT4	VOUT2	DM	VSB	XIN
K	NC	VINP5	VOUT6	VOUT3	VOUT5	DP	VOUT8	TESTEN
	1	2	3	4	5	6	7	8

Fig 5-2 Package Information (CSP0608-80pin, 0.65mm pitch)

## 6. Pin Description

Block	Pin Name	Pin		Function	I/O	D/A	Reset State (Note*1)	Vinmax [V] (Note*2)	Note	
		CSP0606-85	CSP0608-80							
Digital										
CPU_IF	SDA	G8	E6	I2C-Bus Data input/Output	I/O	D	I	-	VDDIO+0.3	Schmitt, NOD
	SCL	F8	E7	I2C-Bus Clock input	I	D	I	-	VDDIO+0.3	CMOS
RTC	C32KOUT	G9	G7	32.768kHz clock buffer output	O	D	O	Clock-out	VDDIO+0.3	CMOS
Power	PWRON	F3	E4	External power on signal input	I	D	I	-	VSYS+0.3	1.4V to VSYS
	SLEEP	G3	F4	Stand-by mode control signal input	I	D	I	-	VSYS+0.3	1.4V to VSYS
	RESETO	H3	F5	Host Reset output	O	D	O	Low	VSYS+0.3	NOD
INTC	INTB	F2	J2	Interrupt request output	O	D	O	Hi-z	VSYS+0.3	NOD
GPIO	GPIO0	D8	D6	General purpose I/O	I/O	D		Note*3	VSYS+0.3/DDIO+0.3	Note*3
	GPIO1	E9	E5	General purpose I/O	I/O	D		Note*3	VSYS+0.3/DDIO+0.3	Note*3
	GPIO2	K9	G6	General purpose I/O	I/O	D		Note*3	VSYS+0.3	Note*3
	GPIO3	G2	H2	General purpose I/O	I/O	D		Note*3	VSYS+0.3	Note*3
	GPIO4	J2	F2	General purpose I/O	I/O	D		Note*3	VSYS+0.3	Note*3
TEST	TESTEN	K10	K8	for TEST (Connect to GND)	I	D	I	PD	VSYS+0.3	CMOS Schmitt

Note\*1: Reset State: RESETO=Low.

Note\*2:Vinmax:Maximum input voltage

Note\*3:GP00-GP04 : "Input" or "Output" is selectable by OTP. Input/Output type (CMOS or NMOS or Analog or Nch Open Drain Output) is selectable by OTP.

Block	Pin Name	Pin		Function	I/O	D/A	Note
		CSP0606-85	CSP0608-80				
RTC	VSB	J9	J7	Coin-charger output (Power supply for RTC)	O	A	
	XOUT	H10	H8	32.768kHz crystal oscillator output	O	A	
	XIN	J10	J8	32.768kHz crystal oscillator Input	I	A	

Block	Pin Name	Pin		Function	I/O	D/A	Note
		CSP0606-85	CSP0608-80				
Power Supply							
	VDDIO	H8	F6	Power supply for CPU IF	-	P	
	GNDD	E8	F7	GND for Logic circuit	-	G	
	GNDAD	D4	D4	Ground for ADC	-	G	
	GNDA	E3	F3	Ground for Analog circuit	-	G	

Block	Pin Name	Pin		Function	I/O	D/A	Note
		CSP0606-85	CSP0608-80				
DCDC							
DCDC1	VINP1	A8	A7	Power supply for DC/DC1	-	P	
	LX1	A9,A10	A8	DC/DC1 switch output	O	A	
	VFB1	C7	C6	DC/DC1 Output voltage feedback input	I/O	A	
	GNDP1	B8,B9	B7	Ground for DC/DC1	-	G	
DCDC2	VINP2	B10	B8	Power supply for DC/DC2	-	P	
	LX2	C9,C10	C8	DC/DC2 switch output	O	A	
	VFB2	C8	C7	DC/DC2 Output voltage feedback input	I/O	A	
	GNDP2	D10	D8	Ground for DC/DC2	-	G	
DCDC3	VINP3	G10	G8	Power supply for DC/DC3	-	P	
	LX3	F9,F10	F8	DC/DC3 switch output	O	A	
	VFB3	D9	D7	DC/DC3 Output voltage feedback input	I/O	A	
	GNDP3	E10	E8	Ground for DC/DC3	-	G	
DCDC4	VINP4	E1	E1	Power supply for DC/DC4	-	P	
	LX4	F1	F1	DC/DC4 switch output	O	A	
	VFB4	E2	E2	DC/DC4 Output voltage feedback input	I/O	A	
	GNDP4	G1	G1	Ground for DC/DC4	-	G	
DCDC5	VINP5	K2	K2	Power supply for DC/DC5	-	P	
	LX5	J1	J1	DC/DC5 switch output	O	A	
	VFB5	H2	G2	DC/DC5 Output voltage feedback input	I/O	A	
	GNDP5	H1	H1	Ground for DC/DC5	-	G	

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Block	Pin Name	Pin		Function	I/O	D/A	Note
		CSP0606-85	CSP0608-80				
LDO							
LDO	VINL1	H6	G5	Power supply for DCDC analog, LDO1, LDO2, LDORTC1, 2, VREF, DET, IO and etc	-	P	
	VINL2	H7	H5	Power supply for LDO5, LDO7 and LDO8	-	P	
	VINL3	H5	G4	Power supply for LDO3 and LDO4	-	P	
	VINL4	H4	G3	Power supply for LDO6, LDO9 and LDO10	-	P	
	VOUT1	J5	H4	LDO1 output	O	A	
	VOUT2	J6	J5	LDO2 output	O	A	
	VOUT3	K5	K4	LDO3 output	O	A	
	VOUT4	J4	J4	LDO4 output	O	A	
	VOUT5	K6	K5	LDO5 output	O	A	
	VOUT6	K4	K3	LDO6 output	O	A	
	VOUT7	K7	H6	LDO7 output	O	A	
	VOUT8	J7	K7	LDO8 output	O	A	
	VOUT9	J3	H3	LDO9 output	O	A	
VOUT10	K3	J3	LDO10 output	O	A		
VREF	H9	H7	Bypass capacitor connecting pin	O	A	Connect only Capacitor load	

Block	Pin Name	Pin		Function	I/O	D/A	Note
		CSP0606-85	CSP0608-80				
Charger							
EXT I/F	DP	K8	K6	DP pin of the USB connector	I	A	
	DM	J8	J6	DM pin of the USB connector	I	A	
Charger	VADP1	B1	B1	Connected to AC Adapter	-	P	
	VADP2	B2	A1	Connected to AC Adapter	-	P	
	VADPA	D1	D1	Connected to AC Adapter	-	P	
	VUSB	A4	A4	Connected to USB	-	P	
	VUSBA	B3	C3	Connected to USB	-	P	
	CHG_LX1	A2	A3	Output VADP side for charge	O	A	
	CHG_LX2	A3	A2	Output VUSB side for charge	O	A	
	ILP	C4	C4	Sense resistance connection pin for limit current monitor (+)	I	A	
	ILM	C5	C5	Sense resistance connection pin for limit current monitor (+)	I	A	
	VSYS1	A6	A5	System power supply	-	P	
	VSYS2	B6	B5	System power supply	-	P	
	VBAT1	A7	A6	Li-ion battery input/output	-	P	
	VBAT2	B7	B6	Li-ion battery input/output	-	P	
	VCHGREGA	D2	D2	Capacitor connection for built-in Regulator	O	A	
	VCHGREGD	B5	B4	Capacitor connection for built-in Regulator	O	A	
	THERMBAT	C6	D5	Sense pins for Battery temperature	I	A	
	ICP	C3	E3	Sense resistance connection pin for charge current monitor (+)	I	A	
	ICM	D3	D3	Sense resistance connection pin for charge current monitor (-)	I	A	
	GNDADP1	C1	C1	Ground	-	G	
	GNDADP2	C2	C2	Ground	-	G	
GNDUSB	B4	B2	Ground	-	G		
GNDUSBA	A5	B3	Ground	-	G		

Table 6-1 Pin Description

## 7. Power Control

This PMU has the power-on/off sequence that can be flexibly set by OTP. The default on/off, timing, and voltage of DCDCx and LDOx are programmable. In addition, GPIO0-GPIO4 pins output the power-on/off signal to external LDO/DCDC by the setting of OTP.

### 7.1 State Machine Diagram

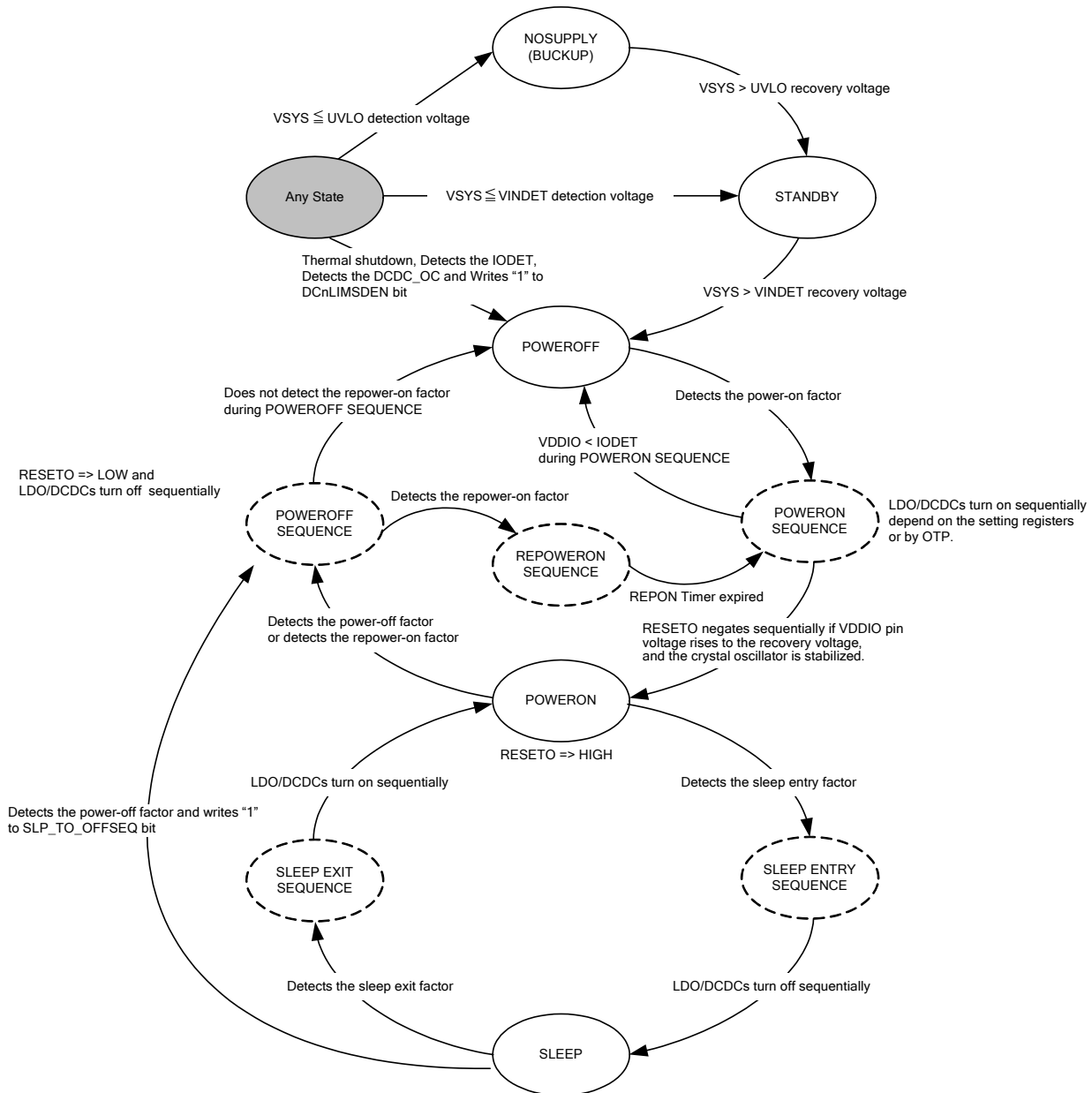


Fig 7-1 Power Control State Machine Diagram

## 8. Regulator

### 8.1 Regulator Table

Symbol	DCDC1	DCDC2	DCDC3	DCDC4	DCDC5
Initial Output Voltage	0.6-3.5V	0.6-3.5V	0.6-3.5V	0.6-3.5V	0.6-3.5V
Maximum Output Current	3000mA	3000mA	3000mA	2000mA	2000mA
External Inductor	1 $\mu$ H	1 $\mu$ H	1 $\mu$ H	1 $\mu$ H	1 $\mu$ H
External Capacitor	22 $\mu$ F	22 $\mu$ F	22 $\mu$ F	22 $\mu$ F	22 $\mu$ F
Output Control	I2C	I2C	I2C	I2C	I2C

Table 8-1 Regulator Table (DC/DC)

Symbol	LDO1	LDO2	LDO3	LDO4	LDO5
Initial Output Voltage	0.9-3.5V	0.9-3.5V	0.9-3.5V	0.9-3.5V	0.6-3.5V
Maximum Output Current	300mA	300mA	300mA	300mA	300mA
External Capacitor	4.7 $\mu$ F	4.7 $\mu$ F	4.7 $\mu$ F	4.7 $\mu$ F	1 $\mu$ F
Output Control	I2C	I2C	I2C	I2C	I2C

Symbol	LDO6	LDO7	LDO8	LDO9	LDO10
Initial Output Voltage	0.6-3.5V	0.9-3.5V	0.9-3.5V	0.9-3.5V	0.9-3.5V
Maximum Output Current	300mA	200mA	200mA	200mA	200mA
External Capacitor	1 $\mu$ F	1 $\mu$ F	1 $\mu$ F	1 $\mu$ F	1 $\mu$ F
Output Control	I2C	I2C	I2C	I2C	I2C

Symbol	LDORTC1	LDORTC2			
Initial Output Voltage	1.7-3.5V	0.9-3.5V			
Maximum Output Current	10mA	10mA			
External Capacitor	1 $\mu$ F	1 $\mu$ F			
Output Control	Always On	Always On			

Table 8-2 Regulator Table (LDO)

## 9. Li-ion Battery Charger

This PMU integrates Li-ion battery charger with the power path control, and supports the following functions.

- ✓ Two external power input ports. ( VADP port for AC adapter , VUSB port for USB bus power )
- ✓ The charging current limit setting for the battery. (max 1.8A)
- ✓ The output current limit setting for system load. (max 2.5A for AC adapter input )
- ✓ Integrated MOSFET of battery side. (No external MOSFET required.)
- ✓ The full charging voltage setting for the various batteries. ( from 4.05V to 4.35V )
- ✓ The thermistor monitor for voltage control compliant with JEITA.

### 9.1 Li-ion Battery Charger Block Diagram

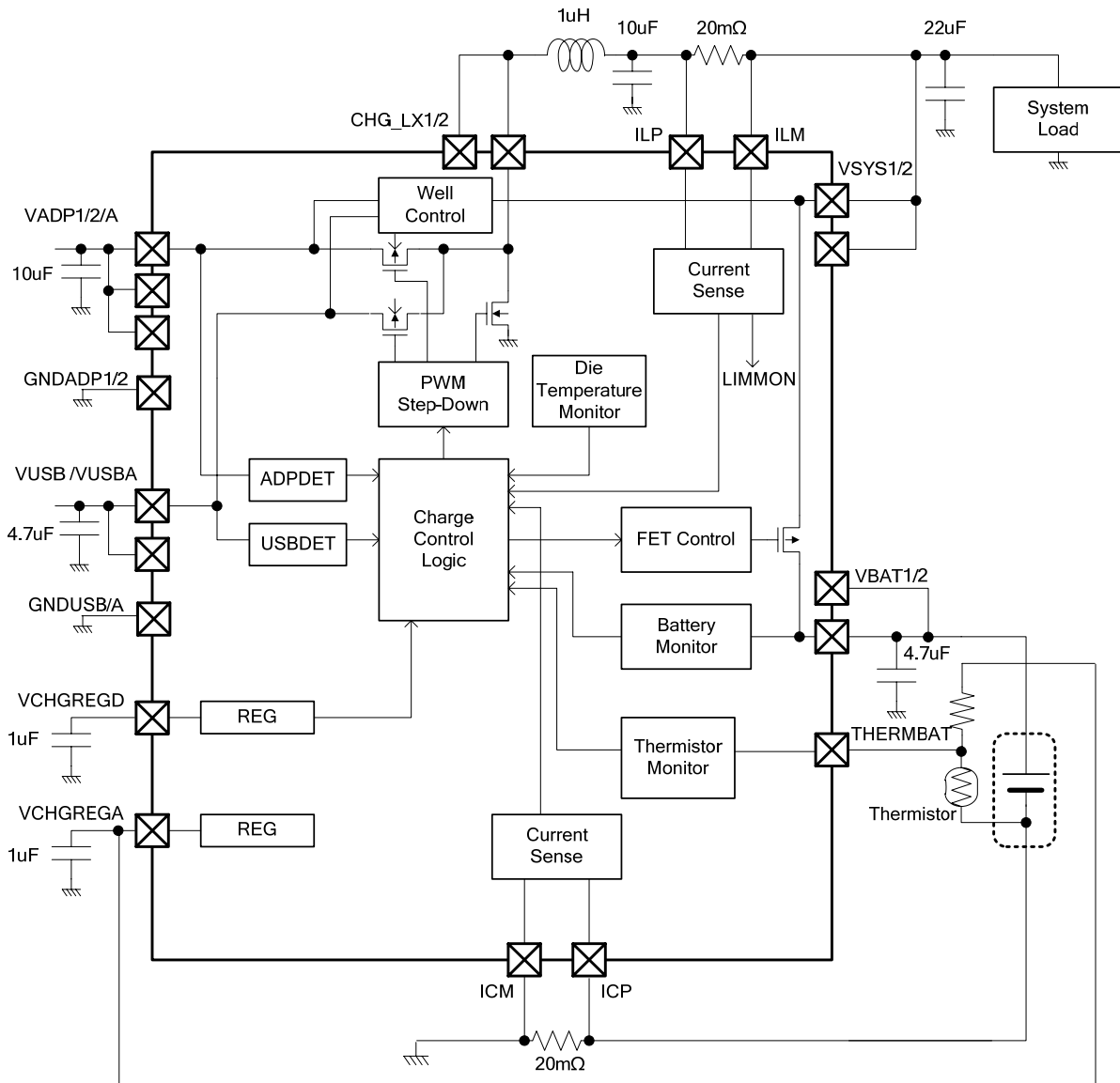


Fig 9-1 Li-ion Battery Charger Block Diagram

## 10. USB External Device Interface

This PMU integrates the external device detection function module. The devices that are compliant with USB Battery Charging Specification Rev.1.2 are called "Generic Charger" in this document. The others are called "Particular Charger" in this document.

This function is the following features.

- Compliant with USB Battery Charging Specification Rev.1.2 (other than ID detection)
- Capable of detecting the devices with the programmable setting.
- Control the DP/DM for detecting the external device port

### 10.1 Block Diagram

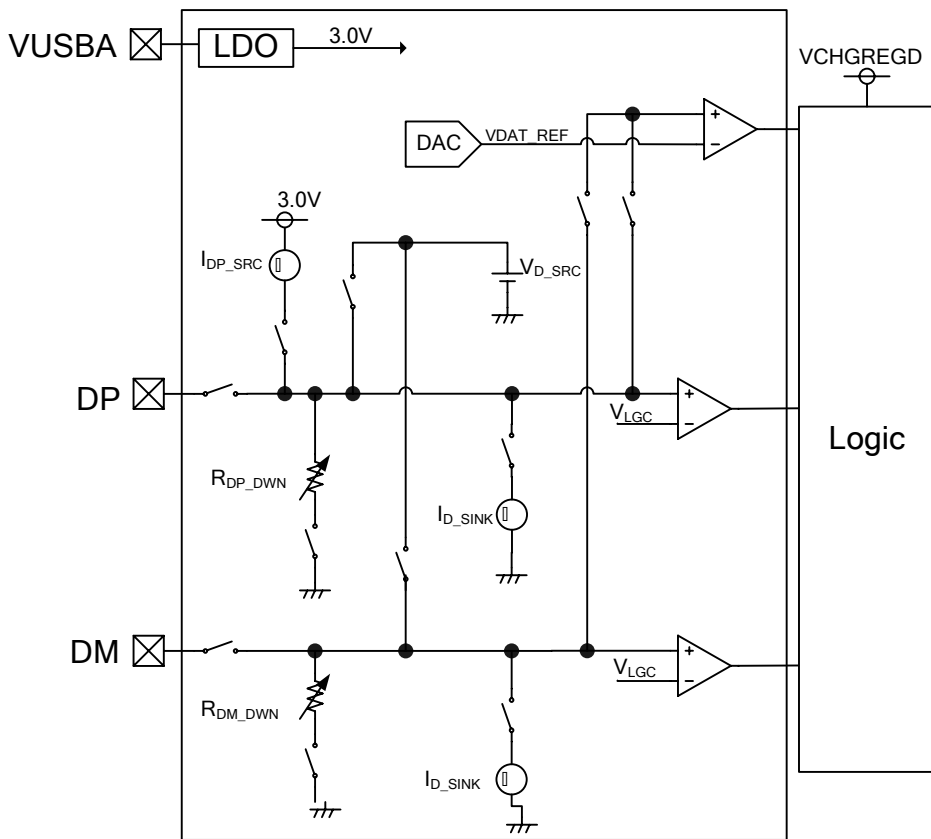


Fig 10-1 USB External Device Interface Block diagram



## 11. Fuel Gauge

This PMU integrates a Fuel Gauge.

- Battery Fuel Gauge for 1-Series Li-ion applications
- Measure battery voltage and temperature by AD converter (12bit)
- Measure battery current by original coulomb counter include offset cancel circuit
- Calculate remaining battery capacity compensate change that depends on temperature and aging
- Predict remaining battery life at present rate of discharge
- Predict remaining time until battery reaches full charge
- Display battery aging state

### 11.1 Fuel Gauge Block Diagram

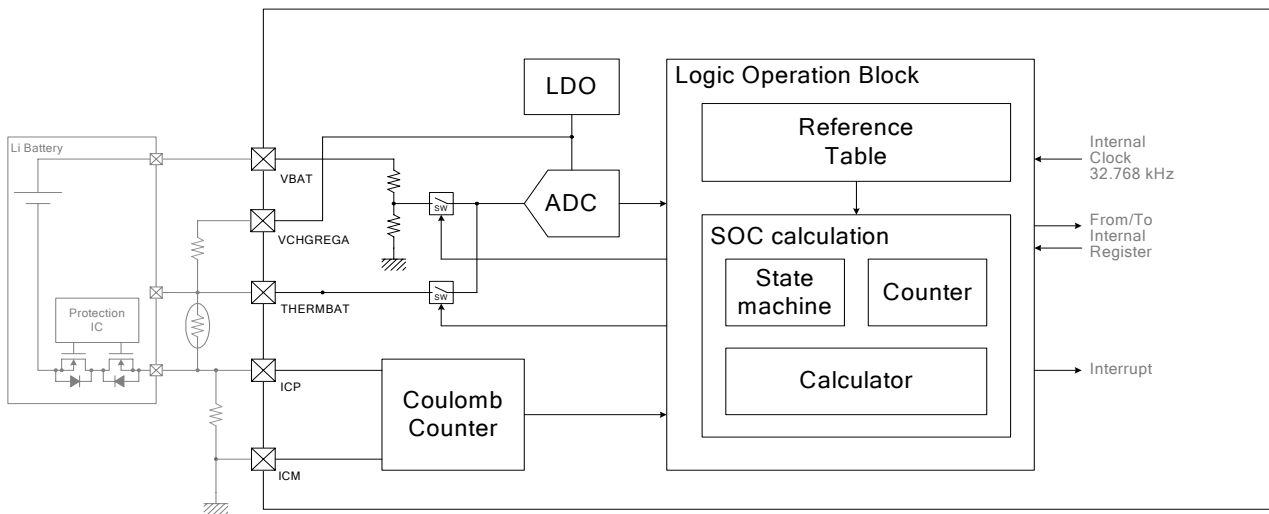


Fig 11-1 Fuel Gauge Block diagram

## 12. Real-Time Clock (RTC)

This PMU RTC has the following features;

- Time counters (counting hours, minutes, and seconds) and calendar counters (counting years, months, days, and weeks) (in BCD format)
- Interrupt circuit configured to generate interrupt signals (with interrupts ranging from 0.5 seconds to 1 month) to the CPU and provided with an interrupt flag and an interrupt halt
- One alarm interrupt circuit (Alarm\_D for year, month, day, hour, minute and second alarm settings)
- Built-in voltage detector
- With Power-on flag
- 32-kHz clock output pin (CMOS output.)
- Automatic identification of leap years up to the year 2099
- Selectable 12-hour and 24-hour mode settings
- High precision oscillation adjustment circuit

### 12.1 Block Diagram

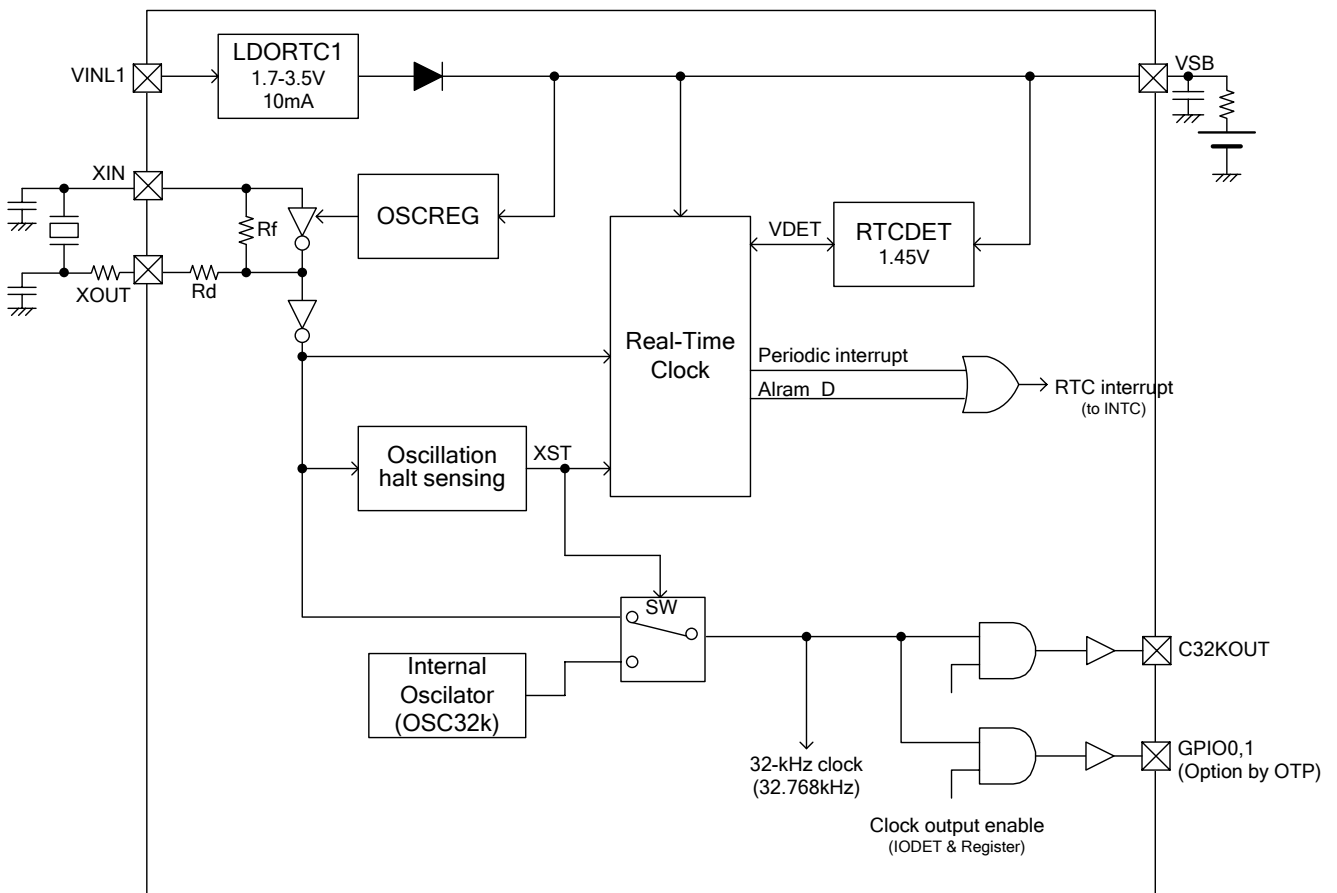


Fig 12-1 Real-Time Clock Block Diagram

## 13. ADC

This PMU has 12-bit A/D converter with 8-channel multiplexer.

- The eight inputs are LIMMON, VBAT, VADP, VUSB, VSYS, THERMBAT and two external pins.
- Built in voltage divider (VBAT, VADP, VUSB and VSYS).
- Single-mode / Auto-mode with the average calculation.
- In single-mode, ADC generates the interrupt signal at the end of conversion.
- In auto-mode, the interval of each conversion is programmable.
- In auto-mode, High/Low thresholds for ADC conversion result to generate the interrupt signal.

### 13.1 Block Diagram

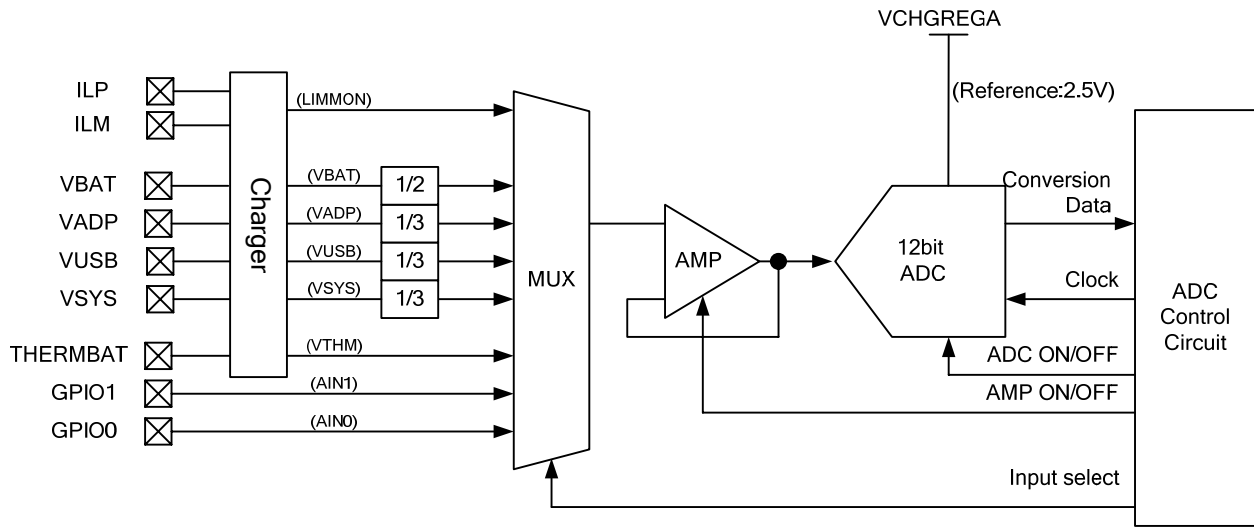


Fig 13-1 ADC Block Diagram

## 14. GPIO

This PMU supports five channels of general purpose input/output.  
GPIO0,1,2,3,4 pins have the function selected by OTP as shown below.

Name	Function	Input, *1,*2	Output, *1,*2	Power,*3	GPIO				
					0	1	2	3	4
AIN0	ADC Input	A	-	-	○	-	-	-	-
AIN1	ADC Input	A	-	-	-	○	-	-	-
N_OE	External power off	N	-	VSYS or VDDIO	○	○	○	○	○
GPIO0	General purpose I/O	C or N	C or N	VSYS or VDDIO	○	-	-	-	-
GPIO1	General purpose I/O	C or N	C or N	VSYS or VDDIO	-	○	-	-	-
GPIO2	General purpose I/O	C or N	C or N	VSYS	-	-	○	-	-
GPIO3	General purpose I/O	C or N	C or N	VSYS	-	-	-	○	-
GPIO4	General purpose I/O	C or N	C or N	VSYS	-	-	-	-	○
ONOB	PWRON pin monitor.	-	N	VSYS	○	○	○	○	○
PSO0	Power-on signal output function	-	C or N	VSYS or VDDIO	○	-	-	-	-
PSO1	Power-on signal output function		C or N	VSYS or VDDIO	-	○	-	-	-
PSO2	Power-on signal output function		C or N	VSYS	-	-	○	-	-
PSO3	Power-on signal output function		C or N	VSYS	-	-	-	○	-
PSO4	Power-on signal output function		C or N	VSYS	-	-	-	-	○
VBUSDET	VBUS voltage detector output	-	N	VSYS	○	○	○	○	○
VBATDET	VBAT voltage detector output	-	N	VSYS	○	○	○	○	○
LDORTC2	LDORTC2 output	-	A	-	-	-	○	-	-
C32KOUT	32 kHz clock output function	-	C or N	VSYS or VDDIO	○	○	-	-	-
LED	LED function	-	N	VSYS	○	○	-	-	-
PSHOLD	PSHOLD (power-on hold) function	N	-	VSYS	○	○	○	○	○
ON_EXTIN	External input for on factor	N	-	VSYS	○	○	○	○	○
**EXON	External LDO*/DCDC* on/off input	N	-	VSYS	*4	*4	*4	*4	*4

Note\*1: Explanation of column of "Input" and "Output" :

A : Analog Input/Output.

C : CMOS Input/Output.

N : NMOS Input(VSYS only)/ Nch Open Drain Output.

Note\*2: CMOS Output or Nch Open Drain Output is selectable by OTP.

Note\*3: VSYS or VDDIO is selectable by OTP.

Note\*4: Refer to the chapter of Mode.

Table 14-1 The function of GPIO0-4 pins

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Dec 2012

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