RC7222-A1

Multi-Functional Ethernet Converter

Datasheet

V1.00

Dec.2009

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Revision History

Version	Date	Description
V1.00	2009-12-4	Preliminary Released

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1 Overview

The RC7222-A1 is a highly integrated ASIC for transmitting Ethernet frames over TDM. The TDM interface is called Wide Access Network(WAN), which includes E1(framed or unframed) or PDH optical port. HDLC protocol is adopted to encapsulate the Ethernet frames, which is compatible with the protocol in the RJ017.

The RC7222-A1 supports mapping of the registers from the remote to the local over the PDH optical frame overhead or SA bits in the G.704 frame, that the MCU in local device can get information of the remote device only from registers of the local RC7222-A1. The RC7222-A1 also supports user-defined management frame, which can be encapsulated and transmitted together with Ethernet frames in HDLC format. Then the MCU can access for each other even over unframed E1.

In addition the RC7222-A1 can be configured by pins that is the RC7222-A1 can work well without MCU.

2 Features

- Ethernet Interface
  - Standard Media Independent Interface (MII) and MDIO management interface for connection to Ethernet PHY
  - 10M/100Mbps, full/half duplex supported, fully IEEE 802.3 compatible
  - Frames with length from 64 to 2031 bytes transparently transferred
  - Illegal frames such as CRC error packets, undersized packets (less than 64 bytes) and oversized packets (more than 2031 bytes) discarded
  - PAUSE flow control ability in full duplex mode
  - Exhaustive alarm detection and performance statistic
- E1/FE1 Interface
  - Compatible with ITU-T recommendations: G.703, G.704, G.706 and G.732
  - Optional line code: HDB3 or NRZ
  - Local oscillator or the clock recovered from the line for Timing source, more flexible for different applications

- Optical Interface
  - 4.096Mbps for channel rate,1B1C coding, with embedded line Clock Data Recovery (CDR) unit
  - A transparent user-defined asynchronous channel with 16KHz sampling frequency through optical frame overhead, which can be used as UART channel less than 4800bps.
  - TTL interface
  - Local oscillator or the clock recovered from the line for Timing source, more flexible for different applications
- G.704 framer /deframer
  - Support G.704 framer/deframer or G.704 bypass(Unframed E1)
  - PCM30/31 selectable
  - CRC-4/Non-CRC-4 multiframe auto adaptive for G.704 deframer, CRC-4 multiframe for G.704 framer only
  - A transparent synchronous 20Kbps data path provided by spare bits (SA) in FE1 mode
- Ethernet frame encapsulation
  - HDLC encapsulation, compatible with RJ017
- Management frame
  - HDLC encapsulation, transmitted with Ethernet frame in the same channel
- External 64Mbit SDRAM with cache from 32 to 512 frames
- Network Management
  - 19200bps UART interface and 100Kbps I^2C interface available for access
  - 8-bit device address
  - Register mapping of the remote RC7222-A1 through SA bits and register mapping of the PHY through MDIO
  - Software reset, that is the MCU can reset the chip through the register
  - Perfect alarm detection and performance statistic, provides performance statistic record with time in seconds
- Automatic line loop-back detection and stop transferring Ethernet frame to MII when a line loop-back is detected, and this method has been registered as patent

- Embedded BERT and various loop back for troubleshooting
- 0.25um CMOS
- Voltages: Core 2.5V; I/O 3.3V
- 128-pin LQFP package

3 Pin Descriptions

3.1 Pin Assignment

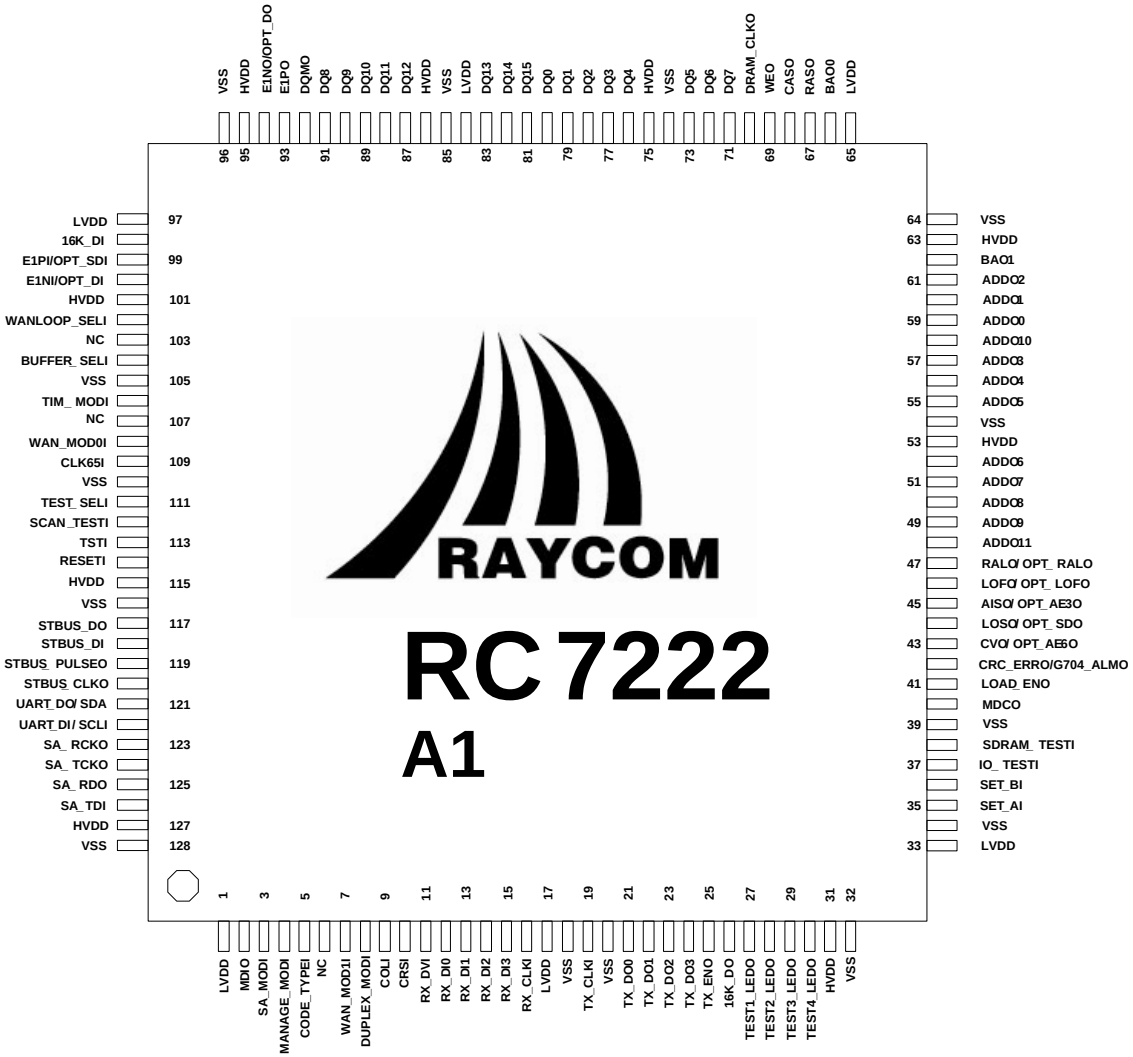

Fig.3-1-1 Pin Assignment

3.2 Pin Description

Symbol explanation

I: Input

O: Output

IO: Bi-directional

PU: Pull-up resistor

PD: Pull-down resistor

Schmitt: Schmitt input

Z: High impedance

Power: Power pin

Table 3-2-1 Pin Descriptions (Arranged as pin No.)

Pin	Pin Name	Type	Descriptions
1	LVDD	Power	2.5V
2	MDIO	IO (6mA)	MII Management interface: data input/output.
3	SA_MODI	I (PD)	Usage of the data path formed by the spare bits in G.704: 1 = transparent user-defined data channel; 0 = RC7222-A1-specific data path
4	MANAGE_MODI	I	Management access interface selection: 1 = I^2C interface; 0 = UART interface
5	CODE_TYPEI	I (PD)	E1 line code type: 1 = NRZ code; 0 = HDB3 code
6	NC	-	Not used, connect high level or nothing.
7	WAN_MOD1I	I (PD)	WAN interface options selection, combined with the signal WAN_MOD0I (PIN108). WAN_MOD1I/WAN_MOD0I=01, it is E1 interface; WAN_MOD1I/WAN_MOD0I=11, it is Optical interface; Refer to *section* ***4.2.1.1*** for details.
8	DUPLEX_MODI	I	Duplex mode for RC7222-A1 MAC 1= MAC module works in half-duplex mode; 0= MAC module works in full-duplex mode

9	COLI	I	MII collision signal, provided by Ethernet PHY. This signal is high when a collision is detected on the media.
10	CRSI	I	MII carrier sense signal, provided by Ethernet PHY. This signal is high if the media is not idle.
11	RX_DVI	I	MII receive data valid indication, active high, sampled by the rising edge of RX_CLKI
12	RX_DI0	I	MII receive data input, sampled synchronously with the rising edge of RX_CLKI
13	RX_DI1		
14	RX_DI2		
15	RX_DI3		
16	RX_CLKI	I	MII receiving clock, provided by Ethernet PHY. The clock frequency is 2.5MHz or 25MHz
17	LVDD	Power	2.5V
18	VSS	Power	Ground
19	TX_CLKI	I	MII transmitting clock, provided by Ethernet PHY. The clock frequency is 2.5MHz or 25MHz
20	VSS	Power	Ground
21	TX_DO0	O (6mA)	MII transmit data output, presented synchronously with the rising edge of TX_CLKI
22	TX_DO1		
23	TX_DO2		
24	TX_DO3		
25	TX_ENO	O (6mA)	MII transmit enable, asserted high, synchronous with the rising edge of TX_CLKI.
26	16K_DO	O (3mA)	Output signal for 16Kbps auxiliary data path in optical interface mode (WAN_MOD1I/WAN_MOD0I=11), otherwise NC.
27	TEST1_LEDO	O (3mA)	Chip work status output, LED indicator can be connected outside to indicate the work status. For more detailed information please refer to the *section* ***4.9.3***
28	TEST2_LEDO		
29	TEST3_LEDO		

30	TEST4_LEDO		
31	HVDD	Power	3.3V
32	VSS	Power	Ground
33	LVDD	Power	2.5V
34	VSS	Power	Ground
35	SET_AI	I	Serial input signal for network management address and user-defined information. 74HC165 can be connected outside to implement parallel-to serial conversion, refer to *section* ***5.2*** for more.
36	SET_BI	I	Serial input signal for bandwidth configuration. 74HC165 can be connected outside to implement parallel-to serial conversion, refer to *section* ***4.3.1*** for more.
37	IO_TESTI	I (PD)	It is used for chip test purpose, It should connect ground in normal use
38	SDRAM_TESTI	I (PD)	External SDRAM test function enable: 1 = SDRAM test mode; 0 = normal Note: The test result will be output via pin TEST_LEDO, refer to *section* ***4.9.1*** for more.
39	VSS	Power	Ground
40	MDCO	O (6mA)	2.048MHz clock output, timing source for MDIO of MII management interface, as well as work clock of the external 74HC165 connected with serial input of SET_AI and SET_BI. Refer to ***Fig. 7.4.3*** for timing diagram.
41	LOAD_ENO	O (6mA)	Shift control signal for serial configuration data input, direct connection to 74HC165. Timing diagram in ***Fig 7.4.3****.*
	Note: Pin42-Pin47 is alarm output pins for WAN interface, high level indicates alarm		

	occurring. Alarm inhibit has been preprocessed in interior chip. Refer to *section* ***4.2.1.2*** for more		
42	CRC_ERRO/ E1_ALMO	O (3mA)	If E1 is set as the WAN interface (WAN_MODI=01): This pin acts as a CRC error indicator; If optical interface is selected (WAN_MODI=11): This pin acts as an AIS or LOF indicator.
43	CVO/ OPT_AE6O	O (3mA)	In E1 mode(WAN_MODI=01): this pin indicates the alarm of Code Violation; In Optic mode (WAN_MODI=11): it indicates BER of 10^{-6}.
44	LOSO/ OPT_SDO	O (3mA)	In E1 mode (WAN_MODI=01): this pin is the indicator of LOS alarm; In Optic mode (WAN_MODI=11): it indicates the optical LOS alarm.
45	AISO/ OPT_AE3O	O (3mA)	In E1 mode (WAN_MODI=01): this pin is the indicator of G.704 AIS alarm; In Optic mode (WAN_MODI=11): it indicates BER of 10^{-3}.
46	LOFO/ OPT_LOFO	O (3mA)	In E1 mode, this pin is the indicator of LOF alarm; In Optic mode (WAN_MODI=11): it indicates the optical LOF alarm.
47	RALO/ OPT_RALO	O (3mA)	In E1 mode (WAN_MODI=01): this pin is the indicator of RAL alarm; In Optic mode (WAN_MODI=11): it indicates the remote alarm of optical line.
48	ADDO11	O (6mA)	SDRAM address outputs, with ADDO11 the most significant bit, and ADDO0 the lowest significant bit.
49	ADDO9		
50	ADDO8		
51	ADDO7		
52	ADDO6		

53	HVDD	Power	3.3V
54	VSS	Power	Ground
55	ADDO5	O (6mA)	SDRAM address outputs, with ADDO11 the most significant bit, and ADDO0 the least significant bit.
56	ADDO4		
57	ADDO3		
58	ADDO10		
59	ADDO0		
60	ADDO1		
61	ADDO2		
62	BAO1	O (6mA)	SDRAM BANK address, most significant bit (MSB)
63	HVDD	Power	3.3V
64	VSS	Power	Ground
65	LVDD	Power	2.5V
66	BAO0	O (6mA)	SDRAM BANK address, least significant bit (LSB)
67	RASO	O (6mA)	Row Address Strobe, Column Address Strobe, Write Enable signal outputs. Combined for SDRAM controlling.
68	CASO		
69	WEO		
70	DRAM_CLKO	O (6mA)	Reference clock for the SDRAM, generated by dividing the CLK65I frequency by half.
71	DQ7	IO (6mA)	Data bus interface to SDRAM
72	DQ6		
73	DQ5		
74	VSS	Power	Ground
75	HVDD	Power	3.3V
76	DQ4	IO (6mA)	Data bus interface to SDRAM
77	DQ3		
78	DQ2		
79	DQ1		
80	DQ0		

81	DQ15		
82	DQ14		
83	DQ13		
84	LVDD	Power	2.5V
85	VSS	Power	Ground
86	HVDD	Power	3.3V
87	DQ12	IO (6mA)	Data bus interface to SDRAM
88	DQ11		
89	DQ10		
90	DQ9		
91	DQ8		
92	DQMO	O (6mA)	Data inhibit signal for SDRAM, direct connection to LDQM and UDQM of SDRAM
	Note :PIN94/PIN99/PIN100 are shared pins for E1 and optical interface, refer to *section* ***4.2.1.1***		
93	E1PO	O (6mA)	When E1 is set as the WAN interface (WAN_MODI=01): HDB3 mode: HDB3+ output NRZ mode: clock signal output
94	E1NO/OPT_DO	O (6mA)	When E1 is set as the WAN interface(WAN_MODI=01): HDB3 mode: HDB3- output NRZ mode: data signal output When optical is set as the WAN interface(WAN_MODI=11): it outputs optical data.
95	HVDD	Power	3.3V
96	VSS	Power	Ground
97	LVDD	Power	2.5V
98	16K_DI	I	When optical is set as the WAN interface(WAN_MODI=11): it is data input of the 16Kbps data channel. Refer to *section* ***4.2.2.1*** for more.

99	E1PI/OPT_SDI	I	When E1 is set as the WAN interface (WAN_MODI=01), HDB3+ code is inputted(HDB3 mode) or NRZ clock signal is inputted (NRZ mode); When optical is set as the WAN interface(WAN_MODI=11): optical LOS indication signal input from external transceiver. Low level for LOS alarm.
100	E1NI/OPT_DI	I	When E1 is set as the WAN interface(WAN_MODI=01):, HDB3- code is inputted(HDB3 mode) or NRZ data is inputted (NRZ mode); When optical is set as the WAN interface(WAN_MODI=11): optical interface data is inputted
101	HVDD	Power	3.3V
102	WANLOOP_SELI	I (PD)	Local loop-back mode configuration for WAN: 1 = loop-back enable; 0 = loop-back disable Refer to Fig.4-1-1 for the loop back point and section ***4.2.4*** for more.
103	NC	-	Not used, connect low level or nothing
104	BUFFER_SELI	I (PD)	Buffer size selection: (See section ***4.7.2*** for detailed description) 1 = large buffer mode; 0 = small buffer mode
105	VSS	Power	Ground

106	TIM_MODI	I	Timing source selection for WAN interface: 1 = local oscillator; 0 = tracing line timing When two devices are used to transmit Ethernet data, one device can be set as local oscillator, the other device can be set as either local oscillator or tracing line timing; when two devices are used to transmit voice service, one should be set as local oscillator and the other must be set as tracing line timing. Refer to section ***4.2.5*** for more.
107	NC	-	Not used. Connect to ground or nothing
108	WAN_MOD0I	I (PU)	WAN interface options selection, combined with the signal WAN_MOD1I (PIN7). WAN_MOD1I/WAN_MOD0I=01, it is E1 interface; WAN_MOD1I/WAN_MOD0I=11, it is Optical interface; Refer to *section* ***4.2.1.1*** for details.
109	CLK65I	I	65.536MHz (± 50ppm) clock.
110	VSS	Power	Ground
111	TEST_SELI	I	Pins for chip test, must be grounded.
112	SCAN_TESTI		
113	TSTI		
114	RESETI	I (Schmitt)	Reset signal for the chip: 0 = reset; 1 = work normally.
115	HVDD	Power	3.3V
116	VSS	Power	Ground
117	STBUS_DO	O (6mA)	ST_BUS data output
118	STBUS_DI	I	ST_BUS data input
119	STBUS_PULSEO	O (6mA)	ST_BUS multi-frame alignment pulse (500Hz)
120	STBUS_CLKO	O (6mA)	ST_BUS clock output (2.048MHz), timing reference for

			STBUS_DI and STBUS_DO.
	Note: PIN 121/PIN122 are the shared pins for UART and I^2C pin, refer to section ***5.2*** for more.		
121	UART_DO/SDA	O/ IO (6mA)	If MANAGE_MODI (PIN4) is pulled low, this pin will be the data output of UART, with the baud rate of 19.2Kbps, in idle state, the pin output high-Z, thus the external pull-up resistor is necessary ; if MANAGE_MODI (PIN4) is pulled high, this pin will acts as a bi-directional data port of I^2C, connecting to SDA of I^2C interface. the external pull-up resistor is necessary.
122	UART_DI/SCLI	I	If MANAGE_MODI (PIN4) is pulled low, this pin will be the data input of UART, with the baud rate of 19.2Kbps; otherwise, this pin acts as a clock port of I^2C, connecting to SCL of I^2C interface.
	Note: PIN 123-PIN126 are for SA interface, SA channel is available only when it is G.704 frame mode and SA_MODI is pulled low, and SA_TDI should be connected by high or low level. Otherwise SA channel is unavailable. Refer to section ***4.8*** for more.		
123	SA_RCKO	O (6mA)	Clock output for data dropping from the SA channel, with the frequency of 20KHz.
124	SA_TCKO	O (6mA)	Clock output for data adding up to the SA channel, with the frequency of 20KHz.
125	SA_RDO	O (6mA)	Output data dropping from the SA channel, synchronous to the rising edge of SA_RCKO.
126	SA_TDI	I	Data input to add into the SA channel. When SA_MODI is high, the data is sampled at the rising edge of SA_TCKO and then added to the channel
127	HVDD	Power	3.3V
128	VSS	Power	Ground

4 Functional Descriptions

4.1 Block Diagram

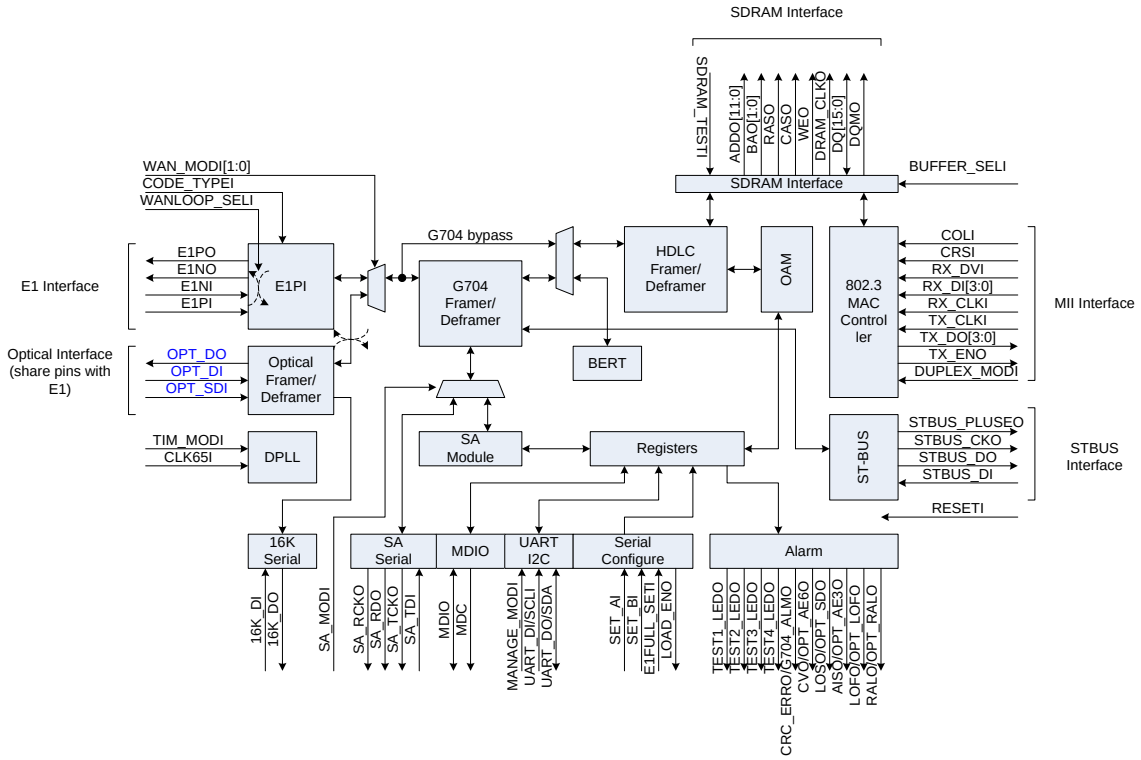

Fig.4-1-1 RC7222-A1 Block Diagram

4.2 WAN Interface

4.2.1 WAN Interface Multiplexing (MUX)

Inputs, outputs and alarm indicators of all WAN interfaces are multiplexed.

4.2.1.1 Input/output Multiplexing Pin

The RC7222-A1 has 2 optional WAN interfaces selected by WAN_MOD0I/WAN_MOD1I: E1 interface (FE1 included) and Optical interface. Both the two interfaces are shared with one group pin. Definition of each pin is listed in the table that followed.

Table 4-2-1-1 WAN interface description

Pin Name	Optical Interface WAN_MODI[1:0]=11	E1 Interface WAN_MODI[1:0]=01

		HDB3 CODE_TYPEI=0	E1 NRZ CODE_TYPEI=1
E1PO	NC	HDB3+ output	Clock output
E1NO/OPT_DO	Data output of optical interface	HDB3- output	Data output
E1PI/OPT_SDI	Optical LOS alarm input, this alarm is disappeared when it is low level	HDB3+ input	Clock input
E1NI//OPT_DI	Data input of optical interface	HDB3- input	Data input

4.2.1.2 Alarm output multiplexing pin

There are 2 groups of alarm output shared with one group pin for the WAN interface, with different definitions in different interface mode.

Table 4-2-1-2 WAN Interface Alarm Specification

Pin Name	E1 Interface mode				Optical Interface Mode	
	HDB3 code		NRZ code			
	G.704 frame	Unframe	G.704 frame	Unframe	G.704 frame	Unframe
E1_LOSO/OPT_SDO	E1_LOS	E1_LOS	None	None	OPT_SD	OPT_SD
AISO/OPT_AE3O	AIS	AIS	AIS	AIS	OPT_AE3	OPT_AE3
LOFO/OPT_LOFO	LOF	None	LOF	None	OPT_LOF	OPT_LOF
CRC_ERRO/G704_ALMO	CRC_ERR	None	CRC_ERR	None	G704_ALM (LOF/AIS)	G704_ALM(AIS)
E1_CVO/OPT_AE6O	E1_CV	None	None	None	OPT_AE6	OPT_AE6
RALO/OPT_RALO	RAL	None	RAL	None	OPT_RAL	OPT_RAL

4.2.2 Optical Interface

The RC7222-A1 has a 4.096Mbps optical interface, with 1B1C coding and TTL voltage level. It multiplexes a 2.048M data stream, an asynchronous 16Kbps user data channel and several alarm control bit overhead. Via the optical line, the RC7222-A1 can be connected to the RC7235, another chip from Raycom, which can resolve the E1 data-stream and the 16Kbps information from the optical line code.

4.2.2.1 Low-speed Serial Data Channel

The optical interface of RC7222-A1 provides a serial data channel with 16 KHz sampling frequency for users. However, with the absence of timing clock signal, it can only act as a low-speed asynchronous data channel, with recommended baud rate of less than 4800Bps.

Generally, this Low-speed serial data channel is used as UART channel to provide communication between two MCU in two ends, to implement remote control and alarm query.

4.2.2.2 Optical Alarm

The optical interface of RC7222-A1 is comprised of two modules: transmitter and receiver. The transmitter multiplexes 2.048M framed E1 data processed by G.704 framer or 2.048M unframed E1 data processed by HDLC framer, local alarm data, serial data with 16KHz sampling frequency for users and some other overhead into the coded optical data, with timing reference of the clock generated by DPLL. It mainly performs such functions as multiplexing, coding and scrambling. The receiver module receives the data-stream from the optical line, resolves the overhead and the E1 frame, and passes them on for subsequent processing. This module implements such functions as data reception, clock recovery, de-scrambling, decoding, de-multiplexing and alarm supervising.

RC7222-A1 supports the detection of optical LOS signal (OPT_SD), which is detected by external optical transceiver and informed through the pin OPT_SDI. Besides, RC7222-A1 supports detection of los of optical frame (OPT_LOF), 10e-3 bit error (OPT_AE3), 10e-6 bit error (OPT_AE6), which is detected by the internal optical deframer.

Alarm OPT_SD or OPT_ LOF detected at the local RC7222-A1 will cause OPT_RAL alarm at the remote RC7222-A1.

In G.704 frame mode the 2.048M framed data stream coming from optical deframer will be sent to G.704 deframer, deframed, and then, Nx64K datastream is sent to HDLC deframer according to timeslot assignment configuration. In addition, G.704 Deframer will detect AIS (all the 2.048M signal are '1') alarm, LOF(Loss Of G.704 Frame), LOMF(Loss Of G.704 Multiframe), CRC_ERR(CRC Error) and RAL(Remote Alarm); Most of the G.704 alarm can be addressed at individual register, only Alarm LOF, LOMF and AIS can be emerged as G704_ALM outputted via pin CRC_ERRO/G704_ALMO; In Non-framed mode the 2.048M unframed data stream will be sent to HDLC Deframer directly without any G.704 alarm detection.

Alarm AIS, LOF and LOMF detected by G.704 deframer at the local device will cause RAL alarm at the remote device.

The optical alarm outputted by pin is specified to have priority and alarm inhibit relationship, as Fig.4-2-2-2-1 shows, the priority of the alarm from high to low is arranged according to the arrow direction: the alarm pointed by arrowhead at the base of the figure has lower priority and will be inhibited by the alarm with higher priority. For example, alarm OPT_LOF will inhibit alarm OPT_RAL/OPT_AE3/AIS and any alarm with lower priority than these three alarms; LOMF alarm will inhibit alarm RAL/CRC_ERR.

The optical alarm in registers is not specified to have priority and alarms inhibit relationship; it should be done in MCU according to Fig.4-2-2-2-1 if the alarm will be readout by MCU.

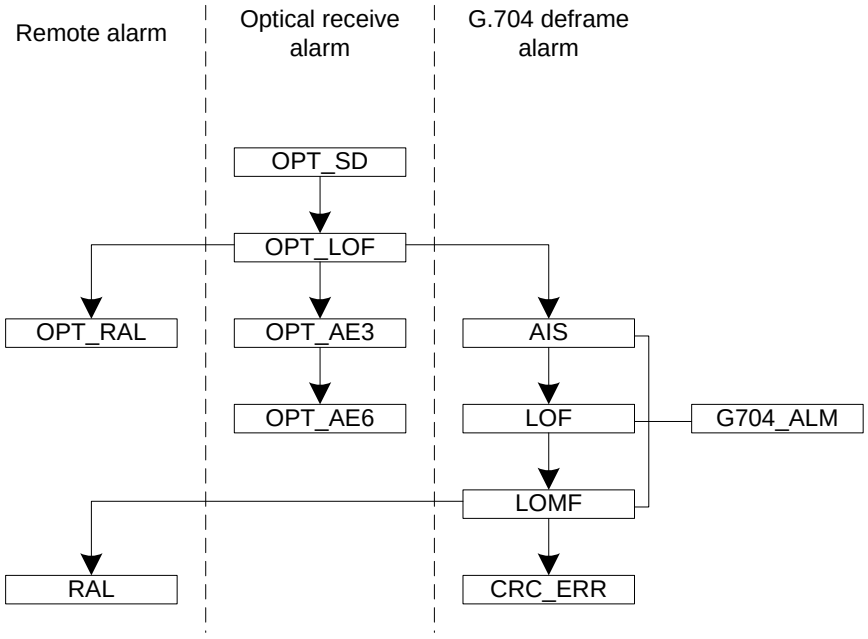

Fig.4-2-2-2-1 Optical alarm priority

4.2.3 E1 Interface

The E1 interface use the clock generated by DPLL to transmit the 2.048M data stream (G.704 frame) from G.704 framer or the 2.048M data stream(Non-framed) from HDLC framer in HDB3 code on the transmit side; On the receive side, the E1 interface implement clock extracting, HDB3 decoding, 2.048M data stream recovering and alarm detection.

The E1 interface support HDB3 code and NRZ code, which can be set by pin CODE_TYPEI; it is HDB3 code when CODE_TYPEI is low level and NRZ code when CODE_TYPEI is high level.

4.2.3.1 E1 Alarm

The E1 block E1PI of RC7222-A1 supports E1 signal loss (E1_LOS) and HDB3 coded violate (E1_CV) alarm detection in HDB3 mode; in NRZ mode, E1_LOS and E1_CV alarm is not detected.

In G.704 frame mode the 2.048M framed data stream coming from E1 Decoder will be sent to G.704 deframer, deframed, and then, Nx64K datastream is sent to HDLC deframer according to timeslot assignment configuration. In addition, G.704 Deframer will detect AIS (all the 2.048M signal are ‘1’) alarm, LOF (Loss Of G.704 Frame), LOMF (Loss Of G.704 Multiframe), CRC_ERR (CRC Error) and RAL (Remote Alarm); Most of the G.704 alarm can be addressed at individual register; In Non-framed mode the 2.048M unframed data stream will be sent to HDLC Deframer directly without any G.704 alarm detection.

Alarm AIS, LOF and LOMF detected by G.704 deframer at the local device will cause RAL alarm at the remote device.

The E1 alarm outputted by pin is specified to have priority and alarm inhibit relationship, as Fig.4-2-3-1-1 shows, the priority of the alarm from high to low is arranged according to the arrow direction: the alarm pointed by arrowhead at the base of the figure has lower priority and will be inhibited by the alarm with higher priority. For example, alarm E1_LOS will inhibit alarm E1_CV/AIS and any alarm with lower priority than these two alarms; LOMF alarm will inhibit alarm RAL/CRC_ERR.

The E1 alarm in registers is not specified to have priority and alarms inhibit relationship; it

should be done in MCU according to Fig.4-2-3-1-1 if the alarm will be readout by MCU.

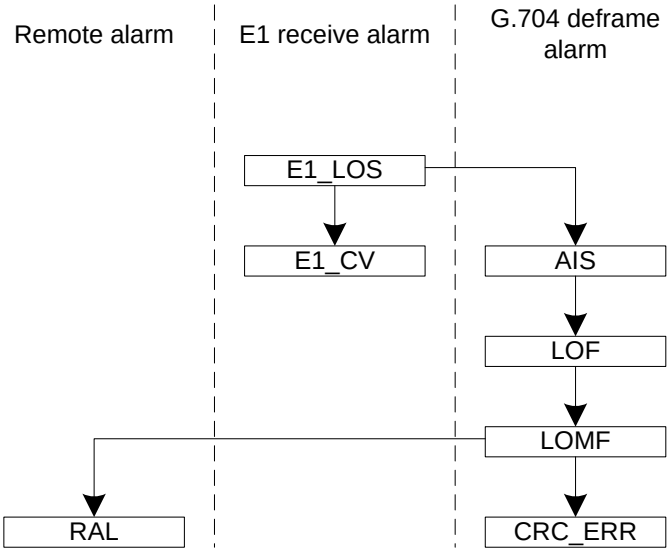

Fig.4-2-3-1-1 E1 alarm priority

4.2.4 WAN interface loopback

The WAN interface of RC7222-A1 supports local loop back and remote loopback.

RC7222-A1 is compatible with the chips of Raycom converter family, so there are several loopback settings reserved as Table 4-2-4-1 shows:

Table 4-2-4-1 WAN Interface loopback

Name	Loopback controller	Directional/ Bi-directional loopback
Local loopback	Pin WAN_LOOPI, the status can be viewed by MIB register WAN_LOOPI (00.18H[3])	Bi-directional loopback, with loopback point at WAN interface
	MIB register Net_wanloop(00.18H[7])	Bi-directional loopback, with loopback point at WAN interface

	Global register cLoop_interE1(11.04H[0])	Directional loopback to the chip at the loopback point of WAN interface
	Global register cLoop_extE1 (11.04H[1])	Directional loopback to the line at the loopback point of WAN interface
Remote loopback	Pin LINE_TESTI, the status can be viewed by MIB register LINE_TESTI (00.18H[2])	Directional loop, Control the remote loopback, the remote loopback is towards line direction at the loopback point of remote WAN interface
	MIB register Net_line_test (00.18H[6])	Directional loop, Control the remote loopback, the remote loopback is towards line direction at the loopback point of remote WAN interface

4.2.4.1 Optical Interface Loopback

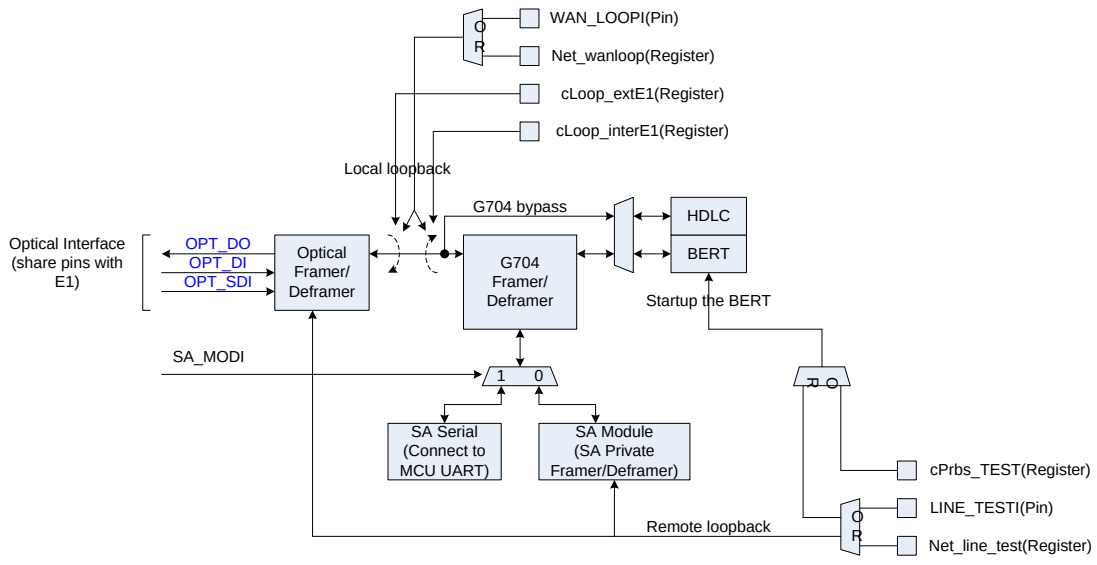

Fig.4-2-4-1-1 Optical Interface loopback

There are 4 types of configuration for local loopback when optical interface is set as WAN interface (note that all the 4 types of configuration have the same priority): Any of *WAN_LOOPI, Net_wanloop*, *cLoop_interE1* and *cLoop_extE1* being set as ‘1’ will activate local loopback; While all the *WAN_LOOPI*, *Net_wanloop*, *cLoop_interE1* and *cLoop_extE1* being ‘0’ will cancel local loopback.

There are 2 types of configuration for remote loopback(note that both the two types of configuration have the same priority): any of *LINE_TESTI* and *Net_line_test* being set as ‘1’ will send loopback instruction to the remote device; while both *LINE_TESTI* and *Net_line_test* being ‘0’ will cancel sending remote loopback instruction.

The remote loopback instructions will be sent to optical framer, framed and then to the remote device via the overhead of optical frame without any restriction; the remote loopback instructions will also be sent to SA private built-in framer and then to the remote device via SA built-in frame. As shown in Fig 4-2-4-1-1, the remote loopback instructions transmitting via SA built-in frame is available only when SA_MODI is pulled low and be in G.704 frame mode.

As Fig.4-2-4-1-1 shows, *LINE_TESTI* and *Net_line_test* can startup the BERT beside sending remote loopback instructions. During the test, the transmitter sends the serial pseudo random sequence into the timeslots that were assigned for Ethernet; the receiver checks if the bit sequence pattern received is the same as that of the transmitter, and checks bit errors as well.

The remote loopback instructions will be received by the remote RC7222-A1 and then be sent to register *Reloop_get(00.0BH[1])*. At the same time, the remote RC7222-A1 will check that if any of register *WAN_LOOPI, Net_wanloop, cLoop_interE1, cLoop_extE1, LINE_TESTI* and *Net_line_test* is ‘1’, any of registers referred above being ‘1’ will not response the loopback instructions and register *Reloop_reply(00.0BH[0])* will be set as ’0’; while all the registers referred above being ‘0’ will response the loopback instructions and register *Reloop_reply(00.0BH[0])* will be set as ‘1’. This design can prevent dead loopback(dead loopback means that the loopback cannot be canceled by any commands) when local loopback and remote loopback are occurred simultaneity.

The loopback status can also be viewed by chip pins: if there is local loopback or remote loopback, pin *TEST1_LEDO/TEST2_LEDO* will output ‘10’, refer to section ***4.9.3*** for more.

4.2.4.2 E1 Interface Loopback

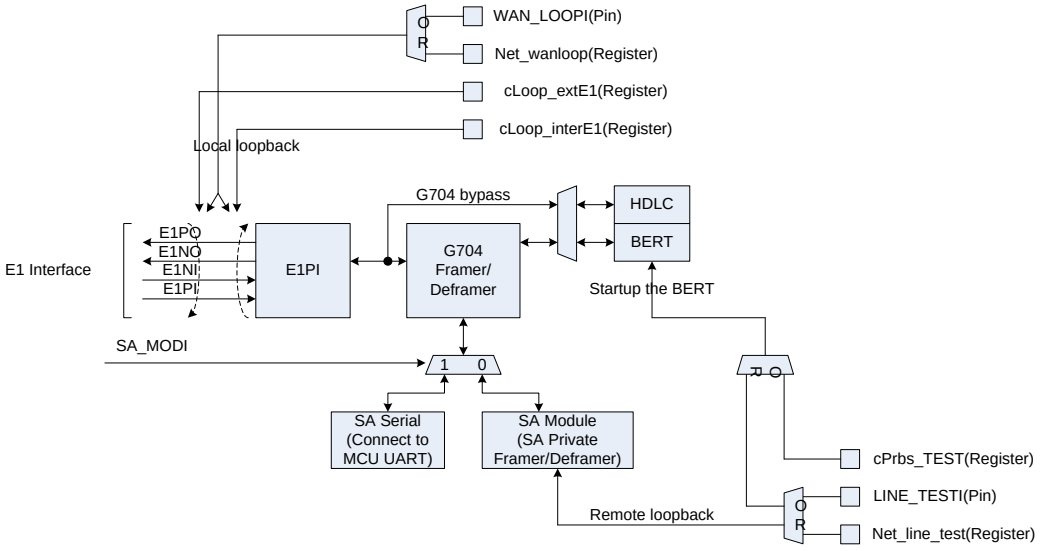

Fig.4-2-4-2-1 E1 Interface Loopback

There are 4 types of configuration for local loopback when E1 interface is set as WAN interface (note that all the 4 types of configuration have the same priority): Any of *WAN_LOOPI, Net_wanloop*, *cLoop_interE1* and *cLoop_extE1* being set as '1' will activate local loopback; While all the *WAN_LOOPI*, *Net_wanloop*, *cLoop_interE1* and *cLoop_extE1* being '0' will cancel local loopback.

There are 2 types of configuration for remote loopback(note that both the two types of configuration have the same priority): any of *LINE_TEST*I and *Net_line_test* being set as '1' will send loopback instruction to the remote device; while both *LINE_TESTI* and *Net_line_test* being '0' will cancel sending remote loopback instruction.

The remote loopback instructions will only be sent to SA private built-in framer and then to the remote device via SA built-in frame. After receiving the loopback instructions from SA built-in frame, the remote device will execute the loopback instruction. As shown in Fig 4-2-4-2-1, the remote loopback instructions transmitting via SA built-in frame is available only when SA_MODI is pulled low and be in G.704 frame mode.

As Fig.4-2-4-1-1 shows, *LINE_TESTI* and *Net_line_test* can startup the BERT beside sending remote loopback instructions. During the test, the transmitter sends the serial pseudo random sequence into the timeslots that were assigned for Ethernet; the receiver checks if the bit

sequence pattern received is the same as that of the transmitter, and checks bit errors as well.

The remote loopback instructions will be received by the remote RC7222-A1 and then be sent to register *Reloop_get(00.0BH[1])*. At the same time, the remote RC7222-A1 will check that if any of register *WAN_LOOPI, Net_wanloop, cLoop_interE1, cLoop_extE1, LINE_TESTI* and *Net_line_test* is '1', any of registers referred above being '1' will not response the loopback instructions and register *Reloop_reply(00.0BH[0])* will be set as '0'; while all the registers referred above being '0' will response the loopback instructions and register *Reloop_reply(00.0BH[0])* will be set as '1'. This design can prevent dead loopback(dead loopback means that the loopback cannot be canceled by any commands) when local loopback and remote loopback are occurred simultaneity.

The loopback status can also be viewed by chip pins: if there is local loopback or remote loopback, pin *TEST1_LEDO/TEST2_LEDO* will output '10', refer to section ***4.9.3*** for more.

4.2.4.3 Remote Loopback Controlled by MCU

The remote loopback instructions described in both section *4.2.4.1* and *4.2.4.2* are controlled by chip and facility for using. However, both optical frame format and SA built-in frame format are private protocols, which is not suitable to transmit management information between RC7222-A1 and the other chip that is compatible with HDLC frame format of RJ017. The following descriptions are 2 types of management information transmitting to realize compatible frame protocol:

One is to use the serial user-defined data channel via SA interface (SA_MODI=1); Connect UART interface of MCU to the SA interface of RC7222-A1, set *SA_NODI* as '1', thus, the SA bits will be used as management data channel accessed by MCU and compatible frame protocol can be transmitted between the two MCU via the channel. As Fig.4-2-4-3-1 shows, the local MCU can transmit remote loopback instructions to the remote MCU via the UART-SA interface.

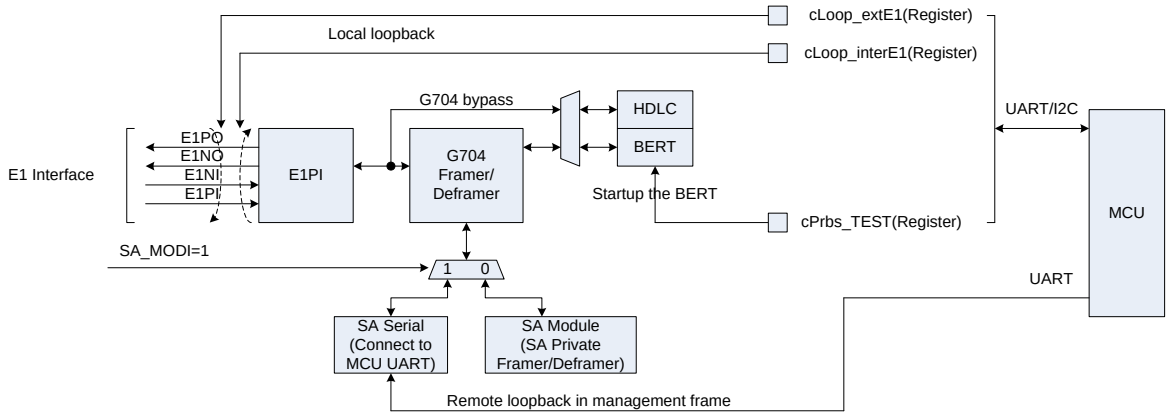

Fig.4-2-4-3-1 MCU Remote Controlling via SA Interface

However, the SA bits used as serial user-defined data channel via SA interface is available only in G.704 frame mode with pin *SA_MODI* being '1'; In unframed mode, the SA bits cannot be used. There is another way to transmit compatible frame protocol between two MCU: HDLC management frame, as Fig.4-2-4-3-2 shows, the remote loopback instructions in management frame will be sent to HDLC, encapsulated, and then be transmitted with Ethernet data together. Refer to *section **4.6.1*** for more.

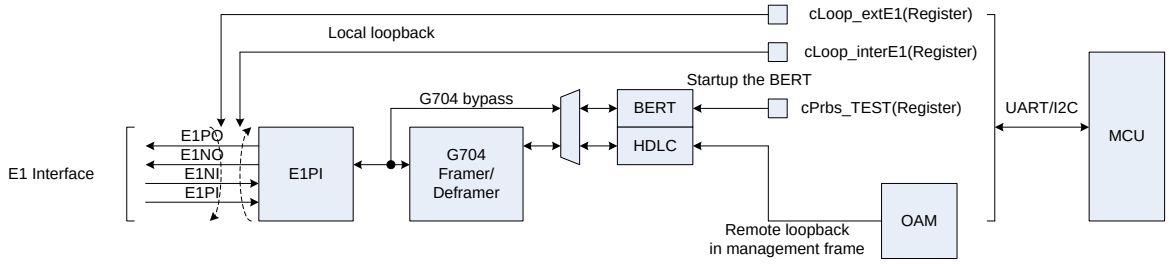

Fig.4-2-4-3-2 MCU Remote Controlling via HDLC Management Frame

4.2.5 Timing In WAN Interface

RC7222-A1 support two optional timing sources: local oscillator or tracing the line timing.

The timing source is selected through the pin *TIM_MODI*(this pin can be viewed by *TIM_MODI(00.06H[1]*)). If the pin *TIM_MODI* is pulled high, the local clock from CLK65I is selected; when the pin *TIM_MODI* is logic low, tracing-line-timing mode is adopted and the

clock recovered from the line is used for transmit timing reference.

As Fig.4-2-5-1shows, when two RC7222-A1 work in point-to-point, there are two allowable timing mode combinations: both in local timing mode or one in local timing mode while the other in tracing line timing mode. Both are suitable for Ethernet transportation. However, for ST_BUS applications, the timing mode of both in local oscillator may lead to slips and bad voice service quality.

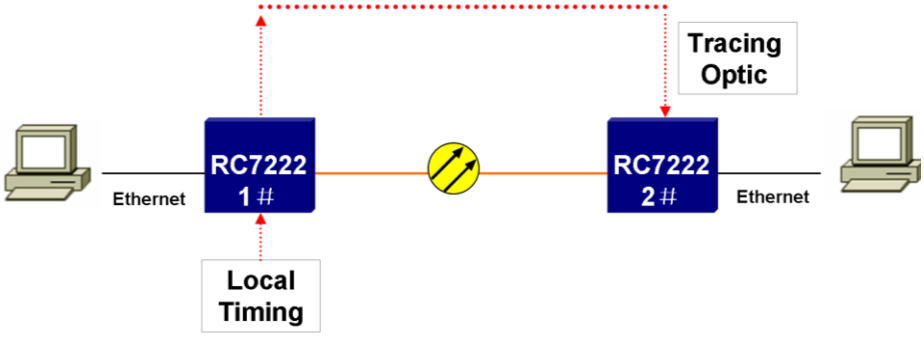

Fig.4-2-5-1 Timing Application

4.2.6 Ethernet Loopback Prevention

RC7222-A1 supports detection of WAN loopback, which stops transferring Ethernet data to the LAN when WAN loopback is detected, avoiding the mess of the Ethernet network.

RC7222-A1 supports specific detection module, which detects WAN loopback by comparing MAC address in transmitting with MAC address in receiving. The result detected is provided by register *Extloop_done(00.OCH[2])*, When a loop-back is detected, the RC7222-A1 set BIT2 of the Management Register 0CH to '1'; otherwise, the bit is always '0'.

When RC7222-A1 detects the WAN loopback, it will stop transferring the Ethernet data to the LAN; when the WAN loop is found canceled, the RC7222-A1 will resume its data transportation. In order to do some test in special conditions, the frame with all '0' in Ethernet source address can still be transmitted when Ethernet data transferring is stopped caused by loopback.

The Ethernet loopback prevention is controlled by register *Loopcut_en_n(00.04H[7])*, when *Loopcut_en_n(00.04H[7])*=0, this function is enabled; while when *Loopcut_en_n(00.04H[7])*=1, the Ethernet data transferring will not be stopped no materr the WAN is looped or not. The default value of *Loopcut_en_n* is '0'.

When register *Loopcut_en_n(00.04H[7])*=0, if WAN loopback is detected, RC7222-A1 will stop transferring Ethernet data to MII interface and output high level via pin *TEST4_LEDO,* connect LED to the pin will be helpful to indicate the Ethernet data cut down. See section ***4.9.3*** for description of *TEST4_LEDO*.

4.3 Timeslot Assignment

4.3.1 Timeslot Assignment Configuration

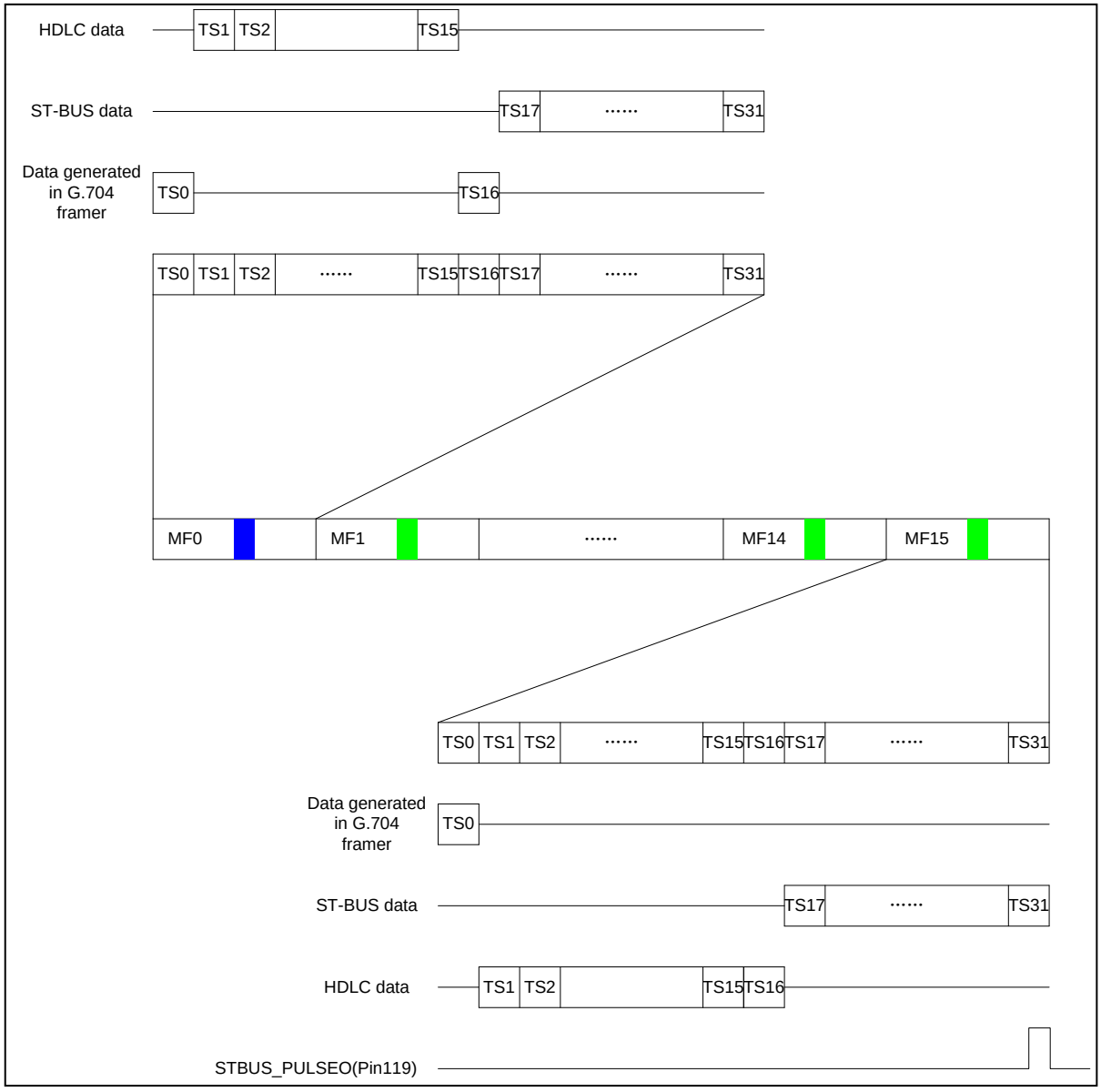

Fig.4-3-1-1 Timeslot Assignment.

As shown in Fig.4-3-1-1, G.704 frame adopts multiframe structure, every 16 frame compose a multiframe. There are 32 timeslots divided in each frame. TS0 is processed by G.704 framer/deframer in RC7222-A1, including frame alignment bit processing, CRC-4 check bit processing, SA spare bits processing and RAL alarm processing. The G.704 deframer in receiving direction will detect CRC-4 multiframe or non-CRC-4 multiframe automatically, and send the result into register *E1CRC_SEL*.

Except for TS0, G.704 framer/deframer will transmit the other 31 timeslots to HDLC framer/deframer or ST-Bus interface according to timeslot assignment.

TS16 is used to transmit HDLC data in PCM31 mode, while in PCM30 mode, it is a 64Kb/s signaling channel assigned to ST-BUS interface, which is used to transmit voice signaling frame. The first timeslot(SFTS0) of signaling frame is used to transmit signaling frame code and alarm and is processed by G.704 framer/deframer, SFTS1-SFTS15 is transmitted to ST-BUS without any processing by G.704.

HDLC data and ST_BUS signals are services to be transported, and they share the bandwidth supplied by the timeslots. The slots which is not allocated to the HDLC data are assigned to ST_BUS services.

RC7222-A1 supports 2 ways to set timeslot assignment: set by pin *SET_BI or* set by register.

After power on reset, the priority of pin S*ET_BI* settings is higher than the settings of register. The priority of the register can be adjust by writing A5 into register *00.58H*, thus, register *00.53H-00.56H* can be set effective and pin *SET_BI* settings will be invalid at the same time.

RC7222-A1 provides register *G.704_bypass(00.06H[7]), Pcm31_sel(00.06H[6]),* and *0.07H-00.0AH* to view timeslot configuration.

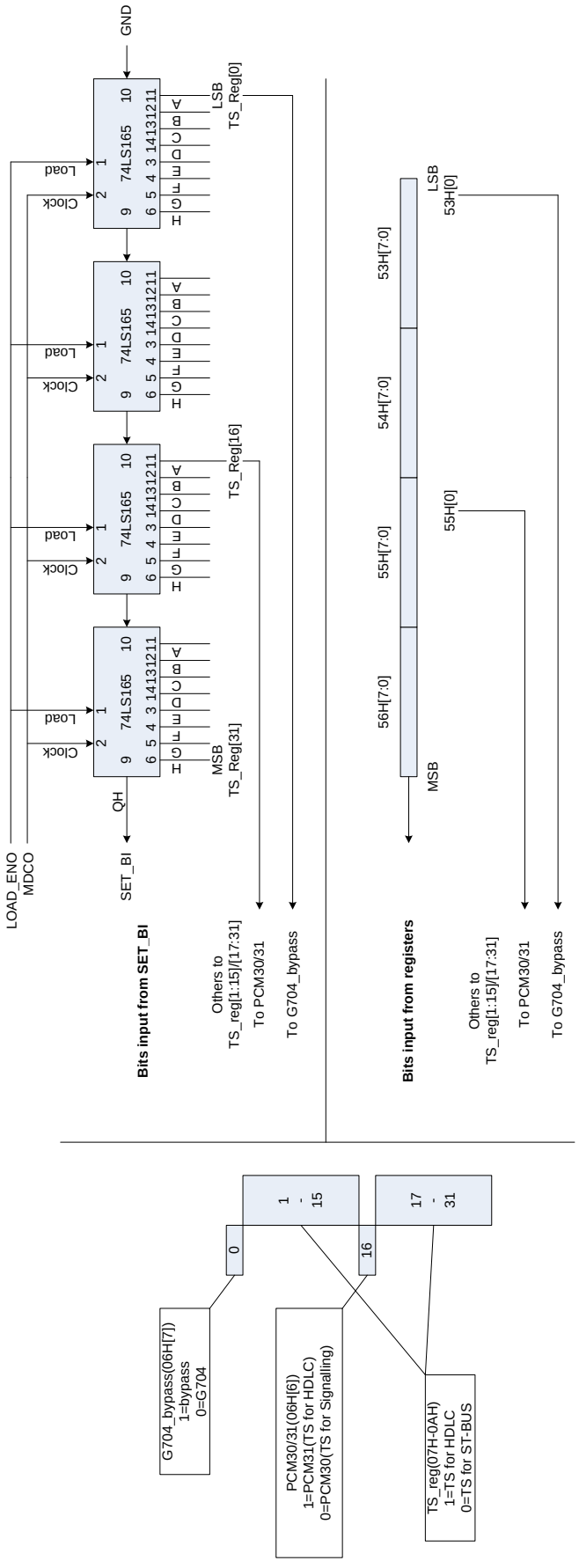

Fig.4-3-1-1 Timeslot Assignment Configuration

Note that the external 74HC165 connected to the serial input interface SET_BI should be connected with a 2.048MHz clock signal(MDCO) and a frame alignment signal (LOAD_ENO) provided by RC7222-A1.

As shown in the following diagram, the RC7222-A1 outputs a LOAD_ENO pulse to trigger the parallel to serial transformer, and then acquire the configuration information via SET_BI, one bit a cycle, from BIT31 to BIT0, at the falling edge of MDCO. The LOAD_ENO outputs a low pulse every the 32nd cycle of the MDCO, with a period of T. See Fig 7.4.4 for the serial configuration timing diagram.

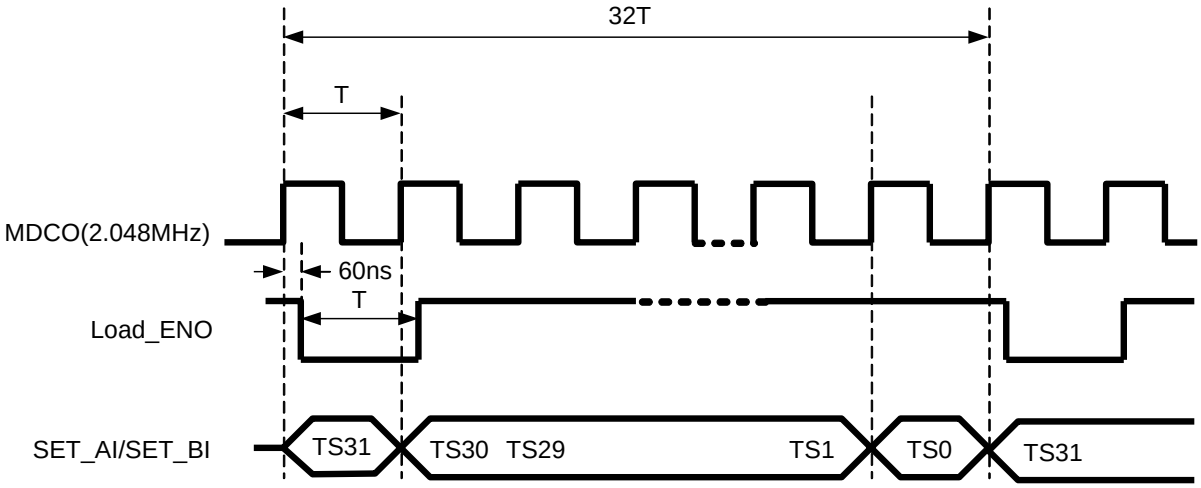

Fig.4-3-1-2 Serial configuration interface schematic diagram

4.4 ST_BUS Bus

The ST_BUS interface has 4 signals as follows:

STBUS_CLKO: The 2.048MHz clock output for ST_BUS, which is used to sample input data and present output data, it is also used to output the multi-frame alignment pulse (STBUS_PULSEO).

STBUS_DI: ST_BUS data input, which is sampled at the rising edge of *STBUS_CLKO*

STBUS_DO: ST_BUS data output, which is presented at the rising edge of *STBUS_CLKO.*

STBUS_PULSEO: The multi-frame alignment pulse output with the pulse width of 2.048M clock cycle. It outputs a high pulse at the same time with the last bit of TS31, the 15th sub-frame of

G.704 multiframe(0-15), marking the start of a new multi-frame. It is presented at the rising edge of STBUS_CLKO.

ST_BUS is used for Nx64K data accessing, especially for voice service accessing. When it is used for voice service accessing, TS16 can be used to carry the signaling, refer to section 4.3.1 for more. Generally, ST_BUS interface need to connect CPLD and provide 8K pulse for CODEC according to STBUS_PULSEO.

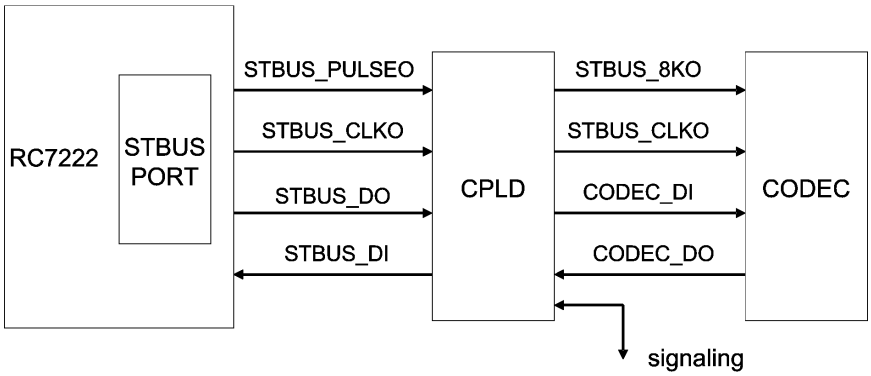

Fig.4-4-1 ST_BUS schematic diagram

4.5 MII Interface

RC7222-A1 provides a standard IEEE 802.3 MII interface, which supports 10/100Mbps and full/half duplex.

4.5.1 MII Interface

Media Independent Interface (MII) is the interface between Ethernet MAC sub-layer and physical layer. Here, it is the interface between RC7222-A1 and Ethernet physical chip(PHY). Note that the interface clock RX_CLKI and TX_CLKI are provided by Ethernet PHY chip.

The connection between the RC7222-A1 and physical layer chip is as follows:

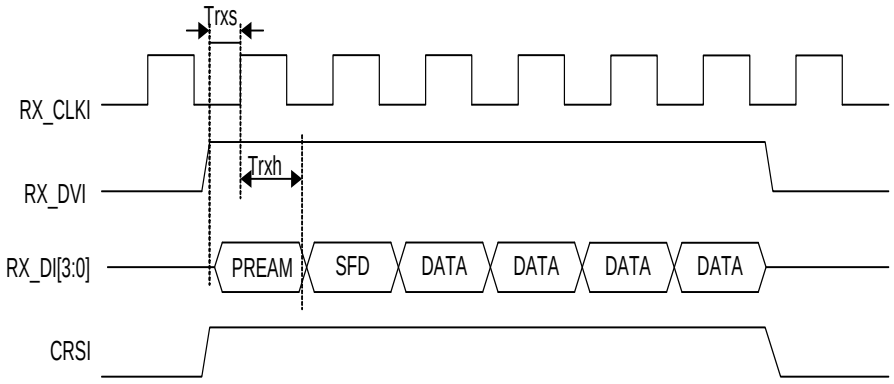

Fig.4-5-1-1 MII Interface Connection

The MII receive and transmit timing diagram are illuminated in ***Fig 7.4.1.1*** and ***Fig 7.4.1.2*** respectively.

4.5.2 MDIO Interface

Generally, Ethernet PHY chip provides a MDIO interface for register accessing. RC7222-A1 also provides a standard IEEE802.3 management interface MDIO for controlling PHY chip, thus, the MCU connected with RC7222-A1 only can access the register of PHY chip by RC7222A1 register.

MDIO interface includes two signals: MDCO and MDIO. The MDCO is a 2.048MHz clock output, and it is the timing reference for the MDIO data. The MDIO is the bi-directional management data. Through the MDIO interface, the RC7222-A1 can access the registers of the Ethernet PHY, retrieving the information.

Part of PHY registers defined in IEEE802.3, such as 10M/100M settings, half/full duplex settings and so on, will be written into MIB register *00.19H-00.1DH* of RC7222-A1 via MDIO interface. Thus, MCU can get information about PHY easily.

When RC7222-A1 is accessed by MCU via UART/I^2C interface, MCU is the master device and RC7222-A1 is the slave device, the address about UART/I^2C should be set via pin SET_AI and be known by MCU; When PHY chip is accessed by RC7222-A1 via MDIO interface, the MDIO address should also be known. The register *Cfg_phy_addr(00.50H)* in RC7222-A1 is used to store MDIO address of PHY chip, which should be identify with PHY chip address.

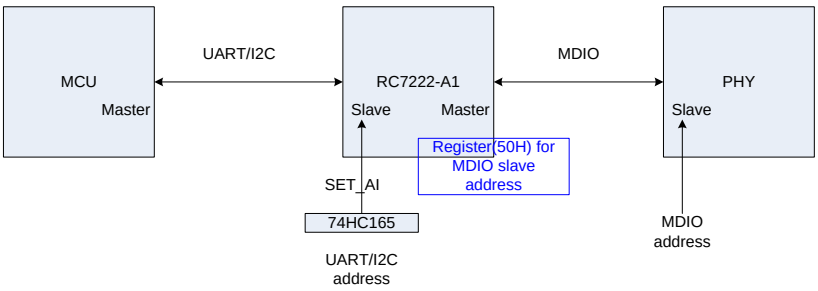

Fig.4-5-2-1 Management Interface Connection

4.5.3 MAC Work Mode

There are several work mode options that need to be configured properly so that the Ethernet MAC controller can work smoothly. They are auto-negotiation, 10M/100M, half/full duplex, flow control and Excessive-collision discarding mode.

10M/100M Mode

10M/100M mode can be configured in Ethernet PHY chip. When the Ethernet PHY chip is operated in 100M mode, the clock signal, RX_CLKI/TX_CLKI, transmitted to RC7222-A1 from PHY chip, will be 25MHz; When the Ethernet PHY chip is operated in 10M mode, the clock signal, RX_CLKI/TX_CLKI, transmitted to RC7222-A1 from PHY chip, will be 2.5MHz; RC7222-A1 will detect the 10M/100M mode automatically by the received clock signal from PHY chip, and send the detection result to register Phy_speed(00.0FH[1]).

Half/Full Duplex Mode

Half/Full duplex mode should be configured both in PHY chip and RC7222-A1, set by pin *DUPLEX_MODI* or register *00.51H[2]*, and viewed by register *duplex_mod(00.04H[2])* for the result. When *duplex_mod(00.04H[2])*=0, it is half duplex mode; while when register *duplex_mod(00.04H[2])*=1, it is full duplex mode.

Note: If pin *DUPLEX_MODI* is pulled low, or both register *00.51H[2]* and register *duplex_mod(00.04H[2])* are set as'1', it is full duplex mode.

Flow Control

Flow control can be configured only in RC7222-A1, set by register *00.51H[1],* and viewed by register *mac_pause(00.04H[1])* for the result. If register *mac_pause(00.04H[1])*=0, the flow

control function is disabled; If register *mac_pause(00.04H[1])*=1, the flow control function is enabled. Note that only in full-duplex mode, RC7222-A1 can realize flow control by sending flow control frame (Pause frame) defined in 802.3; while the flow control function is not supported in half-duplex mode.

If the flow control function is enabled, the RC7222-A1 can take use of it to inform the sender to pause sending frames, to avoid the data buffer overflow.

Excessive-collision Discarding

This function can be configured only in RC7222-A1, set by register 51H[3], and viewed by register Col16_discard_en (00.04H[3]) for the result. When register Col16_discard_en (00.04H[3]) =1, RC7222-A1 will discard the current Ethernet packet transmitted (MII interface output direction) after 16 consecutive collisions; while when register Col16_discard_en （00.04H[3])=0, the MAC controller will go on retrying, neglecting the excessive collisions.

As collision occurs only in half-duplex mode, the excessive-collision discarding function only be found in half-duplex mode.

Auto-negotiation

Auto-negotiation can be configured only in Ethernet PHY chip. When auto-negotiation is enabled in Ethernet PHY chip, once the negotiation is completed with the other party, the PHY chip will configure itself to the desired connection mode, i.e.,10M/100M,half/full duplex mode. RC7222-A1 will monitor the negotiation result and keep it the same with PHY chip.

RC7222-A1 provides several configuration ways for some functions, the duplex mode described above, for example, can be set by PIN or register, thus, for items like this, RC7222-A1 provides 2 registers: register for configuration and register for finial configuration result. Table 4-5-3-2 is the table list for that corresponding relationship.

Table 4-5-3-2 Ethernet interface work mode configuration

No.	Functional Description	RC7222-A1 Configuration	RC7222-A1 Status	Ethernet PHY Configuration

1	10M/100M	-	Phy_speed(00.0FH[1]) 0=10Mb/s 1=100Mb/s	Configure speed register
2	Half/full duplex	Pin DUPLEX_MODI or register 00.51H[2]	duplex_mod(00.04H[2]) 0=half-duplex+full-duplex 1=full-duplex only	Configure duplex register
3	Flow control	Register 00.51H[1]	mac_pause(00.04H[1]) 0=close 1=open pause	-
4	Excessive-collision discarding	Register 51H[3]	Col16_discard_en(00.04H[3]) 0= Do not discard packet after consecutive collision 1= Discard packet after 16 consecutive collision	-
5	Auto-negotiation	Read the negotiation result from PHY Mapping register and keep it the same with PHY chip.		Configure Auto-Negotiation register

4.6 HDLC Framer/Deframer

The HDLC framer/deframer of RC7222-A1 supports 2 kinds of HDLC frame:

(1) HDLC frame compatible with RJ017: it is used to encapsulate and transmit Ethernet frame so that RC7222-A1 can communicate with RJ017;

(2) HDLC frame with special format: it is used to encapsulate and transmit Ethernet frame.

Note: There is CRC check byte in HDLC frame, CRC-H is used to indicate the CRC check format in the HDLC frame with Ethernet frame inside, while CRC-O is used to indicate the CRC-check byte in the HDLC frame with management frame(described in section ***4.6.1***) inside. Besides, there is CRC check byte called CRC-E in Ethernet frame.

Note that management frame format is defined by user, which will be encapsulated in HDLC

frame by RC7222-A1 and then be transmitted transparently.

If the HDLC deframer can not find the legal HDLC frame, the HDLC loss of frame alarm will be asserted in *Rj_hdlc_los(00.0C[1]).*

RJ017 HDLC frame format is defined like this: Remove 32 bits CRC-E from Ethernet frame, add 16bits CRC-H to the end of frame, use 7EH to be the frame header and end separately. As Fig.4-6-1 shows:

Fig.4-6-1 RJ017 HDLC frame format

4.6.1 Management frame

Management frame is used to transmit configuration and alarm information between two MCU of Local RC7222-A1 and remote one. The same as Ethernet frame, management frame can also be encapsulated in HDLC frame and be transmitted with Ethernet frame together, called In-band management frame.

Generally, the SA bits is also used as management data channel between the two MCU of local device and remote device .However, the SA bits used as serial user-defined data channel via SA interface is available only in G.704 frame mode with pin *SA_MODI* being '1'; In unframed mode, the SA bits cannot be used. While management frame encapsulated in HDLC frame can be transmitted without such trouble, as long as Ethernet frame can be transmitted, the management frame encapsulated in HDLC frame can also be transmitted.

Management frame format and encapsulation

Since both management frame and Ethernet frame are transmitted by the same channel, how to differentiate the two frames is necessary. There is a special requirement and processing for the management frame in RC7222-A1:

(1) The maximum length of payload of management frame is 59 bytes;

(2) It adopts CRC check (CRC-O) when the Management frame payload is encapsulated into the HDLC frame, there are two optional CRC-O format in register cTOAM_Oreder(11.03H[3]) and register cROAM_Oreder(11.03H[1]), when cTOAM_Oreder/cROAM_Oreder is set as '1', the CRC-O format is the same as the

CRC-H format defined in RJ017; when cTOAM_Oreder/cROAM_Oreder is set as ‘0’, the CRC-O format is complied with the standard of china Mobil.

Thus, the device can differentiate the management frame and Ethernet frame in the receiving side correctly.

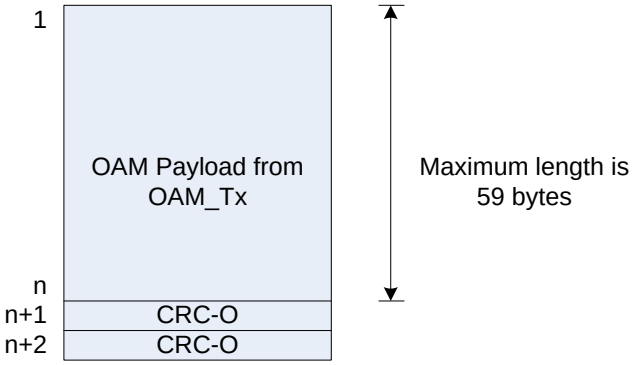

Fig.4-6-1-1 Management frame format

Management frame Transmitting

The management frame is transmitted by MCU. The MCU send the management frame payload into Management frame transmitting buffer *OAM_Tx (10.80H-10.BAH)*, note that 10.80H is the first byte; The length in bytes of management frame payload needed to be transmitted is sent to payload length register cGT_MngLen (10.04H[5:0]), note that the payload length is 1-59 bytes.

The management frame transmitting is triggered by register cGT_MngEn (10.03H[0]): Register cGT_MngEn do the inversion act, from ‘0’ to ‘1’, will trigger to transmit the management frame once. Note that register cGT_MngEn will not be back to ‘0’ automatically, so it need to be written back to ‘0’ by MCU after doing the trigger operation every time.

The management frame data from register OAM_Tx will be read by RC7222-A1 according to register cGT_MngLen, done by CRC-O checking and HDLC coding, and then be transmitted to WAN interface. The priority of management frame is higher than that of Ethernet frame, when both management frame and Ethernet frame need to be transmitted, the management frame will be transmitted first.

Note: The Ethernet frame encapsulated in HDLC frame format of RC7222-A1 is compatible with that of RJ017, that is, RC7222-A1 can communicate with the device which is compatible with RJ017. While if RC7222-A1 transmit management frame to the device that do not support

management frame, the alarm such as ultra-short frame count alarm or error frame count alarm may occurred.

Management frame Receiving

The datastream received by RC7222-A1 from WAN interface include management frame and Ethernet frame, both frame encapsulated in HDLC frame will be deframed by HDLC deframer of RC7222-A1. The frame with both maximum payload length of 59 bytes and correct CRC-O check will be known as management frame.

RC7222-A1 send the received management frame into management frame receiving buffer OAM_Rx(10.C0H-10.FAH), and write the payload length of management frame into register sGR_MngLen (10.53H[5:0]); when the receiving of management frame is finished, the buffer full flag register aGR_mng_get(10.54H[0]) will be set as '1', and then MCU can read the payload of received management frame.

When the buffer full flag aGR_mng_get is set as '1', the buffer will not receive management frame. Thus, when MCU finish to read out all the payload of received management frame, it should clear the buffer full flag aGR_mng_get by register cGR_mng_clr(10.44H[0]) and get ready to receive new management frame.

Register cGR_mng_clr=1 will clear the buffer full flag aGR_mng_get, which will make new management frame receiving, thus, MCU should write '0' into register cGR_mng_clr in time to exit clear status.

Table 4-6-1-1 Management frame transmitting and receiving

Step	Management frame transmitting
1	MCU write the payload of management frame into register OAM_Tx (10.80H-10.BAH), 10.80H is the first byte
2	MCU write the payload length in bytes into register cGT_MngLen (10.04H[5:0]), the valid length is 1-59 byte
3	MCU write and trigger register cGT_MngEn (10.03H[0]) to make cGT_MngEn do the inversion act, from '0' to '1', which will trigger to transmit the management frame once.

4	MCU write register cGT_MngEn (10.03H[0]) back to '0' to end Management frame transmitting
	Management frame receiving
Polling	MCU do the polling to the buffer full flag aGR_mng_get, when aGR_mng_get is found as '1', it will enter into the receiving steps
1	MCU read out the length of payload from the register sGR_MngLen (10.53H[5:0]), the valid length is 1-59 byte
2	According to register sGR_MngLen, MCU read out the data from register OAM_Rx(10.C0H-10.FAH)
3	MCU write '1' into the register cGR_mng_clr(10.44H[0]) after reading
4	MCU write '0' to register cGR_mng_clr(10.44H[0]) to end management frame receiving and then enter into polling status.

4.7 SDRAM Interface

4.7.1 SDRAM Pin

An external 64Mbit SDRAM is needed as the data buffer of the RC7222-A1. The SDRAM is required to be 1M×4Bank×16bit = 64Mbit, with CAS latency = 2 and BURST-8 supported. The following SDRAM are recommended: K4S641632F-75/TC1H/TL1H, K4S641632E TL1L, K4S641632H TC75 of Samsung corporation, HY57V641620HG TH and HY57V641620E series SDRAM of Hynix company.

Note: HY57V641620E series SDRAM of Hynix can't be used due to the mismatched timing order when communicating with RC7222, while that trouble is disappeared in RC7222-A1.

Interface signals between the RC7222-A1 and external SDRAM are: RASO, CASO, WEO, DQMO, BAO [1:0], ADDO [11:0], DQ [15:0] and DRAM_CLKO. The frequency of the DRAM_CLKO that the RC7222-A1 supplies to the SDRAM is half of the frequency of the CLK65I. The SDRAM interface timing is illustrated in ***Fig 7.4.2*** and the connection between the RC7222-A1 and SDRAM is as follows:

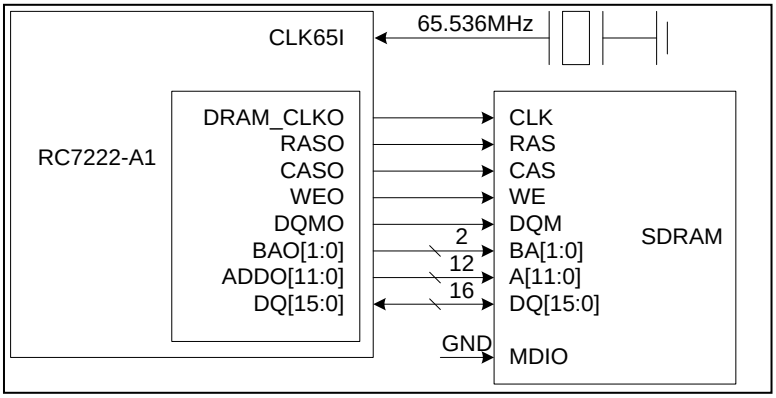

Fig.4-7-1-1 Connection between RC7222-A1 and SDRAM

The RC7222-A1 integrates a SDRAM tester in the SDRAM controller, which can scan throughout all the SDRAM cells for chip flaw or connection defects. The function will be described in section ***4.9.1.***

4.7.2 Buffer Size Adjustment

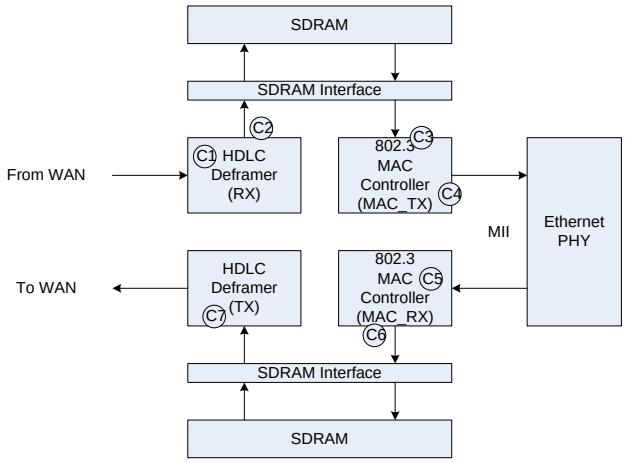

Fig.4-7-2-1 SDRAM buffer schematic diagram.

The 64Mbit SDRAM is partitioned into two logical data buffers, one for the data received from WAN interface(from WAN interface to MII interface)and the other for the data transmitted to WAN interface(from MII interface to WAN interface).

From WAN interface to MII interface, the bit rate of WAN interface is much lower than that of MII interface, without data burst emergency, the buffer size is fixed, with low delay.

From MII interface to WAN interface, the bit rate of MII interface is much higher than that of

WAN interface, e.g., the bit rate of MII interface is 100MHz, while the maximum bit rate of WAN interface(either Optical interface or E1 interface) is only 2.048MHz, thus, it seems to need large enough buffer tolerance to reduce dropped packet caused by data bursting. However, more large buffer tolerance will cause more higher delay of data transmission. It need to make a trade-off between outburst tolerance and too much delay avoidance. The adjustment is described as follows.

From MII interface to WAN interface, RC7222-A1 provides two buffer size modes: the large one and the small one. It can be configured via the pin *BUFFER_SELI.* When the pin *BUFFER_SELI* is pulled high, the buffer works in large mode and can store up to 512 frames; otherwise, it works in small mode and the buffer size will adjust itself automatically according to the E1 slots occupied for Ethernet, ranges from 32 frames to 256 frames. For example, if the Ethernet takes only 1 slot (64Kb/s) for transmission, the buffer can store up to 32 frames; if the Ethernet takes 2 slot for transmission, the buffer can store up to 64 frames; if the Ethernet employs all 32 slots, the buffer will be able to store up to 256 Ethernet frames.

When the optical mode or E1 mode is selected for the WAN interface, small buffer size is recommended. The buffer mode configuration can be viewed by register BUFFER_SEL. The logic level of Pin will change the value of register *00.06H[3]*.

4.7.3 Frame Statistic

RC7222-A1 provides frame statistic function throughout all the HDLC framer/deframer, SDRAM and MAC controller for monitoring Ethernet work status, connection defect and dropped packet. As Fig.4-7-2-1 shows, from WAN interface to MII interface, at statistic point C1 of HDLC deframer, the HDLC frame number and byte is counted for statistic, which is separately sent to register *hdlc_RxPktCnt* and *hdlc_RxByteCnt*, note that both the CRC-H correct and error frame are included in those two registers.

After the CRC-H checking for the received HDLC frame, the error CRC-H frame is counted for statistic, and the statistic result will be then sent to register *hdlc_RxCrcPkt*; Deframe HDLC and get the data frame length, the ultra-long frame statistic is sent to register *hdlc_RxOversizePkt* and ultra-short frame statistic is sent to register *hdlc_RxUndersizePkt,* all these statistic information can show the data quality received from WAN interface.

The correct data frame from HDLC deframer after CRC-H checking is written to SDRAM, at statistic point C2, the dropped frame caused by buffer tolerance shortage, is counted for statistic, and the statistic result will then be sent to register *hdlc_RxAbandonPkt*. Since the maximum bit rate of DataStream received from WAN interface is 2.048Mb/s, and the lowest read rate from SDRAM by MAC controller is not less than 5Mb/s(it is 10M and half-duplex mode for MII interface), the frame will not be discarded in normal condition, so register *hdlc_RxAbandonPkt* should be '0', while when the register is not '0', there may be some failure in SDRAM interface connection or chip works abnormal.

When MAC transmitting module(MAC_TX) read data frame from SDRAM, at statistic point C3, the error frame will be counted for statistic , and the statistic result will then be sent to register *Eth_TxBadPkt* (both ultra-long frame and ultra- short frame are known as error frame).

When MAC transmitting module (MAC_TX) transmit data frame to PHY chip, at statistic point C4, the statistic of correct byte transmitted to PHY chip is sent to register *Eth_TxGoodByte,* and the statistic of correct frame transmitted to PHY chip is sent to register *Eth_TxGoodPkt.* When flow control function is enabled (register *mac_pause(00.04H[1])*=1), it provides transmitted pause frame statistic register *Eth_TxPausePkt.* Although the statistic point C4 of register *Eth_TxPausePkt* is in the direction from MAC controller to PHY chip, this register indicate the burst level of data transmitted from PHY chip to MAC_RX.

If Ethernet interface works in half-duplex mode, it provides statistic register *Eth_Collision* for Ethernet collision counting at statistic point C4; if Ethernet interface works in half-duplex mode and the Ethernet packet is allowed to be discard after 16 consecutive collisions (*Col16_discard_en*=1), it provides statistic register *Eth_TxExcessiveCol* for Ethernet frame number counting.

When MAC receiving module receive data frame from PHY chip, at statistic point C5, the statistic of total byte received from PHY chip, including all the byte of correct and error frame, is sent to register *Eth_RxBytecnt*. After frame length checking and CRC-R checking, there is:

Undersize frame statistic register *Eth_RxErrorsizePkt,*

Oversize frame statistic register *Eth_RxOversizePkt,*

CRC check error frame statistic register *Eth_RxCrcerrorPkt* (note that oversize and undersize frame are not included) ,

Broadcast frame statistic register *Eth_RxBroadcost* (note that CRC-E error frame is not included),

Multi-broadcast frame statistic register *Eth_RxMulticast(* note that broadcast frame and CRC-E error frame are not included),

Correct frame statistic register *Eth_RxGoodPkt*(note that oversize, undersize and CRC error frame are not included),

Correct byte statistic register *Eth_RxGoodByte*(note that oversize, undersize and CRC-error frame are not included).

Note that in half-duplex mode, the receiving may not be completed caused by collision, thus the undersize packet formed in that condition will be discarded directly and not be counted into the register *Eth_RxErrorsizePkt* .

If flow-control function is not enabled (register *mac_pause(00.04H[1]*)=0), when Ethernet data burst, the frame will be discarded caused by insufficient buffer size, thus at statistic point C6, the dropped frame caused by buffer tolerance shortage, is counted for statistic, and the statistic result will then be sent to register *Eth_RxAbandonPkt*.

From HDLC framer to WAN interface direction, HDLC framer read data from SDRAM, monitor the length of frame at statistic point C7, the oversize and undersize frame will be counted into register *hdlc_TxEPktCnt* when occurred. In normal condition, MAC-RX module will not write error frame into SDRAM, if *hdlc_TxEPktCnt* is not '0', it indicates that there may be failure in the connection of SDRAM interface.

The Ethernet frame and HDLC overhead compose the HDLC frame by HDLC framer, register *hdlc_TxByteCnt* is for the total byte statistic of HDLC frame and register *hdlc_TxPktCnt* if for the frame number statistic of the transmitted HDLC frame. After statistic, the HDLC frame will be coded and transmitted.

Note: the longest Ethernet frame RC7222-A1 supported is 2031 byte, the Ethernet frame with more than 2031 byte is defined as oversize frame; the shortest Ethernet frame RC7222-A1 supported is 64 byte, the Ethernet frame with less than 64 byte is defined as undersize frame. Both the oversize frame and undersize frame are known as error frame.

4.8 SA Bit Application

There are 5 SA bits in TS0 of the odd sub-frames defined In G.704, used for custom alarm and control information transmission. RC7222-A1 provide two mode for these bits usage, which can be selected via PIN *SA_MODI*: Serial user-defined data channel accessed by external components via SA interface (SA_MODI=1) and RC7222-A1-private built-in data channel(SA_MODI=0).

In the RC7222-A1-private built-in data path, the SA bits of RC7222-A1 frame by frame compose a consecutive data frame called built-in frame. By built-in frame, local information included in the MIB registers from *00.00* to *00.7EH* can be transferred to remote MIB register *00.80-00.FEH,* orderly. It needs 320ms to transfer all the contents of *00.00-00.7EH* to the remote, that is, every 320ms, the contents of MIB register *00.80-00.FEH* will be updated once.

The status of the received SA built-in frame can be viewed by register *remote_valid(00.0FH[0]),* if *remote_valid*=1, the SA built-in frame is received normally, all the remote information via SA built-in frame is update normally, including MIB register *00.80-00.FEH* and *Remote_e1full(00.0EH[0]).*

If *remote_Valid*=0, there is something wrong with SA built-in frame receiving, such as AIS or LOF is detected in the receiving of WAN interface, SA_MODI is configured as ‘1’ , LOF is detected in built-in frame or bit-error is detected in built-in frame. Refer to register 00.0DH [1:0] for the LOF in built-in frame (*manage_lof*) and the bit-error in built-in frame (*manage_err*)

When SA_MODI=1, the SA bits will be used as serial user-defined data channel accessed by external components via SA interface. Note that this mode is available only when G.704 Deframer/framer is not bypass (in G.704 frame mode).

RC7222-A1 supports synchronous SA interface with bit rate of 20kb/s, the SA_RCKO with 20KHz is the sampled clock for SA data output, SA_RDO outputted from RC7222-A1 is presented at the rising edge of SA_RCKO, while the external component will sample SA_RDO at the falling edge of SA_RCKO; the SA_TCKO with 20KHz is the sampled clock for SA data input, SA_TDI inputted to RC7222-A1 is sampled at the rising edge of SA_TCKO, while the external component will present SA_TDI at the falling edge of SA_TCKO.

4.9 Test Function

4.9.1 SDRAM Test

RC7222-A1 integrates a SDRAM tester in the SDRAM controller, which can scan throughout all the SDRAM cells for chip flaw or connection defects.

When the pin *SDRAM_TESTI* is pulled high, the RC7222-A1 will enter into SDRAM scanning test: *TEST1_LEDO&TEST2_LEDO* will output '01'; The test procedures include: SDRAM initialization, mode setup, auto refreshing, writing and reading to/from all the SDRAM cells. During the testing, the pin *TEST3_LEDO* output low level, when all the procedures are completed, the pin *TEST3_LEDO* will output high level; If there is something wrong during the test, the pin *TEST4_LEDO* will output high. Otherwise, it output low level. Refer to Table 4-9-3-1 for more about the rest indicators.

4.9.2 Bit Error Test

RC7222-A1 provides the embedded Bit Error Ratio Tester(BERT) to support bit error test function for WAN diagnosis, which is helpful for fault localization and failure detection to WAN interface and transmission line.

There are 3 kinds of way to start BERT: by pin LINE_TESTI, by register *Net_line_test (00.18H[6])* or by register *cPrbs_TEST (11.04H[2]),* note that beside starting up the BERT, pin *LINE_TESTI* and register *Net_line_test* can send remote loopback instructions. Refer to Fig.4-2-4-1-1 for more about the three kinds of configuration way.

Here takes the configuration by register *cPrbs_TEST*(11.04H[2]) for example to describe BERT function. When register *cPrbs_TEST* =1, the BERT transmitter inserts the serial pseudo random sequence (X^{15}-1) to the timeslots that were assigned for Ethernet; the BERT receiver checks if the bit sequence pattern received is the same as that of the transmitter, and checks bit errors as well, at the same time, it will generate Loss of synchronization alarm (register *TEST3_LEDO*=1, pin *TEST3_LEDO* outputs high level) and bit error alarm (register *TEST4_LEDO*=1, pin *TEST4_LEDO* outputs high level).

When pin *LINE_TESTI* and register *Net_line_test* is '1', besides starting up the BERT, RC7222-A1 will send remote loopback instructions towards WAN interface direction. If the

remote device is RC7222-A1, the loopback instruction will be implemented. Thus BERT function can be achieved. While if register *cPrbs_TEST* is set as '1', RC7222-A1 can only start up BERT function, Remote loopback instruction cannot be sent, so it needs to adopt other ways to achieve remote loopback, such as do loopback in remote device manually.

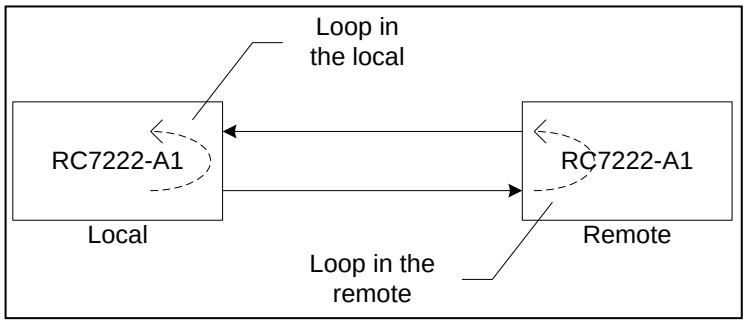

Fig.4-9-2-1 Bit Error Test Illustration

Notes: the bit error test function is based on the slots that were assigned to the Ethernet, if no slot is assigned to the Ethernet, this function cannot be provided. For example, if only timeslot 1 and timeslot 5 are assigned to transmit Ethernet data, the serial pseudo random sequence can only be inserted to timeslot 1 and timeslot 5, the BERT receiver will only check the bit errors from timeslot 1 and timeslot 5.

4.9.3 Test Indicators

TEST1_LEDO and TEST2_LEDO are used to indicate the status of the RC7222-A1, TEST3_LEDO and TEST4_LEDO are used to show the test results.

Table 4-9-3-1 Test Indicators

Work State	TEST1_LEDO &TEST2_LEDO	TEST3_LEDO	TEST4_LEDO

Work normally	00	Pulse high = software reset occurred. 0= no software reset. The pulse signal is very temporary	1 = WAN loop-back is detected; and the Ethernet transmission is paused.. 0 = normal.
SDRAM test	01	1 = SDRAM test ends 0 = test is underway	1 = SDRAM test error 0 = no errors
Local loop-back or loop-back to remote	10	Pulse high = software reset occurred. 0= no software reset. The pulse signal is very temporary	1 = WAN loop-back is detected; and the Ethernet transmission is paused 0 = normal.
Initiate the remote loop-back instruction and the bit error test	11	1 = loss of pattern 0 = sync pattern	1 = bit error occurs 0 = no errors

4.10 Software Reset

RC7222-A1 support software reset function to avoid abnormal processing to a large number invalid Ethernet packets when Ethernet network is failed. Compared with the power-on reset, the software reset only implements initializations to some of the modules, such as SDRAM controller, Ethernet MAC module, HDLC framer and deframer module and some data buffers, while some other modules such as E1 framer/de-framer, E1 interface, optical interface and management registers will still work on.

RC7222-A1 provides a register *Reset_en(00.18H[4])* to enable or disable software Reset function. When *Reset_en*=1, the software reset function can be used. When *Reset_en*=1, write '1' into *Reset_cmd(00.18H[5])*, the software reset is completed, after software reset, RC7222-A1 will write '0' into register *Reset_cmd* automatically.

5 Management Description

5.1 Register Address Organization

The register of RC7222-A1 is organized as 3 pages named as Page00, Page10 and Page11 separately, and page01 is reserved. Each page consists of 256 bytes, with address space from 01H to FFH. The address of all the registers in this article will consist of page address and register address in page, e.g.:*00.18H[5]*. Descriptions of the 3 register pages is as follow:

Page00 is configuration and alarm register called MIB register page. Registers from 00H to 7EH are configuration and alarm registers for local device; Registers from 80H to FEH in local RC7222-A1 are the mapping of 00H-7EH registers in remote RC7222-A1, which is transmitted by SA built-in channel, refer to section ***4.8*** for more about SA bits.

Note: Part of register status of PHY chip can be got from register 00.19H-00.1DH in page00 of RC7222-A1. Part of PHY status defined in IEEE802.3, such as 10M/100M settings, half/full duplex settings and so on, will be written into register 00.19H-00.1DH of RC7222-A1 via MDIO interface. Thus, MCU can get information about PHY easily.

Page10 is the management frame receiving & transmitting register, called management frame register(OAM register).

Page11 is the added functional register during chip updating progress, called globe register.

Note: Register FFH is a special register, when UART interface is used to access registers of RC7222-A1 (Pin MANAGE_MODI=0), register FFH is unavailable; when I^2C interface is used to access registers of RC7222-A1 (pin MANAGE_MODI=1), register FFH is the page selection register. Register FFH can be accessed directly, the three FFH in three register pages compose a FFH register. Use I^2C write command to write the page address that required to be accessed into FFH register, Page00, for example, and then use I^2C read/write command to access register of Page00.

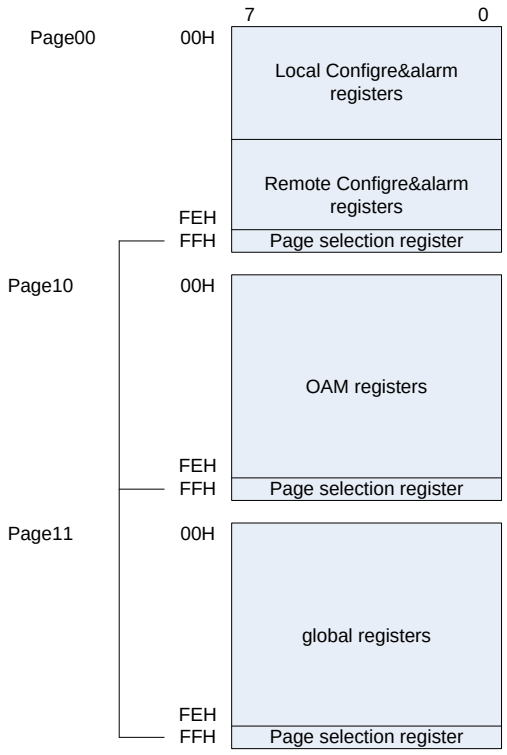

Fig.5-1-1 Register Address Organization

5.2 Management Interface（UART/I2C）

The RC7222-A1 management interface has two options: UART and I^2C.

There are three pins for management interface: *MANAGE_MODI, UART_DO/SDA* and *UART_DI/SCLI.* When *MANAGE_MODI* is pulled low, it is UART mode, and the interface signal is UART_DO and UART_DI; while when *MANAGE_MODI* is pulled high, it is I^2C mode, and the interface is SDA and SCLI.

UART Interface: UART interface consist of two signals, UART_DI, the data input signal; and UART_DO, the data output signal. It is 19200 baud per second, 8-bit data, 1-bit start, 1-bit stop, odd parity and no flow control.

I2C interface: I2C interface consist of two signals, SDA, the bi-directional data signal; and SCLI, the input clock signal. RC7222-A1 can only act as a slave device of the standard 100Kbps I2C interface with 7 bit address input.

The device address for management is input via pin SET_AI. Note that if UART interface is selected as management interface, the device address for UART management is 8 bits , while if I^2C interface is selected as management interface, the device address for I^2C management is

7 bits.

The user-defined signal with 8 bits (*SELF_PIN[7:0])* can also be input by pin *SET_AI*, the value of SELF_PIN can be read from register *00.15H.* it is facility for device designing. For example, PCB version can be sent to chip via SELF_PIN and read by MCU. Since the value of SELF_PIN can be sent to the remote device, some card alarm and status can be sent via SELF_PIN to the remote device, the LINK status of Ethernet PHY chip, for example, can be sent via SELF_PIN to the remote device.

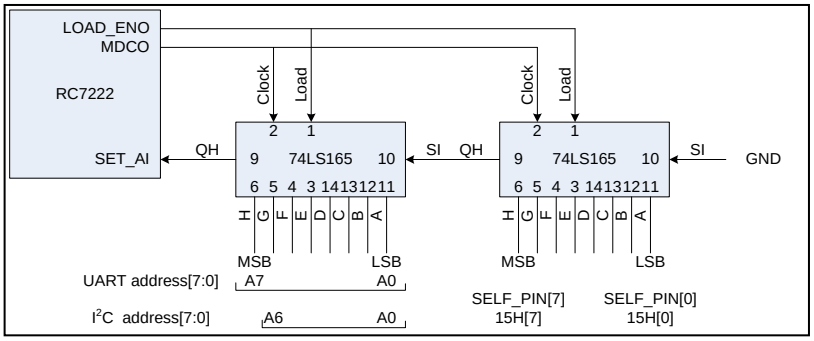

Fig.5-2-1 Device address for management and Use-defined signal input

5.3 UART Instructions

The management system(MCU) initiates configuration instructions and inquiry instructions to RC7222-A1 via UART interface; the RC7222-A1 will acknowledge when it receives the instructions. RC7222-A1 does not initiate any instructions.

The format of configuration instructions and inquiry instructions is shown in Table 5-3-1, the format of acknowledge instructions is shown in Table 5-3-2.

Table 5-3-1 UART Instructions of Configuration and Inquiry

Frame Flag	Device Address	Command Type	Sequence	Register address	Data	Checksum
2Byte	1 Byte	1 Byte	2 Byte	1 Byte	4Byte	1 Byte

Table 5-3-2 UART acknowledge instructions

Frame Flag	Device Address	Device Name	Sequence	Register address	Data	Checksum

2Byte	1 Byte	2 Byte	2 Byte	1Byte	8 Byte	1 Byte

Table 5-3-3 Descriptions for UART configuration and inquiry instruction

Byte	Name	Descriptions	
1	Frame Flag	7EH	
2		81H	
3	Device Address	When Device Address is identical with the address inputted from pin SET_AI, the corresponding RC7222-A1 will respond, otherwise, it will not send acknowledged frame	
4	Command type	02H: Inquire Page00 register	06H: configure Page00 register
		03H: Inquire Page10 register(OAM register)	07H: configure Page10 register (OAM register)
		05H: Inquire Page11 register (Globe register)	09H: configure Page11 register (Globe register)
5	Sequence	Sequence number of frame. Note 1	
6			
7	Register address	Register address.	
8	Data	00H	Configuration data [7:0]
9		00H	00H
10		00H	00H
11		00H	00H
12	Check sum	Frame check byte, calculate throughout 1-11 bytes of the frame. The configuration and inquiry will be ignored if the checksum is incorrect. Note 2	

Note1: RC7222-A1 will not process the Sequence byte received, but inserts this received sequence into acknowledge frame and transmits back to MCU, thus, MCU can match the

inquire/configuration frame and acknowledged frame.

Note2: Check sum=byte1 xor byte2 xor byte3 ..... Xor byte10 xor byte11

Table 5-3-4 Descriptions for UART Acknowledged Frame

Byte	Name	Descriptions
1	Frame Flag	7EH
2		81H
3	Device Address	It is identical with the address inputted from pin SET_AI
4	Device Name	72H
5		22H
6	Sequence	Sequence number of acknowledged frame, identical with the frame sequence number of corresponding inquire/configuration instruction.
7		
8	Register address	Register address(reg_addr)
	Data Note1	Inquire or configure page 00/10/11 register
9		Data(reg_addr)
10		Data(reg_addr+1)
11		Data(reg_addr+2)
12		Data(reg_addr+3)
13		Data(reg_addr+4)
14		Data(reg_addr+5)
15		Data(reg_addr+6)
16		Data(reg_addr+7)
17	Check sum	Frame check byte, calculate throughout 1-16 bytes of the frame Note 2

Note1: RC7222-A1 will return back 8-byte data in its acknowledged frame at a time, the 8-byte data is the value in the 8 registers from register(reg_addr) to register(reg_addr+7).

Note2: Check sum=byte1 xor byte2 xor byte3 ..... Xor byte15 xor byte16

5.4 I²C Instruction

RC7222-A1 can only act as a slave device of the standard 100Kbps I²C interface.

I²C instruction includes write instruction and read instruction. Writing and reading operations need to select page register first, as Fig.5-1-1 shows, the register address of RC7222-A1 is divided into 4 pages, the selection of page register for reading/writing is decided by register FFH[1:0], for example, if FFH[1:0]=11, MCU can only read/write Page11 register of RC7222-A1; if MCU need to do read/write operation to Page10 register, it need to write '10' into register FFH[1:0] first, and then the MCU can access into Page10 register.

Table 5-4-1 I2C configuration and inquiry instruction Frame Format

	Read/write operation	Frame format
1	Write page name into register FFH[1:0]	The frame format of these two write instructions are the same. The write operation will write one byte into one register once, refer to Table 5-4-2 for more
2	Write register of page00/10/11	
3	Read register of page00/10/11	The read operation will read several bytes from one register and the subsequent register once. Refer to Table 5-4-4 for more

Table 5-4-2 I2C write operations to register

Byte	Description										
	S/Sr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	ACK	P
1	S	Chip address[6:0], identical with the address inputted from pin SET_AI							W	A Note 1	
2		Page register address(FFH) or Register address in page 00/10/11								A	

3		Data(reg_addr)	A	P

Note1: The fonts in black color indicates that it is from MCU to RC7222-A1, while the fonts in blue color indicates that it is from RC7222-A1 to MCU. I^2C data signal is bi-directional data signal, during write operation, only ACK signal is from RC7222-A1 and be outputted to MCU.

Table 5-4-3 I2C read operation to register

Byte	Description									
	S/Sr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	ACK	P
1	S	Chip address[6:0], identical with the address inputted from pin SET_AI							W	A Note 1	
2		Register address(reg_addr)								A	
3	Sr Note 2	Chip address[6:0], identical with the address inputted from pin SET_AI							R	A	
4		Data(reg_addr)								A	
5		Data(reg_addr+1)								A	
.....		.....								A	
4+n		Data(reg_addr+n)								Ã	P

Note1: The fonts in black color indicates that it is from MCU to RC7222-A1, while the fonts in blue color indicates that it is from RC7222-A1 to MCU.

Note2: The read operation need to write the expect register address first, and then read the register by restart way.

5.5 Register Description

5.5.1 MIB Register

Mapping Register

Registers from *00.00H* to *00.7EH* of MIB register (Page00) is configuration and alarm register for local device; Registers from *00.80H* to *00.FEH* in local RC7222-A1 are the mapping of

00.00H-00.7EH registers in remote RC7222-A1, which is transmitted by SA built-in channel, thus, *00.80H-00.FEH* is available only in G.704 framed mode(G.704_bypass=0) and data channel formed by the SA bits is dedicated for the RC7222-A1-specific usage (SA_MOD=0). refer to section ***4.8*** for more about SA bits.

Statistic and Latch Register

Both the performance statistic register (the register with the suffix '_cnt') and the alarm latch register (the register with the suffix '_P') in MIB register (page00) are updated periodically.

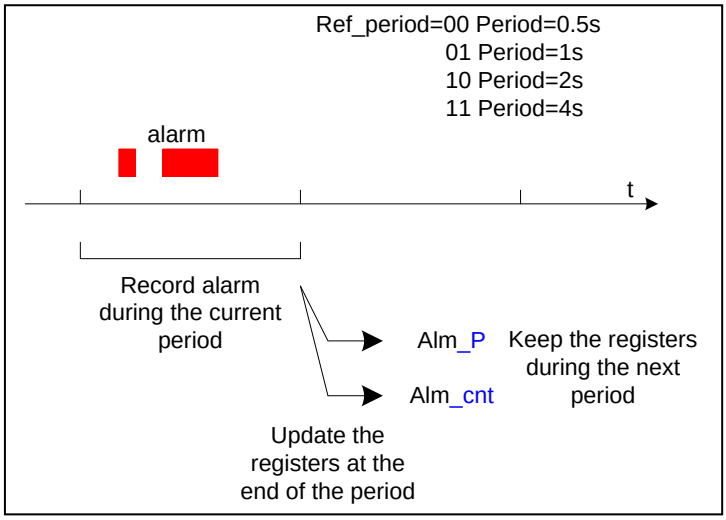

Fig. 5-5-1-1 the update of Statistic and latch register

RC7222-A1 will set the timing period of the timer by register *ref_period* (*00.0BH[7:6]*), monitor and record the alarm during each timing period, write alarm into the alarm latch register and alarm statistic value into the alarm statistic register; the value of alarm latch register and alarm statistic register will keep unchanged during the next timing period.

Note that the alarm statistic register is a counter which will stop counting when it is full, for example, *CRC_cnt* is a 8-bit counter which can count for 255 CRC bit errors at most, if the number of CRC bit error occurred during one timing period is over 255, the value of *CRC_cnt* is 255.

The start of timing period can be indicated by register *tim_show(00.18H[1:0]*). the value of register *tim_show* will be accumulated at each start of time period , which can be monitored by MCU. The MCU will read the latched alarm and alarm statistic when the register *tim_show* is changed, thus, it provides facility for timing statistic function, statistic for bit error second, for

example.

The default value of Register *ref_period* is '01', that means the default timing period is one second.

Multiple Configuration Sources

RC7222-A1 support multiple configuration sources for some configuration item, the timeslot assignment, for example, can be configured by Pin, register or remote chip(timeslot coupling).

Generally, in default, the priority of pin settings is higher than the settings of register, the device can work normally without MCU controlling; the register settings can be set effective and the Pin settings will be invalid at the same time.

For example, timeslot assignment can be configured by both Pin *SET_AI* and register *00.53H-00.56H*, in default, the priority of register settings is lowest, it can be only configured by Pin *SET_AI*; it can be configured by MCU via registers, just to make register 00.53H-00.56H effective by writing A5 into register *00.58H[7:0]*, and then configure 00.53H-00.56H, and the pin *SET_BI* settings will be invalid at the same time.

RC7222-A1 provides status register specially to show the configuration result for multiple configuration source. In the following register list, the table format with gray color shading indicate that the corresponding register has multiple configuration source.

Alarm Inhibit

All the alarm of RC7222-A1 has the corresponding alarm register, part of the alarm can also be output via pin. The alarm outputted by pin is specified to have priority and alarm inhibit relationship, while the alarm in registers is not specified to have priority and alarms inhibit relationship.

The priority and alarm inhibit relationship of alarm registers should be done in MCU according to the description about alarm inhibit relationship in section ***4.2*** if the alarm will be readout by MCU.

Table 5-5-1-1 MIB register (Page00)

Add	Bit	Name	R/W	Default	Description
Chip ID Register					
00H	7-0	Device NameH	RO	72H	**RC7222-A1 ID**
01H	7-0	Device NameL	RO	22H	
02H	7-0	IC VERSIONH	RO	10H	**IC version, Note: the version of RC7222 is 0000H, and the version of RC7222-A1 is 1000H**
03H	7-0	IC VERSIONL	RO	00H	
Configuration register(with priority controlling)					
57H	7-0	Cfg_04H_Prior	WR	00	**Make Ethernet MAC configuration register(51H) effective** A5= register(51H) is effective; Other values= pin settings is effective; Note: in practical application, only *Duplex_mod* of register(51H) has multiple configuration source, it needs to write 'A5' into register(57H) to make register(51H) effective, thus, the *Duplex_mod* of register(51H) is effective.
58H	7-0	Cfg_070AH_Prior	WR	00	**Make timeslot assignment register(56H-53H) effective** A5= register(56H-53H) is effective; Other values= pin settings is effective; Note: timeslot assignment can be configured by Pin SET_AI or register(56H-53H), refer to section ***4.3 f***or more.
59H	7-0	Cfg_06H_Prior	WR	00	**Make configuration register(52H) effective** A5= register(52H) is effective; Other values= pin settings is effective;

51H	7	Loopcut_en_n	WR	00	**WAN interface loopback** 0= stops transferring Ethernet data to the LAN when WAN loopback is detected, avoiding the mess of the Ethernet network. 1= go on transferring ignorant of the WAN loop
	6	Reserved	WR		**Reserved**
	5	Reserved	WR		**Reserved**
	4	Reserved	WR		**Reserved**
	3	Col16_discard_en	WR		**Discard the Ethernet packet after 16 consecutive collisions** 1= In Ethernet half-duplex mode, the device will discard the current Ethernet packet transmitted (MII interface output direction) after 16 consecutive collisions; 0= the MAC controller will go on retrying, neglecting the excessive collisions.
	2	Duplex_mod	WR		**Duplex mode selection** 1 = Only full-duplex mode is supported 0 = Half-duplex mode
	1	Mac_pause	WR		**Flow control** 1 = PAUSE frame enable. 0 = PAUSE frame disable.
	0	Reserved	WR		**Reserved**
52H	7-5	Reserved	-	00H	**Reserved**
	4	Reserved_Test	RW		Reserved for Test Note: if this register is valid(59H is configured to A5), Reserved_Test must be set to 1 to disable the test function.

	3	BUFFER_SEL	RW		**Buffer size selection from MII to WAN direction** 1 = large buffer size, Strong ability of anti-burst, high delay; 0 = small buffer size, weak ability of anti-burst, low delay.
	2	Reserve	-		**Reserved**
	1	TIM_MOD	RW		**Timing mode selection** 1 = local oscillator 0 = tracing the line timing via WAN interface
	0	Reserved	RW		**Reserved**
53H	7-0	Bandwidth(7-0)	WR	00	**Timeslot Assignment** Each bit corresponds to a timeslot, the bit7 of 56H corresponds to timeslot 31, and the bit0 of 53H corresponds to timeslot 0. 1= the corresponding timeslot is assigned to HDLC (Ethernet) 0= the corresponding timeslot is assigned to ST-BUS interface
54H	7-0	Bandwidth(15-8)	WR	00	
55H	7-0	Bandwidth(23-16)	WR	00	
56H	7-0	Bandwidth(31-24)	WR	00	
Status register(the final configuration result)					
04H	7	Loopcut_en_n	RO	0	**WAN interface loopback** 0= stops transferring Ethernet data to the LAN when WAN loopback is detected, avoiding the mess of the Ethernet network. 1= go on transferring ignorant of the WAN loop Refer to section 4.2.6 for more.
	6	Reserved	RO	0	**Reserved**
	5	Reserved	RO	0	**Reserved**
	4	Reserved	RO	0	**Reserved**

	3	Col16_discard_en	RO	0	**Discard the Ethernet packet after 16 consecutive collisions** 1= In Ethernet half-duplex mode, the device will discard the current Ethernet packet transmitted (MII interface output direction) after 16 consecutive collisions; 0= the MAC controller will go on retrying, neglecting the excessive collisions.
	2	Duplex_mod	RO	0	**Duplex mode selection** 1 = Only full-duplex mode is supported 0 = Half-duplex mode Note: Duplex_mod can be configured by pin DUPLEX_MODI or *register duplex_mod(51H[2])*
	1	Mac_pause	RO	0	**Flow control** 1 = PAUSE frame enable. 0 = PAUSE frame disable.
	0	Reserved	RO	0	**Reserved**
	Note: Duplex_mod can be configured by pin DUPLEX_MODI or register *duplex_mod(51H[2])*				
05H	7	Reserved	RO	1	**Reserved**
	6	WAN_MOD1I (from Pin)	RO	-	**WAN interface selection** WAN_MOD1I&WAN_MOD0I: 01= E1 interface is used as WAN interface; 11= optical interface is used as WAN interface
	5	WAN_MOD0I (from Pin)	RO	-	
	4	Reserved	RO	1	**Reserved**
	3	Reserved	RO	-	**Reserved**

	2	SA_MODI (from Pin)	RO	-	**Usage of SA bits** 0 = The SA bit is used to form the private built-in frame 1 = The SA bit is used to form the serial user-defined data channel, which is open to SA interface Refer to section ***4.8*** for more
	1	CODE_TYPEI (from Pin)	RO	-	**E1 interface code type** 0=HDB3 1=NRZ
	0	Reserved	RO	-	**Reserved**
	Note: the registers marked with 'from Pin' is from pin directly, the MCU can get the current configuration by the registers				
06H	7	G.704_bypass	RO	-	**G.704 framer/deframer bypass (framed /unframed)** 1=G.704 framer/deframer is bypass(unframed) 0=G.704 framer/deframer works(framed)
	6	Pcm31_sel	RO	-	**PCM30/31** 1=PCM31 mode 0=PCM30 mode

	5	E1crc_sel	RO	-	**G.704 CRC-4 multiframe mode in WAN interface input direction** 0 = CRC-4 is not adopted by the transmitter (Non-CRC-4 multiframe) 1 = CRC-4 is adopted by the transmitter (CRC-4 multiframe) Note: the G.704 deframer can do self-check and self-adaption in WAN interface input direction, register E1crc_sel indicates the result of self-check. In WAN interface output direction, the G.704 framer can only send CRC-4 multiframe. Refer to section ***4.3*** for more
	4	Reserved	RO	-	Reserved
	3	BUFFER_SEL	RO	-	**Buffer size selection from MII to WAN direction** 1 = large buffer size, Strong ability of anti-burst, high delay; 0 = small buffer size, weak ability of anti-burst, low delay. Refer to section ***4.5.2*** for more
	2	Reserved	RO	-	**Reserved**
	1	TIM_MOD	RO	-	**Timing mode selection** 1 = local oscillator 0 = tracing the line timing via WAN interface Refer to section ***4.2.5*** for more
	0	Reserved	RO	-	**Reserved**

	Note: *G.704_bypass/PCM31_sel* is decided by timeslot assignment; *E1CRC_sel* is the self-adaption result of G.704 deframer; *BUFFER_SEL* can be configured by pin *BUFFER_SELI* or register *BUFFER_SEL(52H[3]);* *TIM_MOD* can be configured by pin *TIM_MODI* or register *TIM_MOD(52H[1])*;				
07H	7-0	Bandwidth(31-24)	RO	-	**Timeslot Assignment** Each bit corresponds to a timeslot, the bit7 of 07H corresponds to timeslot 31, and the bit0 of 0AH corresponds to timeslot 0. 1= the corresponding timeslot is assigned to HDLC (Ethernet) 0= the corresponding timeslot is assigned to ST-BUS interface Note only when BAND_MOD=1, the configuration of timeslot assignment can be carried out , refer to section ***4.3*** for more. Note: the bit0 of 0AH is 1 means unframed mode.
08H	7-0	Bandwidth(23-16)	RO		
09H	7-0	Bandwidth(15-8)	RO		
0AH	7-0	Bandwidth(7-0)	RO		
	Note: timeslot assignment can be configured by Pin *SET_AI* or register *00.53H-00.56H*, refer to section ***4.3*** for more.				
Configuration and alarm Register					
0BH	7-6	Ref_period	WR	01	The update period of Statistic and latched register 00 = 0.5s; 01 = 1s; 10 = 2s; 11 = 4s Refer to '5.5.1 statistic and latch register' for the definition of update period
	5-4	Reserved	WR	00	**Reserved**

	3	Reserved	WR	0	**Reserved**
	2	Reserved	RO	0	**Reserved**
	1	Reloop_get	RO	0	**Receive the valid remote loopback instruction** 1= received the valid remote loopback instruction 0=not received the valid remote loopback instruction
	0	Reloop_reply	RO	0	**Respond to remote loopback** 1= Respond to the remote loopback instruction, the loopback is activated by local and toward line direction at the loopback point of local WAN interface 0=Do not respond to the remote loopback instruction RC7222-A1 will execute the remote loopback conditionally when receive the remote loopback direction, refer to section ***4.2.4.1*** and ***4.2.4.2*** for more.
0CH	7	TEST1_LODO_P	RO	0	**Test indicators** Refer to Table 4-9-3-1 for descriptions Note that these registers are latch register, update periodically, refer to 'Statistic and Latch Register' in section ***5.5.1*** for more.
	6	TEST2_LODO_P	RO	0	
	5	TEST3_LODO_P	RO	0	
	4	TEST4_LODO_P	RO	0	
	3	Reserved	RO	0	**Reserved**
	2	Extloop_done	RO	0	**WAN interface loopback alarm** 1= loopback to the chip at the loopback point of WAN interface is detected The WAN interface loopback can be detected by comparing Ethernet MAC address, refer to section ***4.2.6*** for more.
	1	Rj_hdlc_los	RO	0	**HDLC frame out of synchronization alarm** 1= frame out of synchronization alarm

	0	Reserved	RO	0	Reserved
0DH	7	OPT_SD	RO	0	**Loss of optical signal alarm**
	6	OPT_LOF	RO	0	**Optical frame out of synchronization**
	5	OPT_AE3	RO	0	**Optical 10-3 bit error alarm**
	4	OPT_AE6	RO	0	**Optical 10-6 bit error alarm**
	3	Opt_rlos	RO	0	**Remote loss of optical signal alarm**
	2	Opt_rlof	RO	0	**Remote Optical frame out of synchronization**
	1	Manage_lof	RO	0	**SA bit built-in frame receiving out of synchronization alarm**
	0	Manage_err	RO	0	**SA bit built-in frame receiving check error alarm**
	Note: All the alarm registers use '1' to indicate alarm, '0' to indicate no alarm All the alarm in *0DH* are shown in real time *Manage_lof/Manage_err* is valid only when the SA bits are employed for RC7222-A1-specific built-in frame(SA_MODI=0), it is used to check the consistency of SA_MODI between local and remote, refer to section ***4.8*** for more.				
0EH	7	Los_P	RO	0	**Loss of E1 signal alarm latch**
	6	Ais_P	RO	0	**All '1' in G.704 frame alarm latch**
	5	Lof_P	RO	0	**G.704 frame out of synchronization alarm latch**
	4	Ral_P	RO	0	**G.704 remote alarm latch**
	3	Opt_los_P	RO	0	**Loss of optical signal alarm latch**
	2	Opt_lof_P	RO	0	**Optical frame out of synchronization alarm latch**
	1	Opt_ral_P	RO	0	**Remote optical alarm latch**

	0	Remote_e1full	RO	0	**Remote G.704 framer/deframer bypass (framed /unframed)** 1=the remote G.704 framer/deframer is bypass (works in the unframed E1 mode); 0= the remote G.704 framer/deframer is not bypass (works in the framed E1 mode); Note that it is valid only when the SA bits are employed for RC7222-A1-specific built-in frame(SA_MODI=0).
	Note: All the registers with the suffix '_P' are latch registers, refer to 'statistic and latch register' in section ***5.5.1*** for the updated of the registers.				
0FH	7	LOSO	RO	0	**Loss of E1 signal alarm**
	6	AISO	RO	0	**All '1' in G.704 frame alarm**
	5	Lomf	RO	0	**G.704 multi-frame out of synchronization alarm**
	4	LOFO	RO	0	**G.704 frame out of synchronization alarm**
	3	CRC_ERRO	RO	0	**G.704 CEC check error alarm**
	2	RALO	RO	0	**G.704 remote alarm**
	1	Phy_speed	RO	0	**MII interface bit rate** 1=100Mbit/s；0=10Mbit/s RC7222-A1 will detect the 10M/100M mode automatically by the clock signal received from PHY chip, *Phy_speed* is the detection result of RC7222-A1

	0	Remote_valid	RO	0	**The receive status of SA built-in frame** 1= SA built-in frame received normal, MIB register *00.80H-00.FEH* and register *Remote_e1full* (show the work status of remote device) are valid; SA built-in frame received abnormal, MIB register *00.80H-00.FEH* and register *Remote_e1full* (show the work status of remote device) are invalid; Refer to section ***4.8*** for more.
	Note: all the alarm in *0FH* are shown in real time				
10H	7-0	CRC_CNT[7:0]	RO	00H	**G.704 CRC4 bit error statistic**
11H	7-0	CV_CNT[15:8]	RO	00H	**E1 interface Code Violation statistic**
12H	7-0	CV_CNT[7:0]	RO	00H	
13H	7-0	CHIP_ADDR	RO	00H	**Chip address inputted via pin SET_AI**
14H	7-0	SELF_DFF	WR	00H	**User-defined information, which is transmitted to remote device via SA built-in frame**
15H	7-0	SELF_PIN	RO	00H	**User-defined information via PIN SET_AI.**
16H	7-0	Reserved	RO	00H	**Reserved**
17H	7-0	Reserved	RO	00H	
18H	7	Net_wanloop	WR	0	**Local WAN interface loopback** 1= loopback
	6	Net_line_test	WR	0	**Local WAN interface test** 1= enable the BERT, insert test stream into WAN interface and activate remote loopback
	5	RESET_CMD	WR	0	**Software Reset** This register is valid when Reset_en=1; Write '1' into *RESET_CMD* to do software reset, it will be cleared automatically after software reset.
	4	RESET_EN	WR	0	**Software reset enable** 1= enable software reset; 0= disable software reset

	3	WANLOOP_SELI (from pin)	RO	0	**Local WAN interface loopback** 1=loopback
	2	LINE_TESTI (from pin)	RO	0	**Local WAN interface test** 1= enable the WAN interface testing, insert test stream into WAN interface and activate remote loopback
	1-0	Tim_show	RO	00	**Period counter, Accumulate after a statistic interval**
	Note1: The registers marked with 'from Pin' is from pin directly, the MCU can get the current configuration by the registers Note2: Refer to section ***4.2.4*** for more about Net_wanloop, Net_line_test, WANLOOP_SELI and LINE_TESTI				
PHY Mapping Register RC7222-A1 periodically retrieves information from the PHY chip via the MDIO interface and records some of the information in the registers 19H-1DH. The address mapping is marked in the name of registers, for example, Reset(0.15) means the name of register is Reset, located in bit15 of register 0 of PHY chip (bit sequence is 15:0, the bit 15 is MSB)					
19H	7	Reset(0.15)	RO	-	1 = Reset chip. 0 = Enable normal operation.
	6	Loopback(0.14)	RO	-	1 = Enable loopback mode 0 = Disable loopback mode
	5	Speed Selection(0.13)	RO	-	1 = 100 Mbps 0 = 10 Mbps
	4	Auto-Negotiation Enable(0.12)	RO	-	1 = Enable auto-negotiate process (overrides speed select and duplex mode bits). 0 = Disable auto-negotiate process.
	3	Power Down(0.11)	RO	-	1 = Enable power down. 0 = Enable normal operation.
	2	Isolate(0.10)	RO	-	1 = Electrically isolate PHY from MII. 0 = Normal operation.

	1	Restart Auto-Negotiation(0.9)	RO	-	1 = Restart auto-negotiation process. 0 = Normal operation.
	0	Duplex Mode(0.8)	RO	-	1 = Enable full-duplex. 0 = Enable half-duplex.
1AH	7	Collision Test (0.7)	RO	-	1 = Enable COL signal test 0 = Disable COL signal test
	6	100BASE-T4 (1.15)	RO	-	1 = 100BASE-T4
	5	100BASE-X full-duplex (1.14)	RO	-	1 = Full-duplex 100BASE-X.
	4	100BASE-X half-duplex (1.13)	RO	-	1 =Half-duplex 100BASE-X.
	3	10 Mb/s full-duplex (1.12)	RO	-	1=10 Mb/s full-duplex
	2	10 Mb/s half-duplex(1.11)	RO	-	1=10 Mb/s half-duplex
	1	MF Preamble Suppression (1.6)	RO	-	0 = Not accept management frames with preamble suppressed.
	0	Auto-Negotiation Complete (1.5)	RO	-	1 = Auto-negotiation process complete. 0 = Auto-negotiation process not complete.
1BH	7	Remote Fault(1.4)	RO	-	1 = Remote fault condition detected. 0 = No remote fault condition detected.
	6	Auto-Negotiation Ability(1.3)	RO	-	1 = Able to perform auto-negotiation.
	5	Link Status(1.2)	RO	-	1 = Link is up. 0 = Link is down.
	4	Jabber Detect(10BASE-T Only)(1.1)	RO	-	1 = Jabber condition detected. 0 = No jabber condition detected.

	3	Extended Capability(1.0)	RO	-	1 = Extended register capabilities.
	2	Remote Fault(4.13)	RO	-	1 = Remote fault. 0 = No remote fault.
	1	Pause(4.10)	RO	-	1 = Pause operation is enabled for full-duplex links. 0 = Pause operation is disabled.
	0	100BASE-T4 (4.9)	RO	-	1 = 100BASE-T4 capability is available.
1CH	7	100BASE-TX full-duplex(4.8)	RO	-	1 = DTE is 100BASE-TX full-duplex capable. 0 = DTE is not 100BASE-TX full-duplex capable.
	6	100BASE-TX (4.7)	RO	-	1 = DTE is 100BASE-TX capable. 0 = DTE is not 100BASE-TX capable.
	5	10BASE-T full-duplex(4.6)	RO	-	1 = DTE is 10BASE-T full-duplex capable. 0 = DTE is not 10BASE-T full-duplex capable.
	4	10BASE-T(4.5)	RO	-	1 = DTE is 10BASE-T capable. 0 = DTE is not 10BASE-T capable.
	3	Acknowledge (5.14)	RO	-	1 = Link Partner has received Link Code Word. 0 = Link Partner has not received Link Code Word.
	2	Remote Fault(5.13)	RO	-	1 = Remote fault. 0 = No remote fault.
	1	Pause(5.10)	RO	-	1 = Pause operation is enabled for link partner. 0 = Pause operation is disabled.
	0	100BASE-T4 (5.9)	RO	-	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.
1DH	7	100BASE-TX full-duplex (5.8)	RO	-	1 = Link Partner is 100BASE-TX full-duplex capable. 0 = Link Partner is not 100BASE-TX full-duplex capable.
	6	100BASE-TX (5.7)	RO	-	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.

	5	10BASE-T full-duplex (5.6)	RO	-	1 = Link Partner is 10BASE-T full-duplex capable. 0 = Link Partner is not 10BASE-T full-duplex capable.
	4	10BASE-T (5.5)	RO	-	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.
	3	Parallel Detection Fault (6.4)	RO	-	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.
	2	Link Partner Next Page Able (6.3)	RO	-	1 = Link partner is next page able. 0 = Link partner is not next page able.
	1	Page Received (6.1)	RO	-	1 = 3 identical and consecutive link code words have been received from link partner. 0 = 3 identical and consecutive link code words have not been received from link partner.
	0	Link Partner Auto Negotiation Able (6.0)	RO	-	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.
50H	7-0	Cfg_phy_addr	WR	01	**PHY management address register** It should be identify with the actual PHY chip address, thus it can read/write registers of PHY chip via MDIO interface. Refer to section ***4.5.2*** for more
Performance statistic for HDLC framer/deframer (1EH-2CH) CRC-H is referred to the CRC check in HDLC frame, the statistic point is indicated in registers. Refer to section ***4.7.3*** for more.					
1EH	7-0	hdlc_TxByteCnt[23:16]	RO	00H	**The total bytes statistic (C7) for the HDLC frame which is transmitted by HDLC framer**
1FH	7-0	hdlc_TxByteCnt[15:8]			
20H	7-0	hdlc_TxByteCnt[7:0]			
21H	7-0	hdlc_ TxPktCnt[15:8]	RO	00H	**The total frame number statistic (C7) for the HDLC frame which is transmitted by HDLC framer**
22H	7-0	hdlc_ TxPktCnt[7:0]			

23H	7-0	hdlc_TxEPktCnt[7:0]	RO	00H	**Error frame statistic (C7) read from SDRAM by HDLC framer**
24H	7-0	hdlc_RxByteCnt[23:16]	RO	00H	**The total bytes statistic (C1) for the HDLC frame which is received from WAN interface by HDLC deframer** The total bytes are the bytes of all the correct and error frame.
25H	7-0	hdlc_RxByteCnt[15:8]			
26H	7-0	hdlc_RxByteCnt[7:0]			
27H	7-0	hdlc_RxPktCnt[15:8]	RO	00H	**The total frame numbers statistic (C1) for the HDLC frame which is received from WAN interface by HDLC deframer** The total frame numbers are the number of all the correct and error frame.
28H	7-0	hdlc_RxPktCnt[7:0]			
29H	7-0	hdlc_RxOversizePkt[7:0]	RO	00H	**The frame number statistic (C1) for the oversize data frame which is received from WAN interface by HDLC deframer**
2AH	7-0	hdlc_RxUndersizePkt[7:0]	RO	00H	**The frame number statistic (C1) for the undersize data frame which is received from WAN interface by HDLC deframer**
2BH	7-0	hdlc_RxCrcPkt[7:0]	RO	00H	**The frame number statistic (C1) for the CRC-H check error frame which is received from WAN interface by HDLC deframer**
2CH	7-0	hdlc_RxAbandonPkt[7:0]	RO	00H	**The statistic of frame abandoned owing to insufficient buffer size when writing to SDRAM (C2)**
Performance statistic for Ethernet MAC (2DH-45H) CRC-E is referred to the CRC check in Ethernet frame, the statistic point is indicated in registers. Refer to section ***4.7.3*** for more.					
2DH	7-0	Eth_RxBytecnt[23:16]	RO	00H	**The received byte statistic (C5) from PHY chip by MAC**
2EH	7-0	Eth_RxBytecnt[15:8]	RO	00H	

2FH	7-0	Eth_RxBytecnt[7:0]	RO	00H	The total bytes are the byte of all the correct and error frame. Note that in half-duplex mode, the receiving may not be completed caused by collision, thus the undersize packet formed in the condition will be discarded directly and not be counted.
30H	7-0	Eth_RxErrorsizePkt[7:0]	RO	00H	**The received undersize frame statistic (C5) from PHY chip by MAC** The undersize frame is referred to the Ethernet frame with less than 64 bytes. Note that in half-duplex mode, the receiving may not be completed caused by collision, thus the undersize packet formed in the condition will be discarded directly and not be counted.
31H	7-0	Eth_RxOversizePkt[7:0]	RO	00H	**The received oversize frame statistic (C5) from PHY chip by MAC** The oversize frame is referred to the Ethernet frame with more than 2031 bytes.
32H	7-0	Eth_RxCrcerrorPkt[7:0]	RO	00H	**The received CRC-E check error frame statistic (C5) from PHY chip by MAC** Not include oversize and undersize frame
33H	7-0	Eth_RxBroadcost[7:0]	RO	00H	**The received broadcast frame statistic (C5) from PHY chip by MAC** Not include CRC-E error frame
34H	7-0	Eth_RxMulticast[7:0]	RO	00H	**The received multicast frame statistic (C5) from PHY chip by MAC** Not include broadcast frame and CRC-E error frame
35H	7-0	Reserved	RO	00H	**Reserved**

36H	7-0	Eth_RxGoodPkt[15:8]	RO	00H	**The received correct frame number statistic (C5) from PHY chip by MAC** Not include oversize frame, undersize frame and CRC-E error frame
37H	7-0	Eth_RxGoodPkt[7:0]	RO	00H	
38H	7-0	Eth_RxGoodByte[15:8]	RO	00H	**The received correct byte statistic (C5) from PHY chip by MAC** Not include oversize frame, undersize frame and CRC-E error frame
3AH	7-0	Eth_RxGoodByte[7:0]	RO	00H	
3BH	7-0	Eth_RxAbandonPkt[15:8]	RO	00H	**The statistic of frame abandoned owing to insufficient buffer size when writing to SDRAM (C6)**
3CH	7-0	Eth_RxAbandonPkt[7:0]	RO	00H	
3DH	7-0	Eth_TxGoodByte[15:8]	RO	00H	**The received correct byte statistic (C3) from SDRAM by MAC** That is the statistic of the correct byte transmitted from MAC to PHY chip
3FH	7-0	Eth_TxGoodByte[7:0]	RO	00H	
40H	7-0	Eth_TxGoodPkt[15:8]	RO	00H	**The received correct frame statistic (C3) from SDRAM by MAC** That is the statistic of the correct frame transmitted from MAC to PHY chip
41H	7-0	Eth_TxGoodPkt[7:0]	RO	00H	
42H	7-0	Eth_TxPausePkt[7:0]	RO	00H	**The transmitted flow control frame statistic (C4) to PHY chip by MAC**
43H	7-0	Eth_TxBadPkt[7:0]	RO	00H	**The error frame statistic (C3) from SDRAM read by MAC**
44H	7-0	Eth_Collision[7:0]	RO	00H	**Ethernet collision statistic (C4) when MAC is transmitting packet to PHY**

45H	7-0	Eth_TxExcessiveCol[7:0]	RO	00H	**The statistic of frame abandoned owing to over 16 consecutive collisions when MAC is transmitting packet to PHY(C4)** Note that this register is valid only when it is half-duplex mode and Col16_discard_en =1.

5.5.2 Management Frame Register

When register page address is ’10’ in I^2C mode or register *cmd* is 03H or 07H in UART mode, the management frame register can be accessed.

Table 5-5-2-1 Management Frame Register(Page10)

Add	Bit	Name	R/W	Default	Description
Configuration register for Management frame transmitting					
03H	0	cGT_MngEn	RW	0	**Trigger to transmit management frame** 0->1= trigger to transmit the management frame once The register will not be back to ‘0’ automatically, it need to be written back to ‘0’ by MCU after doing the trigger operation every time.
04H	5-0	cGT_MngLen	RW	08H	**The length of payload of the transmitted management frame** The valid length of management frame is 1-59 byte
Status register for Management frame transmitting					

28H	0	sGT_MngEn	RO	0	**The transmitting module of Management frame busy** 1= The transmitting module is transmitting management frame, register cGT_MngEn, cGT_MngLen and OAM_Tx is forbidden to operate at that time; 0= The transmitting module is idle
Configuration register for Management frame receiving					
44H	0	cGR_mng_clr	RW	0	**Clear flag of buffer full for management frame receiving** 1= clear the buffer full flag(aGR_mng_get), When the buffer full flag *aGR_mng_get* is set as '0', the buffer will get ready to receive new management frame. Thus, MCU should clear the buffer full flag *aGR_mng_get* when finish to read out all the payload of received management frame.
Status register for Management frame receiving					
53H	5-0	sGR_MngLen	RW	08H	**The length of payload of the received management frame** The valid length of management frame is 1-59 byte
Alarm register for Management frame receiving					
54H	0	aGR_mng_get	RO	0	**Flag of buffer full for management frame receiving** 1= Receive one management frame, ask MCU for reading; 0= Indicate that the buffer for management receiving is empty When the buffer full flag *aGR_mng_get* is '1', the buffer will stop to receive new management frame.
Buffer register for Management frame					

80H-BAH	7-0	OAM_Tx	RW	00H	Buffer for the transmitted management frame payload Byte in 0x80 is the first transmitted byte
C0H-FAH	7-0	OAM_Rx	RO	00H	Buffer for the received management frame payload Byte in 0xC0 is the first received byte

5.5.3 Global Register

When register page address is '11' in I^2C mode or register *cmd* is 05H or 09H in UART mode, the management frame register can be accessed.

Table 5-5-3-1 Global Register(Page11)

Add	Bit	Name	R/W	Default	Description
00H	0	Reserved	RW	0	Reserved register for update settings of RC7222-A1, note that these three registers should keep the default value, otherwise the device may work abnormal.
01H	0	Reserved	RW	0	
02H	0	Reserved	RW	1	
03H	3	cTOAM_Oreder	RW	0	CRC-O format selection when transmitting management frame 0=CRC-O format comply with the standard of china mobile enterprise 1=CRC-O format comply with CRC-H format defined in RJ017 Refer to section ***4.6.1*** for more
	1	cROAM_Oreder	RW	0	CRC-O format selection when receiving management frame 0=CRC-O format comply with the standard of china mobile enterprise 1=CRC-O format comply with CRC-H format defined in RJ017 Refer to section ***4.6.1*** for more

04H	2	cPrbs_TEST	RW	0	**Enable BERT** 1= Enable BERT, insert the serial pseudo random sequence to the timeslots that were assigned for Ethernet and receive the bit sequence. 0=Disable BERT
	1	cLoop_extE1	RW	0	**Loopback to line at the loopback point of E1 interface** 1= loopback
	0	cLoop_interE1	RW	0	**Loopback to device at the loopback point of E1 interface** 1=loopback

6 Application

6.1 Ethernet Bridge System

The RC7222-A1, combined with a few peripheral circuits, can be used to implement an Ethernet remote bridge via the E1 link. Furthermore, it provides an ST_BUS interface, and can multiplex some services of 64Kbps (such as voice services) into the E1 frame for transportation.

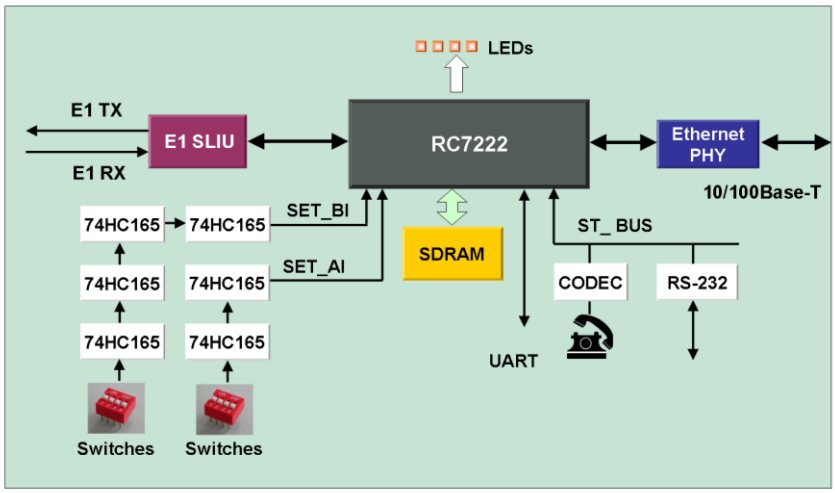

Fig. 6-1-1 Ethernet Bridge System Structure

6.2 Ethernet Optical Modem

The RC7222-A1 can map the Ethernet data into E1 frames and subsequently transfer them through optical lines. In this mode, the RC7222-A1 can be used to achieve an Ethernet optical modem. It can also integrate some 64Kbps services via the ST_BUS interface.

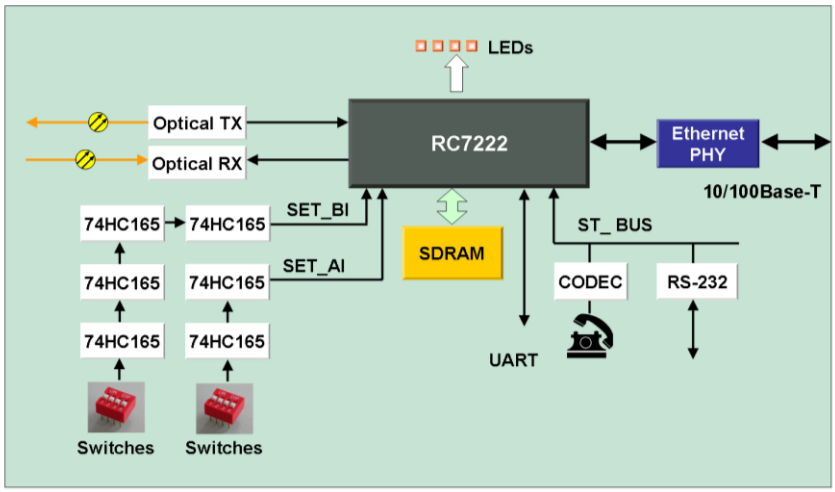

Fig. 6-2-1 Ethernet Optical Modem Structure

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Permanent device damage may occur if absolute maximum ratings are exceeded, hence the maximum ratings must never be exceeded for even an instant.

Table 7-1-1 Absolute Maximum Ratings (VSS = 0V)

Symbol	Item	Limits	Unit
HVDD	Power Supply Voltage	-0.3 to 4.0	V
LVDD		-0.3 to 3.0	V
Vi	Input Voltage	-0.3 to HVDD+0.5	V
Vo	Output Voltage	-0.3 to HVDD+0.5	V
Iout	Output Current /Pin	±30	mA
Tstg	Storage temperature	-65 to 150	ºC

7.2 Normal Operating Conditions

Table 7-2-1 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	HVDD	3.0	3.3	3.6	V
	LVDD	2.3	2.5	2.7	V
Input Voltage	Vi	Vss	---	HVDD	V
Ambient Temperature	Ta	0	25	70	ºC
Normal Input for Rising Time	Tri	---	---	50	ns

Normal Input for Falling Time	tiff	---	---	50	ns
Schmitt Input for Rising Time	tri	---	---	5	ms
Schmitt Input for Falling Time	tfi	---	---	5	ms

7.2.1 Power Consumption

Generally, the power consumption for 3.3V is 100mW; and the power consumption for 2.5V is 220mW.

7.3 DC Characteristics

Table 7-3-1 DC Characteristics（HVDD=3.3VDC±0.3V，VSS=0V，Tj=-40°C～85°C）

Symbol	Item	Conditions	Min	Typ.	Max	Unit
Idds	Quiescent Current	Quiescent conditions （Tj=85°C）	---	---	21	uA
ILi	Input Leakage Current	---	-5	---	5	uA
Ioz	Off state leakage Current	---	-5	---	5	uA
Voh	High Level Output Voltage	Ioh= -6mA HVDD=Min	HVDD -0.4	---	---	V
Vol	Low Level Output Voltage	Ioh= 6mA HVDD=Min	---	---	0.4	V
Vih	High Level Input Voltage	LVTTL Level HVDD=max	2.2	---	---	V
Vil	Low Level Input Voltage	LVTTL Level HVDD=Max	---	---	0.8	V
Vt2+	Positive Trigger Voltage	LVTTL Schmitt	1.1	---	2.4	V
Vt2-	Negative Trigger Voltage	LVTTL Schmitt	0.6	---	1.8	V
Vh2	Hysteretic Trigger Voltage	LVTTL Schmitt	0.1	---	---	V
Ci	Input Terminal	f=1MHz，HVDD=0V	---	---	8	pF

	Capacitance					
Co	Output Terminal Capacitance	f=1MHz，HVDD=0V	---	---	8	pF
Cio	Input/Output Terminal Capacitance	f=1MHz，HVDD=0V	---	---	8	pF

7.4 AC Characteristic

7.4.1 MII Interface Timing

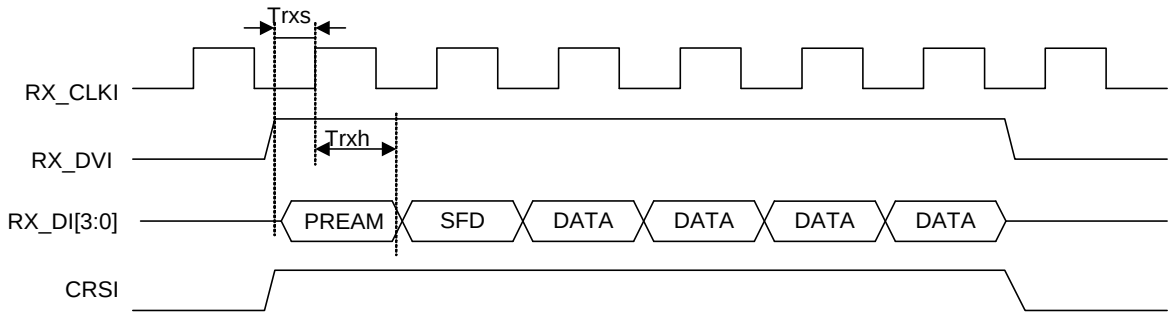

Fig. 7-4-1-1 MII Receive Timing

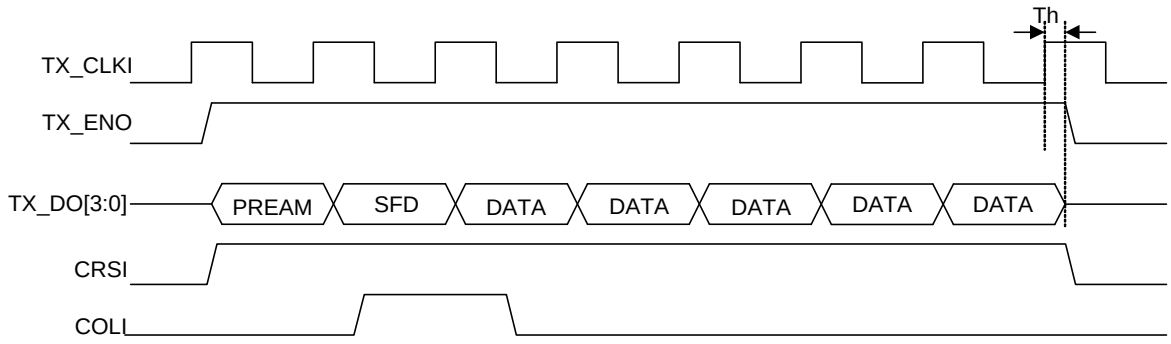

Fig. 7-4-1-2 MII Transmit Timing

Table 7-4-1-1 Timing Specifications of MII Interface

Symbol	Descriptions	Min.	Type.	Max.

Trxs	Setup to RX_CLKI rising edge	3ns		-
Trxh	Hold after RX_CLKI rising edge	3ns		-
Th	TX_CLKI rising edge to output	3ns		10ns

7.4.2 SDRAM Interface Timing

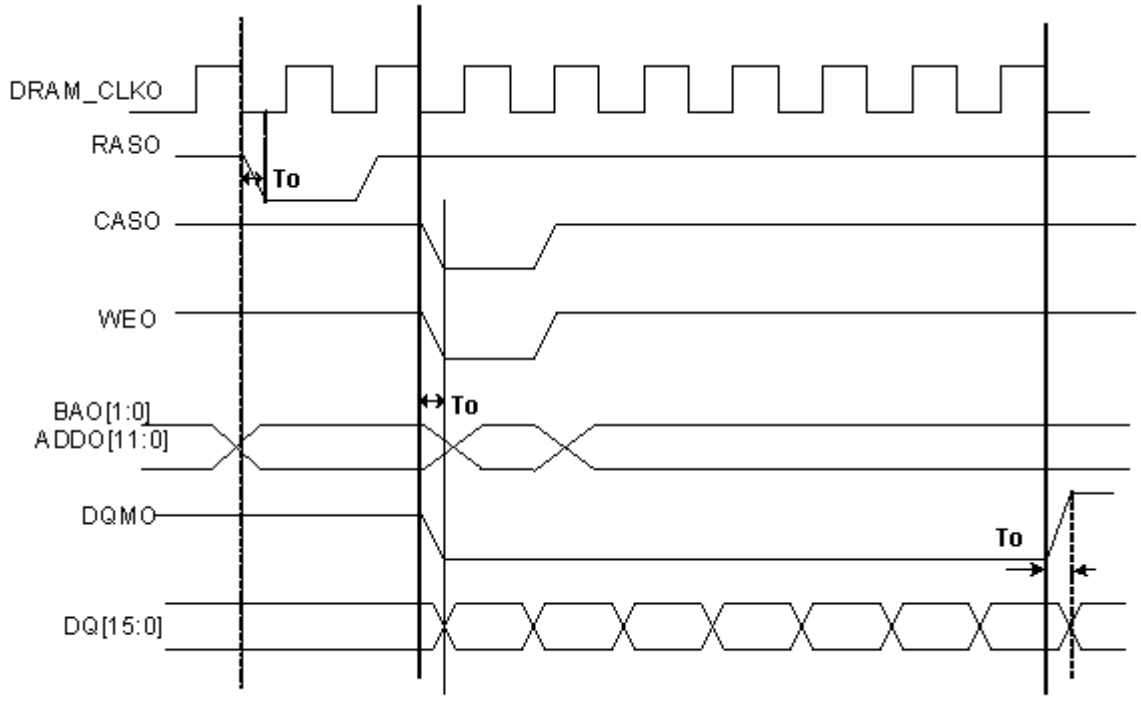

Fig. 7-4-2-1 SDRAM interface timing for write

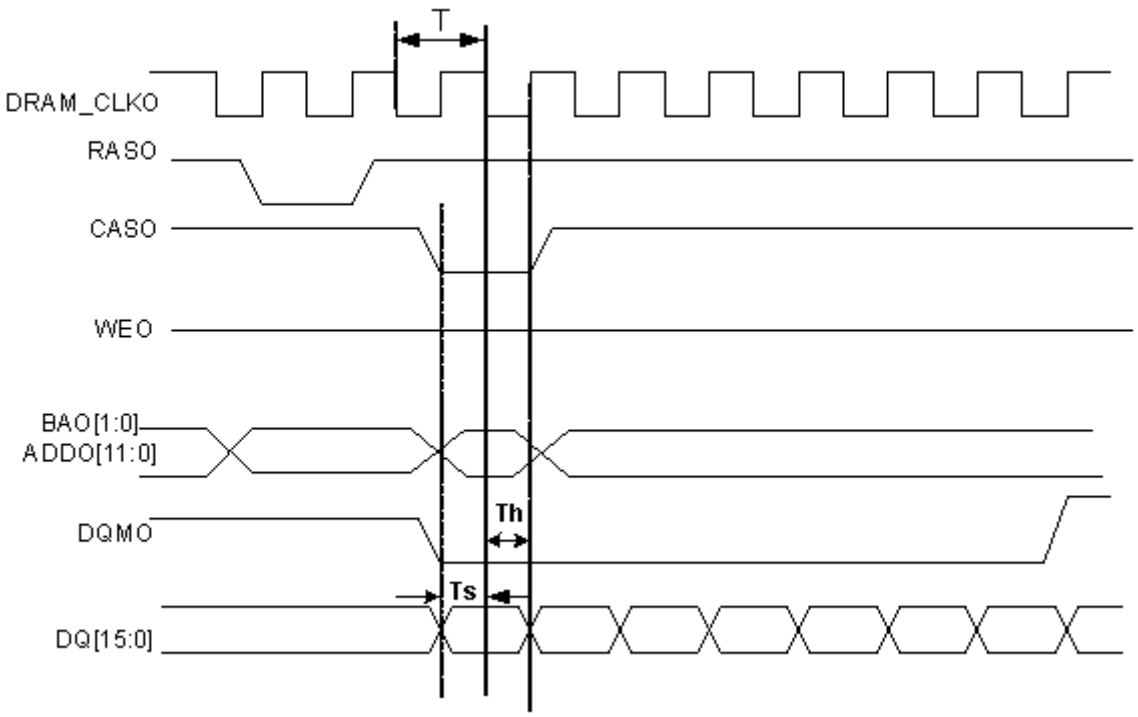

Fig. 7-4-2-2 SDRAM interface timing for read

Table 7-4-2-1 Timing Specifications of SDARM Interface

Symbol	Descriptions	Min.	Type.	Max.
T	Clock period of DRAM_CLKO		2×Tclk65i	
To	DRAM_CLKO falling edge to output	0		3ns
Ts	Setup to DRAM_CLKO falling edge	3ns		
Th	Hold after DRAM_CLKO falling edge	0		

7.4.3 ST_BUS Interface Timing

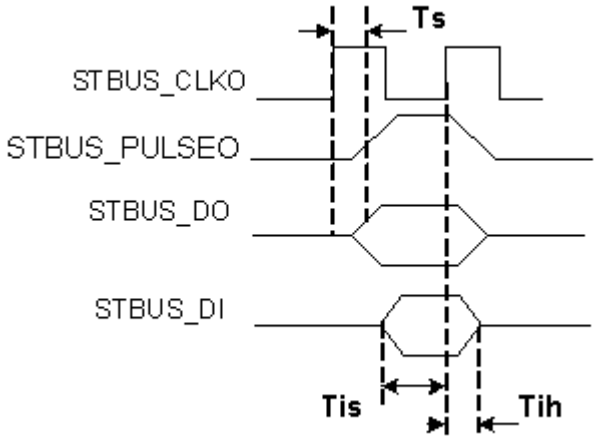

Fig. 7-4-3-1 ST_BUS Interface Timing

Table 7-4-3-1 Timing specification of ST_BUS Interface

Symbol	Descriptions	Min.	Type.	Max.
Ts	STBUS_CLKO rising edge to output	15ns		20ns
Tis	Setup to STBUS_CLKO rising edge	3ns		-
Tih	Hold after STBUS_CLKO rising edge	3ns		-

7.4.4 Serial Configuration Interface Timing

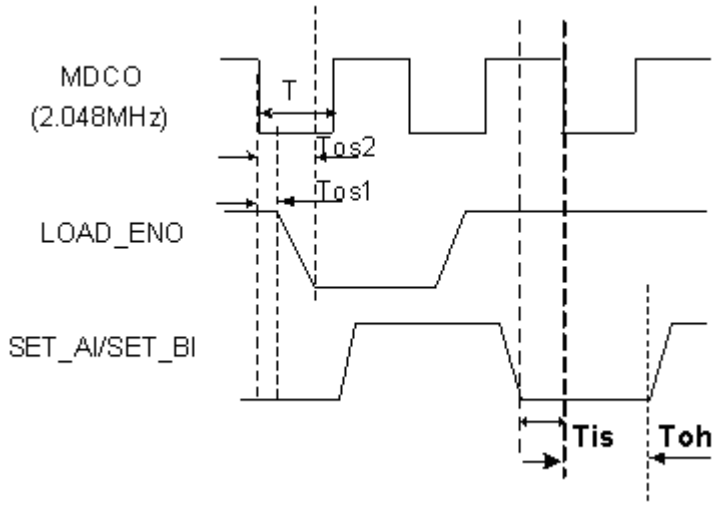

Fig. 7-4-4-1 Serial Configuration Interface Timing

Table 7-4-4-1 Timing specification of Serial configuration interface

Symbol	Descriptions	Min.	Type.	Max.
Tos1	MDCO falling edge to output (min)	60ns		
Tos2	MDCO falling edge to output (max)			80ns
Tis	Setup to MDCO falling edge	0		
Tih	Hold after MDCO falling edge	60ns		

8 Package Information

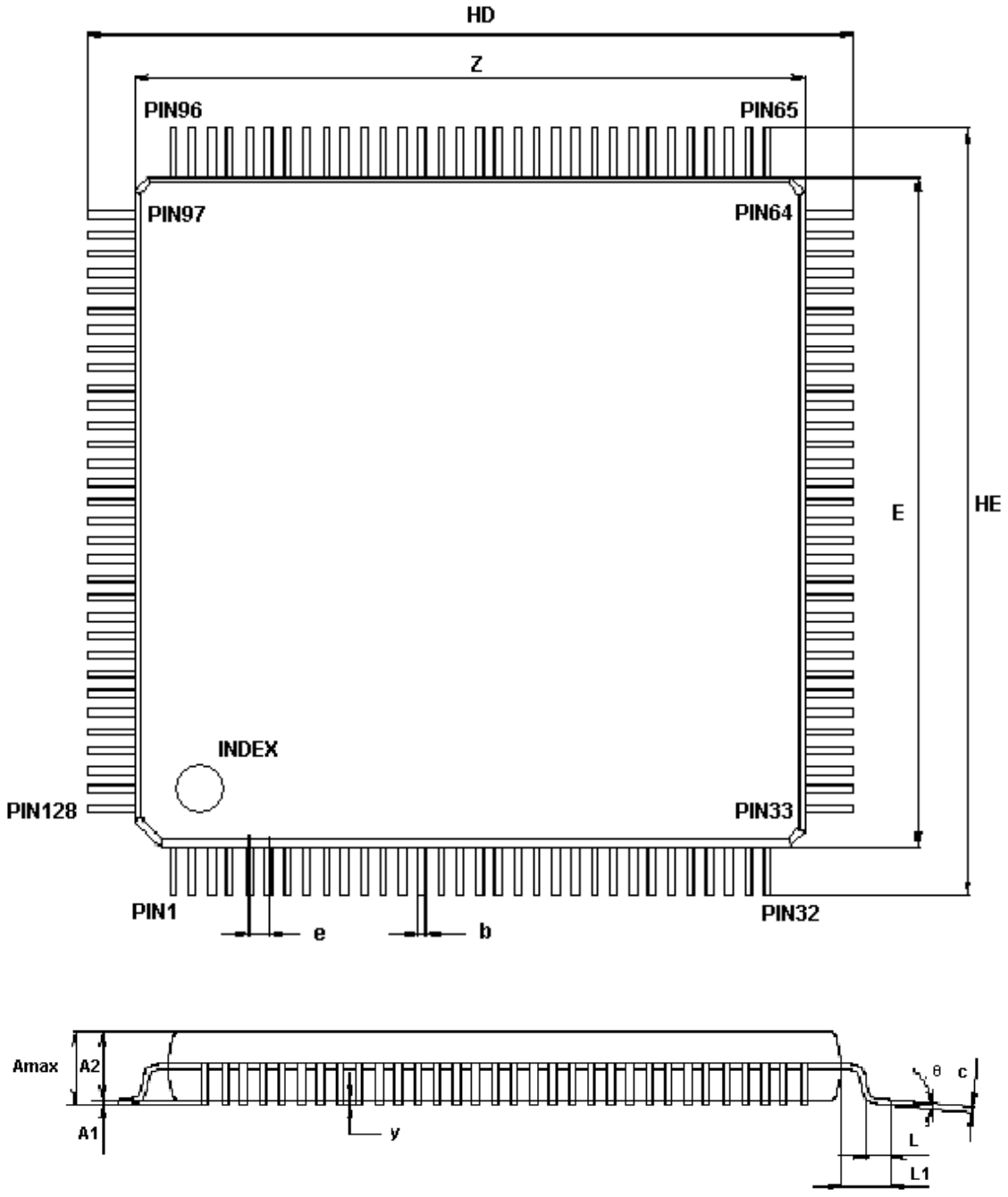

Fig. 8-1 RC7222-A1 Package

Table 8-1 Package Dimension

Symbol	Dimension in Millimeter (mm)

	Min.	Nom.	Max.
E		14	
Z		14	
Amax			1.7
A1		0.1	
A2		1.4	
e		0.4	
b	0.13		0.23
c	0.09		0.2
θ	0°		10°
L	0.3		0.75
L1		1	
HE		16	
HD		16	
y			0.08