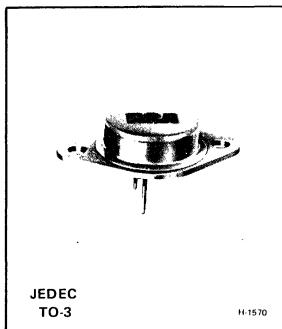




# Power Transistors

**RCA423**



JEDEC  
TO-3

H-1570

## High-Voltage, High-Power Silicon N-P-N Power Transistor

For Switching and Linear Applications in  
Military, Industrial, and Commercial Equipment

### Features:

- Maximum safe-area-of-operation curves
- Low saturation voltage:  $V_{CE}(\text{sat}) = 0.8 \text{ V}$  (max.)
- High voltage rating:  $V_{CEO}(\text{sus}) = 325 \text{ V}$
- High dissipation rating:  $P_T = 125 \text{ W}$

RCA-423 is an epitaxial silicon n-p-n power transistor utilizing a multiple-emitter-site structure. This device employs the popular JEDEC TO-3 package.

Featuring high breakdown-voltage ratings and low saturation-

voltage values, the 'RCA-423' is especially suitable for use in inverters, deflection circuits, switching regulators, high-voltage bridge amplifiers, ignition circuits, and other high-voltage switching applications.

### MAXIMUM RATINGS, *Absolute-Maximum Values*:

COLLECTOR-TO-BASE VOLTAGE, $V_{CBO}$ .....	400 V
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### COLLECTOR-TO-EMITTER

#### SUSTAINING VOLTAGE:

With base open,  $V_{CEO}(\text{sus})$  ..... 325 V

### COLLECTOR-TO-EMITTER

#### BREAKDOWN VOLTAGE:

With base open,  $V_{(BR)}\text{CEO}$  ..... 400 V

### EMITTER-TO-BASE

VOLTAGE,  $V_{EBO}$  ..... 5 V

### COLLECTOR CURRENT:

Continuous,  $I_C$  ..... 7 A

Peak ..... 10 A

BASE CURRENT (Continuous),  $I_B$  ..... 2 A

### TRANSISTOR DISSIPATION, $P_T$ :

At case temperatures up to  $25^\circ\text{C}$   
and  $V_{CE}$  up to 75 V ..... 125 W

At case temperatures up to  $25^\circ\text{C}$   
and  $V_{CE}$  above 75 V ..... See Fig. 2.

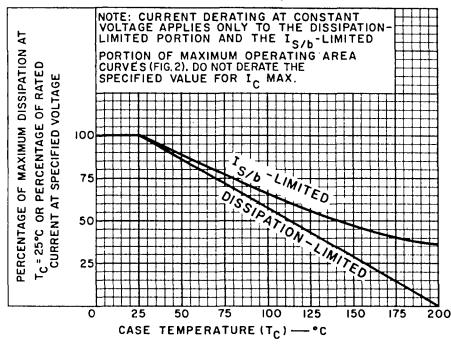
At case temperatures above  $25^\circ\text{C}$   
and  $V_{CE}$  above 75 V ..... See Figs. 1 & 2.

### TEMPERATURE RANGE:

Storage & Operating (Junction) .....  $-65$  to  $+200^\circ\text{C}$

### PIN TEMPERATURE (During Soldering):

At distances  $\geq 1/32$  in. (0.8 mm)  
from case for 10 s max. .....  $230^\circ\text{C}$



92CS-19296

Fig.1—Dissipation and current derating curves.

ELECTRICAL CHARACTERISTICS, Case Temperature ( $T_C$ ) = 25°C Unless Otherwise Specified

Characteristic	Symbol	Test Conditions				Limits			Units	
		DC Voltage (V)		DC Current (A)						
		$V_{CE}$	$V_{BE}$	$I_C$	$I_B$	Min.	Typ.	Max.		
Collector-Cutoff Current: With base open	$I_{CEO}$	400				—	—	0.25	mA	
With base-emitter junction reverse-biased	$I_{CEV}$	400	-1.5			—	—	0.25		
With base-emitter junction reverse-biased & $T_C = 125^\circ\text{C}$	$I_{CEV}$		-1.5			—	—	0.5		
Emitter-Cutoff Current	$I_{EBO}$		-5			—	—	5.0	mA	
DC Forward-Current Transfer Ratio	$h_{FE}$	5 5		1.0 <sup>a</sup> 2.5 <sup>a</sup>		30 10	— —	90 —		
Collector-to-Emitter Sustaining Voltage: With base open (See Figs. 3 & 4.)	$V_{CEO}(\text{sus})$			0.1		325 <sup>b</sup>	—	—	V	
Base-to-Emitter Saturation Voltage	$V_{BE}(\text{sat})$			1.0 <sup>a</sup>	0.1	—	0.9	1.5	V	
Collector-to-Emitter Saturation Voltage	$V_{CE}(\text{sat})$			1.0 <sup>a</sup>	0.1	—	0.2	0.8	V	
Second-Breakdown Collector Current: (With base forward-biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}^c$	150				0.3	—	—	A	
Gain-Bandwidth Product	$f_T$	10		0.2		—	4.0	—	MHz	
Switching Time: $(I_{B1} = 0.1 \text{ A}, I_{B2} = -0.5 \text{ A})$									$\mu\text{s}$	
Rise (See Figs. 10, 12, & 13.)	$t_r$			1.0		—	0.35	—		
Storage (See Figs. 11, 12, & 13.)	$t_s$			1.0		—	1.4	—		
Fall (See Figs. 9, 12, & 13.)	$t_f$			1.0		—	0.15	—		
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	10		5		—	—	1.4	$^\circ\text{C/W}$	

<sup>a</sup> Pulsed; pulse duration  $\leq 350 \mu\text{s}$ , duty factor = 2%.

<sup>b</sup> CAUTION: The sustaining voltage  $V_{CEO}(\text{sus})$  MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

<sup>c</sup>  $I_{S/b}$  is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

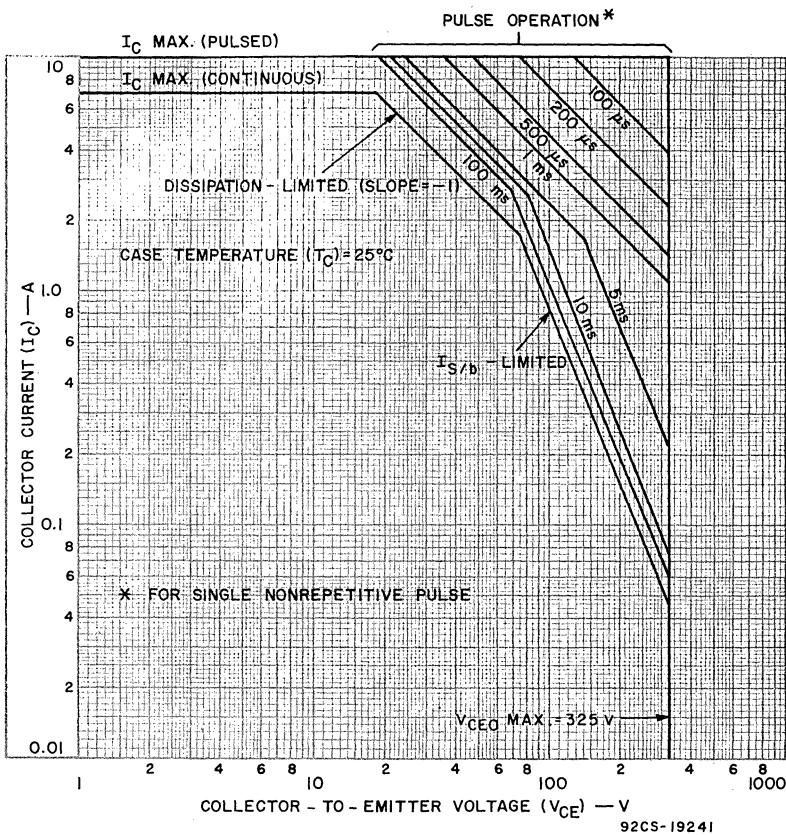


Fig.2—Maximum operating areas.

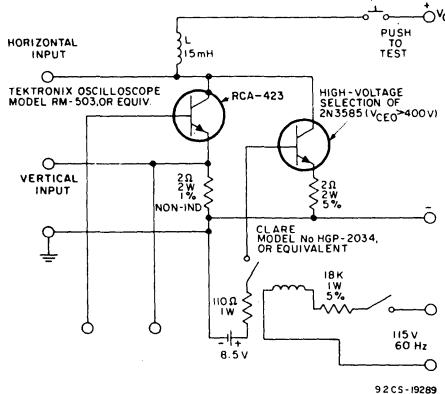
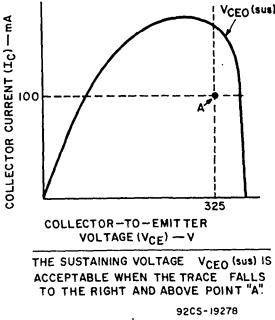
Fig.3—Circuit used to measure sustaining voltage,  $V_{CEO}(\text{sus})$ .

Fig.4—Oscilloscope display for measurement of sustaining voltage (test circuit shown in Fig.3).

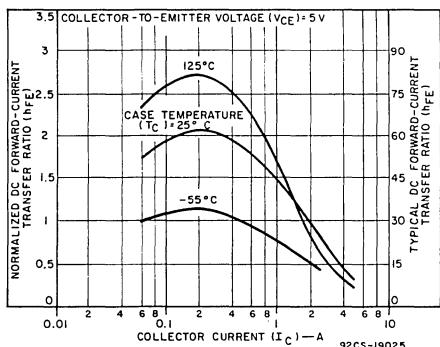


Fig.5—Typical dc beta characteristics.

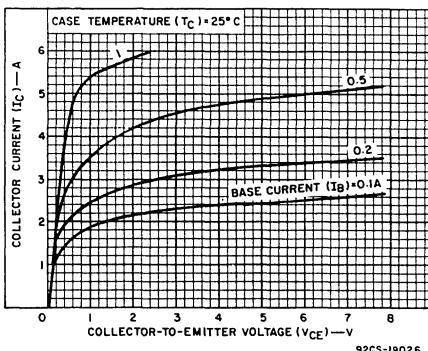


Fig.6—Typical output characteristics.

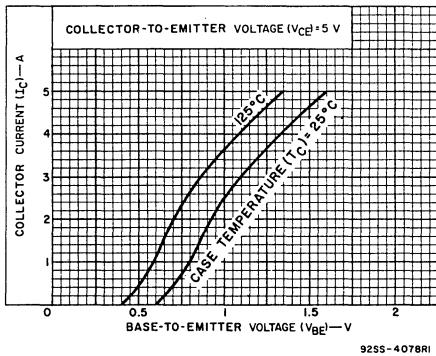


Fig.7—Typical transfer characteristics.

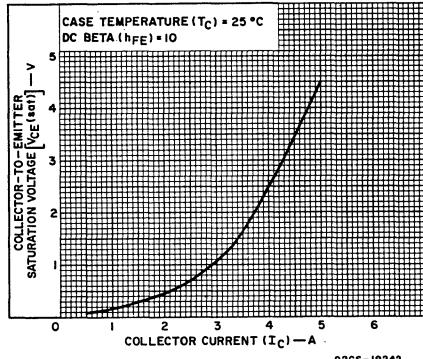


Fig.8—Typical saturation voltage characteristic.

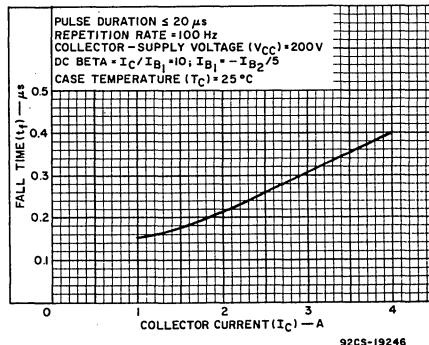


Fig.9—Typical fall time vs. collector current.

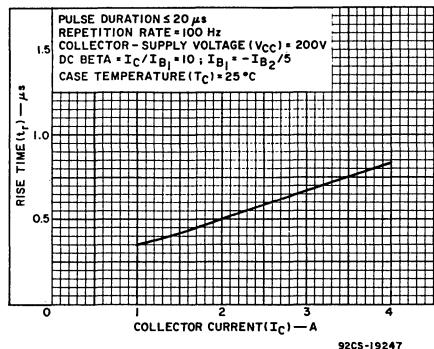


Fig.10—Typical rise time vs. collector current.

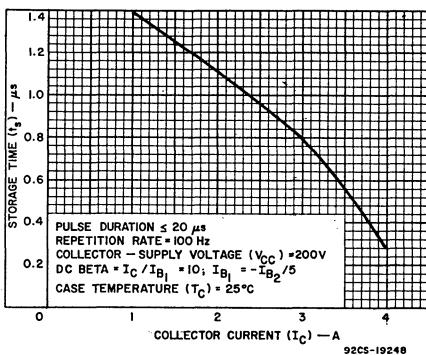


Fig.11—Typical storage time vs. collector current.

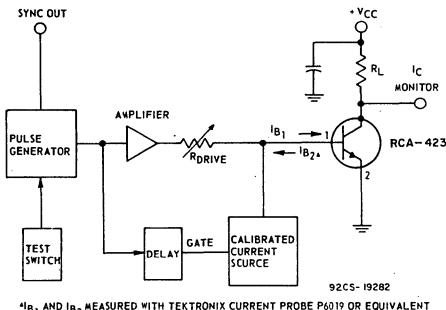


Fig.12—Circuit used to measure switching times.

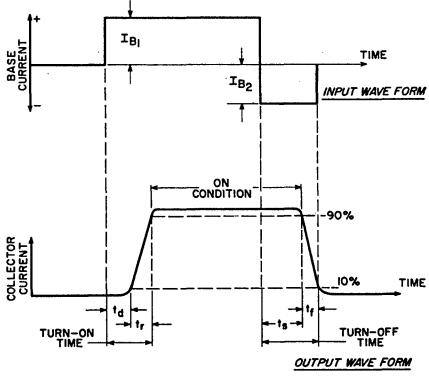


Fig.13—Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig.12).

## TERMINAL CONNECTIONS

Pin 1 — Base

Pin 2 — Emitter

Mounting Flange, Case — Collector