Description

RailClamps® are ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients).

The RClamp™0524J has a typical capacitance of only 0.30pF between I/O pins. This allows it to be used on circuits operating in excess of 3GHz without signal attenuation. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge). Each device is designed to protect four lines (two differential pairs).

The RClamp0524J is in a 8-pin, RoHS/WEEE compliant, SLP2710P8 package. It measures 2.7 x 1.0 x 0.58mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free NiPdAu. They are designed for easy PCB layout by allowing the traces to run straight through the device. The combination of small size, low capacitance, and high level of ESD protection makes them a flexible solution for applications such as HDMI, DisplayPort™, MDDI, and eSATA interfaces.

Features

- ESD protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-5 (Lightning) 5A (8/20µs)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Package design optimized for high speed lines
- Flow-Through design
- Protects four I/O lines
- Low capacitance: **0.3pF** typical (I/O to I/O)
- Low clamping voltage
- Low operating voltage: 5V
- Solid-state silicon-avalanche technology

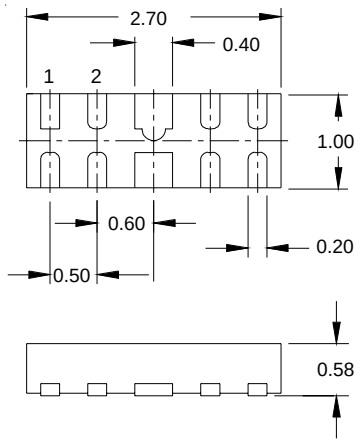
Mechanical Characteristics

- SLP2710P8 8-pin package (2.7 x 1.0 x 0.58mm)
- RoHS/WEEE Compliant
- Lead Pitch: 0.5mm
- Lead finish: NiPdAu
- Marking: Marking Code
- Packaging: Tape and Reel per EIA 481

Applications

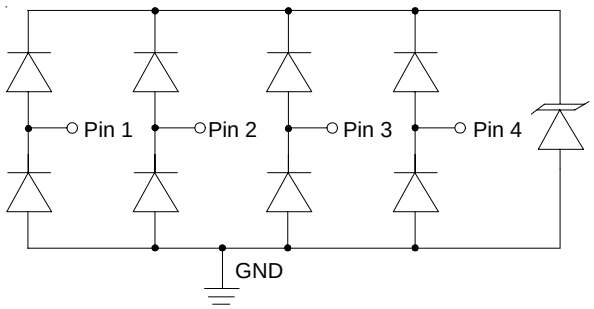
- High Definition Multi-Media Interface (HDMI)
- Digital Visual Interface (DVI)
- DisplayPort™ Interface
- MDDI Ports
- LVDS
- Serial ATA
- PCI Express

Dimensions



Nominal Dimensions in mm

Circuit Diagram



4-Line Protection

Absolute Maximum Rating

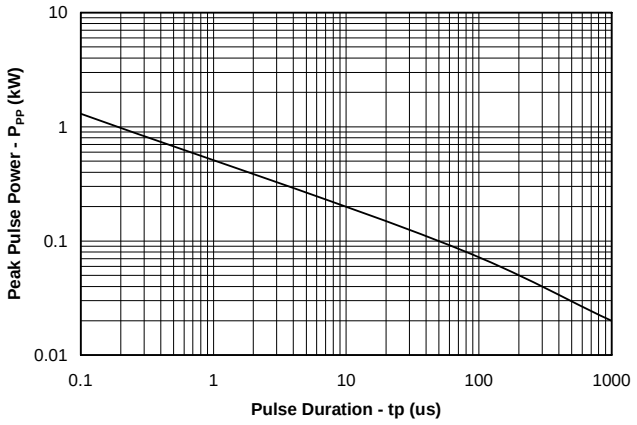
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	150	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 17 +/- 12	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

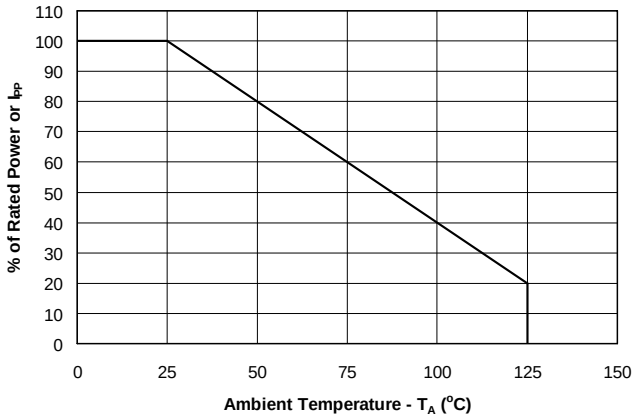
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to ground			5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Any I/O pin to ground	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C Any I/O pin to ground			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs Any I/O pin to ground			15	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Between I/O pins		0.30	0.4	pF
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Any I/O pin to ground			0.8	pF

Typical Characteristics

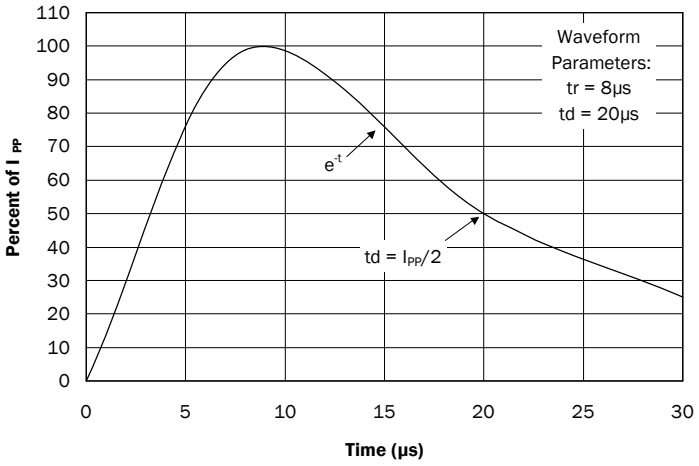
Non-Repetitive Peak Pulse Power vs. Pulse Time



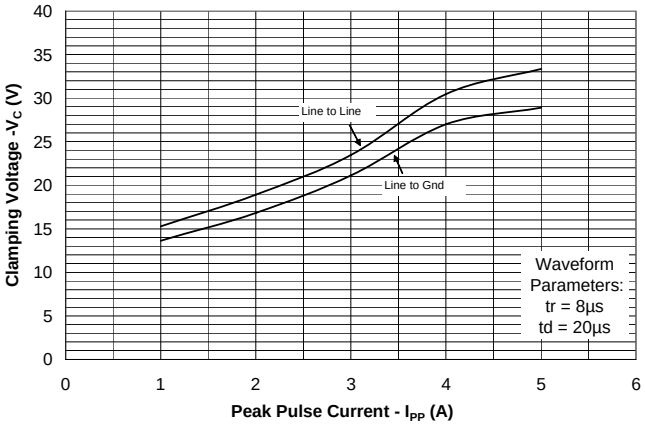
Power Derating Curve



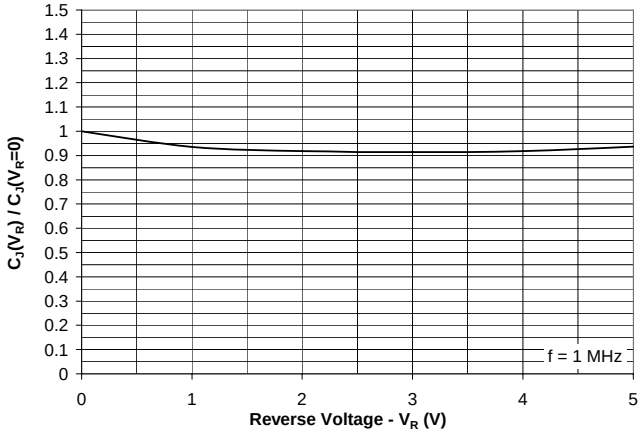
Pulse Waveform



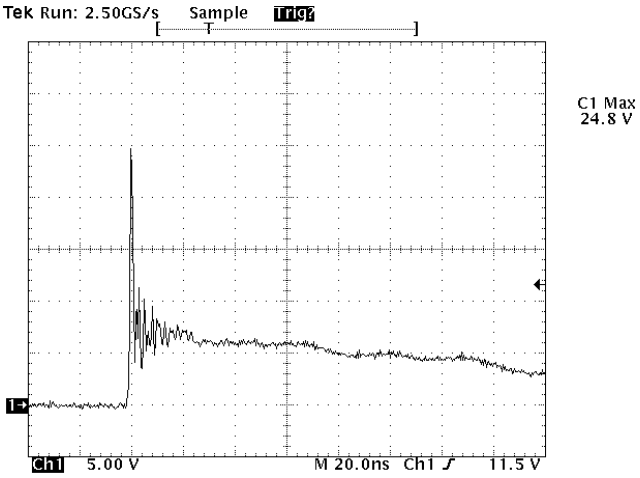
Clamping Voltage vs. Peak Pulse Current



Normalized Capacitance vs. Reverse Voltage

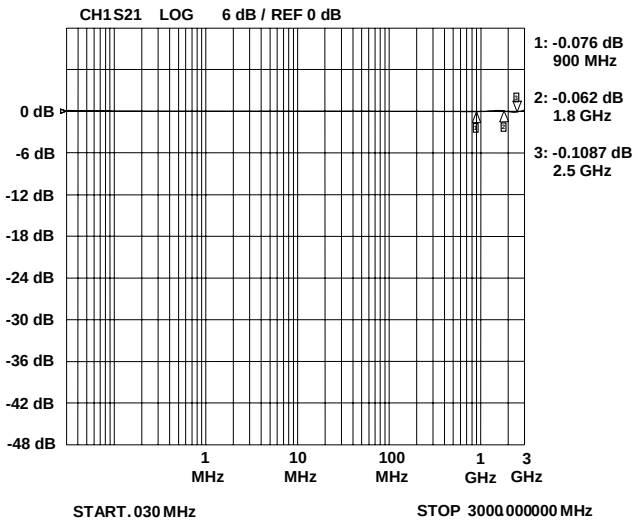


ESD Clamping for +8kV pulse per IEC 61000-4-2

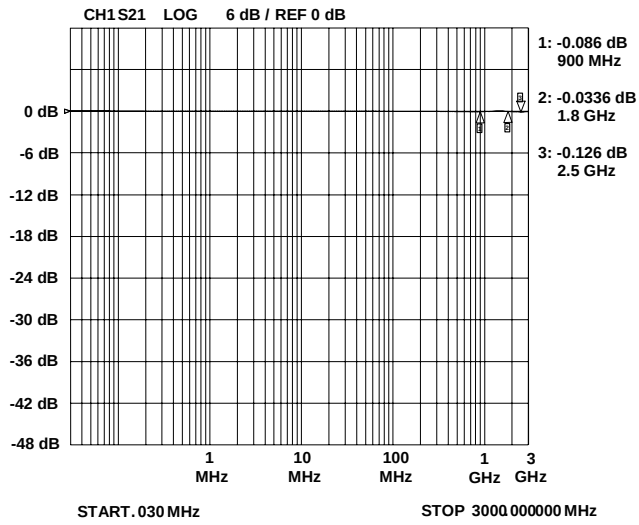


Typical Characteristics (Con't)

Insertion Loss S21 - I/O to I/O



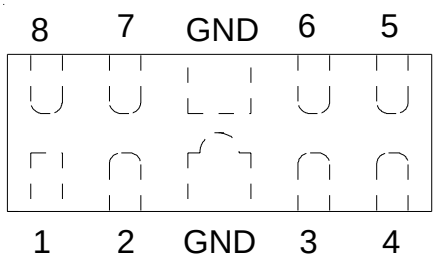
Insertion Loss S21 - I/O to GND



Applications Information

Design Recommendations for HDMI Protection

Adding external ESD protection to HDMI ports can be challenging. First ESD protection devices have an inherent junction capacitance. However, adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The RClamp0524J is specifically designed for protection of high-speed interfaces such as HDMI. They present <0.3pF capacitance between the pairs while being rated to handle >±8kV ESD contact discharges (>±15kV air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless SLP package that is less than 1.1mm wide. They are designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes even more critical as signal speeds increase.



Pin	Identification
1, 2, 3, 4	Input Lines
5, 6, 7, 8	Output Lines (No Internal Connection)
GND	Ground

SLP2710P8 Pin Configuration (Top View)

Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the RClamp0524J. The solid line represents the PCB trace. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 8, pin 2 to pin 7, pin 3 to pin 6, pin 4 to pin 5). For example, line 1 enters at pin 1 and exits at Pin 8 and the PCB trace connects pin 1 and 8 together. This is true for lines connected at pins 2, 3, and 4 also. Ground is connected at the center tabs. One large ground pad should be used in lieu of two separate pads.

TDR Measurements for HDMI

The combination of low capacitance, small package, and flow-through design means it is possible to use these devices to meet the HDMI impedance requirements of 100 Ohm ±15% without any PCB board modification. Figures 3 and 4 show impedance test results for a TDR risetime of 200ps and 100ps respectively, using a Semtech evaluation board with 100 Ohm traces through-out. Measurements were taken using a TDR method as outlined in the HDMI Compliance Test Specification (CTS). In each case, the device meets the HDMI CTS

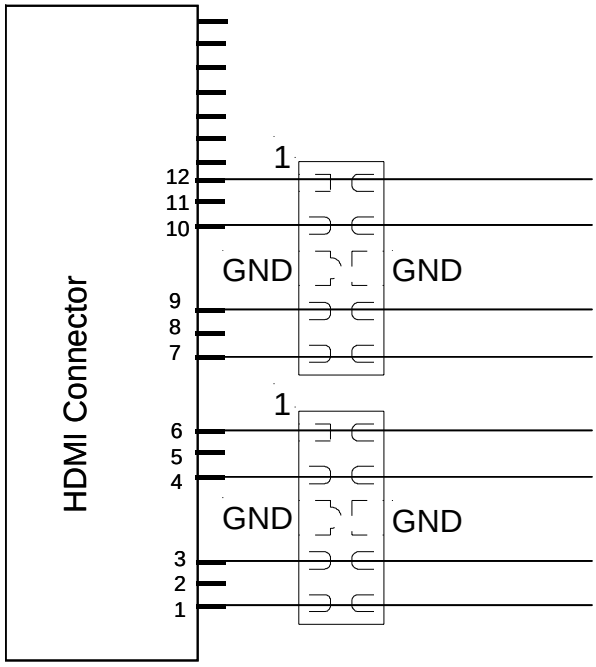


Figure 1. Flow through Layout Using RClamp0524J

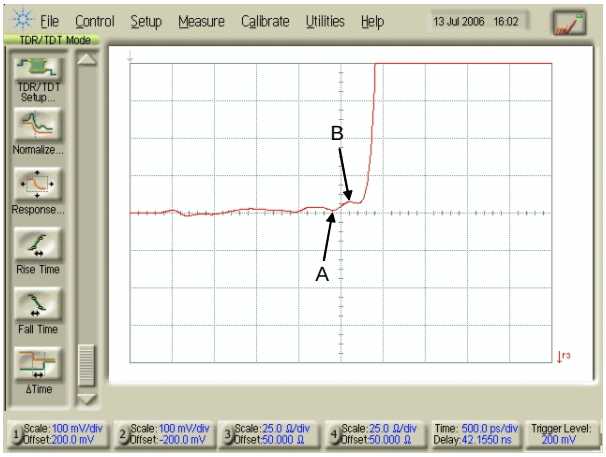
Applications Information

requirement of 100 Ohm ±15% with plenty of margin. For signal integrity purposes, the best results will be obtained by using the RClamp0524J to protect the high-speed differential pairs. This is because the device is designed such that the data lines from the connector line up with the I/O pins of the device without altering the trace routing. Either the RClamp0504P or RClamp0524J may be used to protect the remaining lines (I^2C, CEC, and hot plug) depending on layout constraints.

Layout Guidelines for Optimum ESD Protection

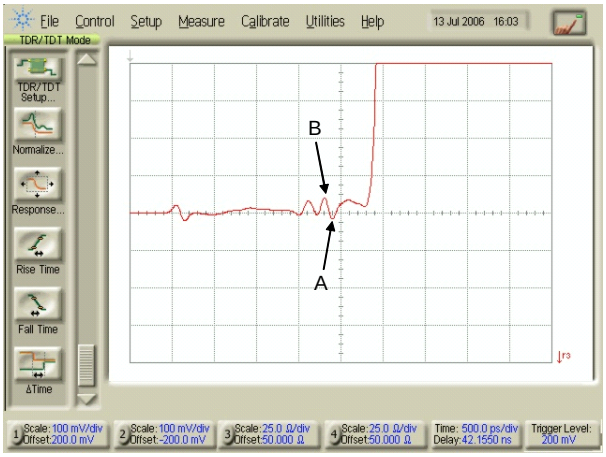
Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible. This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible. Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.



	A	B	
X-axis	1.905	2.081	**(nsec)**
Y-axis	101.0	107.0	**(Ohm)**

Figure 2 - TDR Measurement with 200ps risetime using Semtech Evaluation Board



	A	B	
X-axis	1.80	2.076	**(nsec)**
Y-axis	96	108.0	**(Ohm)**

Figure 3 - TDR Measurement with 100ps risetime using Semtech Evaluation Board

Note: Measurements were taken on SLP HDMI EVAL Rev C Board that has 100Ω differential traces impedance throughout (No trace Compensation).

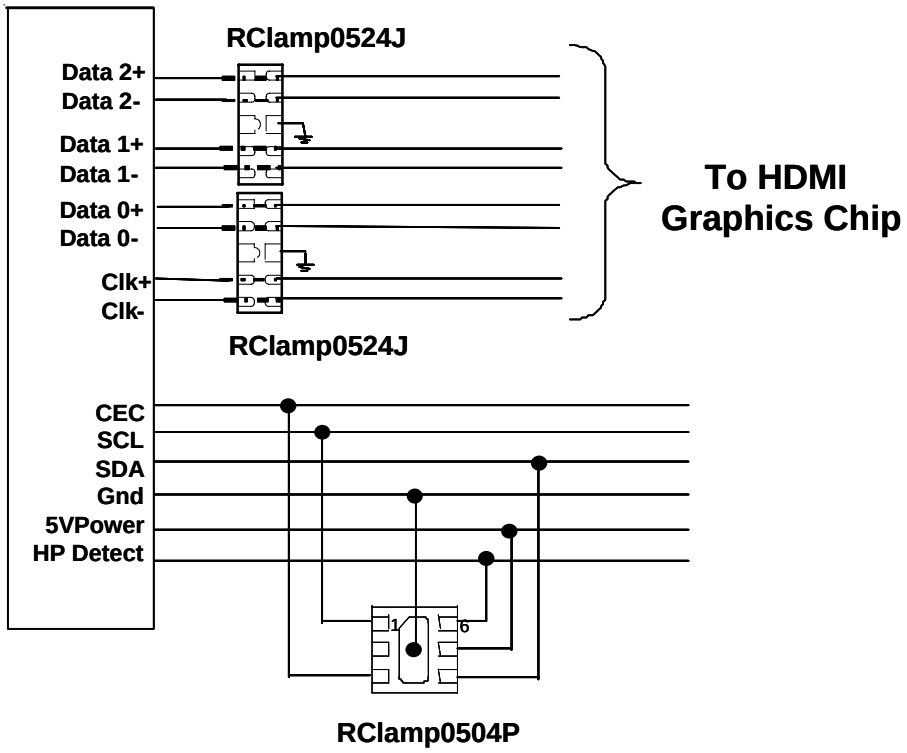


Figure 4. HDMI Protection Example

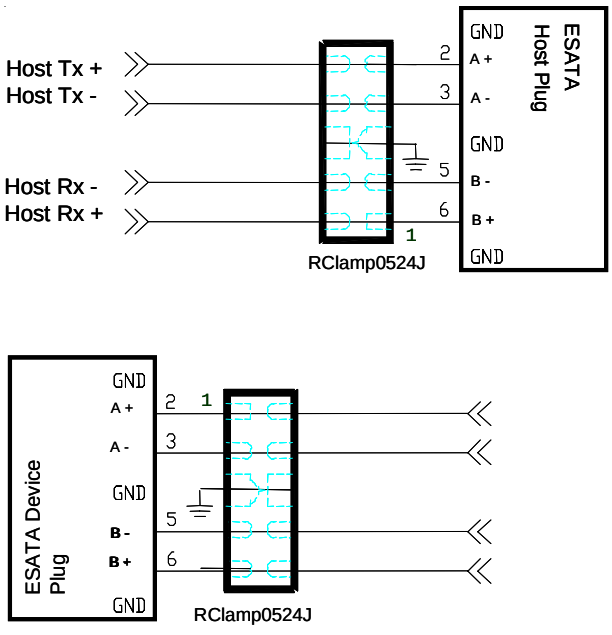


Figure 5. eSATA Protection Example

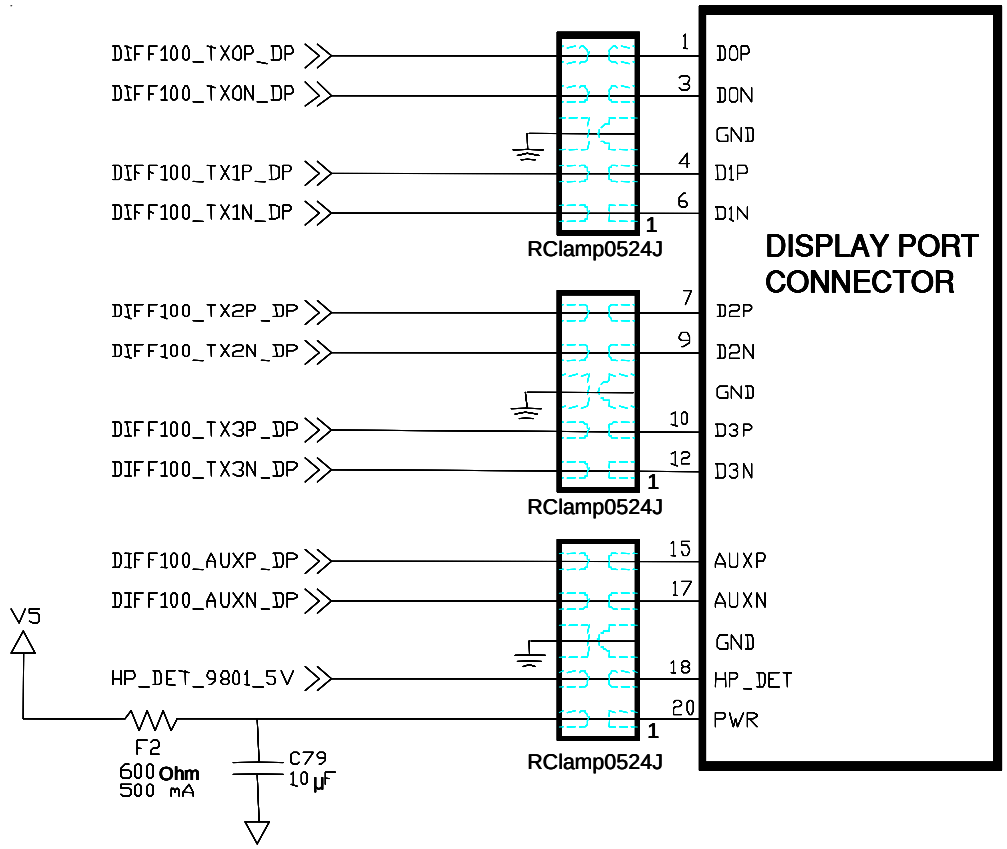
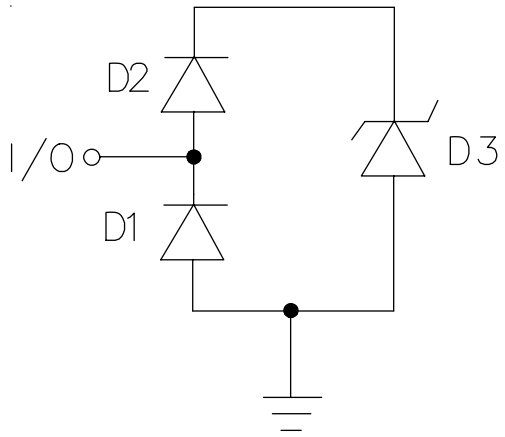


Figure 6. DisplayPort Protection Example

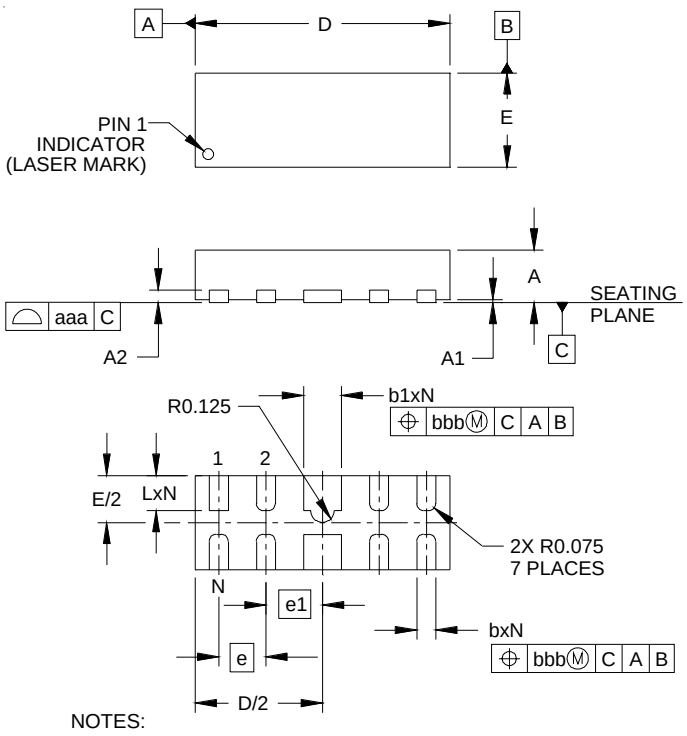
Applications Information *Spice Model*



RClamp0524J Spice Model

RClamp0524J Spice Parameters				
Parameter	**Unit**	**D1 (LCRD)**	**D2 (LCRD)**	**D3 (TVS)**
IS	Amp	1E-20	1E-20	2E-12
BV	Volt	100	100	9.36
VJ	Volt	0.7	0.7	0.6
RS	Ohm	0.458	1.0	2.6
IBV	Amp	1E-3	1E-3	1E-3
CJO	Farad	0.4E-12	0.6E-12	56E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.23
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

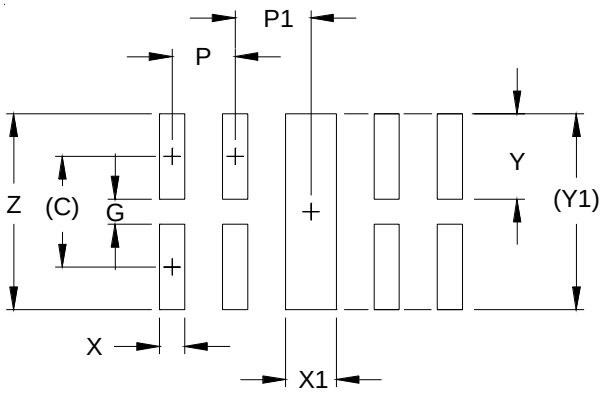
Outline Drawing - SLP2710P8



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	.023	.026	0.50	0.58	0.65
A1	0.00	.001	.002	0.00	0.03	0.05
A2		(.005)			(0.13)	
b	.006	.008	.010	0.15	0.20	0.25
b1	.014	.016	.018	0.35	0.40	0.45
D	.102	.106	.110	2.60	2.70	2.80
E	.035	.039	.043	0.90	1.00	1.10
e	.020 BSC			0.50 BSC		
e1	.024 BSC			0.60 BSC		
L	.012	.015	.017	0.30	0.38	0.425
N	10			10		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SLP2710P8

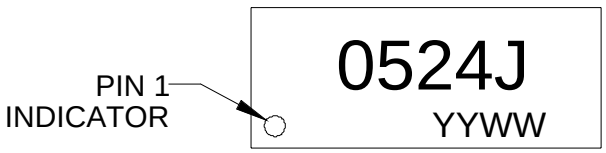


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.034)	(0.875)
G	.008	0.20
P	.020	0.50
P1	.024	0.60
X	.008	0.20
X1	.016	0.40
Y	.027	0.675
Y1	(.061)	(1.55)
Z	.061	1.55

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

PROTECTION PRODUCTS

Marking Codes



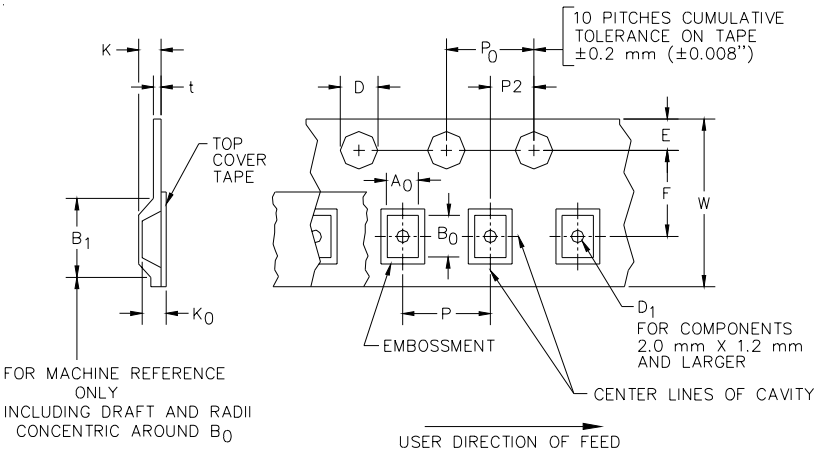
YYWW = Date Code

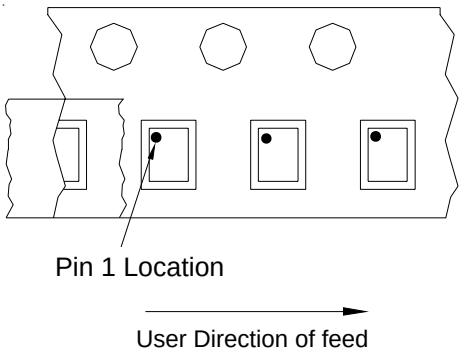
Ordering Information

Part Number	Number of Lines	Qty per Reel	Reel Size
RClamp0524J.TCT	4	3000	7 Inch

Note: Lead finish is lead-free NiPdAu.

Tape and Reel Specification





Device Orientation in Tape

Part Number	A0	B0	K0
RClamp0524J	1.21 +/-0.10 mm	2.91 +/-0.10 mm	0.66 +/-0.10 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm	1.5 + 0.1 mm - 0.0 mm)	0.5 mm ±0.05	1.750±.10 mm	3.5±0.05 mm	2.4 mm	4.0±0.1 mm	4.0±0.1 mm	2.0±0.05 mm	0.4 mm	8.0 mm + 0.3 mm - 0.1 mm

Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804