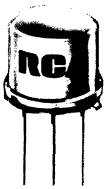
RCA
Solid State
Division

Power Transistors

RCS882



JEDEC TO-39

H-1381

High-Voltage Silicon P-N-P Transistor

For High-Speed Switching and Linear-Amplifier Applications in Industrial and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves**
- **High voltage ratings:**
  V_{CEO}(sus) = −300 V max.

The RCA-RCS882 is an epitaxial silicon p-n-p transistor with high breakdown voltages, high frequency response, and fast switching speeds. This device is provided in the JEDEC TO-39 hermetic package.

Typical applications include high-voltage differential and operational amplifiers; high-voltage inverters; and high-voltage, low-current switching and series regulators.

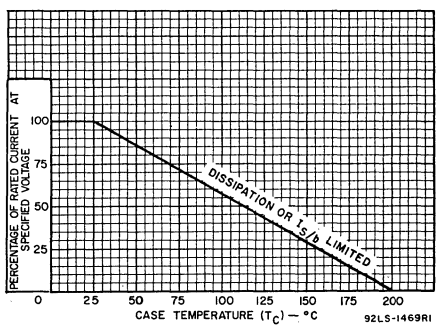


Fig. 1 — Dissipation derating curve.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	−350	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
With external base-to-emitter resistance (R_{BE}) = 50 Ω	V_{CER}(sus)	−350	V
With base open	V_{CEO}(sus)	−300	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	−6	V
COLLECTOR CURRENT	I_C	−1	A
BASE CURRENT	I_B	−0.5	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		7.5	W
At case temperatures above 25°C		See Figs. 1 and 4	
At ambient temperatures up to 50°C		0.75	W
At ambient temperatures above 50°C — Derate linearly at		5	mW/°C
TEMPERATURE RANGE;			
Storage and Operating (Junction)		−65 to +200	°C
LEAD TEMPERATURE (During soldering):			
At distance ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		255	°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		VOLTAGE V dc			CURRENT mA dc		RCS882		
		V_{CB}	V_{CE}	V_{BE}	I_C	I_B	Min.	Max.	
Collector-Cutoff Current:									
With emitter open	I_{CBO}	−280					–	−50	
With base open	I_{CEO}		−250			0	–	−50	μA
With base-emitter junction reverse-biased	I_{CEV}		−300	1.5			–	−50	
Emitter-Cutoff Current	I_{EBO}			6	0		–	−20	μA
DC Forward-Current Transfer Ratio	h_{FE}		−10		−35[b]		20	–	
Collector-to-Emitter Sustaining Voltage:									
With base open	$V_{CEO}(sus)$				−50	0	−300[a]	–	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$				−50		−350[a]	–	
Base-to-Emitter Saturation Voltage	V_{BE}		−10		−50[b]		–	−1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				−50[b]	−5	–	−3	V
Magnitude of Common-Emitter, Small-Signal, Short-Circuit Foward-Current Transfer Ratio: f = 5 MHz	$\|h_{fe}\|$		−10		−10		3	–	
Real Part of Common-Emitter Small-Signal, Short-Circuit Impedance: f = 1 MHz	$Re(h_{ie})$		−10		−5		–	300	Ω
Common-Base, Short-Circuit, Input Capacitance: f = 1 MHz	C_{ib}			5	0		–	75	pF
Output Capacitance: f = 1 MHz	C_{ob}	−10					–	15	pF
Forward-Bias, Second-Breakdown Collector Current: 0.4-s, non-repetitive pulse	$I_{S/b}$[c]	−75					−100	–	mA
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						–	23.3	°C/W

[a]CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 2.

[b]Pulsed: Pulse duration = 300 μs; duty factor ≤ 2%.

[c]$I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.

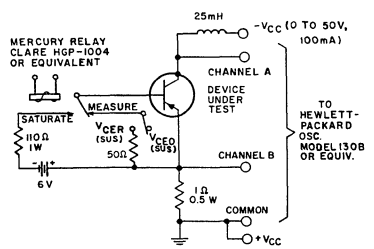
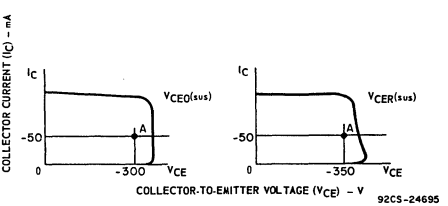


Fig. 2 – Circuit used to measure sustaining voltages, $V_{CEO}(sus)$ and $V_{CER}(sus)$.



The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ are acceptable when the trace falls to the right and above point "A".

Fig. 3 – Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 2).

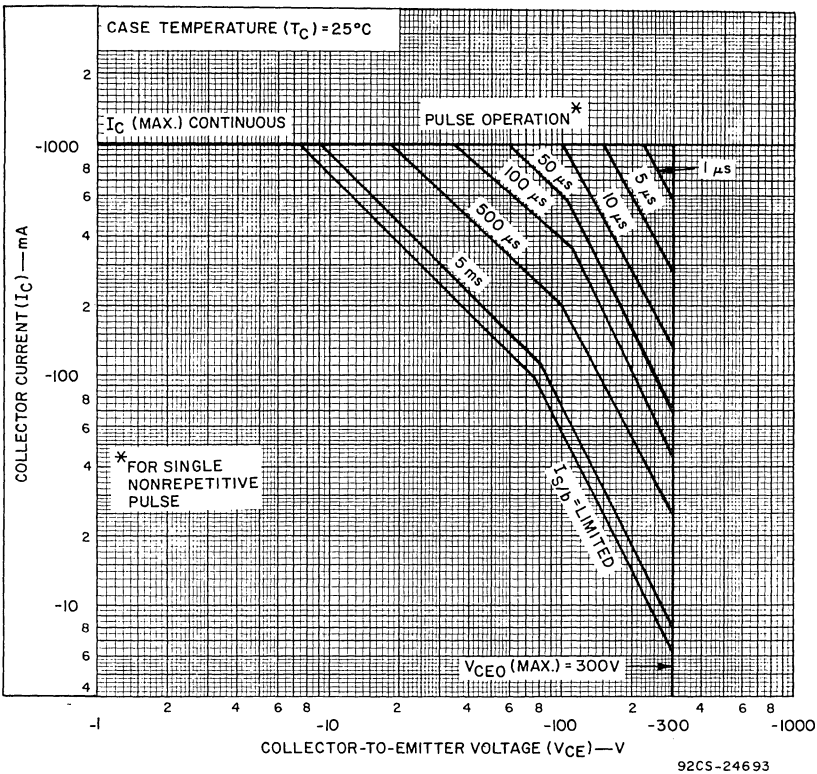


Fig. 4 — Maximum safe operating areas.

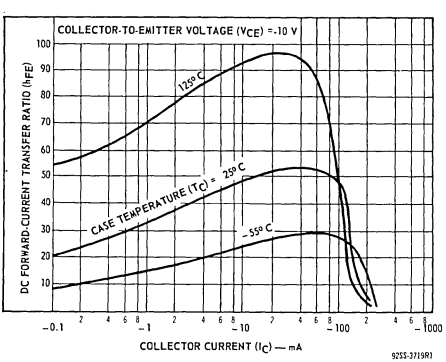


Fig. 5 — Typical dc beta characteristics.

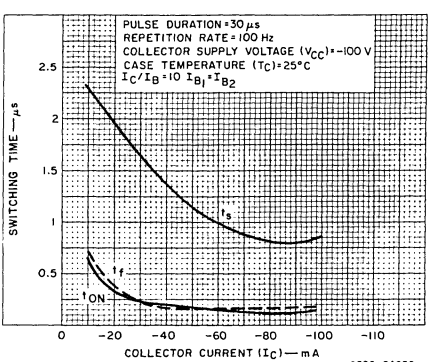


Fig. 6 — Typical saturated switching times.

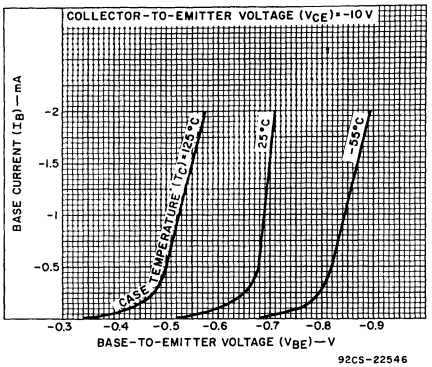


Fig. 7 — Typical input characteristics.

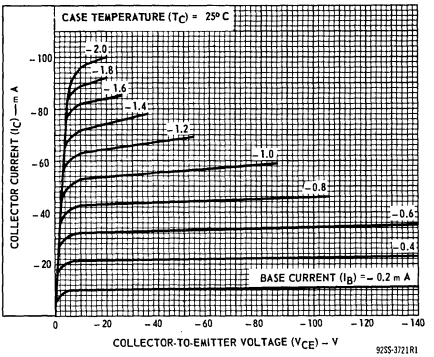


Fig. 8 — Typical output characteristics.

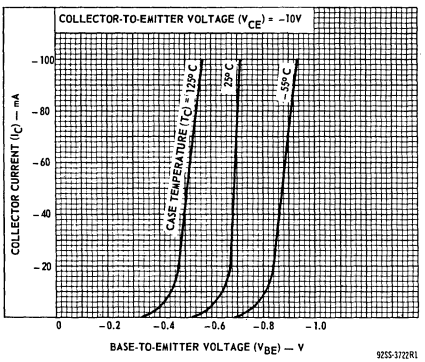


Fig. 9 — Typical transfer characteristics.

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Lead 3 — Collector, Case