# RClamp01501ZC

## Low Voltage RailClamp®
## 1.5V ESD and EOS Protection

**PROTECTION PRODUCTS**

## Description

RClamp®01501ZC is a low capacitance ESD protection device specifically designed to protect high-speed differential lines. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp01501ZC features extremely good ESD protection characteristics highlighted by low ESD clamping voltage, and low TLP trigger voltage. RClamp01501ZC has a maximum capacitance of 0.25pF allowing it to be used on Thunderbolt and USB 3.1 high speed lines. These devices may also be used for EOS protection due to their high peak pulse current capability (5A, tp = 8/20µs). Each device will protect one high-speed data line operating up to 1.5 volts.

RClamp01501ZC is in a DFN 0.60x0.30X0.25mm-2 Lead package. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical.

## Features

- ESD and EOS Protection
- ESD withstand voltage
  - IEC 61000-4-2 (ESD) ±18kV (air), ±12kV (contact)
- Ultra-Low capacitance: 0.25pF max
- Working voltage: 1.5 V
- Protects one high-speed data line
- Low reverse leakage current: 0.5µA max at $V_R$=1.5 V
- Solid-state silicon-avalanche technology

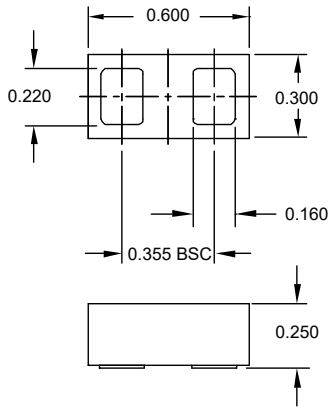
## Mechanical Characteristics

- Package: DFN 0.60x0.30X0.25mm-2 Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: NiAu
- Marking : Marking Code
- Packaging : Tape and Reel

## Applications

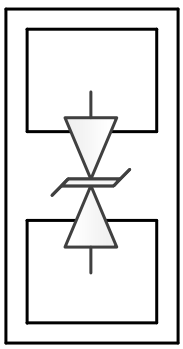
- USB 3.1 Gen 1 and Gen 2
- USB Type-C
- Thunderbolt 3
- DisplayPort 2.0

## Nominal Dimensions




**Nominal Dimensions in mm**

## Device Schematic



**RClamp01501ZC (Bottom View)**

## Absolute Maximum Ratings

| Rating | Symbol | Value | Units |
|---|---|---|---|
| Peak Pulse Power (tp = 8/20µs) | $P_{PK}$ | 20 | W |
| Peak Pulse Current (tp = 8/20µs) | $I_{PP}$ | 5 | A |
| ESD per IEC 61000-4-2 (Air)(1)<br>ESD per IEC 61000-4-2 (Contact)(1) | $V_{ESD}$ | ±18<br>±12 | kV |
| Operating Temperature | $T_{OP}$ | -40 to +85 | °C |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

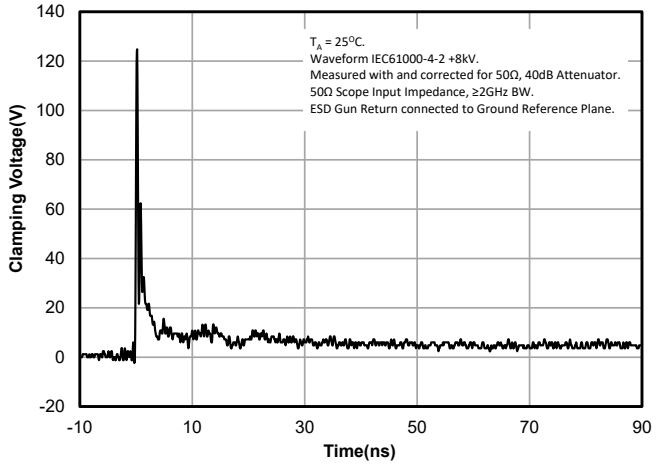
## Electrical Characteristics (T=25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Reverse Stand-Off Voltage | $V_{RWM}$ | -40°C to 85°C | | | 1.5 | V |
| Reverse Breakdown Voltage | $V_{BR}$ | $I_t$ = 1mA | 2.8 | 3.4 | 4.5 | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 1.5V | | <0.1 | 0.5 | µA |
| Clamping Voltage[2] | $V_C$ | $I_{PP}$ = 5A, tp = 1.2/50µs (Voltage), 8/20µs (Current) Combination Waveform, $R_S$ = 2 Ω | | 2.7 | | V |
| ESD Clamping Voltage[3] | $V_C$ | $I_{PP}$ = 4A, tp = 0.2/100ns (TLP) | | 2.5 | | V |
| ESD Clamping Voltage[3] | $V_C$ | $I_{PP}$ = 16A, tp = 0.2/100ns (TLP) | | 5.5 | | |
| Dynamic Resistance[3, 4] | $R_{DYN}$ | tp = 0.2/100ns (TLP) | | 0.23 | | Ω |
| Junction Capacitance | $C_J$ | $V_R$ = 0V to $V_R$ =1.5V, f = 1MHz | | 0.23 | 0.25 | pF |
| Insertion Loss | $S_{21}$ | f = 10GHz | | -0.7 | | dB |

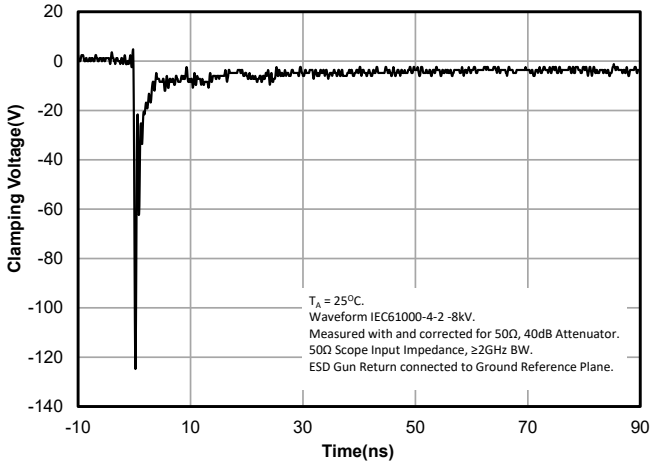
Notes:
(1): ESD gun return path connected to Ground Reference Plane (GRP).
(2): Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, $R_S$ =2 Ω. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
(3): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, $I_{TLP}$ and $V_{TLP}$ averaging window: $t_1$ = 70ns to $t_2$ = 90ns.
(4): Dynamic resistance calculated from $I_{TLP}$ = 4A to $I_{TLP}$ = 16A

# Typical Characteristics

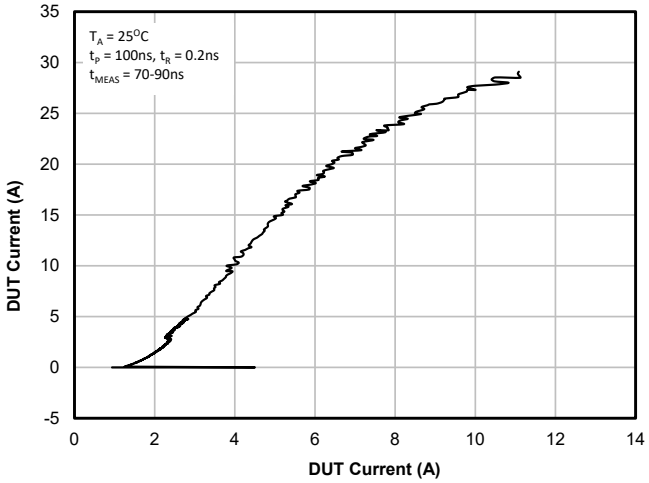
### ESD Clamping (+8kV Contact per IEC 61000-4-2)



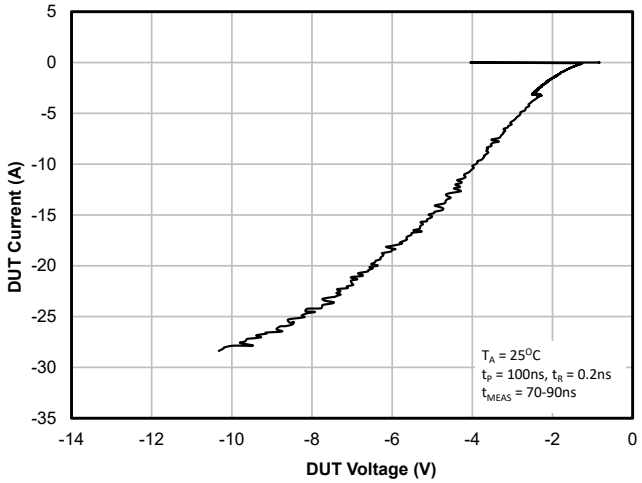

### ESD Clamping (-8kV Contact per IEC 61000-4-2)



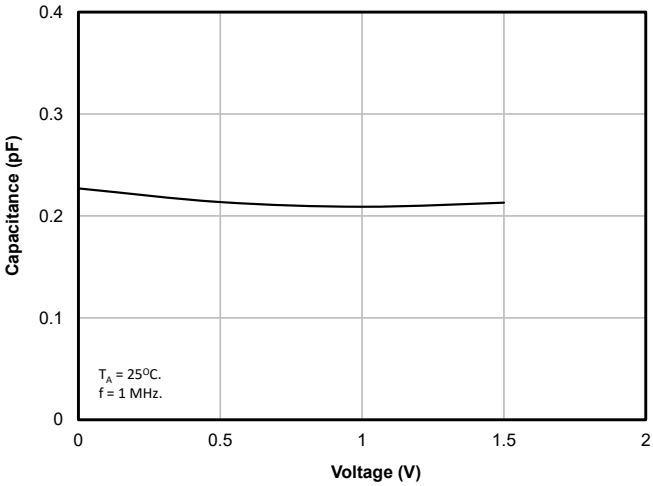

### TLP IV Curve (Positive)



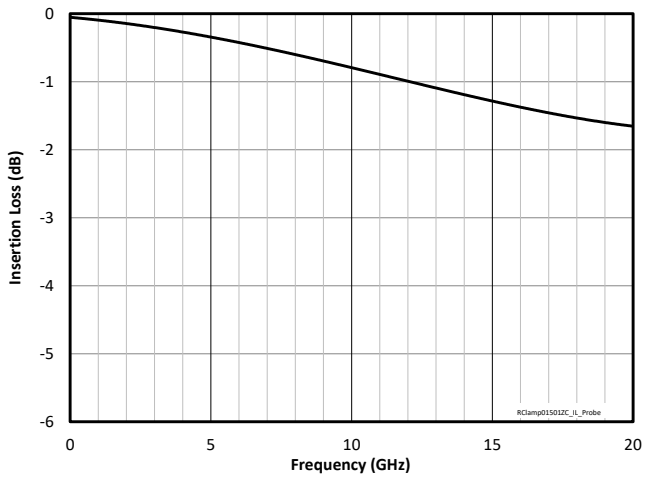

### TLP IV Curve (Negative)




### Capacitance vs. Reverse Voltage




### Insertion Loss (S21)



# Application Information

### Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

### Solder Stencil

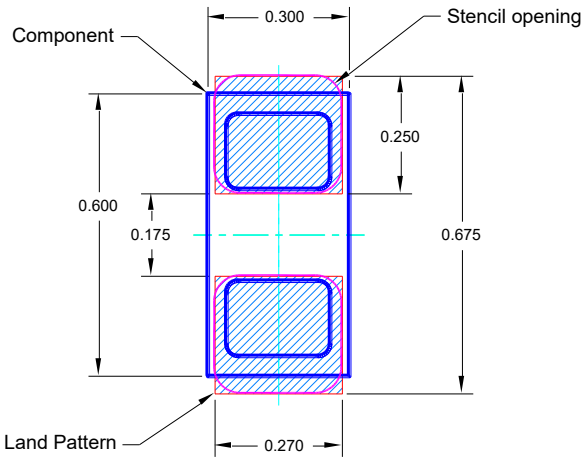
Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W )/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended. A 0.100mm (0.004") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

### Recommended Mounting Pattern




All Dimensions are in mm.

Land Pad. Stencil opening Component

**Table 1 - Assembly Guidelines**

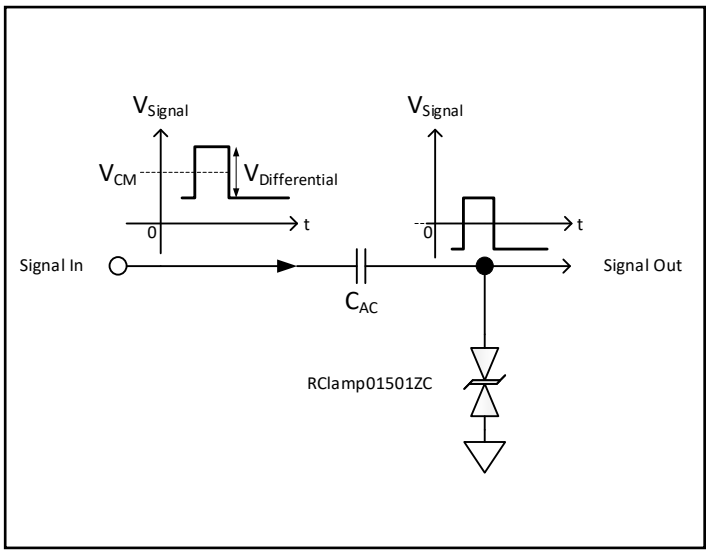
| Assembly Parameter | Recommendation |
|---|---|
| Solder Stencil Design | Laser Cut, Electro-Polished |
| Aperture Shape | Rectangular with Rounded Corners |
| Solder Stencil Thickness | 0.075mm (0.003") or 0.100mm (0.004") |
| Solder Paste Type | Type 4 Size Sphere or Smaller |
| Solder Reflow Profile | Per JEDEC J-STD-020 |
| PCB Solder Pad Design | Solder Mask Defined or Non Solder Mask Defined |
| PCB Pad Finish | OSP or NiAu |

# Application Information

### Device Placement for High Speed Applications

RClamp01501ZC is specifically designed for ESD protection of Thunderbolt 3 and USB 3.x high speed data lines. It features low typical capacitance of 0.23pF and operates with a maximum working voltage of 1.5V. In applications where the common mode voltage is higher than 1.5V, placement of the RClamp01501ZC with respect to the AC coupling capacitors is critical. A general diagram for the placement of the RClamp01501ZC with respect to the AC coupling capacitors is shown in Figure 1. If the line to be protected operates at a voltage higher than the 1.5V working voltage, the TVS should be placed on the AC coupled side of the signal. This will block the common mode voltage and restrict the voltage across the TVS to the differential signal voltage. For differential signal voltages less than the 1.5V working voltage maximum, RClamp01501ZC will be operational and effectively protect the line.

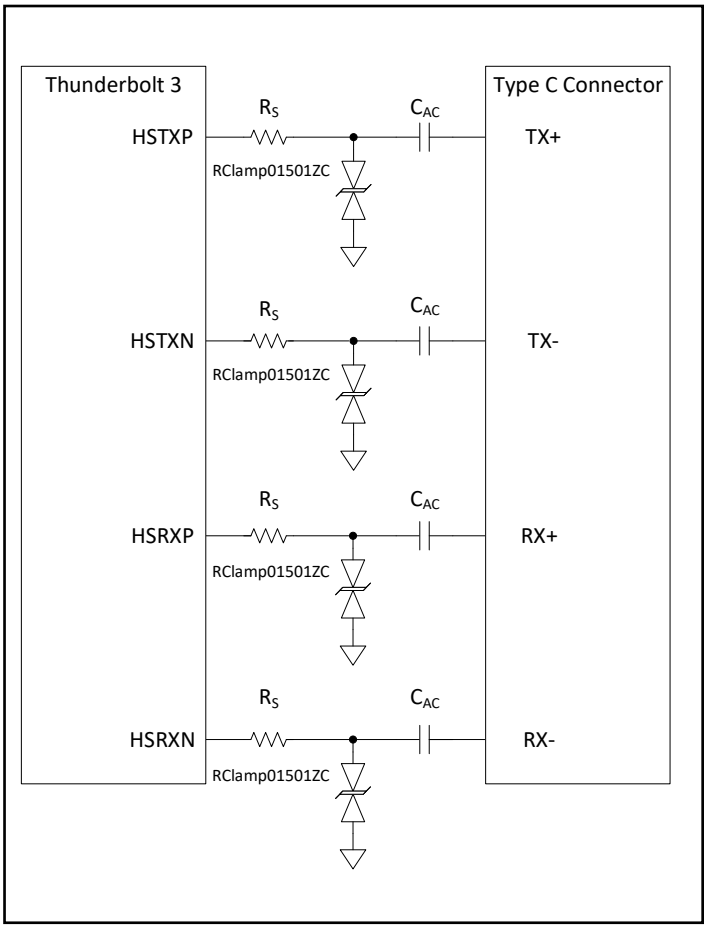
**Figure 1 - RClamp01501ZC and AC Coupling Capacitor**




### Thunderbolt 3 Protection

A typical protection scheme for a differential pair of Thunderbolt 3 high speed data lines is shown in Figure 2. In this configuration the high speed Thunderbolt 3 lines are transmitting with a maximum output voltage of less than 1V, therefore the TVS can be placed on the transceiver side of the AC coupling capacitor. By placing RClamp01501ZC on the transceiver side of AC coupling capacitors on the RX line, the voltage across the TVS is restricted to the differential signal voltage, even when operating in alternate modes interfacing to DisplayPort 1.4a and HDMI. These interfaces transmit at higher common mode voltages, and their maximum differential signal voltages are within the operating range of the RClamp01501ZC.

**Figure 2 - Thunderbolt 3 Protection**



# Application Information Continued

### DisplayPort Line Protection

When RClamp01501ZC is used to protect a dedicated DisplayPort signal line, then AC coupling capacitors should be used on both TX and RX lines as shown in Figure 3. In this case on the transmitting line the TVS should be placed on the connector side of the AC coupling capacitor to block the common mode voltage of the TX signal from the TVS. On the RX line the TVS should be placed on the transceiver side of the AC coupling capacitor to block the common mode voltages of incoming signals.

### USB 3.x protection

RClamp01501ZC can also be used to protect USB 3.x high speed TX and RX lines, as shown in Figure 4. As per the USB specifications, AC coupling capacitors are required on TX lines. In this case the RClamp01501ZC should be placed on the connector side of the AC coupling capacitor as shown in Figure 3. It is recommended that RX AC coupling capacitors be used. In this case the TVS should be placed on the transceiver side of the capacitors.

**Figure 3 - DisplayPort Line Protection**

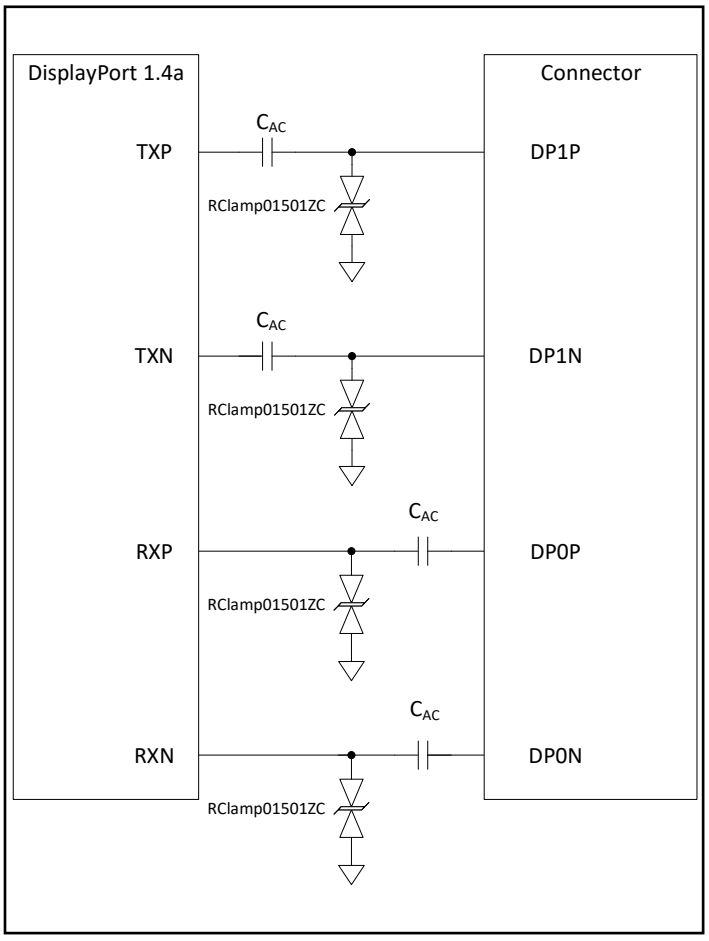
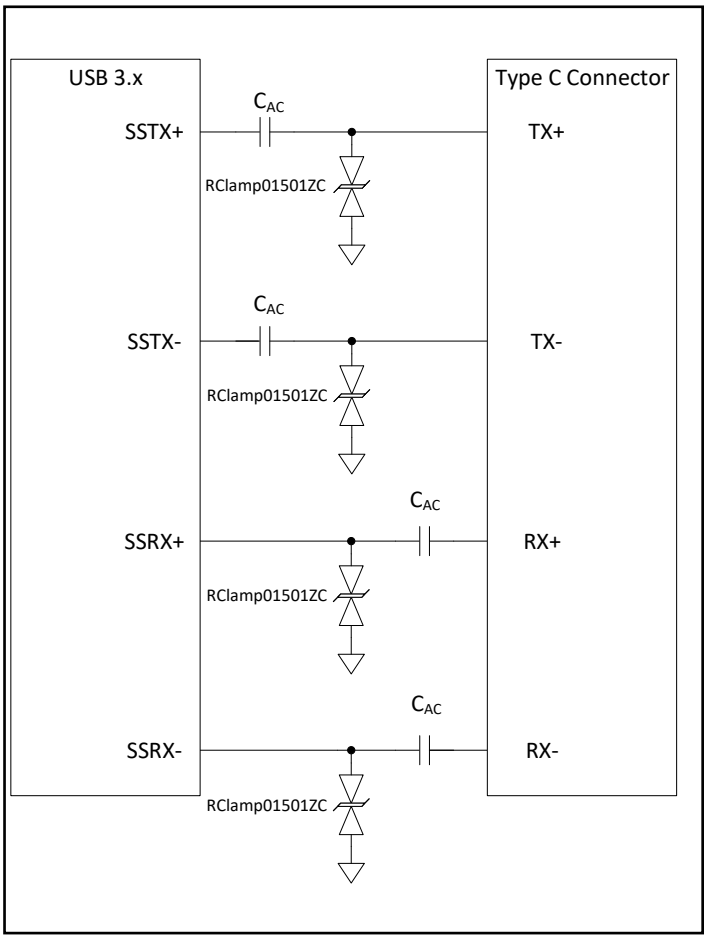
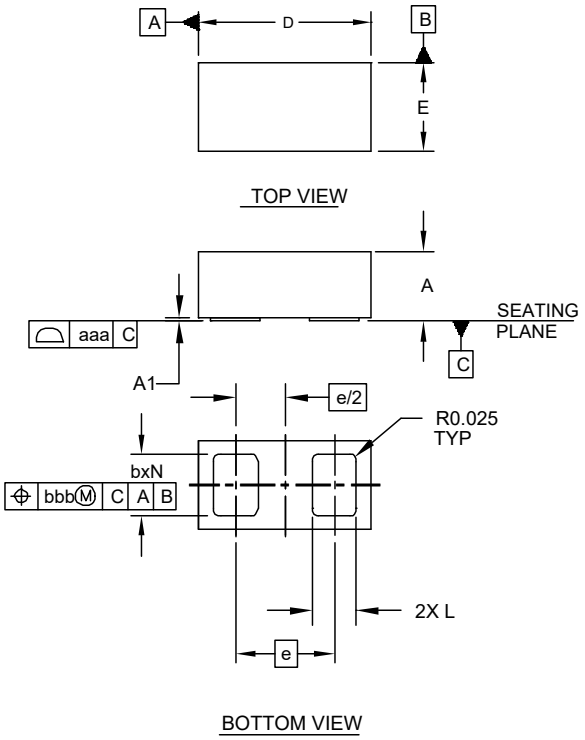



**Figure 4 - USB3.x Protection**



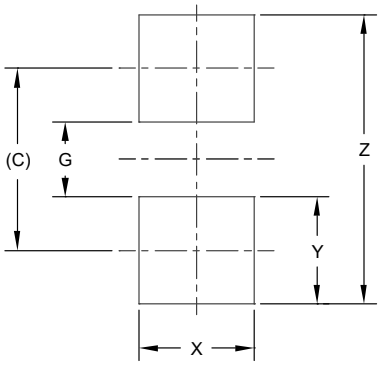
# Outline Drawing - DFN 0.60x0.30X0.25mm-2 Lead




| DIMENSIONS | | | |
|---|---|---|---|
| DIM | MILLIMETERS | | |
| | MIN | NOM | MAX |
| A | 0.235 | 0.250 | 0.265 |
| A1 | 0.000 | 0.010 | 0.050 |
| b | 0.200 | 0.220 | 0.240 |
| D | 0.580 | 0.600 | 0.620 |
| E | 0.280 | 0.300 | 0.320 |
| e | 0.355 BSC | | |
| L | 0.140 | 0.160 | 0.180 |
| N | 2 | | |
| aaa | 0.08 | | |
| bbb | 0.10 | | |

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

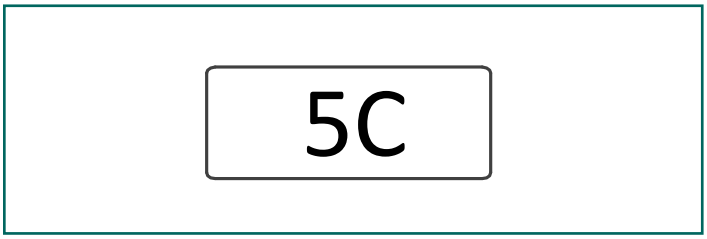
# Land Pattern - DFN 0.60x0.30X0.25mm-2 Lead




| DIMENSIONS | |
|---|---|
| DIM | MILLIMETERS |
| (C) | (0.425) |
| G | 0.175 |
| X | 0.270 |
| Y | 0.250 |
| Z | 0.675 |

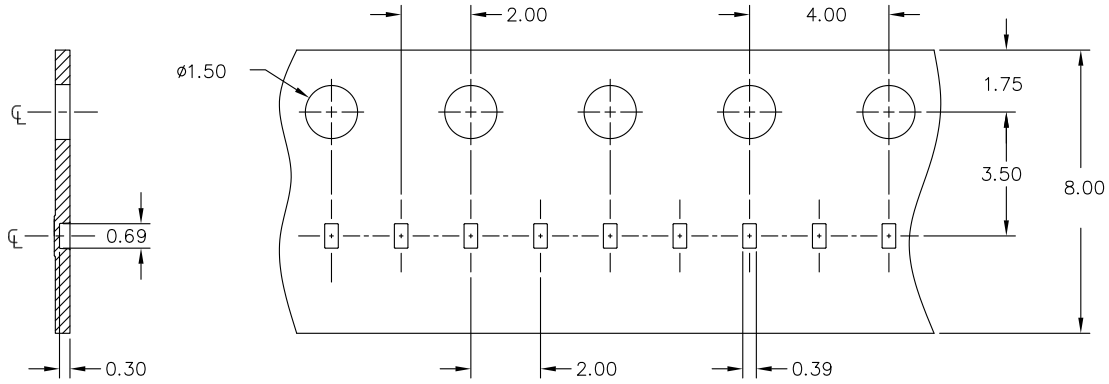
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
COMPANY'S MANUFACTURING GUIDELINES ARE MET.

## Marking Code

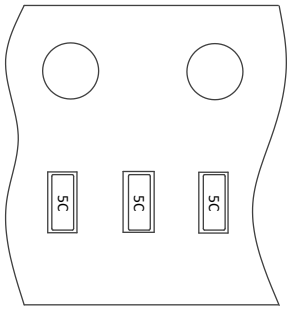



Notes: Device is electrically symmetrical.

## Tape and Reel Specification




Note: All dimensions are nominal dimensions in mm.




## Ordering Information

| Part Number | Qty per Reel | Reel Size |
|---|---|---|
| RClamp01501ZCFT | 15000 | 7 Inch |
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