

PROTECTION PRODUCTS

Description

RClamp®01811ZA is a low capacitance FemtoClamp™ ESD protection device specifically designed to protect high-speed differential lines. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp01811ZA ESD protection characteristics include low typical dynamic resistance of 0.13 Ohms, low peak ESD clamping voltage, and high ESD withstand voltage per IEC 61000-4-2 ($\pm 12\text{kV}$ contact). It also features high EOS peak pulse current rating of 8A ($t_p = 8/20\mu\text{s}$). RClamp01811ZA maximum capacitance is limited to 1.2pF with low insertion loss at 2.5GHz and 5GHz.

RClamp01811ZA is in a DFN 0.60 x 0.30 x 0.25mm 2-lead package. The small package gives the designer the flexibility to protect single lines in space-constrained applications.

Features

- ESD withstand voltage
 - ♦ IEC 61000-4-2 (ESD): $\pm 12\text{kV}$ (Contact), $\pm 20\text{kV}$ (Air)
- Low ESD Clamping
- Low capacitance: 1.2pF Maximum
- Protects one high-speed data line
- Working voltage: 1.8V
- Low reverse leakage current: 100nA max at $V_R = 1.8\text{V}$
- Solid-state silicon-avalanche technology

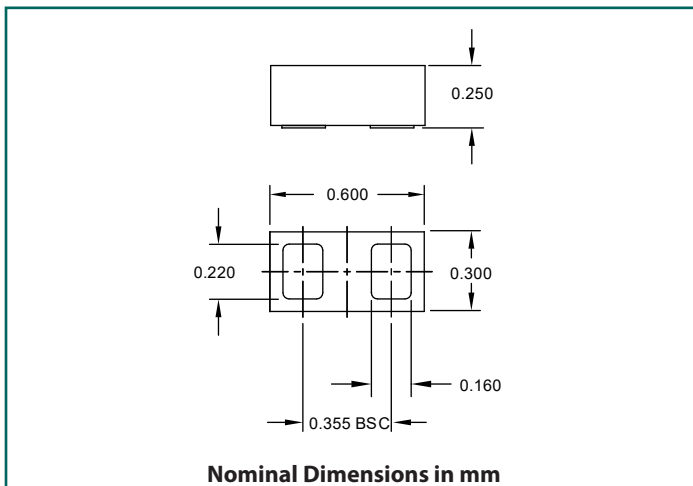
Mechanical Characteristics

- Package: DFN 0.60 x 0.30 x 0.25mm 2-Lead
- Pb-free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-free
- Marking: Marking Code
- Packaging: Tape and Reel

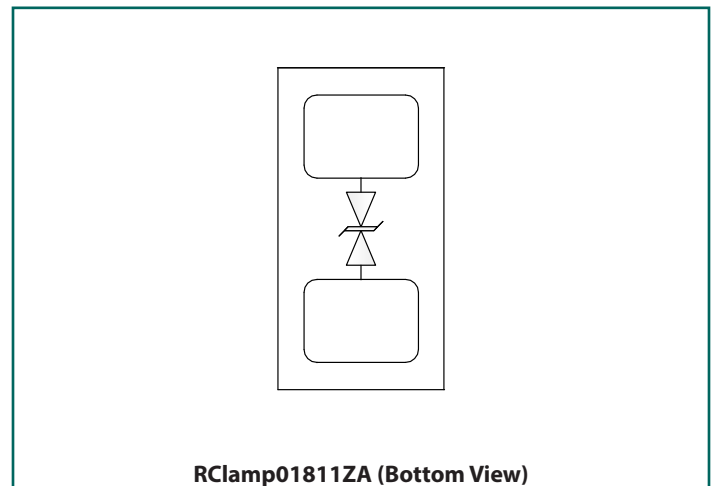
Applications

- Cellphones and accessories
- Notebooks & Handhelds

Nominal Dimensions



Schematic and Pin Configuration



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{PK}	45	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	8	A
ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V _{ESD}	±12	kV
ESD per IEC 61000-4-2 (Air) ⁽¹⁾		±20	
Operating Temperature	T _{OP}	-40 to +85	°C
Junction Temperature and Storage Temperature	T _J and T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}	-40°C to 85°C			1.8	V
Reverse Breakdown Voltage	V _{BR}	I _t = 10mA	2.2	2.6	3.4	V
Reverse Leakage Current	I _R	V _{RWM} = 1.8V		<10	100	nA
Clamping Voltage ⁽²⁾	V _C	I _{PP} = 8A, tp = 1.2/50μs (Voltage), 8/20μs (Current) Combination Waveform, R _s = 2Ω		4.8	5.8	V
ESD Clamping Voltage ⁽³⁾	V _C	tp = 0.2/100ns (TLP)	I _{PP} = 4A	4		V
			I _{PP} = 16A	5.5		
Dynamic Resistance ⁽³⁾⁽⁴⁾	R _{DYN}	tp = 0.2/100ns (TLP)		0.13		Ohms
Junction Capacitance	C _J	V _R = 0V to V _{RWM} , f = 1MHz		0.55	1.2	pF
Insertion Loss	I _L	f = 2.5GHz		0.25		dB
		f = 5GHz		0.70		dB

Notes:

(1): ESD gun return path connected to Ground Reference Plane (GRP).

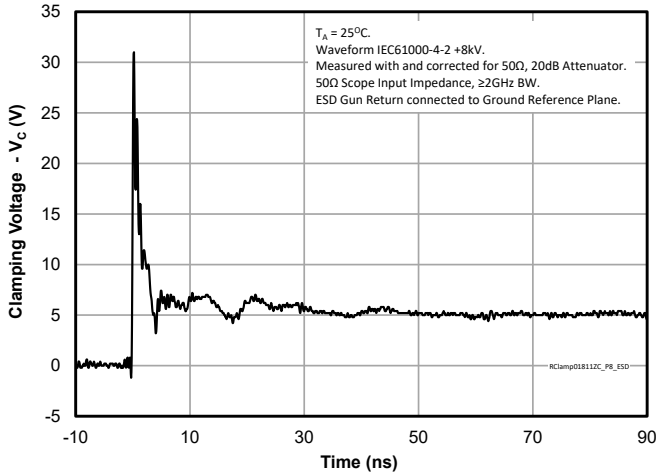
(2): Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, R_s = 2 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

(3): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t₁ = 70ns to t₂ = 90ns.

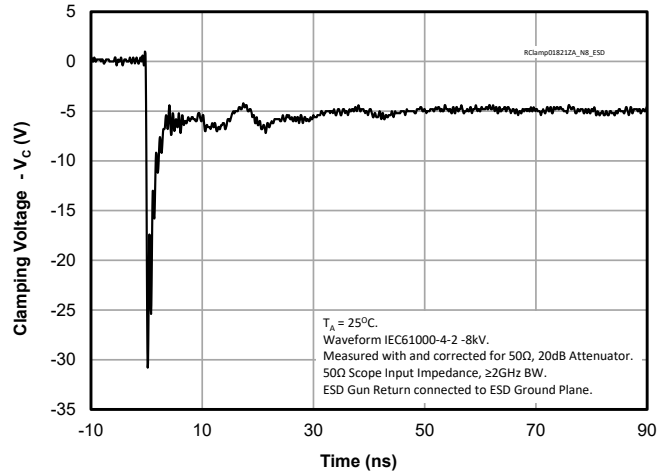
(4): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

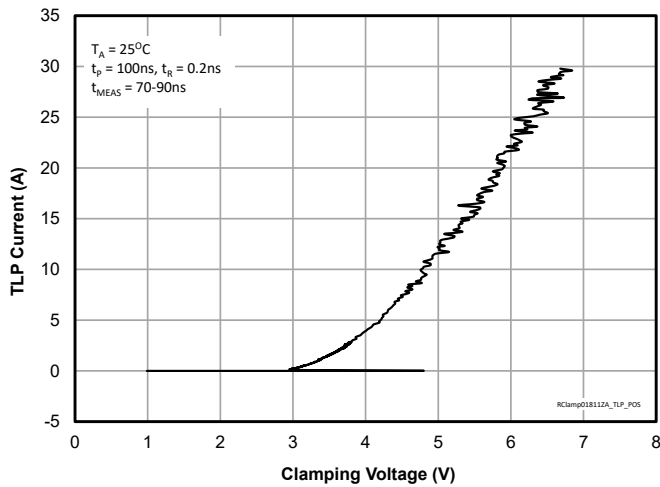
ESD Clamping (+8kV Contact per IEC 61000-4-2)



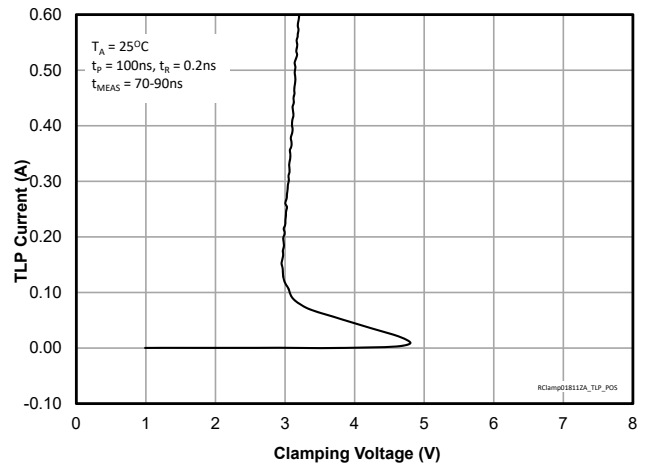
ESD Clamping (-8kV Contact per IEC 61000-4-2)



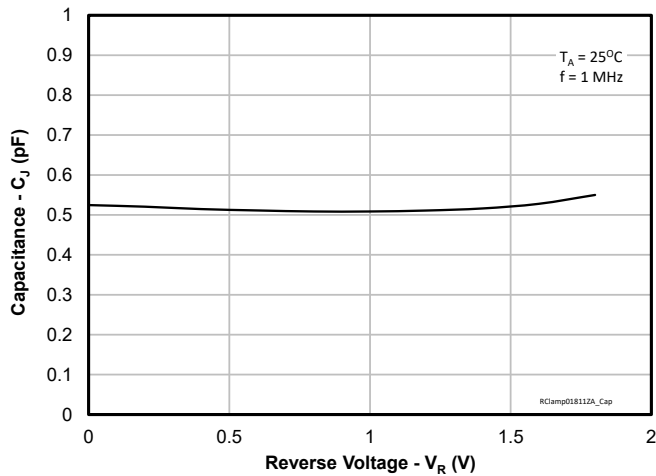
TLP Characteristic



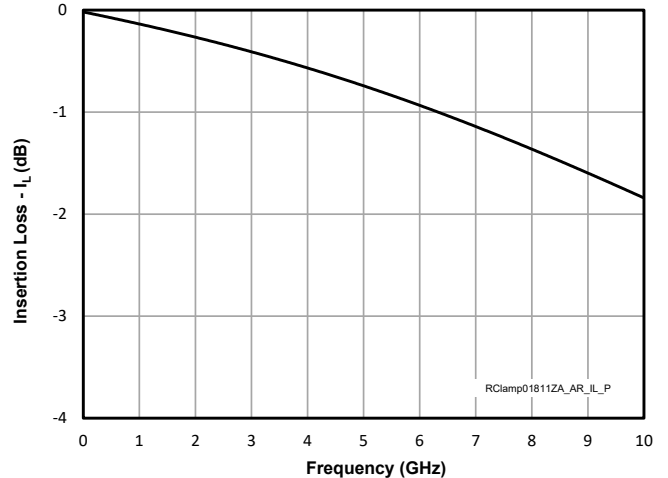
TLP Characteristic (Low Current Detail)



Capacitance vs. Reverse Voltage



Insertion Loss (S21)



Application Information

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

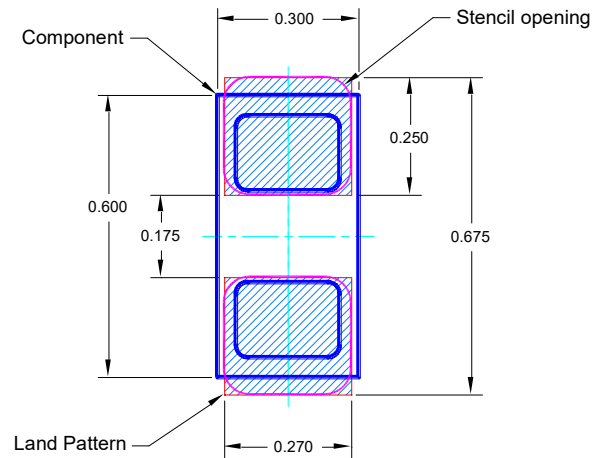
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended. A 0.100mm (0.004") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern



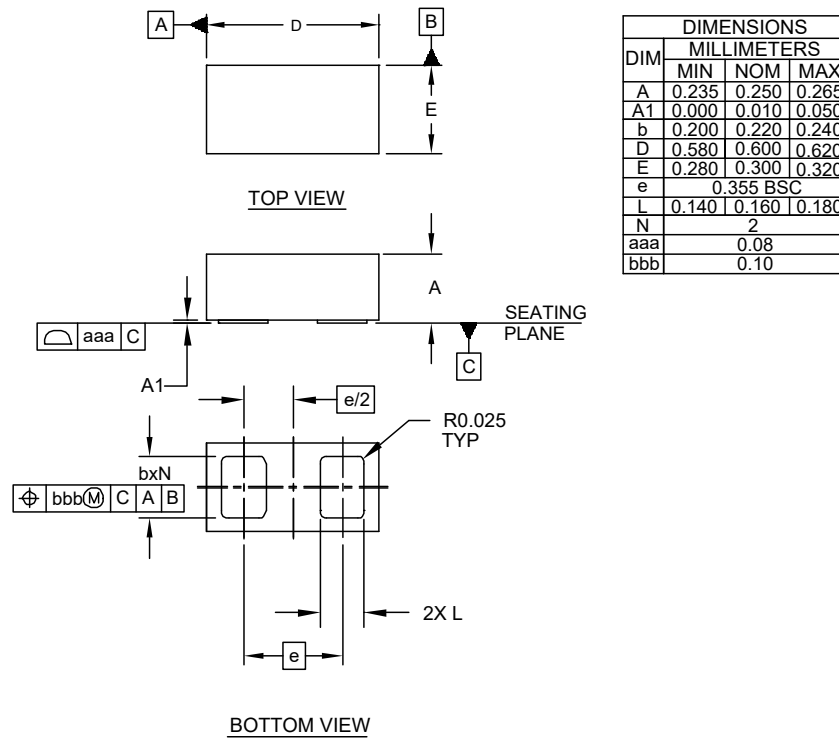
All Dimensions are in mm.

Land Pad.
 Stencil opening
 Component

Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003") or 0.100mm (0.004")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Solder Mask Defined or Non Solder Mask Defined
PCB Pad Finish	OSP or NiAu

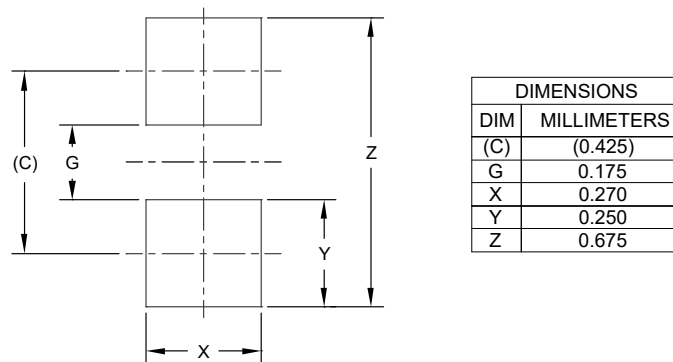
Outline Drawing - DFN 0.60x0.30x0.25mm 2-Lead



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

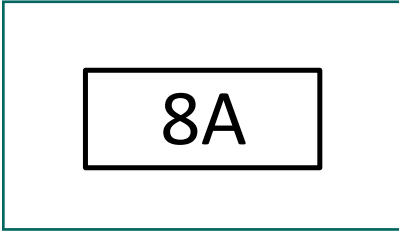
Land Pattern - DFN 0.60x0.30x0.25mm 2-Lead



NOTES:

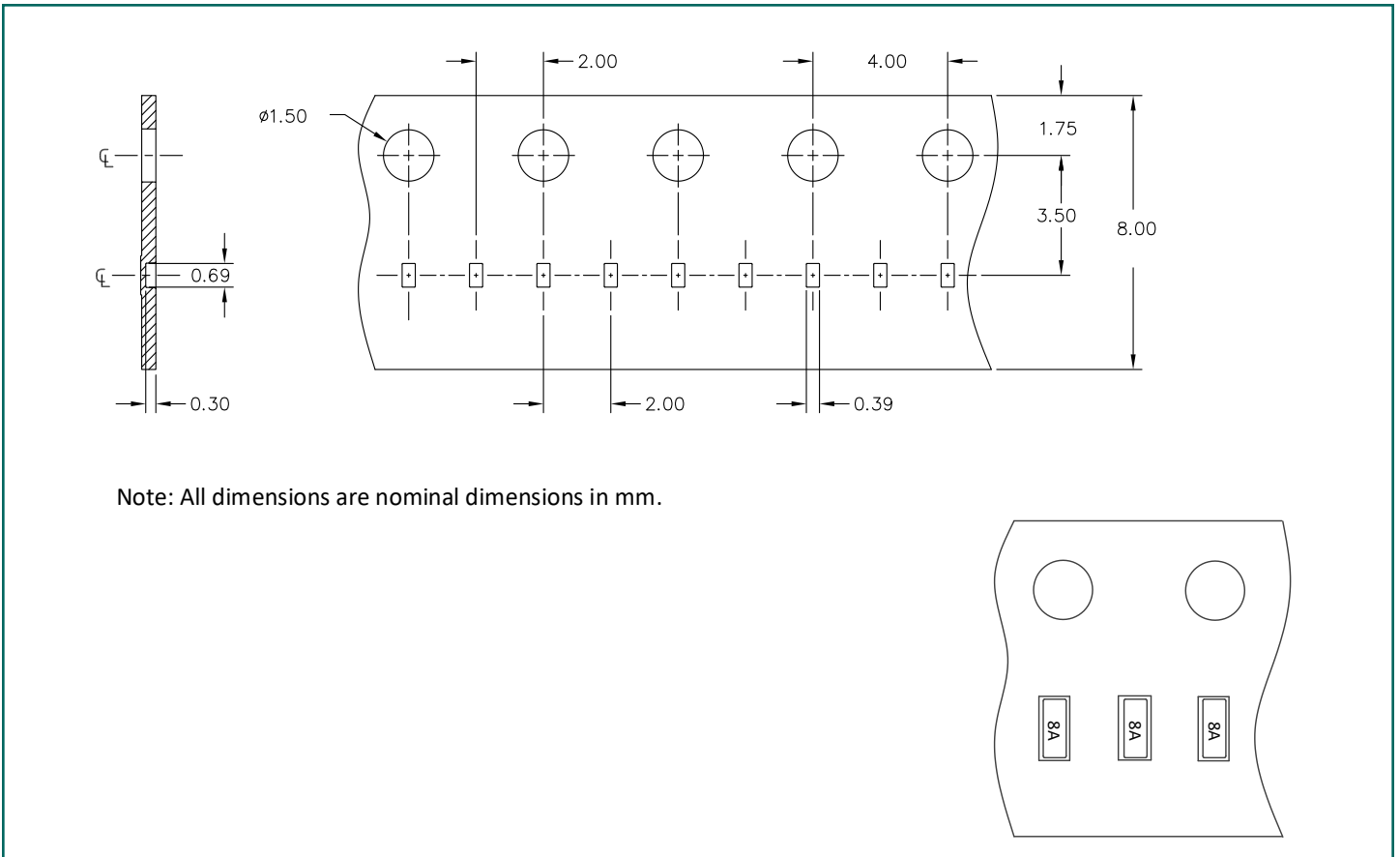
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Notes: Device is electrically symmetrical.

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp01811ZA.F	15000	7 Inch

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Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com