RClamp0512TQ

Low Capacitance RailClamp®
2-Line Surge and ESD Protection

PROTECTION PRODUCTS

Description

RClamp®0512TQ is specifically designed to provide secondary surge and ESD protection on high-speed ports. RClamp0512TQ integrates low capacitance, surge-rated steering diodes with a high power transient voltage suppressor (TVS). The TVS utilizes snap-back or "crow-bar" technology to minimize device clamping voltage and features high surge current capability of 20A (tp=8/20us). ESD characteristics are highlighted by high ESD withstand voltage (+/-30kV per IEC 61000-4-2) and extremely low dynamic resistance (0.075 Ohms typical). Each device will protect two lines operating at 5 volts and are qualified to AEC-Q100, Grade 1 (-40 to +125 °C) for automotive applications.

RClamp0512TQ is in a DFN 1.0 x 0.6 x 0.4mm 3-Lead package. The flow- through package design simplifies PCB layout.

Features

- Transient Protection to
  - IEC 61000-4-2 (ESD) 30kV (Air), 30kV (Contact)
  - IEC 61000-4-4 (EFT) 4kV (5/50ns)
  - IEC 61000-4-5 (Lightning) 20A (8/20µs)
  - ISO-10605 (ESD) 30kV (Air), 30kV (Contact)
- Qualified to AEC-Q100, Grade 1
- Very Small PCB Area: 0.6mm^2
- Protects Two High-Speed Data Lines
- Working Voltage: 5V
- Low Capacitance: 3pF Maximum
- Dynamic Resistance: 0.075 Ohms (Typ)
- Solid-State Silicon-Avalanche Technology

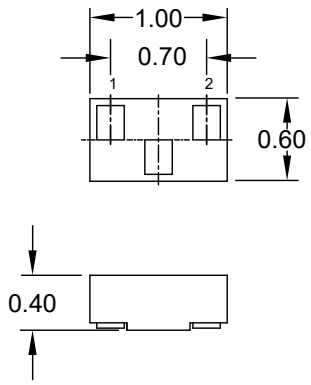
Mechanical Characteristics

- Package: DFN 1.0 x 0.6 x 0.4mm 3-Lead
- Pb-free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-free
- Molding Compound Flammability Rating: UL 94V-0
- Marking : Marking Code + Dot Matrix Date Code
- Packaging : Tape and Reel

Applications

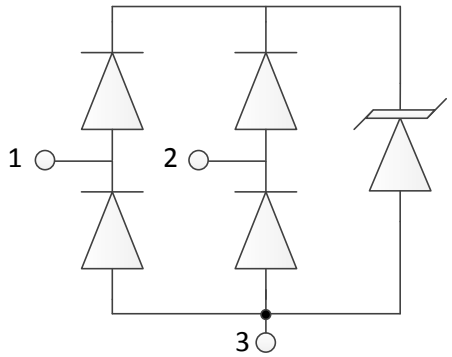
- Automotive Applications
- Industrial Equipment
- Integrated Magnetics / RJ-45 Connectors
- 10/100/1000 Ethernet
- 2.5GbE
- USB 2.0

Nominal Dimensions



Nominal Dimensions in mm

Functional Schematic



Device Schematic

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	170	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	20	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(1)	V_{ESD}	±30 ±30	kV
ESD per ISO-10605 (Contact)(2) ESD per ISO-10605 (Air)(2)	V_{ESD}	±30 ±30	kV
Operating Temperature	T_{OP}	-40 to +125	^{O}C
Junction Temperature and Storage Temperature	T_J & T_{STG}	-55 to +150	^{O}C

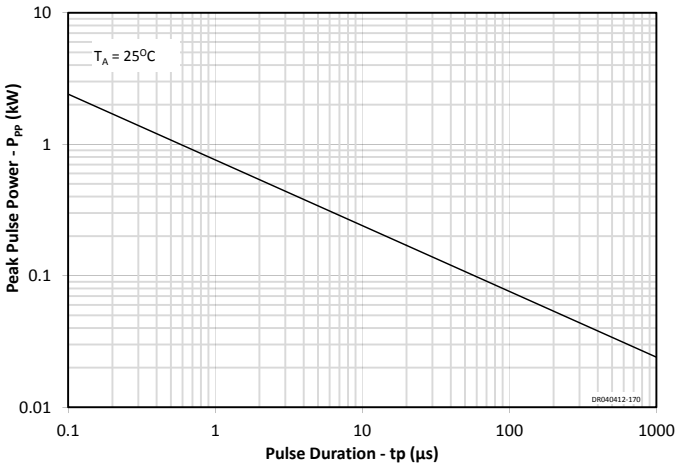
Electrical Characteristics (T=25^{O}C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40^{O}C to 125^{O}C, Between any two pins				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 10mA, Pin 1 or 2 to Pin 3	-40^{O}C to 125^{O}C	6.5	9.5	11.5	V
Holding Current	I_H			75	150	250	mA
Reverse Leakage Current	I_R	V_{RWM} = 5V	T = 25^{O}C		0.01	0.100	µA
			T = 125^{O}C		0.03	0.250	µA
Clamping Voltage(3)	V_C	I_{PP} = 20A, Pin 1 or 2 to Pin 3			5	8.5	V
ESD Clamping Voltage(4)	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP) Pin 1 or 2 to Pin 3			4.3		V
ESD Clamping Voltage(4)	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP) Pin 1 or 2 to Pin 3			5.2		V
Dynamic Resistance(4), (5)	R_{DYN}	tp = 0.2/100ns (TLP), Pin 1 or 2 to Pin 3			0.075		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz, Pin 1 or 2 to Pin 3			2	3	pF
		V_R = 0V, f = 1MHz, Pin 1 to Pin 2			1.1	2	pF

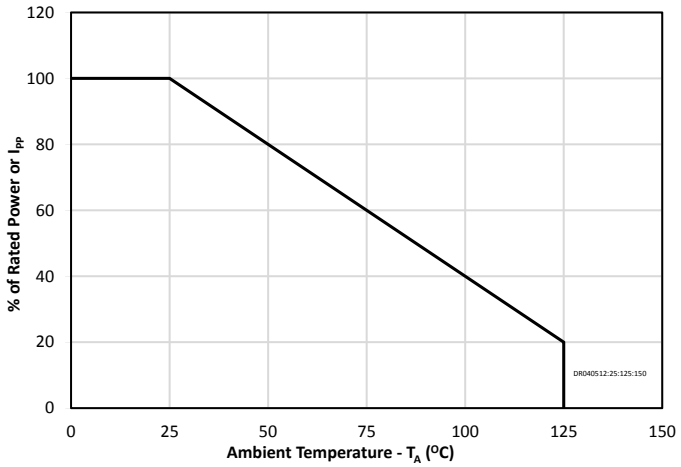
Notes:
(1): ESD Gun return path to Ground Reference Plane (GRP)
(2): ESD Gun return path to Horizontal Coupling Plane (HCP); Test conditions: a)150pF/330pF, 330Ω b) 150pF/330pF, 2kΩ
(3): Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, R_S = 2Ω. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
(4): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(5): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

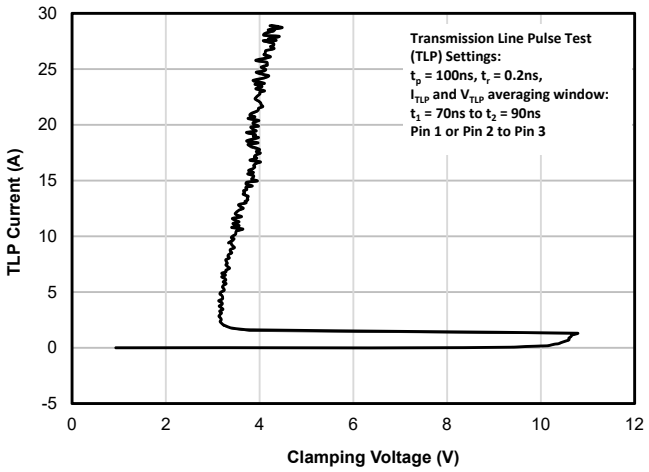
Non-Repetitive Peak Pulse Power vs. Pulse Time



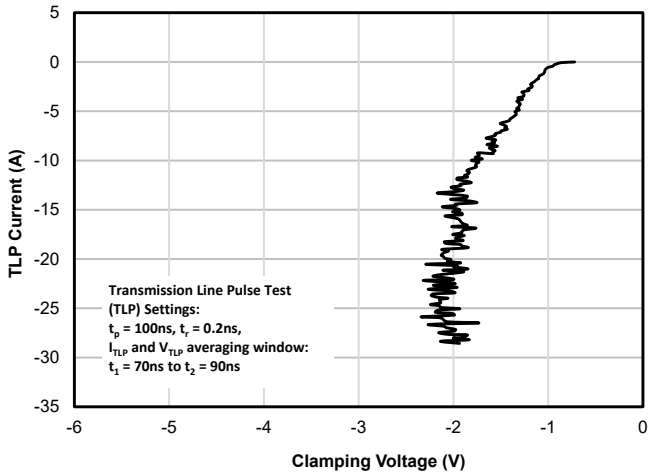
Power Derating Curve



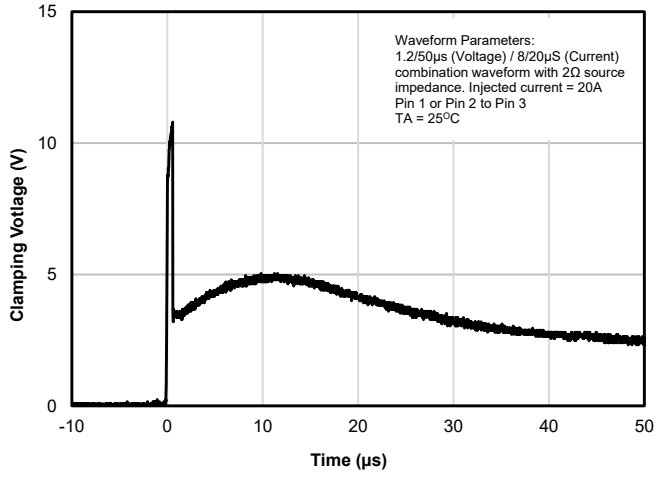
TLP IV Curve (Positive Pulse)



TLP IV Curve (Negative Pulse)

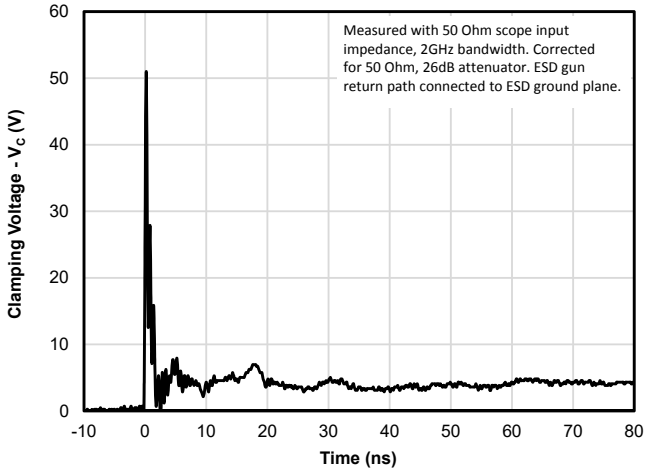


Clamping Characteristic (20A, tp =1.2/50µs)

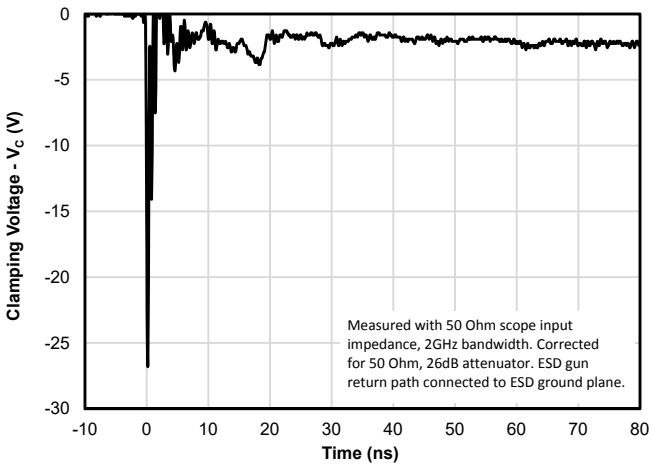


Typical Characteristics (Continued)

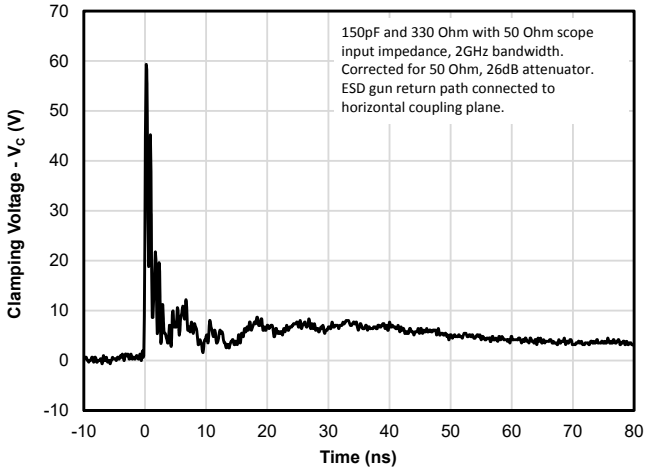
ESD Clamping (+8kV Contact per IEC 61000-4-2)



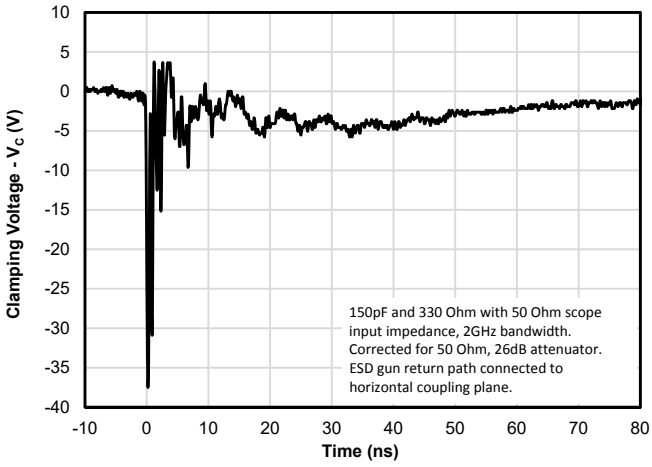
ESD Clamping (-8kV Contact per IEC 61000-4-2)



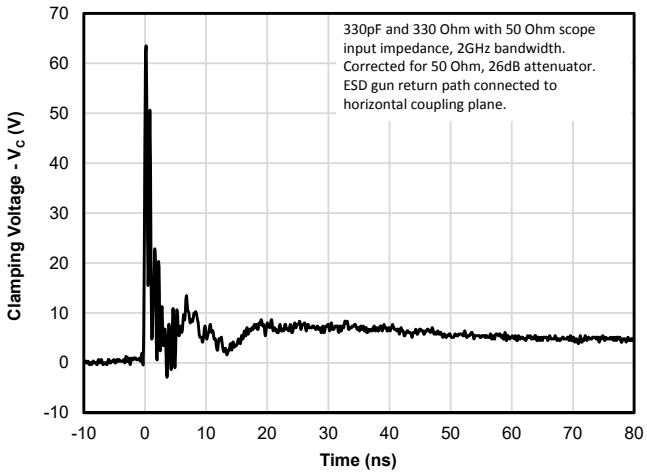
ESD Clamping (+15kV Contact per ISO-10605 150pF, 330Ω)



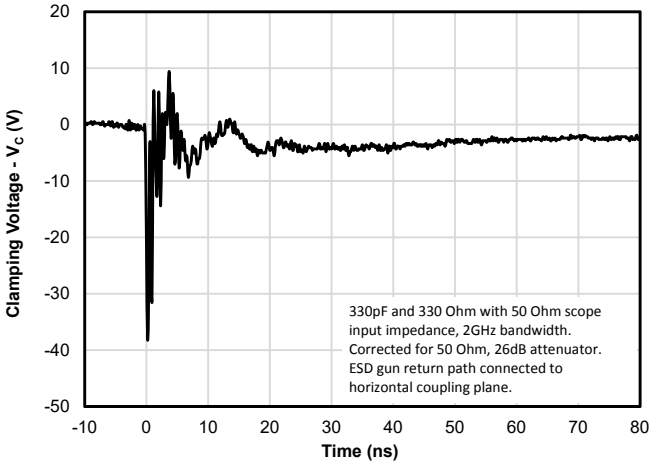
ESD Clamping (-15kV Contact per ISO-10605 150pF, 330Ω)



ESD Clamping (+15kV Contact per ISO-10605 330pF, 330Ω)

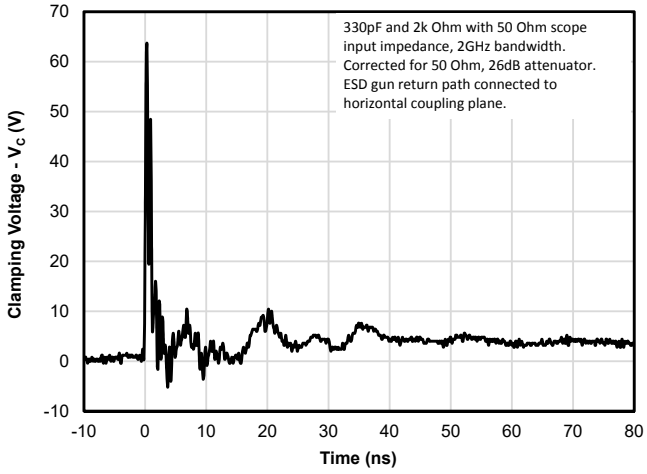


ESD Clamping (-15kV Contact per ISO-10605 330pF, 330Ω)

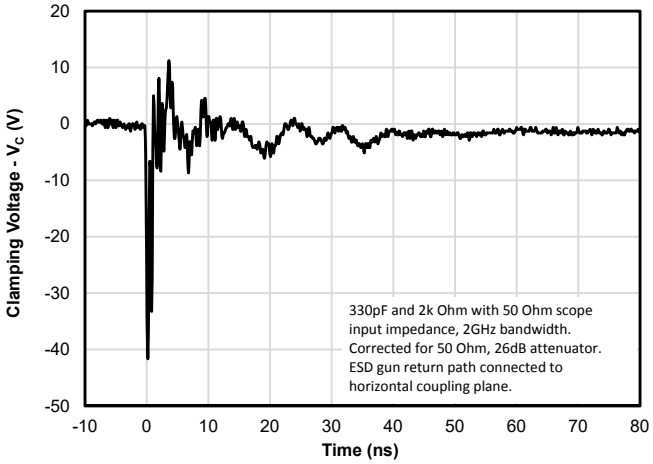


Typical Characteristics

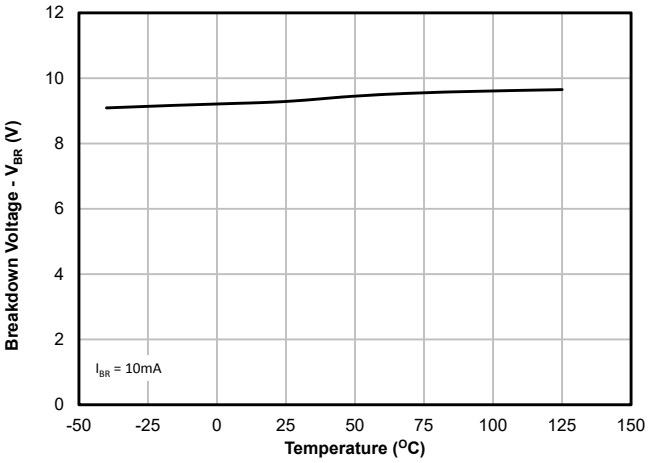
ESD Clamping (+15kV Contact per ISO-10605 330pF, 2kΩ)



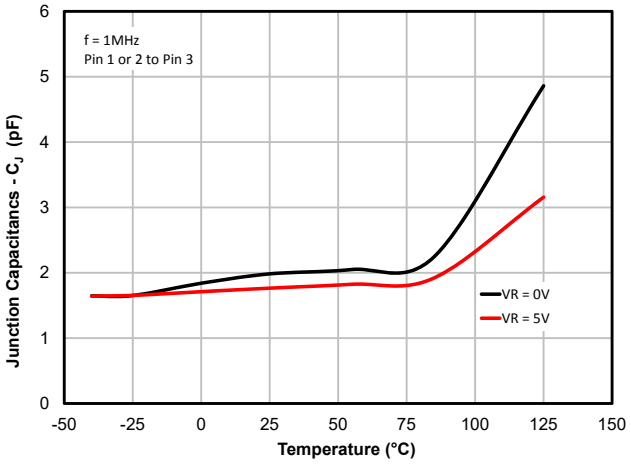
ESD Clamping (+15kV Contact per ISO-10605 330pF, 2kΩ)



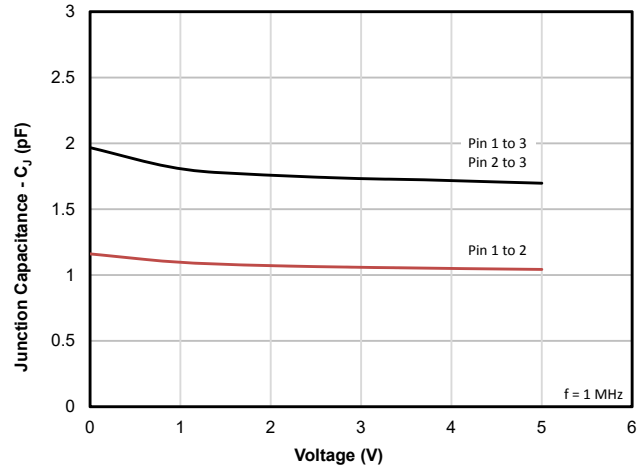
Breakdown Voltage (V_{BR}) vs. Temperature



Capacitance vs. Temperature

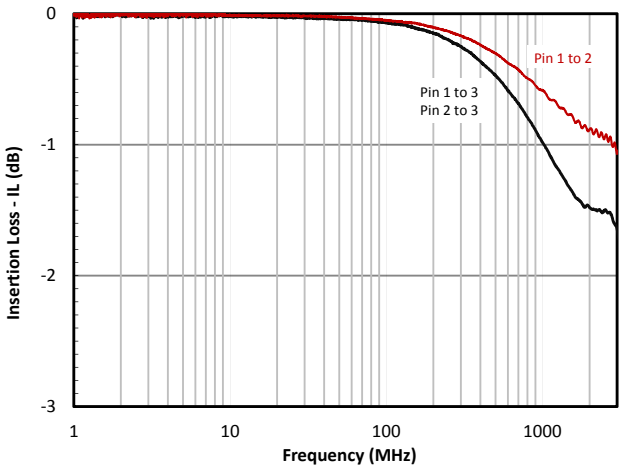


Capacitance vs. Reverse Voltage

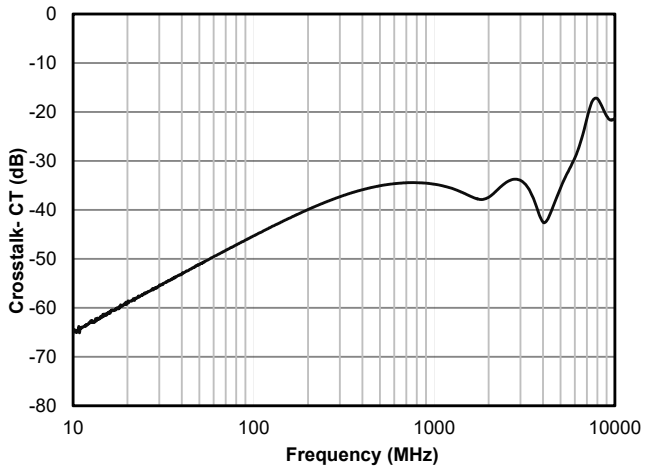


Typical Characteristics (Continued)

Insertion Loss - S21



Analog Crosstalk



Application Information

Device Operation

This device utilizes a multi-junction structure that is designed to switch to a low voltage state when triggered by ESD, EOS, or other transient events. During normal operation, the device will present a high-impedance to the circuit for voltage up to the working voltage (V_{RWM}) of the device. When the voltage across the device terminals exceeds the breakdown voltage (V_{BR}), avalanche breakdown occurs in the blocking junction causing the device to "snap-back" or switch to a low impedance on-state. This has the advantage of lowering the overall clamping voltage (V_C) as ESD peak pulse current (I_{PP}) flows through the device. Once the current decreases below the holding current (I_H), the device will return to a high-impedance off-state.

IV Characteristic Curve (Pin 1 to Pin 2)

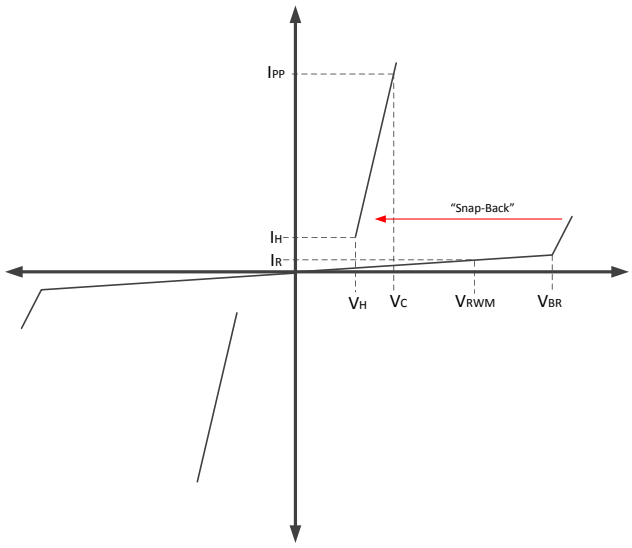


Table 1 - Parameter Definition	
Symbol	Parameter
V_{RWM}	Maximum Working Voltage
V_{BR}	Breakdown Voltage
V_C	Clamping Voltage
I_H	Holding Current
I_R	Reverse Leakage Current
I_{PP}	Peak Pulse Current

Application Information

Ethernet Protection

Ethernet ports are exposed to external transient events in the form of ESD, EFT, lightning, and cable discharge events (CDE). Test standards that model these events include IEC 61000-4-2 for ESD, IEC 61000-4-4 for EFT, and IEC 61000-4-5 and GR-1089 for lightning. Any of these events can cause catastrophic damage to the PHY IC.

When designing Ethernet protection, the entire system must be considered. Over-voltage events can be common mode (with respect to ground) or differential (line-to-line). An Ethernet port includes interface magnetics consisting of transformers integrated with common mode chokes. The transformer center taps are connected to ground via an RC network or "Bob Smith" termination. The purpose of this termination is to reduce common mode emissions. The transformer provides common mode isolation to transient events, but no protection for differential surges. During a differential transient event, current will flow through the transformer, charging the windings on the line side. Energy is transferred to the secondary until the surge subsides or the transformer saturates.

A typical protection scheme which utilizes the RClamp0512TQ is shown in Figure 1. The devices are located on the PHY side of the transformer with one device placed across each line pair. Parasitic inductance in the protection path should be minimized by locating RClamp0512TQ as physically close to the magnetics as possible, and preferably on the same side of the PCB. Reducing parasitic inductance is especially important for suppressing fast rise time transients such as ESD and EFT. Inductance in the path of the protection device increases the peak clamping voltage seen by the protected device (V = L di/dt). For example, 1nH of inductance can increase the peak clamping voltage by 30V for a 30A (8kV) ESD pulse with a 1ns rise time. Differential pairs are routed through each RClamp0512TQ at pins 1 and 2. Pin 3 of the device is not connected.

Placing the protection on the PHY side of the magnetics is advantageous in that the magnitude and duration of the surge is attenuated by the transformer windings. The amount of attenuation will vary by vendor and configuration of the magnetics. The Ethernet transformer has to be able to support the impulse tests without failure. A typical Ethernet transformer can withstand a few hundred amperes (tp=8/20us) before failure occurs, but this needs to be verified by testing. Alternatively, the protection can be placed on the line side of the transformer. However, the additional protection afforded by the transformer is lost, and the ability of the system to withstand high energy surges is limited to the capability of the protection device.

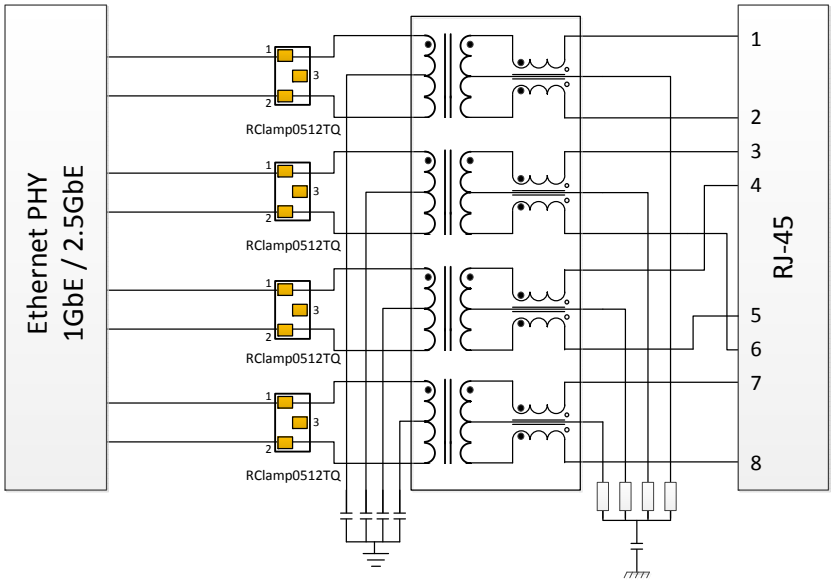


Figure 1 - 1GbE / 2.5GbE Protection Circuit

Application Information

USB Interface Protection

RClamp0512TQ may be used to protect D+ and D- lines in USB 2.0, USB 3.2 Gen 1×1 and USB 3.2 Gen 2×1 applications. In each case, USB D+ and D- pins are routed through RClamp0512TQ at pin1 and pin 2. Pin 3 is connected to the ground plane. Figures 2 and 3 below are examples of protecting USB 3.2 Gen 1×1 Type-A interfaces (host side shown).

For USB 3.2 Gen 1×1 applications, RClamp3324T is recommended for protecting the 5Gb/s SuperSpeed line pairs. Lines are routed through the device at pins 1-4. Traces should be kept the same length to avoid impedance mismatch. Ground is connected at pins 5 and 6. The differential impedance of each pair can be controlled for USB 3.2 Gen 1×1(85 Ohms +/-15%) while maintaining a minimum trace-to-trace and trace-to-pad spacing. Individual PCB design constraints may necessitate different spacing or trace width. Both ground pads should be connected for optimal performance. Ground connection is made using filled via-in-pad. Additional information may be found on the device data sheet.

For USB 3.2 Gen 2×1 applications, RClamp0561Z is recommended for protecting the 10Gb/s SuperSpeed+ line pairs. One device is connected between each line and ground. RClamp0561Z has a maximum capacitance of 0.15pF allowing it to be used on transmission lines operating in excess of 10GHz. Single line devices make it easier for the designer to route the traces and maintain equal distance between the differential pairs for maximum signal integrity.

Single line devices such as uClamp0571P are recommended for surge and ESD protection of the VBus line. This device features high surge and ESD capability and may be used on 5V power rails. In power delivery (PD) applications, higher working voltage TVS device may be needed. Options exist for ESD and surge protection up to 24V.

Device Placement

Placement of the protection component is a critical element for effective ESD suppression. TVS diodes should be placed as close to the connector as possible. This helps reduce transient coupling to nearby traces. Ground connections should be made directly to the ground plane using micro-vias. This reduces parasitic inductance in the ground path and minimizes the clamping voltage seen by the protected device.

Figure 2 - USB 3.2 Type-A Protection Example

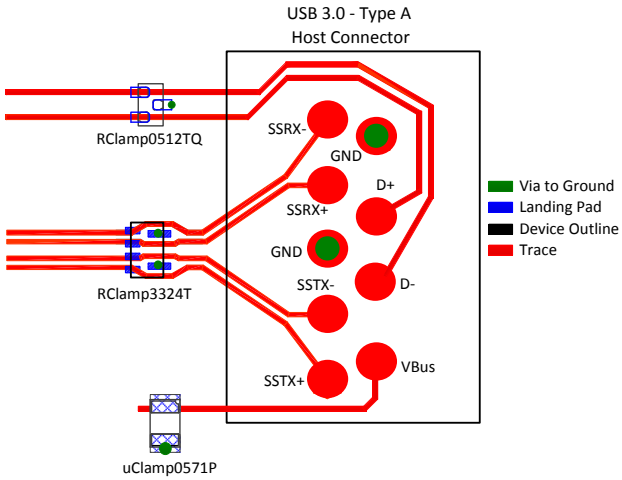
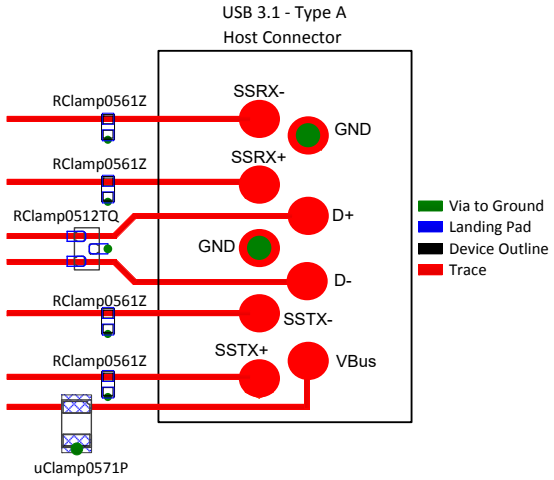


Figure 3 - USB 3.2 Type-A Protection Example



Applications Information

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 2. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

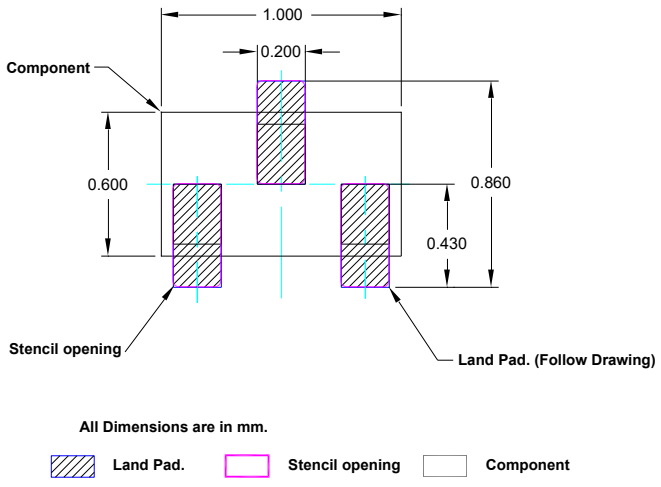
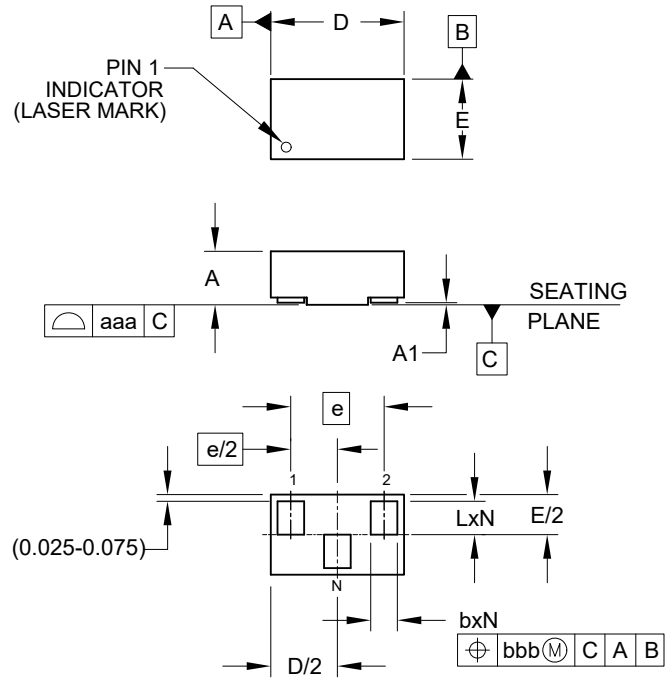


Table 2 - Recommended Assembly Guidelines	
Assembly Parameter	**Recommendation**
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - DFN 1.0 x 0.6 x 0.4mm 3-Lead

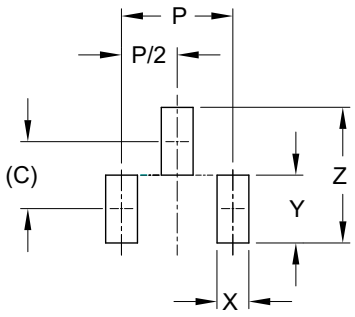


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.35	0.40	0.45
A1	0.00	0.015	0.05
b	0.15	0.20	0.25
D	0.95	1.00	1.075
E	0.55	0.60	0.675
e	0.70 BSC		
L	0.20	0.25	0.30
N	3		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - DFN 1.0 x 0.6 x 0.4mm 3-Lead

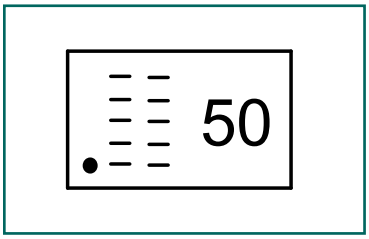


DIMENSIONS	
DIM	MILLIMETERS
C	(0.42)
P	0.70
X	0.20
Y	0.43
Z	0.85

NOTES:

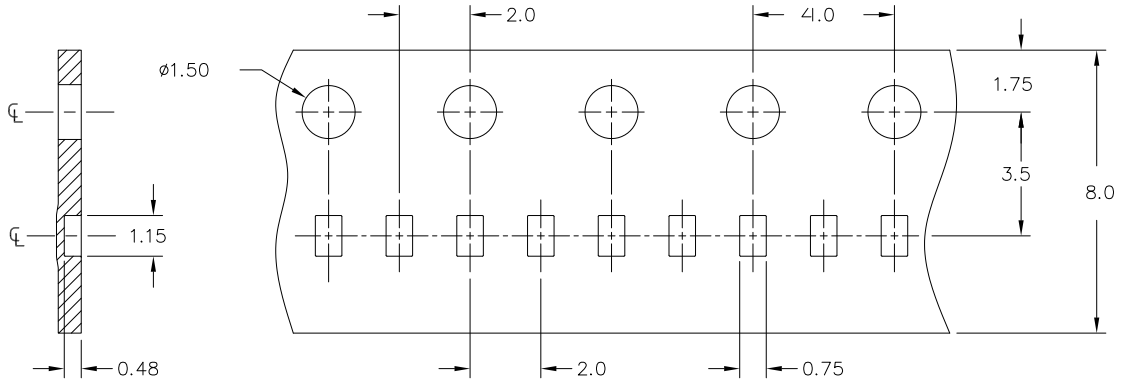
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

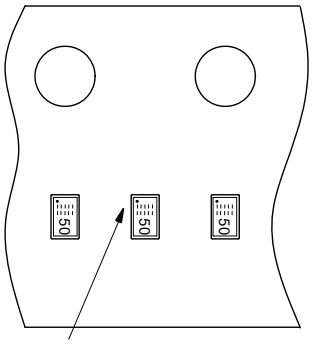


Notes: Marking will also include line matrix date code

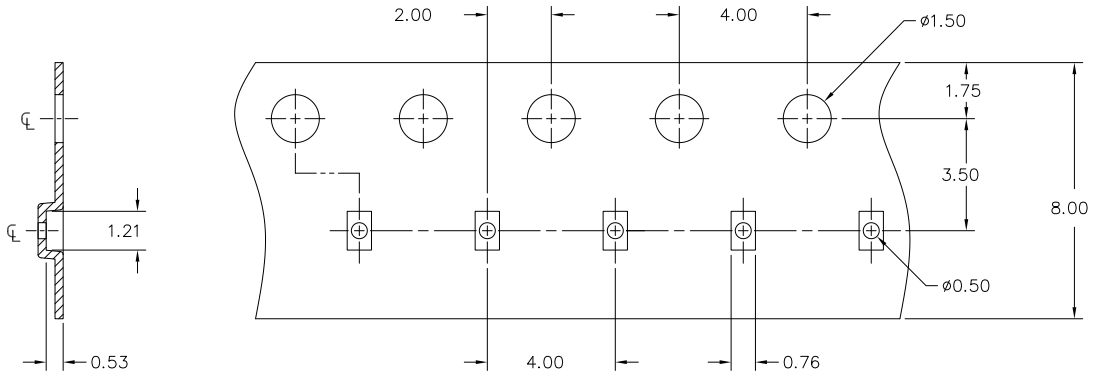
Tape and Reel Specification - Paper Tape, 2mm Pitch



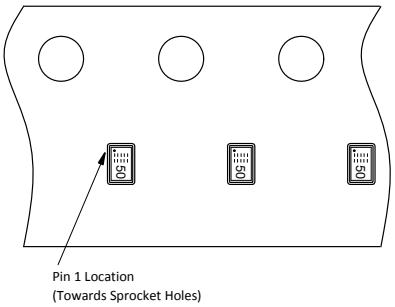
Note: All dimensions are nominal dimensions in mm.



Tape and Reel Specification - Plastic Tape, 4mm Pitch



Note: All dimensions are nominal dimensions in mm.



Ordering Information

Part Number	Qty per Reel	Reel Size	Carrier Tape	Pitch
RClamp0512TQTNT	10000	7 Inch	Paper	2mm
RClamp0512TQTCT	3000	7 Inch	Plastic	4mm
RailClamp and RClamp are registered trademarks of Semtech Corporation.				

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