RClamp10012PQ

2-Line ESD Protection for Automotive Ethernet

PROTECTION PRODUCTS

Description

RClamp®10012PQ is a 2-line interface solution designed specifically for ESD protection of Ethernet interfaces in automotive applications. These devices utilize silicon avalanche technology for superior protection performance compared to ceramic-based solutions. These bidirectional TVS diodes have a trigger voltage >100V and have a deep snap-back characteristic for minimizing ESD clamping voltage. They feature maximum ESD withstand voltage of ±12kV contact, ±17kV air discharge per IEC 61000-4-2. These devices are designed for OPEN Alliance Ethernet interfaces in automotive applications and are qualified to AEC-Q100, Grade 1.

RClamp10012PQ is in a DFN 2.0 x 1.0 x 0.60mm 5-Lead package. Flow-through package design simplifies PCB layout and maintains signal integrity on high-speed lines.

Features

- Transient Protection to
  - IEC 61000-4-2 (ESD) 17kV (Air), 12kV (Contact)
  - IEC 61000-4-4 (EFT) 4kV (5/50ns)
  - IEC 61000-4-5 (Lightning) 3A (8/20µs)
- ESD protection for two high-speed lines
- Package design optimized for easy layout
- TVS Diode Working Voltage: 30V
- TVS Trigger Voltage: >100V
- Solid-State Silicon-Avalanche Technology
- Qualified to AEC-Q100, Grade 1

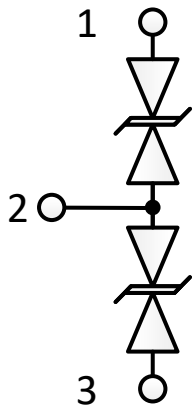
Mechanical Characteristics

- Package 2.0 x 1.0 x 0.60mm 5-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Molding Compound Flammability Rating: UL 94V-0
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

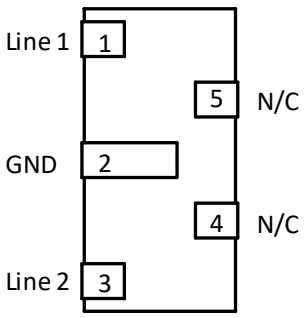
Applications

- OPEN Alliance 100/1000BASE-T1 Ethernet
- Automotive in-vehicle network lines

Circuit Diagram



Pin Configuration



Top View

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20µs)	I_{PP}	3	A
ESD per IEC 61000-4-2 (Contact) (1), (2) ESD per IEC 61000-4-2 (Air) (1), (2)	V_{ESD}	±12 ±17	kV
ESD per ISO-10605 (Contact)(2) (3) ESD per ISO-10605 (Air)(2) (3)	V_{ESD}	±15 ±22	kV
Junction Temperature and Operating Temperature	T_J & T_{OP}	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

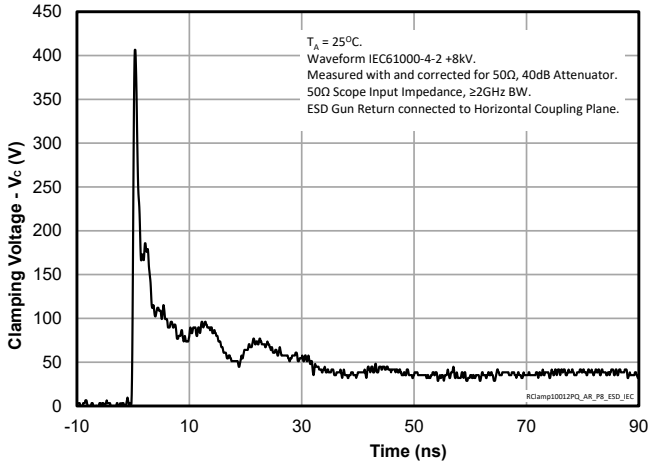
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 125°C, Pin 1 or 3 to Pin 2				30	V
Trigger Voltage	V_{Trig}	Pin 1 or 3 to Pin 2	T = 25°C	110	125	140	V
			-40°C to 125°C	105		150	
Reverse Leakage Current	I_R	V_{RWM} = 30V Pin 1 or 3 to Pin 2	T = 25°C		<1	200	nA
			T = 125°C		5	500	
Clamping Voltage (4)	V_C	I_{PP} = 3A, tp = 1.2/50µs (Voltage), 8/20µs (Current) Combination Waveform			25		V
ESD Clamping Voltage(5)	V_C	tp = 0.2/100ns (TLP), Pin 1 or 3 to Pin 2	I_{TLP} = 4A		30		V
			I_{TLP} = 16A		58		
Dynamic Resistance(5), (6)	R_{DYN}	tp = 0.2/100ns (TLP), Pin 1 or 3 to Pin 2			2.3		Ohms
Capacitance	C_J	V_R = 0V, f = 1MHz, Pin 1 or 3 to Pin 2			1.2	1.4	pF
Capacitance matching	$_{\Delta}C$	C_{Line1} - C_{Line2} , or C_{Line2} - C_{Line1}			0.02	0.1	pF

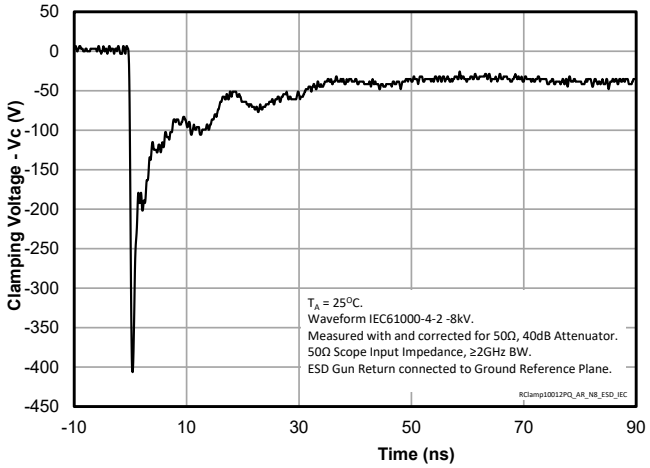
Notes:
(1): ESD Gun return path to Ground Reference Plane (GRP)
(2): ESD pulse applied to Pin 1 or Pin 3
(3): ESD Gun return path to Horizontal Coupling Plane (HCP); Test conditions: 150pF/330pF, 2kΩ
(4): Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, R_S = 42 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
(5): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(6): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

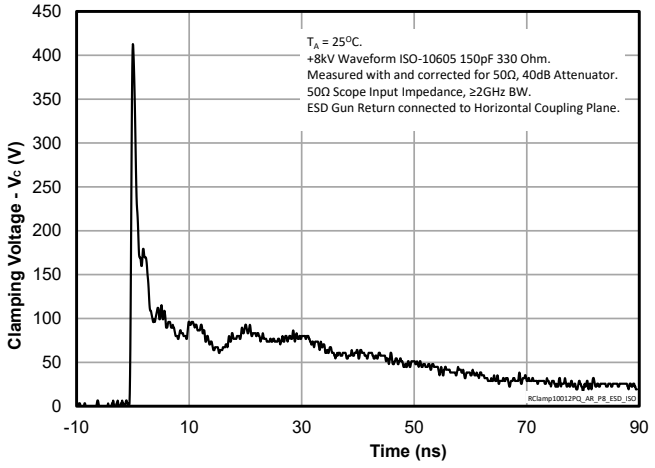
ESD Clamping (+8kV Contact per IEC 61000-4-2)



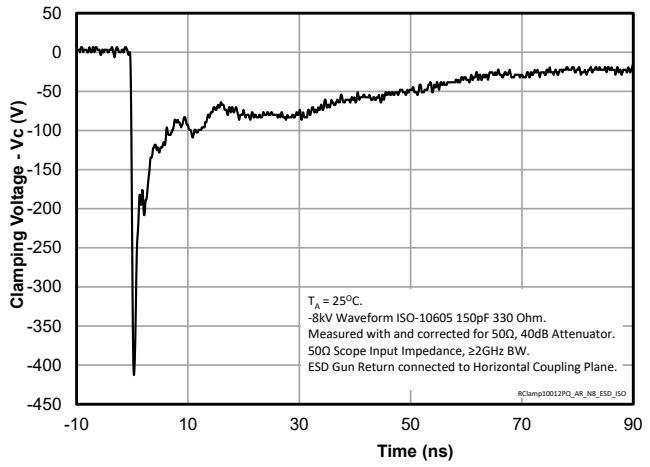
ESD Clamping (-8kV Contact per IEC 61000-4-2)



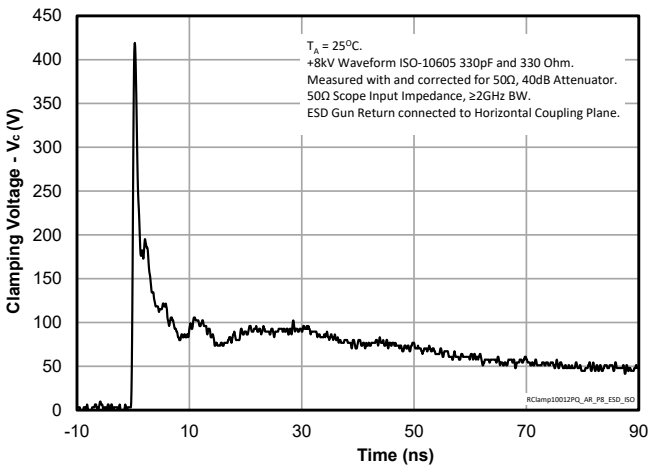
ESD Clamping (+8kV Contact ISO-10605 150pF 330 Ohm)



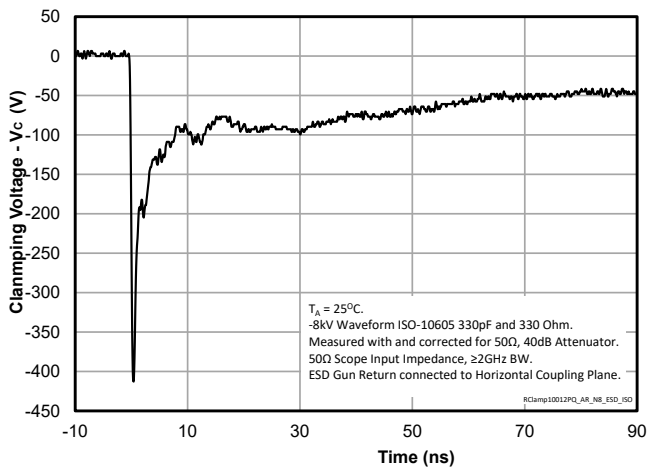
ESD Clamping (-8kV Contact ISO-10605 150pF 330 Ohm)



ESD Clamping (+8kV Contact ISO-10605 330pF 330 Ohm)

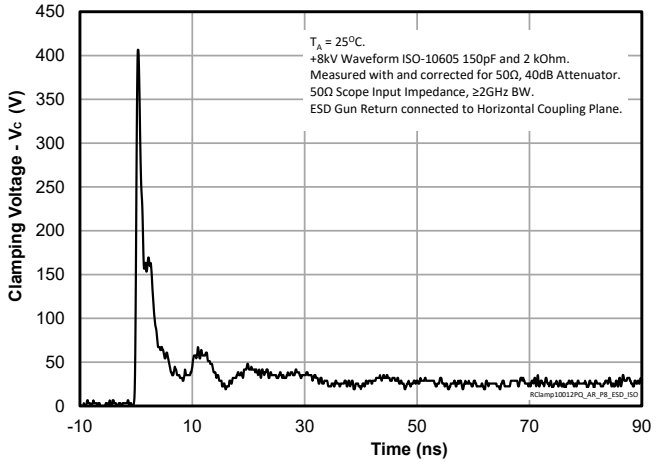


ESD Clamping (-8kV Contact ISO-10605 330pF 330 Ohm)

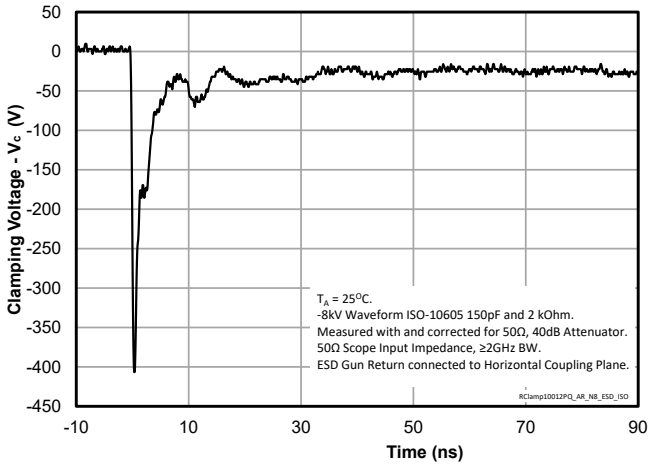


Typical Characteristics

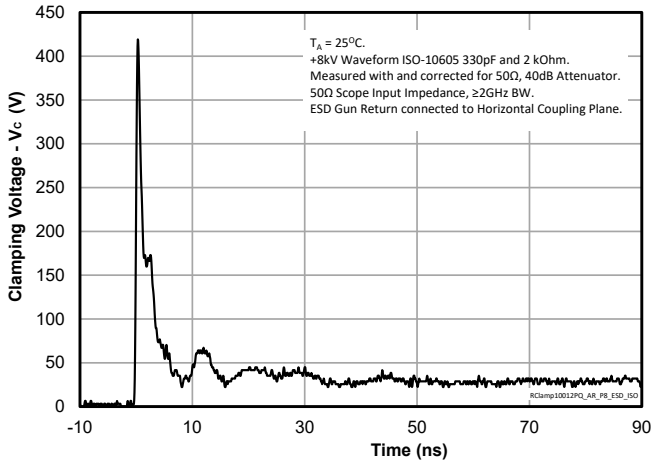
ESD Clamping (+8kV Contact ISO-10605 150pF 2 kOhm)



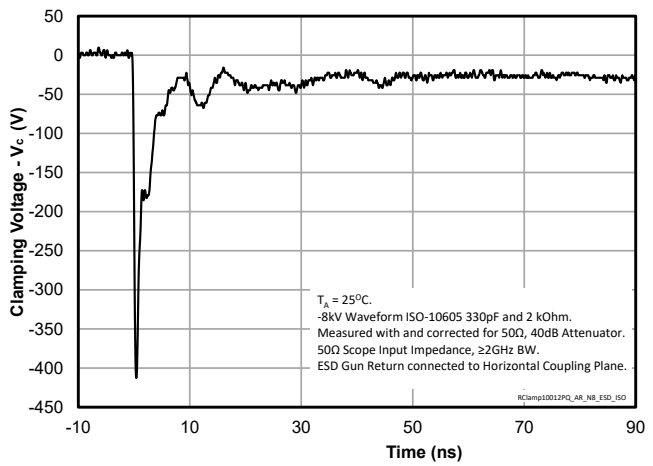
ESD Clamping (-8kV Contact ISO-10605 150pF 2 kOhm)



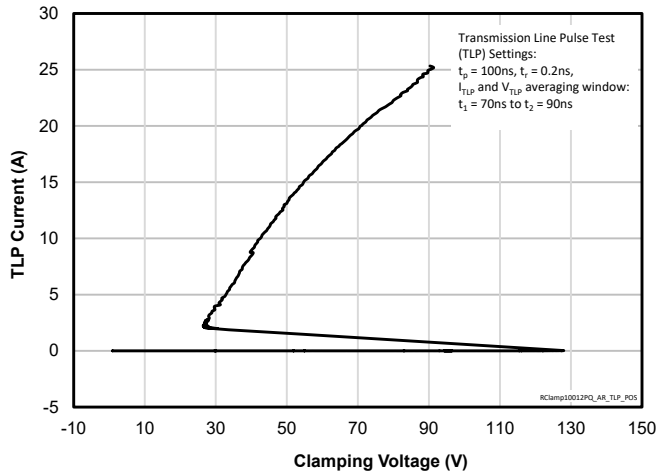
ESD Clamping (+8kV Contact ISO-10605 330pF 2 kOhm)



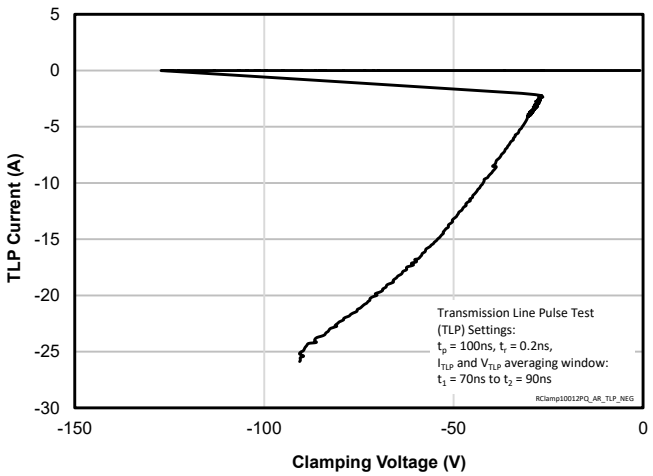
ESD Clamping (-8kV Contact ISO-10605 330pF 2 kOhm)



TLP Characteristic (Positive)

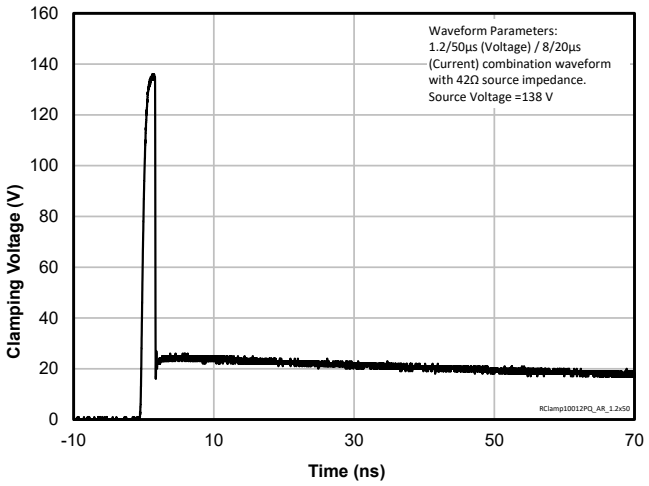


TLP Characteristic (Negative)

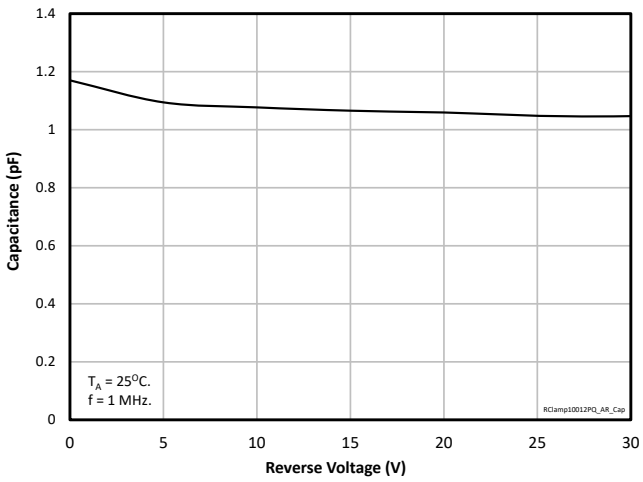


Typical Characteristics

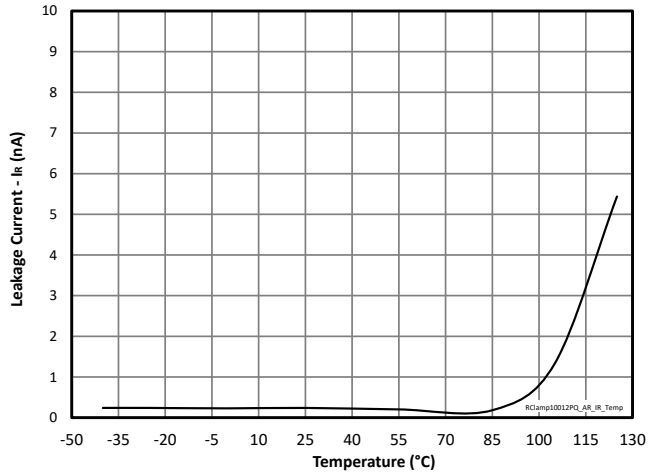
Clamping Characteristic (Ipp = 3A, tp=1.2/50us)



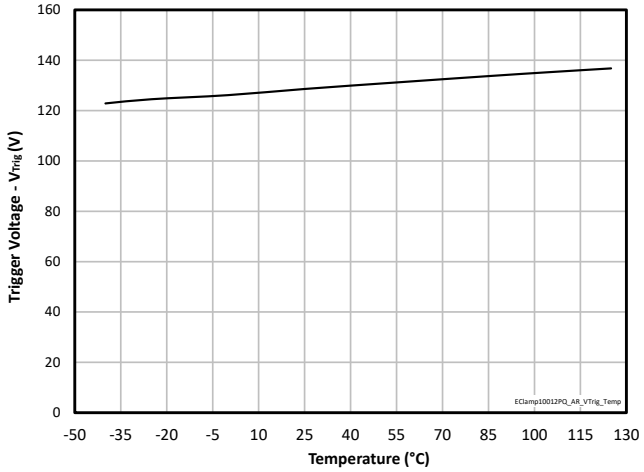
Junction Capacitance vs. Reverse Voltage



Reverse Leakage vs. Temperature

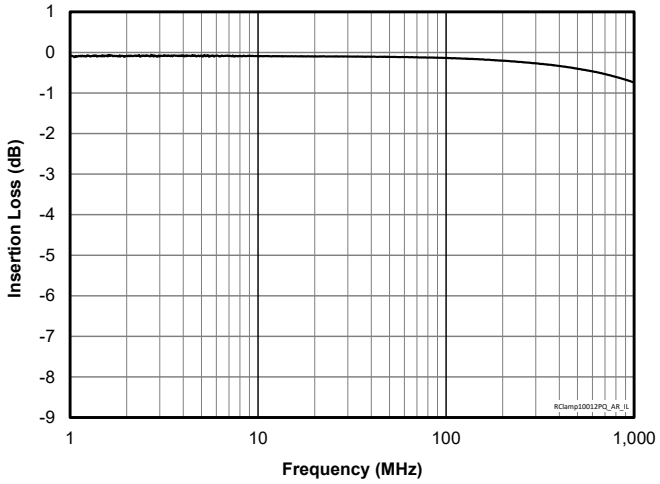


Trigger Voltage (VTrig) vs. Temperature

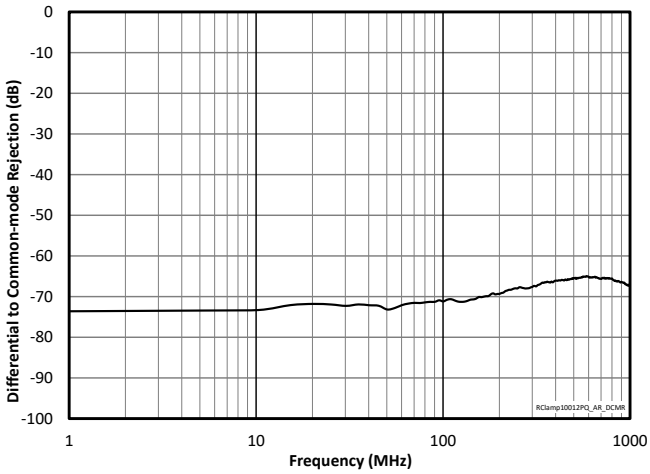


Typical Characteristics

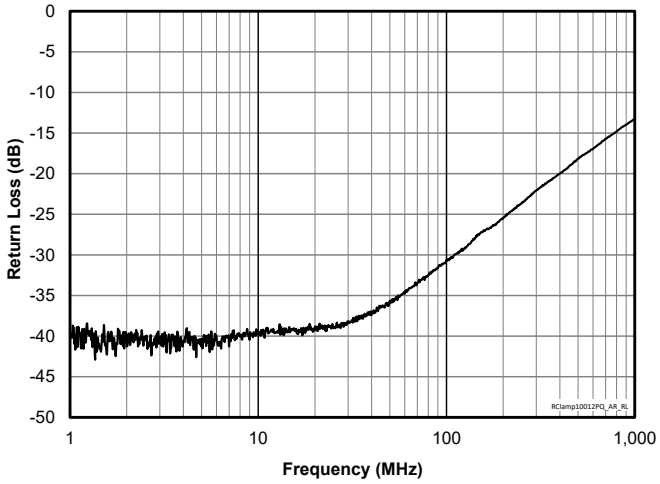
Insertion Loss (S_{DD21})



Differential to Common Mode Rejection (S_{sd21})



Return Loss (S_{DD11})



Application Information

Overview

RClamp10012PQ is an ESD/EOS protection device designed for OPEN Alliance Ethernet interfaces in automotive applications. Each device integrates two TVS diodes with a rated working voltage of 30V and a minimum trigger voltage of 100V. RClamp10012PQ is qualified to AEC-Q100, Grade 1.

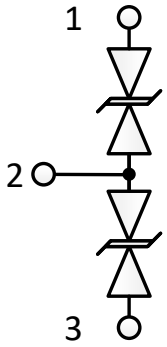


Figure 1 - RClamp10012PQ Schematic Diagram

OPEN Alliance IEEE 100BASE-T1 EMC Test Specification for ESD Suppression Devices

The OPEN Alliance test specification is intended to be a standardized scale for EMC testing of ESD protection devices to be used in 100BASE-T1 Ethernet interfaces in automotive applications. It includes test set up, test procedures, and recommended limits for the following:

- Evaluation of datasheet parameters
- Mixed mode S-Parameter measurement
- ESD Withstand Voltage
- Impact to ESD discharge current in a defined 100BASE-T1 network
- Unwanted clamping effect at RF immunity tests

RClamp10012PQ has been characterized to the ESD and mixed mode insertion loss requirements of the OPEN Alliance IEEE 100BASE-T1 EMC Test Specification for ESD suppression devices. A summary of test results is detailed below. For detailed set up information and test procedures, refer to the OPEN Alliance IEEE 100BASE-T1 EMC Test Specification for ESD suppression devices.

ESD Withstand Voltage

RClamp10012PQ is designed using silicon avalanche technology which yields low TLP dynamic resistance resulting in low ESD clamping voltage. Additionally, there is no inherent wear out mechanism associated with solid-state protection technology; RClamp10012PQ will withstand >1000 discharges as required by the OPEN Alliance test specification without damage or degradation. RClamp10012PQ has a maximum ESD withstand voltage of ±12kV contact, ±17kV air discharge per IEC 61000-4-2.

ESD Discharge Current

Simulating ESD discharge current through a 100BASE-T1 transceiver is defined in the OPEN Alliance specification. A contact ESD discharge of 4kV and 6kV (per IEC 61000-4-2) is applied to an evaluation board with a simulated 100BASE-T1 front end. This includes RClamp10012PQ, common mode choke, and a termination network. ESD current flow is measured into a defined load resistor for each line. Limits are set by the specification for each discharge level. Figures 2 and 3 show test results using RClamp10012PQ. For each discharge level, RClamp10012PQ limits the current flow well below the specification recommendation.

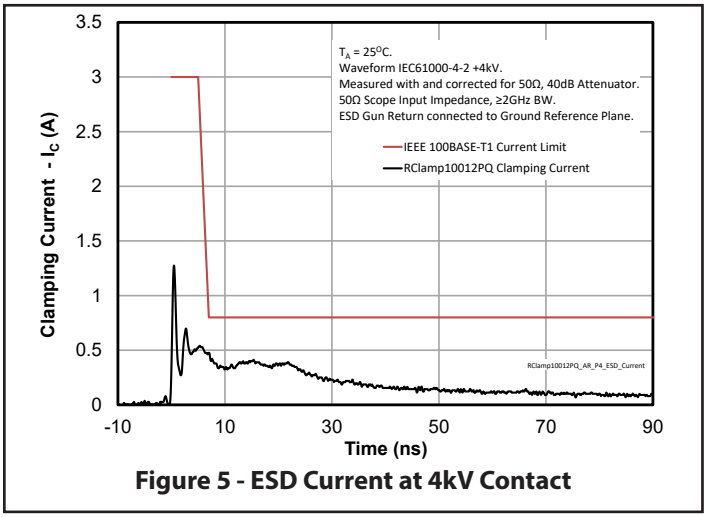


Figure 5 - ESD Current at 4kV Contact

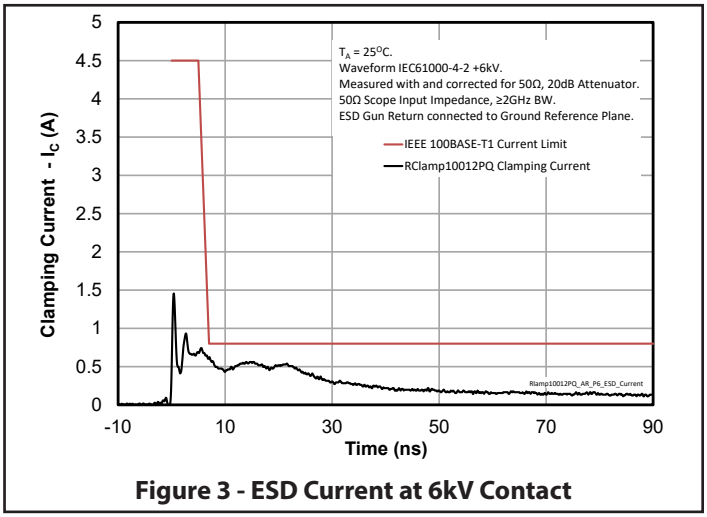


Figure 3 - ESD Current at 6kV Contact

Mixed Mode S-Parameters

RClamp10012PQ is evaluated for mixed mode S-parameters which include Insertion Loss (IL) (SDD21), Return Loss (RL) (SDD11), and Differential to Common Mode Rejection (DCMR) (Ssd21). After the initial measurements, the device is subjected to 20 ESD discharges of ±8kV on each signal pin per ISO-10605 (C=150pF, R=330Ω). Results are shown in Figures 4 – 6 below. In each case, RClamp10012PQ results safely meet the recommended limits of the OPEN Alliance test specification.

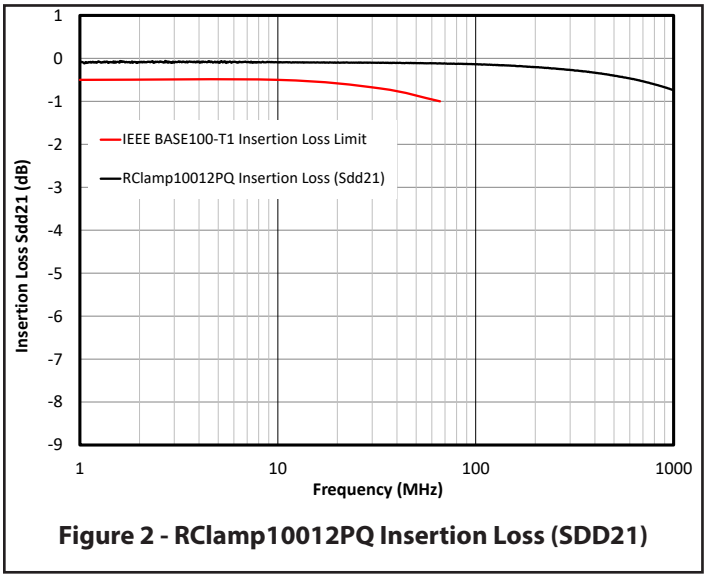


Figure 2 - RClamp10012PQ Insertion Loss (SDD21)

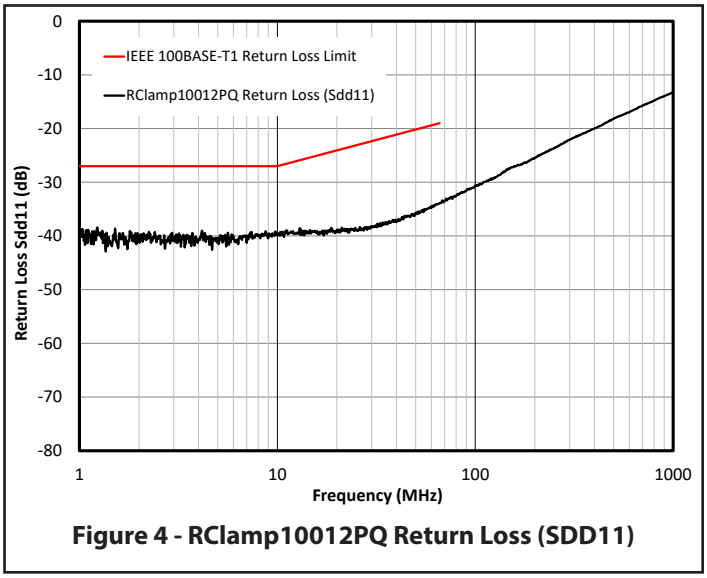


Figure 4 - RClamp10012PQ Return Loss (SDD11)

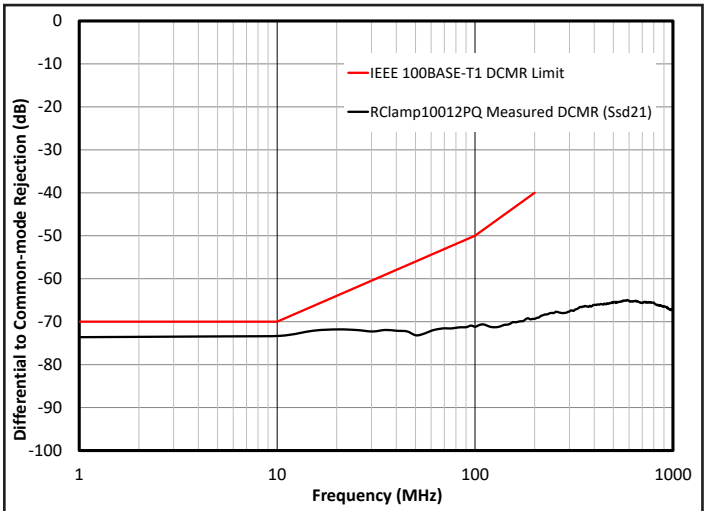


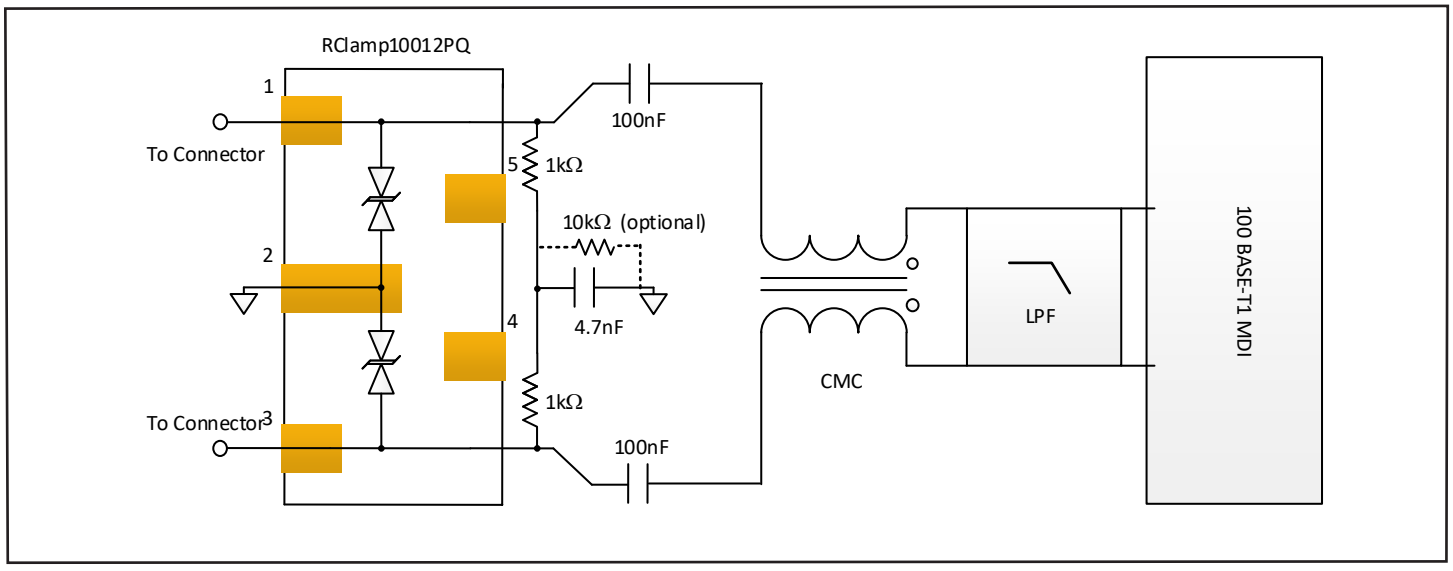
Figure 6 - Differential to Common Mode Rejection (Ssd21)

RF Clamping

An RF clamping test is defined in the OPEN Alliance specification to ensure the TVS device does not affect the EMC performance of the complete module. RClamp10012PQ is evaluated for unwanted RF clamping using a network analyzer in conjunction with a specified RF amplifier, RF attenuator, and device test fixture. The test fixture includes RClamp10012PQ and a common mode choke designed for 100BASE-T1 applications. RClamp10012PQ was evaluated for Class I (33dBm), Class II (36dBm), and Class III (39dBm). RClamp10012PQ does not exhibit an RF clamping effect up to 39dBm (Class III).

Device Connection and Layout Guidelines

A typical 100BASE-T1 protection example using RClamp10012PQ is shown in Figure 7. Signal lines enter at pins 1 and 3 and connect to external coupling capacitors in series with a common mode choke. A bidirectional TVS (ESD protection diode) is connected between each line and pin 2. Pin 2 is connected to ground. The capacitance of each TVS diode to ground is limited to 1.4pF to ensure signal integrity. Termination resistors matched to 1% are connected between pins 1 and pins 3. The resistors are connected to ground via a capacitor (a parallel 10kΩ resistor is optional). It is recommended that the capacitor have a minimum voltage rating of 100V. The internal TVS diodes will protect the capacitors from damage during an ESD event.



Layout Guidelines

Placement of the protection component is a critical element for effective ESD suppression. RClamp10012PQ should be placed before the CM choke and as close to the connector as possible. Placing the protection device close to the connector minimizes transient coupling into nearby traces. Ground connections should be made directly to the ground plane using micro-vias. This reduces parasitic inductance in the ground path and minimizes the clamping voltage seen by the protected device.

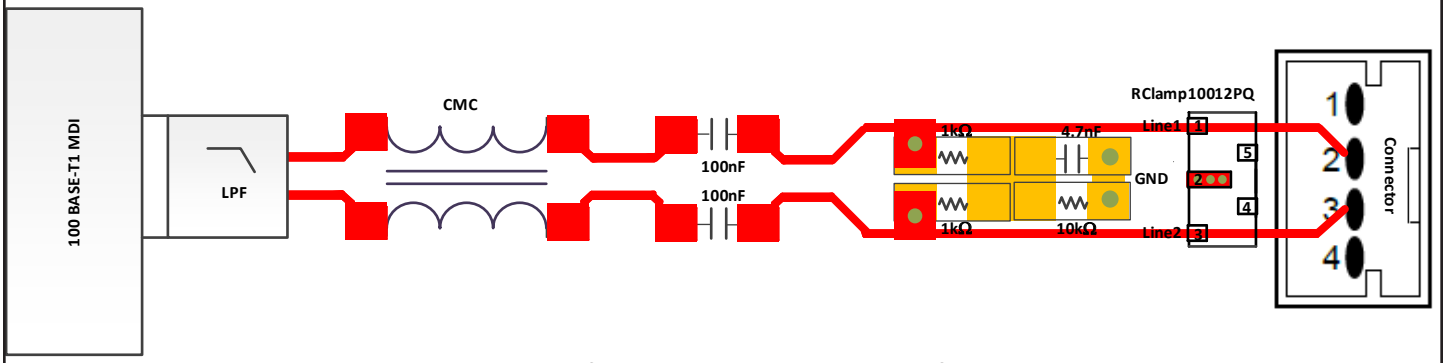


Figure 7 - Layout Example of RClamp10012PQ Protection for 100 BASE-T1 MDT.
Placement of 1.05KΩ Resistors, 10KΩ Resistor and 4.7nF Cap is on Bottom (Yellow) Layer

MDI interface

Figures 7 and 8 shows the layout examples of MDI circuitry which will be used for each PHY port. The common mode termination depends on OEM requirements and might vary for different OEMs. The common mode choke is expected to be compliant to the OPEN Alliance CMC specification. The 100nF coupling capacitors should have maximum 10% tolerance and ≥100V voltage range. For the 10kΩ resistor and 4.7nF capacitor, there is no specific power rating required, but components should be rated for a minimum of 50V.

The differential signal pair TRX_P/TRX_M shall be routed close together with a controlled impedance of 100Ohm. Since the symmetry is critical for the EMC performance, keep both traces of the differential pair as identical as possible. To increase the effectiveness of the choke or transformer for higher frequencies and to minimize parasitic capacitances, a cut-out of the ground plane may be placed beneath the differential signal path from the PHY to the connector. The choke shall be placed close to the PHY.

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 2. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended. Assuming a 100um thick stencil, the aperture dimensions shown will yield an area ratio of approximately 0.75.

Recommended Mounting Pattern

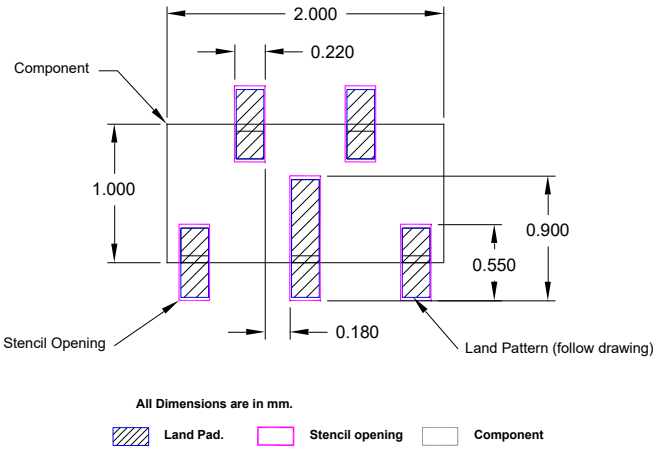
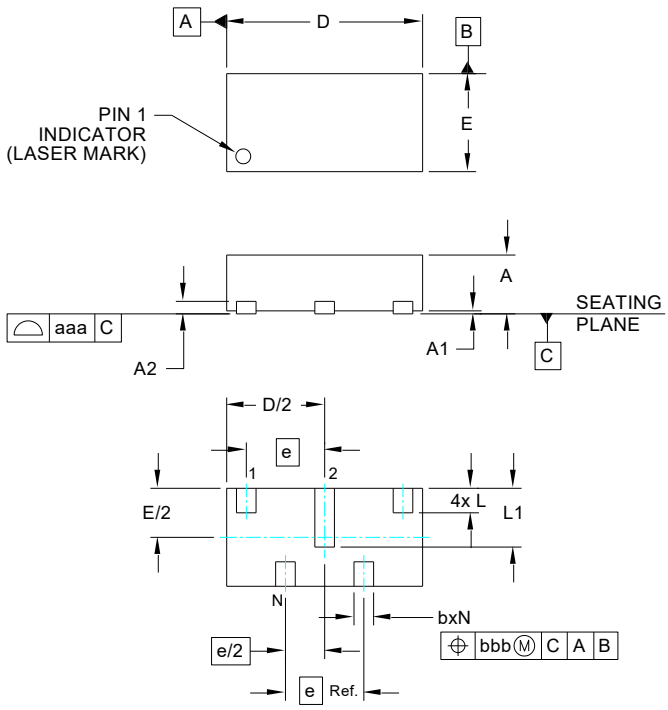


Table 2 - Recommended Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - DFN 2.0 x 1.0 x 0.60mm 5-Lead

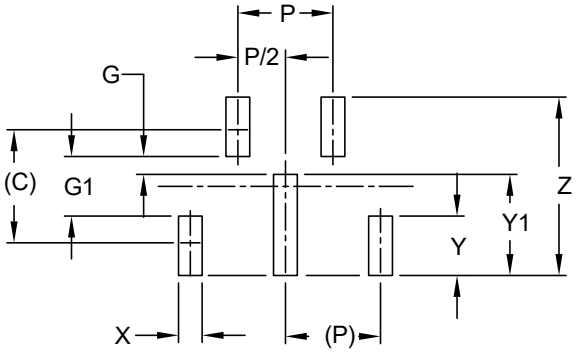


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.55	0.60	0.65
A1	0.00	0.03	0.05
A2		(0.127)	
b	0.15	0.20	0.25
D	1.95	2.00	2.05
E	0.95	1.00	1.05
e		0.80 BSC	
L	0.20	0.25	0.30
L1	0.55	0.60	0.65
N		5	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - DFN 2.0 x 1.0 x 0.60mm 5-Lead

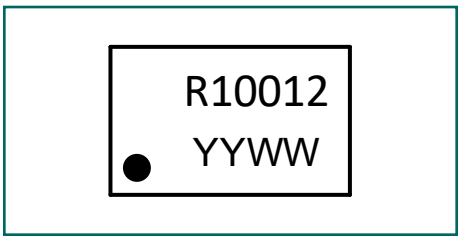


DIMENSIONS	
DIM	MILLIMETERS
C	(0.95)
G	0.15
G1	0.50
P	0.80
X	0.20
Y	0.50
Y1	0.85
Z	1.50

NOTES:

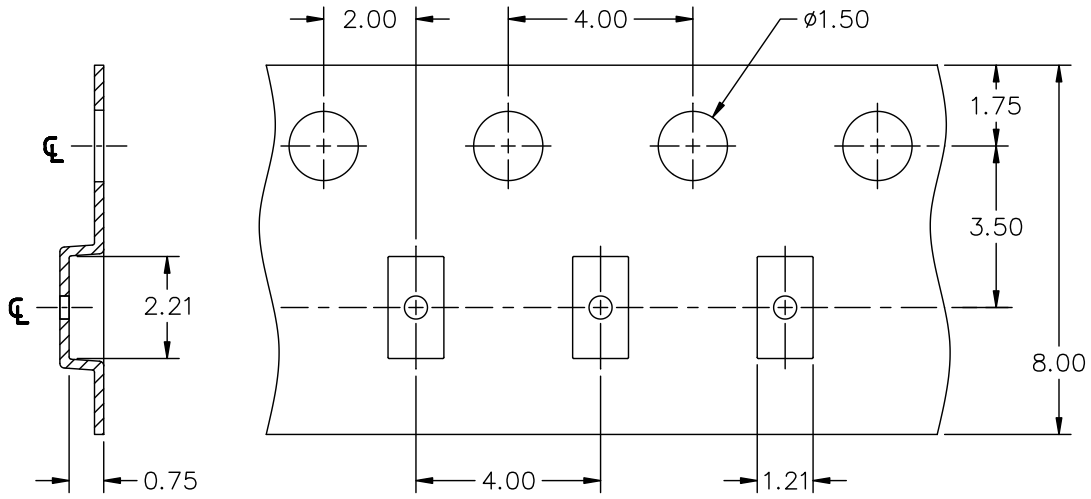
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

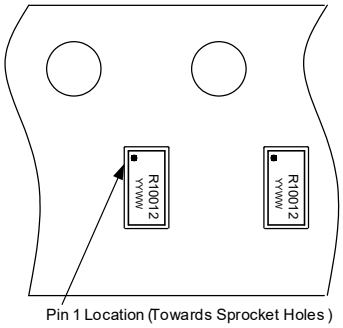


YYWW = Alphanumeric character Date Code

Tape and Reel Specification



Note: All dimensions are nominal dimensions in mm.



Ordering Information

Part Number	Qty per Reel	Reel Size	Carrier Tape	Pitch
RClamp10012PQTCT	3000	7 Inch	Plastic	4mm
RailClamp and RClamp are trademarks of Semtech Corporation.				

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