

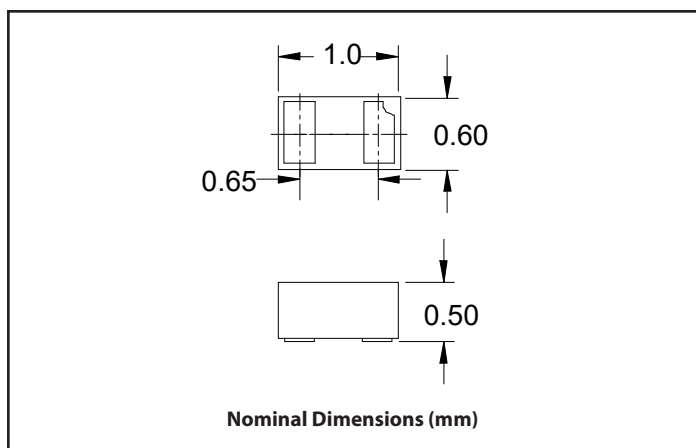
## PROTECTION PRODUCTS

### Description

RClamp®3361P is an ultra low capacitance ESD protection device specifically designed to protect high-speed Ethernet lines. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation. The device features high surge capability of 7A ( $t_p = 8/20 \mu s$ ). ESD characteristics are highlighted by low peak ESD clamping voltage, and high ESD withstand voltage ( $\pm 12kV$  contact per IEC 61000-4-2). RClamp3361P has a typical capacitance of 0.2pF ideal for high speed lines. Each device will protect one high-speed data line operating up to 3.3 volts.

RClamp3361P is in a 2-pin SLP1006P2 package. It measures 1.0 x 0.6 mm with a nominal height of 0.5mm. The leads are finished with lead-free NiPdAu. This ultra small package design simplifies PCB layout and facilitates matching trace lengths for consistent impedance between high speed differential lines. The combination of small size, low capacitance, and high ESD surge capability makes them ideal for use in industrial and consumer applications.

### Package Dimension



### Features

- ESD withstand voltage:  $\pm 15kV$  (air),  $\pm 12kV$  (contact) per IEC 61000-4-2
- High Surge Capability: 7A ( $t_p = 8/20 \mu s$ ,  $R_s = 2\Omega$ ) per IEC 61000-4-5
- Ultra-Low capacitance: 0.2pF Typical
- Protects one high-speed data line
- Working voltage:  $\pm 3.3V$
- Low reverse leakage current: 50nA max at  $V_R = 3.3V$
- Low Insertion Loss: 0.39dB (Typical) at 5GHz
- Large operating bandwidth: 11.3 GHz
- Solid-state silicon-avalanche technology

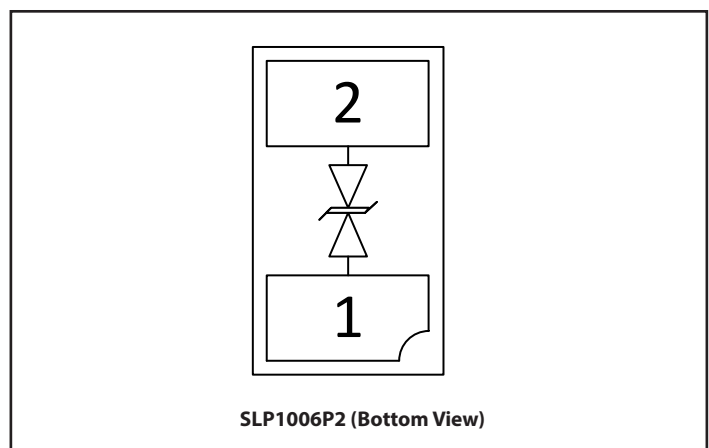
### Mechanical Characteristics

- SLP1006P2 package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 1.0 x 0.6 x 0.5 mm
- Lead Finish: NiPdAu
- Marking: Marking code
- Packaging: Tape and Reel

### Applications

- 2.5G/5G/10GbE
- USB 3.0 and USB 3.1
- Thunderbolt
- HD-SDI

### Schematic & Pin Configuration



## Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P <sub>PK</sub>	60	W
Peak Pulse Current (tp = 8/20μs)	I <sub>PP</sub>	7	A
ESD per IEC 61000-4-2 (Air) <sup>(1)</sup> ESD per IEC 61000-4-2 (Contact) <sup>(1)</sup>	V <sub>ESD</sub>	±15 ±12	kV
Operating Temperature	T <sub>J</sub>	-40 to +85	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

## Electrical Characteristics (T=25°C unless otherwise specified)

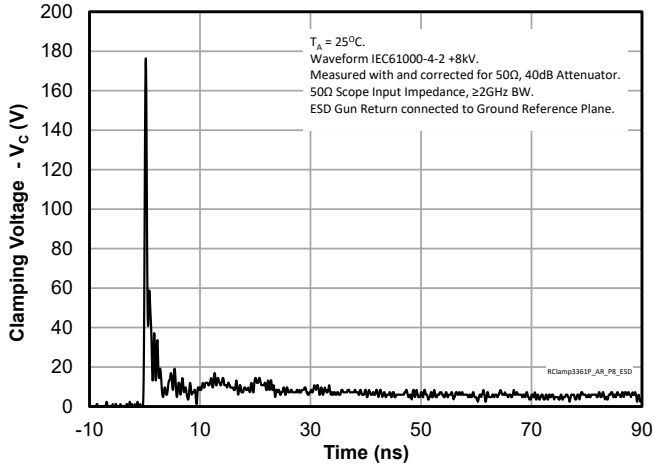
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	T = -40 °C to +125 °C, Pin 1 to 2 or 2 to 1			3.3	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>BR</sub> = 1 mA T = -40°C to 85°C	5.5	7.7	9	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 3.3V	T = 25°C	<1	50	nA
			T = 85°C	<1	150	
Clamping Voltage <sup>2</sup>	V <sub>C</sub>	I <sub>PP</sub> = 7A, tp = 1.2/50 μs (Voltage), 8/20 μs (Current) Combination Waveform		6.5	8.5	V
ESD Clamping Voltage <sup>3</sup>	V <sub>C</sub>	tp = 0.2/100ns (TLP)	I <sub>TLP</sub> = 4A	4.3		V
			I <sub>TLP</sub> = 16A	8.7		
Dynamic Resistance <sup>3,4</sup>	R <sub>DYN</sub>	tp = 0.2/100ns		0.37		Ω
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0V, f = 1MHz		0.2	0.25	pF
Cutoff Frequency	F <sub>C</sub>	-3dB		11.3		Ghz

Notes:

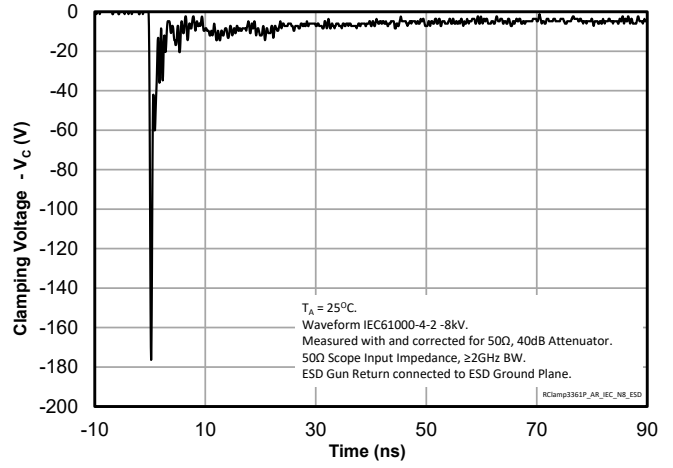
- 1) ESD gun return path connected to ESD ground plane
- 2) Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, R<sub>s</sub> = 2 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
- 3) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I<sub>TLP</sub> and V<sub>TLP</sub> averaging window: t1 = 70ns to t2 = 90ns.
- 4) Dynamic resistance calculated from I<sub>TLP</sub> = 4A to I<sub>TLP</sub> = 16A

# Typical Characteristics

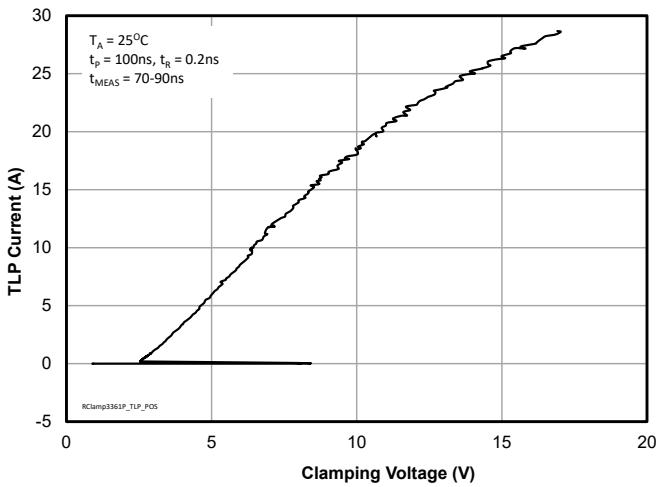
**ESD Clamping (+8kV Contact per IEC 61000-4-2)**



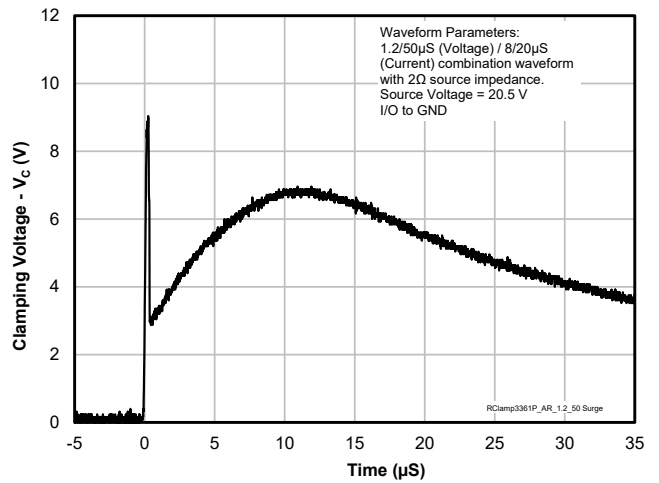
**ESD Clamping (-8kV Contact per IEC 61000-4-2)**



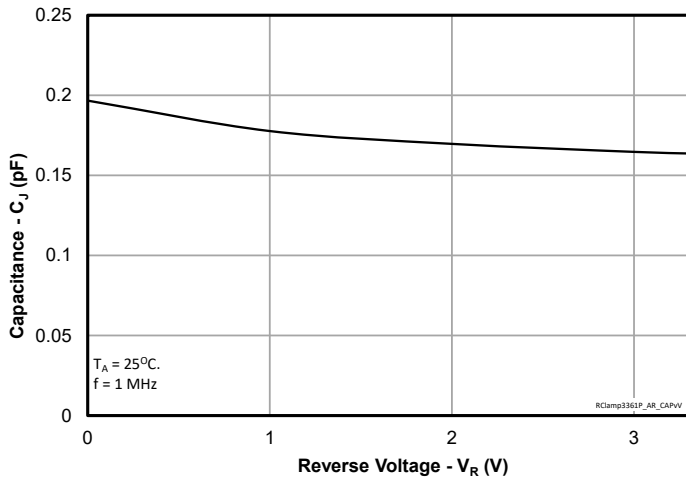
**TLP Characteristic (Positive Pulse)**



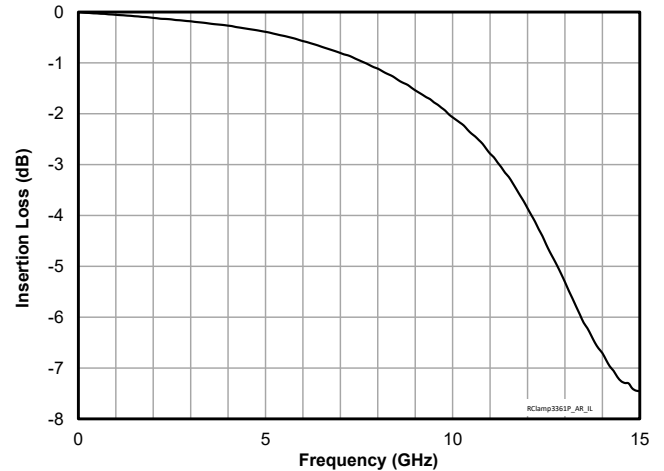
**Clamping Characteristic (7A, Combination Waveform)**



**Capacitance vs. Reverse Voltage**



**Insertion Loss - S21**



# Application Information

## Ethernet Protection

Ethernet ports are exposed to external transient events in the form of ESD, EFT, lightning, and cable discharge events (CDE). Test standards that model these events include IEC 61000-4-2 for ESD, IEC 61000-4-4 for EFT, and IEC 61000-4-5 and GR-1089 for lightning. Any of these events can cause catastrophic damage to the PHY IC.

When designing Ethernet protection, the entire system must be considered. Over-voltage events can be common mode (with respect to ground) or differential (line-to-line). An Ethernet port includes interface magnetics consisting of transformers integrated with common mode chokes. The transformer center taps are connected to ground via an RC network or “Bob Smith” termination. The purpose of this termination is to reduce common mode emissions. Note that components in the RC network should be chosen with a large enough current and voltage ratings to withstand ESD and EOS events.

The transformer provides common mode isolation to transient events, but no protection for differential surges. During a differential transient event current will flow through the transformer charging the windings on the line side. Energy is transferred to the secondary until the surge subsides or the transformer saturates.

A typical protection scheme which utilizes RClamp3361P is shown in Figure 1. Four RClamp3361P devices are located on the PHY side of the transformer. Each device will protect one line pair. When connected in this configuration the devices can protect the PHY IC from a 500V surge ( $t_p = 1.2/50\mu s$ ,  $R_s = 42\Omega$ ). Placing the protection on the PHY side of the magnetics is advantageous in that the magnitude and duration of the surge is attenuated by the transformer windings. The amount of attenuation will vary by vendor and configuration of the magnetics. The Ethernet transformer must be able to support the impulse tests without failure. A typical Ethernet transformer can withstand a few hundred amperes ( $t_p=8/20\mu s$ ) before failure occurs, but this needs to be verified by testing.

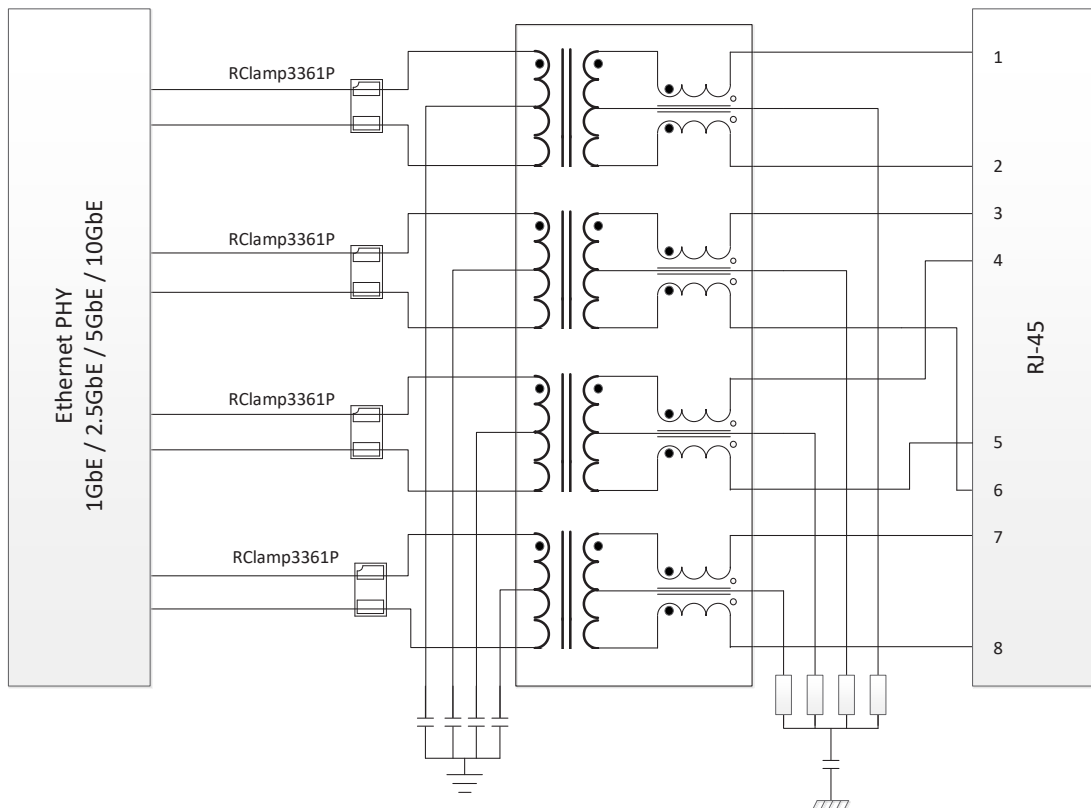


Figure 1 - Ethernet Protection Circuit

# Application Information

## Device Placement and Layout

Placement of the protection component is a critical element for effective transient voltage suppression. Parasitic inductance in the protection path should be minimized by locating RClamp3361P as physically close to the magnetics as possible, and preferably on the same side of the PCB. Traces can be routed straight through the device from the PHY to the magnetics, as shown in Figure 2.

Reducing parasitic inductance is especially important for suppressing fast rise time transients such as ESD and EFT. Inductance in the path of the protection device increases the peak clamping voltage seen by the protected device ( $V = L di/dt$ ). For example, 1nH of inductance can increase the peak clamping voltage by 30V for a 30A (8kV) ESD pulse with a 1ns rise time.

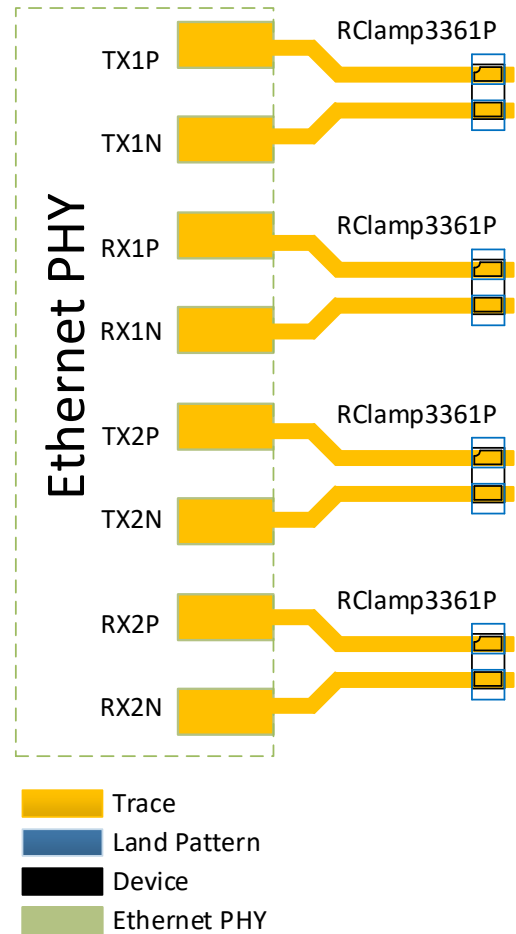
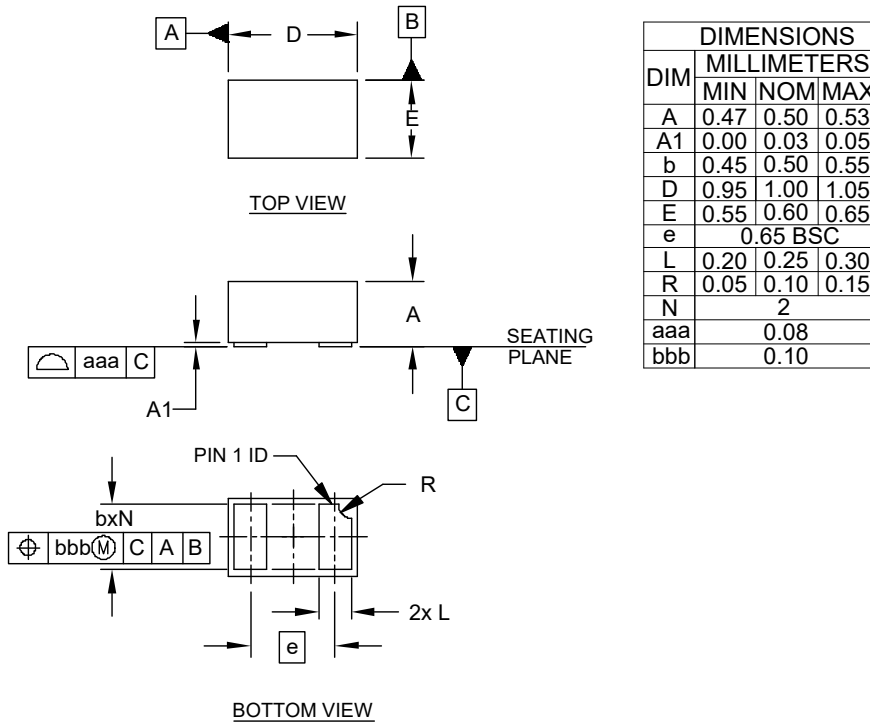


Figure 2 - Four Device Layout Example

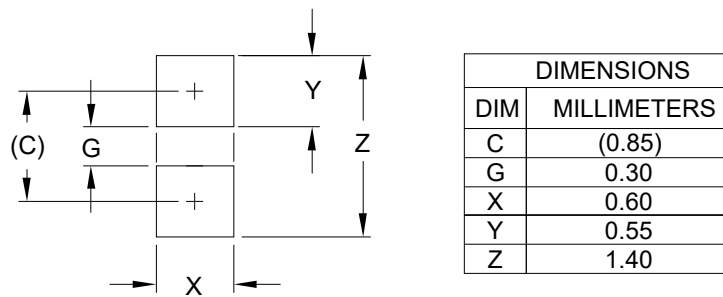
## Outline Drawing - SLP1006P2



**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

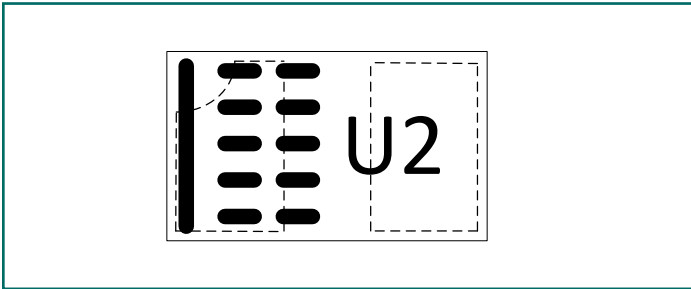
## Land Pattern - SLP1006P2



**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

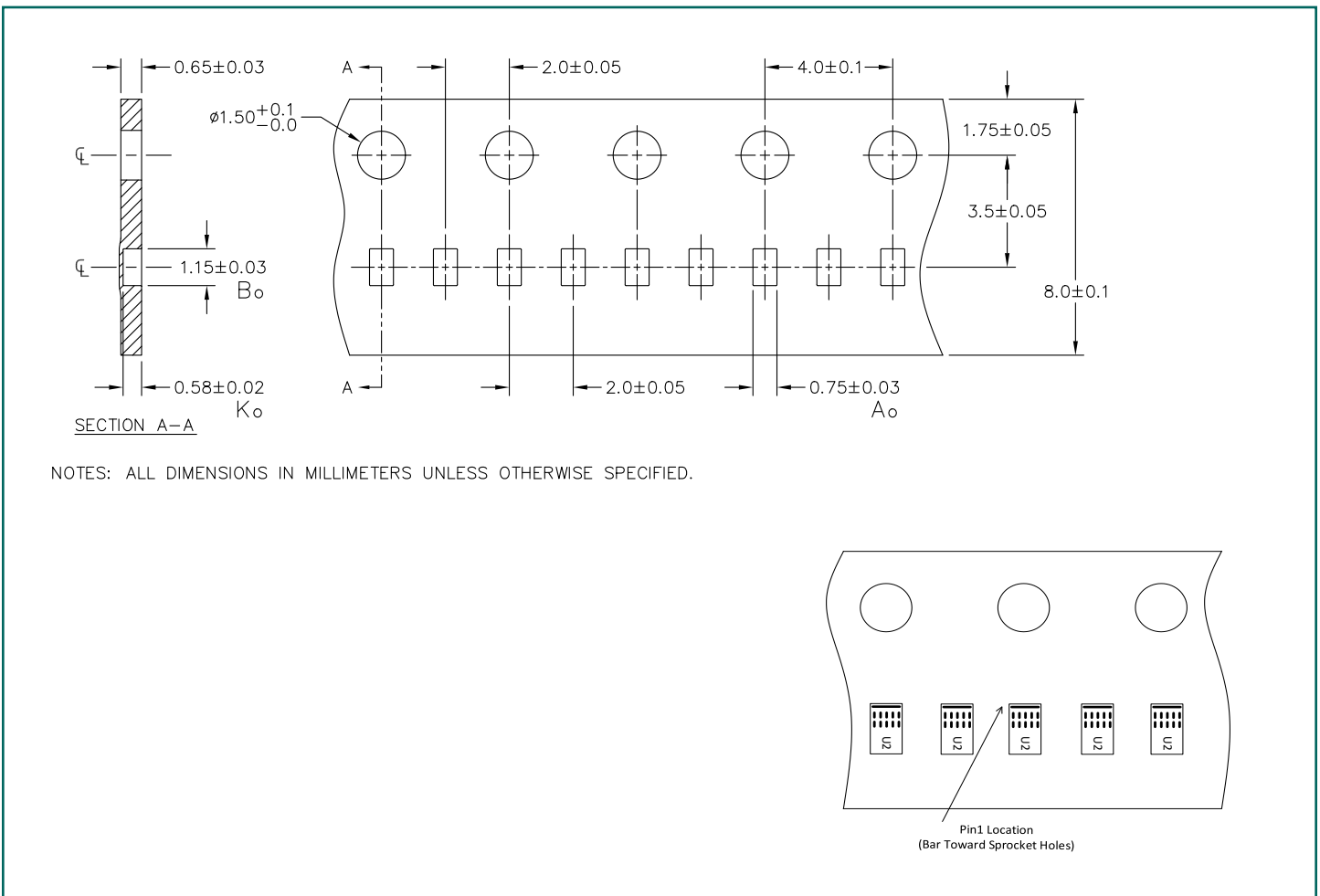
# Marking



**Notes:**

- 1. Device is electrically symmetrical.
- 2. Marking will also include line matrix date code.
- 3. Bar indicates Pin 1 location

## Tape and Reel Specification



## Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp3361P.TFT	15,000	7"
RClamp is trademark of Semtech Corporation.		



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