RClamp3382P

Low Capacitance RailClamp® 2-Line Surge and ESD Protection for Ethernet Interfaces

PROTECTION PRODUCTS

Description

RClamp®3382P is a high performance TVS array designed to protect 2 differential lines from overvoltage events caused by ESD, lightning, CDE (Cable Discharge Events) and EFT (electrical fast transients). RClamp3382P features high surge current capability and may be used to protect Ethernet interfaces in MagJacks, communications equipment, security cameras, and industrial equipment.

RClamp3382P integrates low capacitance, surge-rated steering diodes with a high power transient voltage suppressor (TVS). The TVS utilizes snap-back or "crow-bar" technology to minimize device clamping voltage and features high surge current capability of 10A (tp=8/20us). ESD characteristics are highlighted by high ESD withstand voltage (+/-25kV per IEC 61000-4-2) and extremely low dynamic resistance. Each device will protect two lines operating at 3.3 volts.

RClamp3382P is in a 6-pin SGP1610N4 package measuring 1.6 x 1.0mm with a nominal height of 0.50mm. Flow- through package design simplifies PCB layout and maintains signal integrity on high-speed lines. The combination of low clamping, high surge capability, and innovative package design enables this device to provide the highest level of transient protection.

Features

- Transient Protection to
  - IEC 61000-4-2 (ESD) 25kV (Air), 25kV (Contact)
  - IEC 61000-4-4 (EFT) 4kV (5/50ns)
  - IEC 61000-4-5 (Lightning) 10A (8/20µs)
- Very Small PCB Area
- Protects Two High-Speed Data Lines
- Working Voltage: 3.3V
- Low Capacitance: 0.25pF Typical
- Dynamic Resistance: 0.60 Ohms (Typ)
- Solid-State Silicon-Avalanche Technology

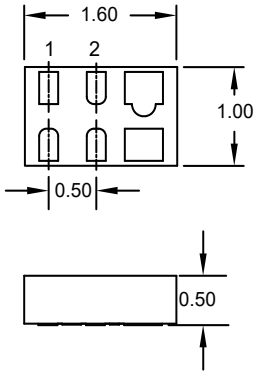
Mechanical Characteristics

- SGP1610N4 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 1.6 x 1.0 x 0.50 mm
- Lead Finish: NiPdAu
- Molding Compound Flammability Rating: UL 94V-0
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

Applications

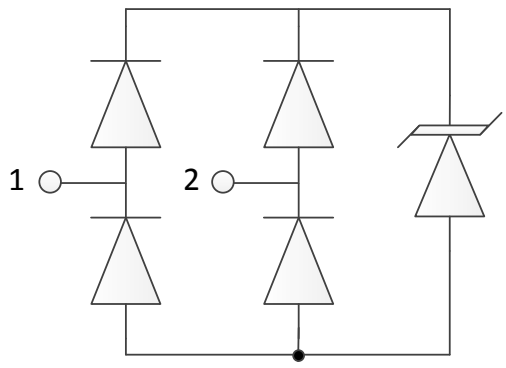
- 1G/2.5G/5G/10G Ethernet
- Integrated Magnetics / RJ-45 Connectors
- Central Office Equipment
- Industrial Equipment
- IP Camera

Nominal Dimensions



Nominal Dimensions (mm)

Functional Schematic



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	200	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	10	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(1)	V_{ESD}	±25 ±25	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

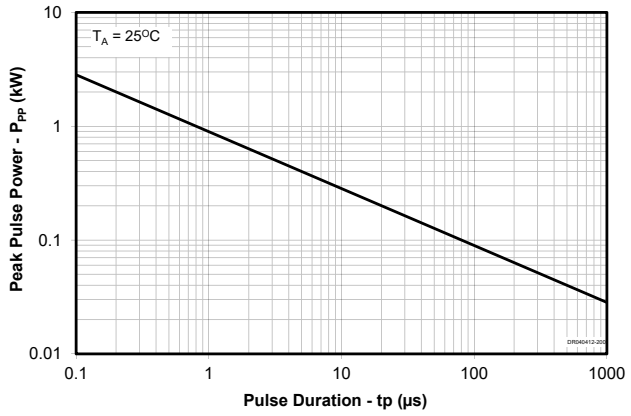
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 125°C Pin 1 to Pin 2				3.3	V
Reverse Breakdown Voltage	V_{BR}	I_t = 10uA Pin 1 to Pin 2		6.5	10.2	12	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V Pin 1 to Pin 2	T = 25°C		0.01	0.050	µA
			T = 125°C		0.03	0.100	µA
Clamping Voltage(2)	V_C	I_{PP} = 10A, tp = 8/20µs, Pin 1 to Pin 2			18.5	20	V
ESD Clamping Voltage(3)	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP) Pin 1 to Pin 2			9.7		V
ESD Clamping Voltage(3)	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP) Pin 1 to Pin 2			17		V
Dynamic Resistance(3), (4)	R_{DYN}	tp = 0.2/100ns (TLP) Pin 1 to Pin 2			0.60		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz Pin 1 to Pin 2	T = 25°C		0.25	0.35	pF

Notes:
(1): ESD Gun return path to Ground Reference Plane (GRP)

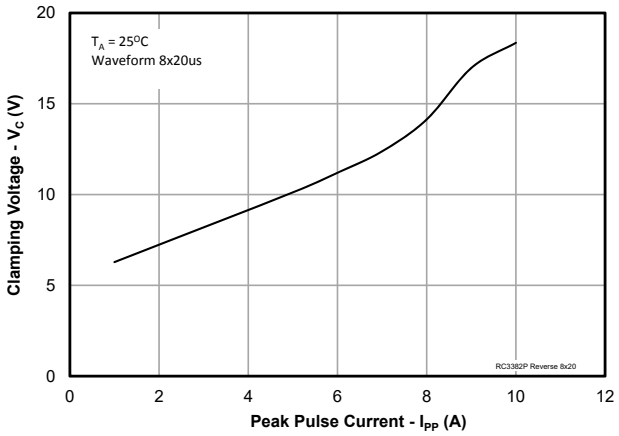
(2): Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, R_S = 2 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
(3): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(4): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

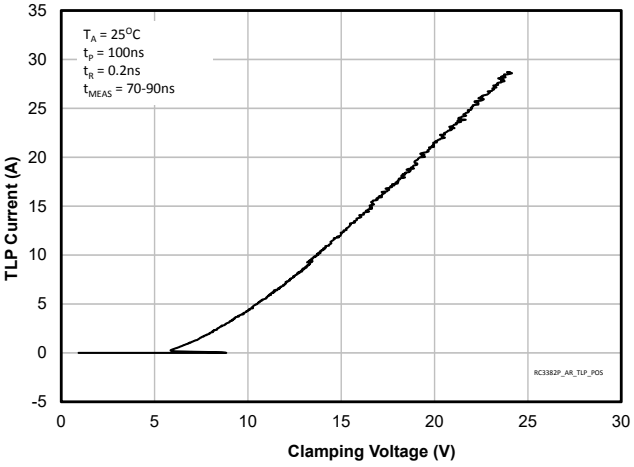
Non-Repetitive Peak Pulse Power vs. Pulse Time



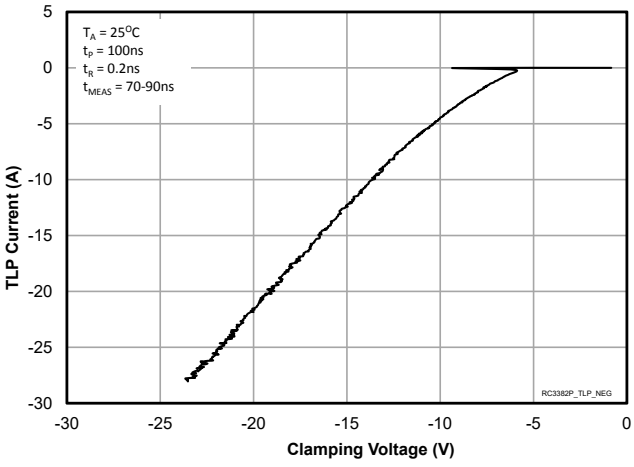
Clamping Voltage vs. Peak Pulse Current (8/20us Pulse)



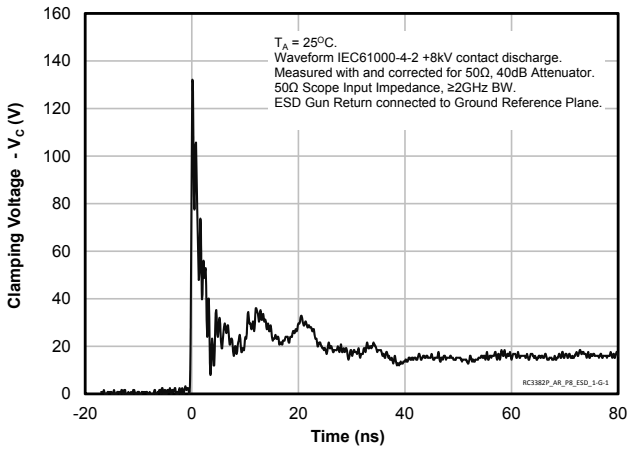
TLP IV Curve (Positive Pulse)



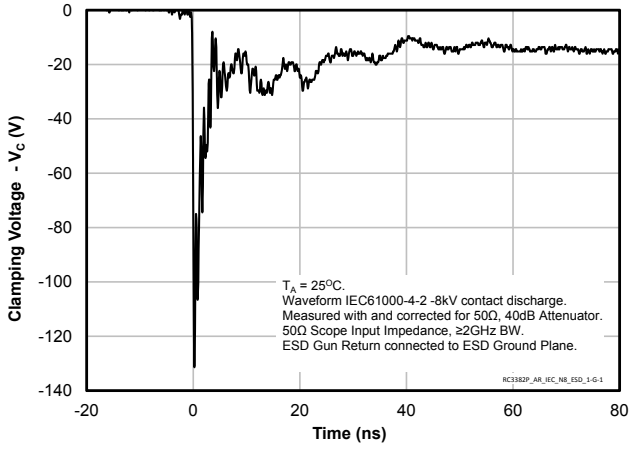
TLP IV Curve (Negative Pulse)



ESD Clamping (+8kV Contact per IEC 61000-4-2)

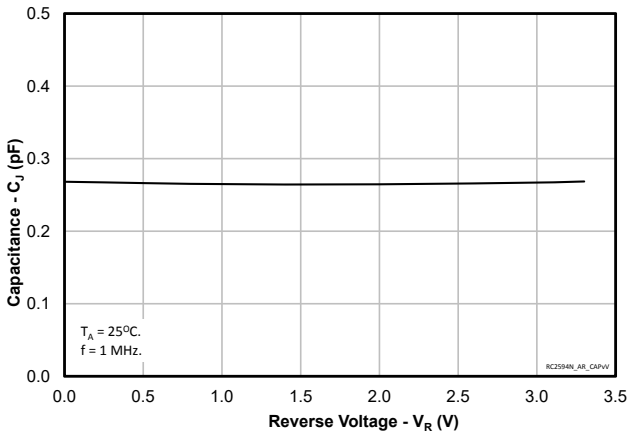


ESD Clamping (-8kV Contact per IEC 61000-4-2)

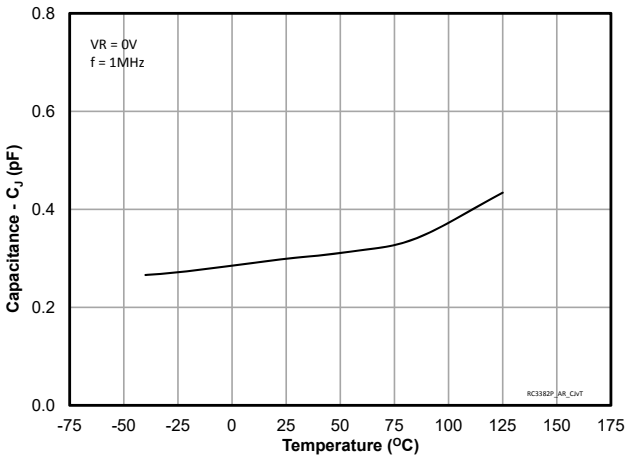


Typical Characteristics (Continued)

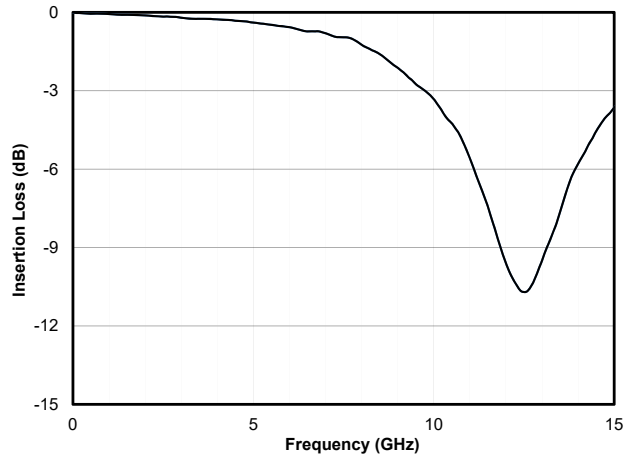
Capacitance vs. Reverse Voltage



Capacitance vs. Temperature



Insertion Loss - S21



Application Information

Ethernet Protection

Ethernet ports are exposed to external transient events in the form of ESD, EFT, lightning, and cable discharge events (CDE). Test standards that model these events include IEC 61000-4-2 for ESD, IEC 61000-4-4 for EFT, and IEC 61000-4-5 and GR-1089 for lightning. Any of these events can cause catastrophic damage to the PHY IC.

When designing Ethernet protection, the entire system must be considered. Over-voltage events can be common mode (with respect to ground) or differential (line-to-line). An Ethernet port includes interface magnetics consisting of transformers integrated with common mode chokes. The transformer center taps are connected to ground via an RC network or "Bob Smith" termination. The purpose of this termination is to reduce common mode emissions. The transformer provides common mode isolation to transient events, but no protection for differential surges. During a differential transient event, current will flow through the transformer, charging the windings on the line side. Energy is transferred to the secondary until the surge subsides or the transformer saturates.

A typical protection scheme which utilizes RClamp3382P is shown in Figure 1. Four each RClamp3382P are located on the PHY side of the transformer. Each device will protect one line pair (two lines). Parasitic inductance in the protection path should be minimized by locating RClamp3382P as physically close to the magnetics as possible, and preferably on the same side of the PCB. Reducing parasitic inductance is especially important for suppressing fast rise time transients such as ESD and EFT. Inductance in the path of the protection device increases the peak clamping voltage seen by the protected device (V = L di/dt). For example, 1nH of inductance can increase the peak clamping voltage by 30V for a 30A (8kV) ESD pulse with a 1ns rise time. Differential pairs are routed through pins 1 to 6, and 2 to 5. Pin 3 and 4 are not connected.

Placing the protection on the PHY side of the magnetics is advantageous in that the magnitude and duration of the surge is attenuated by the transformer windings. The amount of attenuation will vary by vendor and configuration of the magnetics. The Ethernet transformer must be able to support the impulse tests without failure. A typical Ethernet transformer can withstand a few hundred amperes (tp=8/20µs) before failure occurs, but this needs to be verified by testing. Alternatively, the protection can be placed on the line side of the transformer. However, the additional protection afforded by the transformer is lost, and the ability of the system to withstand high energy surges is limited to the capability of the protection device.

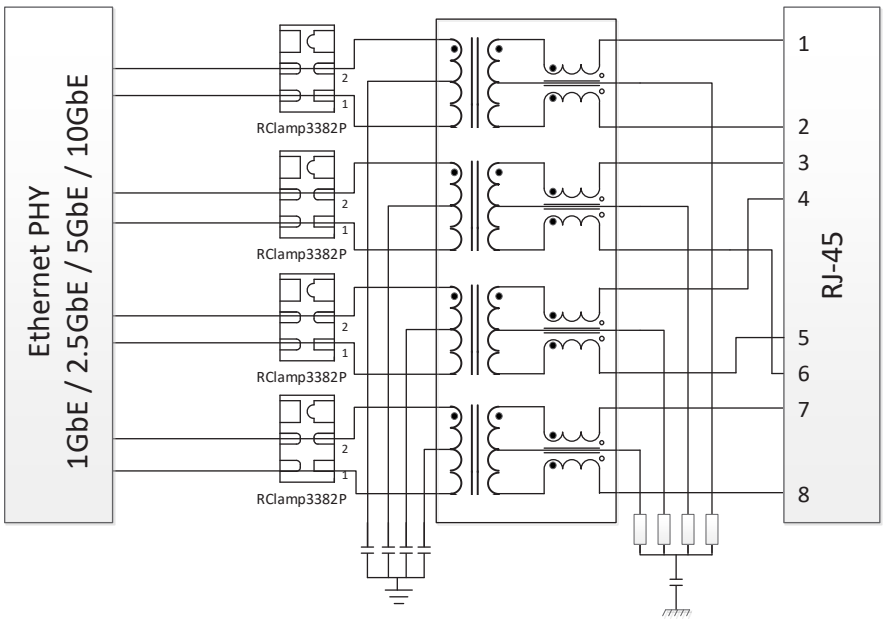
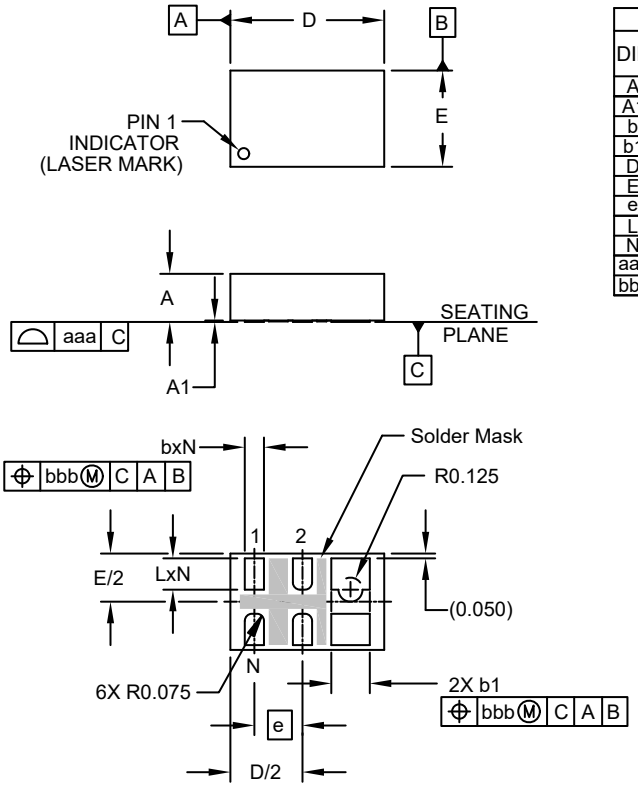


Figure 1 - Ethernet Protection Circuit

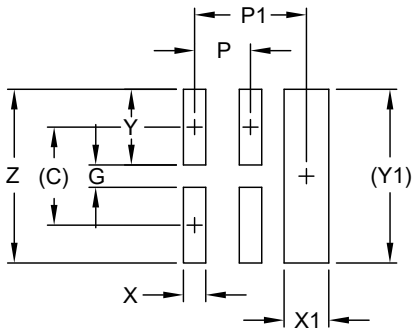
Outline Drawing - SGP1610N4



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.015	0.05
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
D	1.55	1.60	1.65
E	0.95	1.00	1.05
e	0.50 BSC		
L	0.275	0.325	0.375
N	4		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

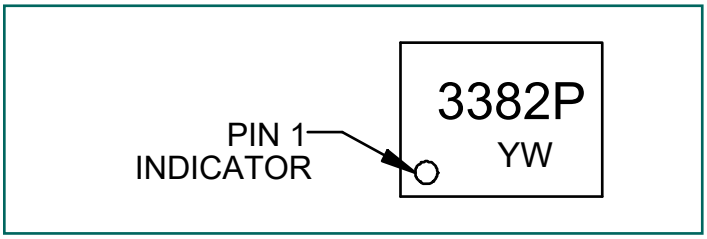
Land Pattern - SGP1610N4



DIMENSIONS	
DIM	MILLIMETERS
C	(0.87)
G	0.19
P	0.50
P1	1.00
X	0.20
X1	0.40
Y	0.68
Y1	(1.55)
Z	1.55

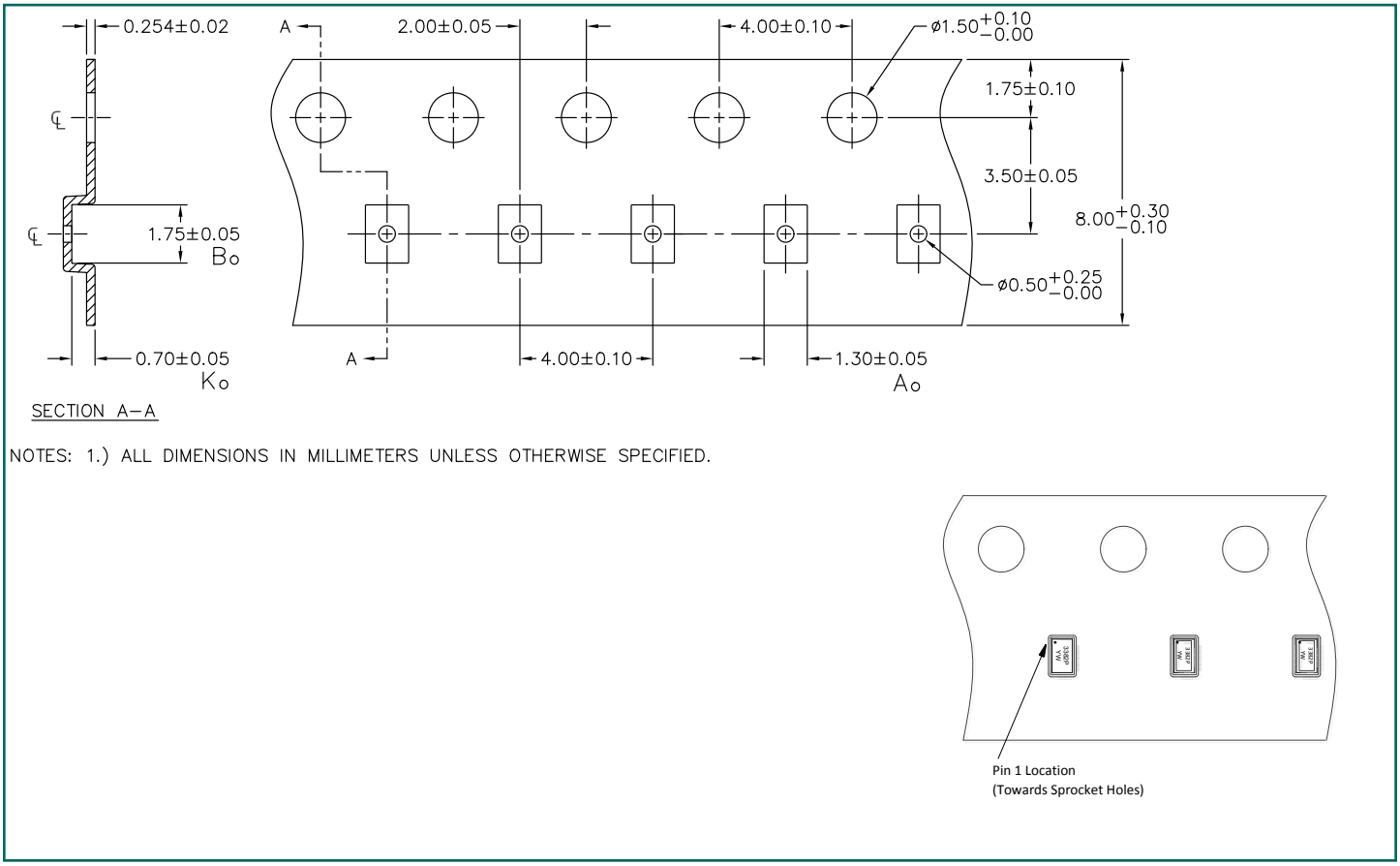
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Notes: Dot indicates Pin 1 Location

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size	Carrier Tape	Pitch
RClamp3382P.TCT	3000	7 Inch	Plastic	4mm
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