RClamp3631P

RailClamp®

1-Line ESD and EOS Protection

PROTECTION PRODUCTS

Description

RClamp®3631P is a bidirectional TVS specifically designed to provide secondary surge and ESD protection for high speed data lines. RClamp3631P utilizes deep snap-back to minimize device clamping voltage. The device features high surge capability of 10A (tp = 8/20 µs). ESD characteristics are highlighted by high ESD withstand voltage (+/-30kV per IEC 61000-4-2) and extremely low dynamic resistance (0.23Ω typical). Each device will protect one to two high speed data lines operating at ±3.63 volts.

RClamp3631P is in a 2-pin SLP1006P2 package. It measures 1.0 x 0.6 mm with a nominal height of 0.5mm. The leads are finished with lead-free NiPdAu. Small package design simplifies PCB layout and facilitates matching trace lengths for consistent impedance between high speed differential lines. The combination of small size, low capacitance, and high ESD surge capability makes them ideal for use in industrial and consumer applications.

Features

- High ESD withstand Voltage: ±30kV (Air and Contact) per IEC 61000-4-2
- High Surge Capability: 10A (tp = 8/20 µs) per IEC 61000-4-5
- Small package optimized for high speed lines
- Protects one line or one line pair
- Low ESD clamping voltage
- Working voltage: ±3.63V
- Low capacitance: 0.35pF Typical
- Low leakage current: 50nA Maximum
- Low dynamic resistance: 0.23Ω Typical
- Solid-state silicon-avalanche technology

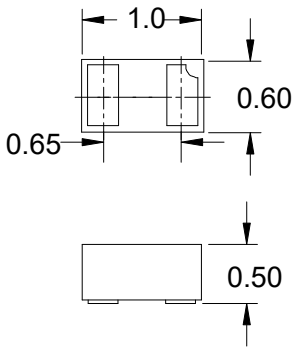
Mechanical Characteristics

- SLP1006P2 package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 1.0 x 0.6 x 0.5 mm
- Lead Finish: NiPdAu
- Marking: Marking code
- Packaging: Tape and Reel

Applications

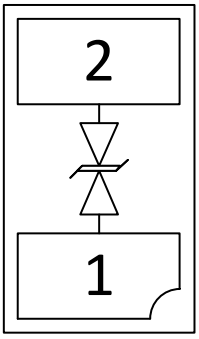
- USB2.0
- 2.5G/5GbE
- Industrial Equipment
- Antenna

Package Dimension



Nominal Dimensions (mm)

Schematic & Pin Configuration



SLP1006P2 (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	30	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	10	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±30 ±30	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	T = -40 °C to +125 °C, Pin 1 to 2 or 2 to 1			3.63	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA, Pin 1 to 2 or 2 to 1	6	8	11	V
Reverse Leakage Current	I_R	V_{RWM} = 3.63 V, Pin 1 to 2 or 2 to 1			50	nA
Clamping Voltage[2]	V_C	I_{PP} = 10A, tp = 1.2/50 µs (Voltage), 8/20 µs (Current) Combination Waveform		6	8	V
ESD Clamping Voltage[3]	V_C	I_{TLP} = 4A, tp = 0.2/100ns (TLP)		3.4		V
ESD Clamping Voltage[3]	V_C	I_{TLP} = 16A, tp = 0.2/100ns (TLP)		6.1		
Dynamic Resistance[3,4]	R_{DYN}	tp = 0.2/100ns		0.23		Ω
Junction Capacitance	C_J	V_R = 0V, f = 1MHz		0.35	0.38	pF

Notes:

1) ESD gun return path connected to ESD ground plane

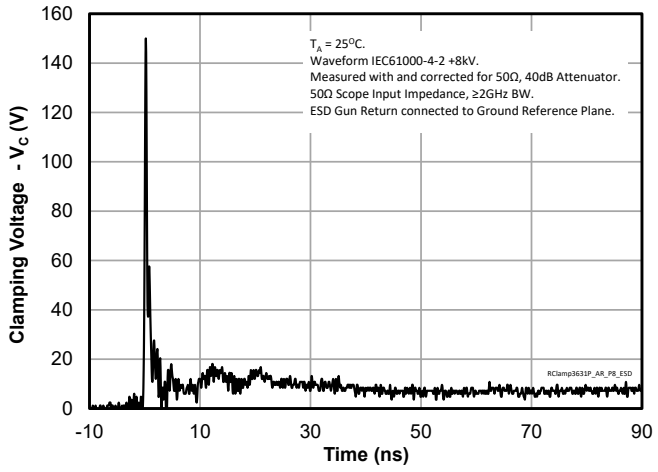
2) Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, R_S = 2 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

3) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.

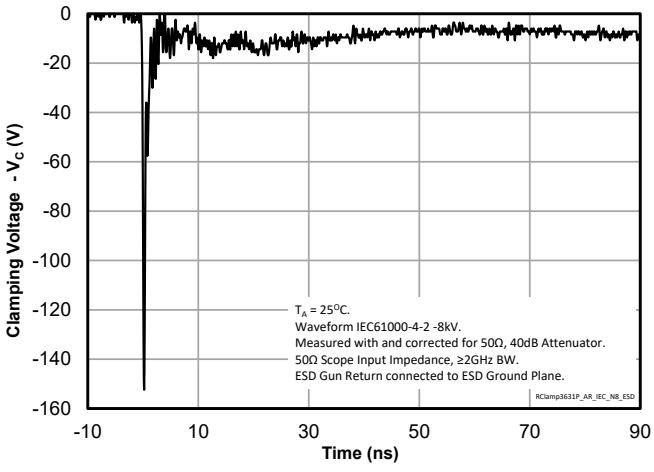
4) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

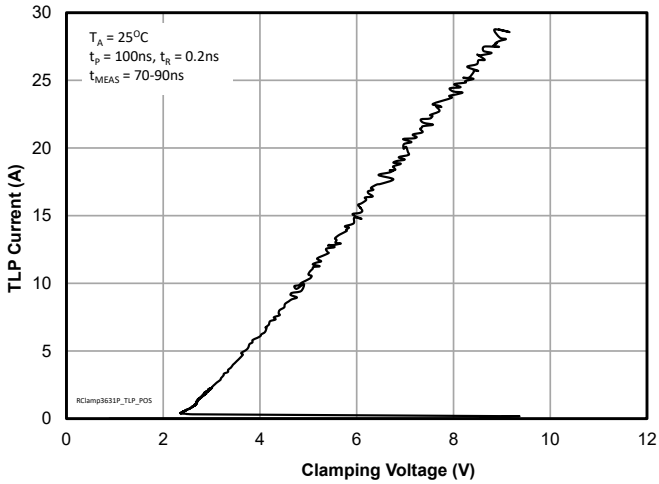
ESD Clamping (8kV Contact per IEC 61000-4-2)



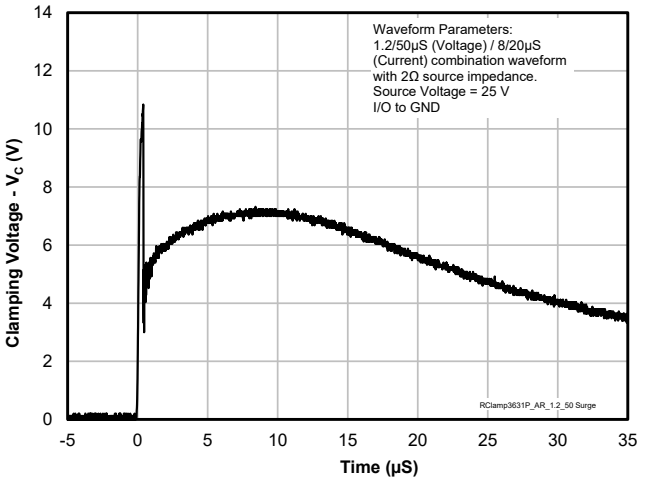
ESD Clamping (-8kV Contact per IEC 61000-4-2)



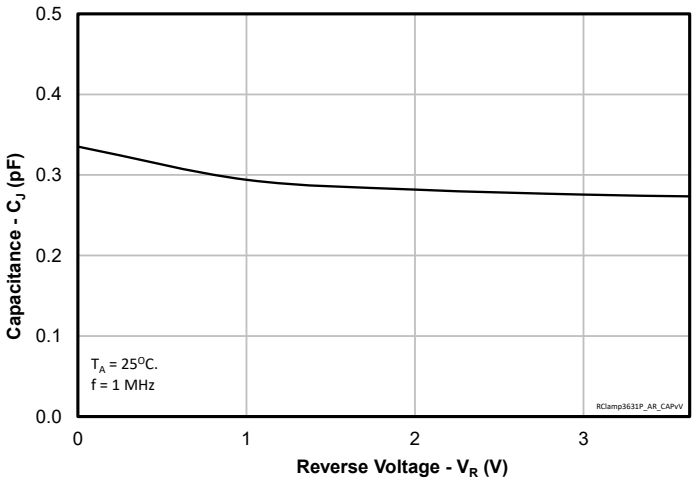
TLP Characteristic (Positive Pulse)



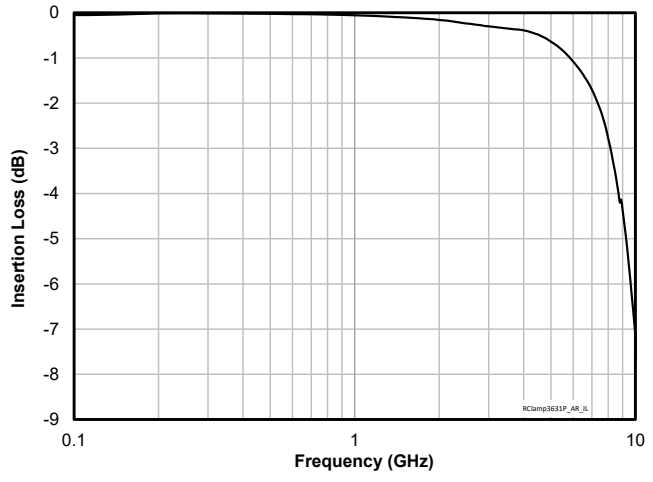
Clamping Characteristic (10A, Combination Waveform)



Capacitance vs. Reverse Voltage



Insertion Loss - S21



Application Information

USB 2.0 Protection and Layout

RClamp3631P is optimized for protection of high speed data lines such as those used in USB 2.0 applications. The typical capacitance of the device is only 0.35pF for maximum signal integrity. A typical protection scheme for USB 2.0 is shown in Figure 1. A single line 5V MicroClamp, such as µClamp0581P, is recommended for ESD and EOS protection of the Vbus.

Each TVS should be connected line to ground. Traces can be routed straight through the devices as shown in Figure 2. Traces should be kept to the same length to avoid impedance mismatch. Individual PCB design constraints may necessitate different spacing or trace width. TVS diodes should be placed as close to the connector as possible. This helps reduce transient coupling to nearby traces. Ground connection should be made directly to the ground plane using micro-vias. This reduces parasitic inductance in the ground path and minimizes the clamping voltage seen by the protected device.

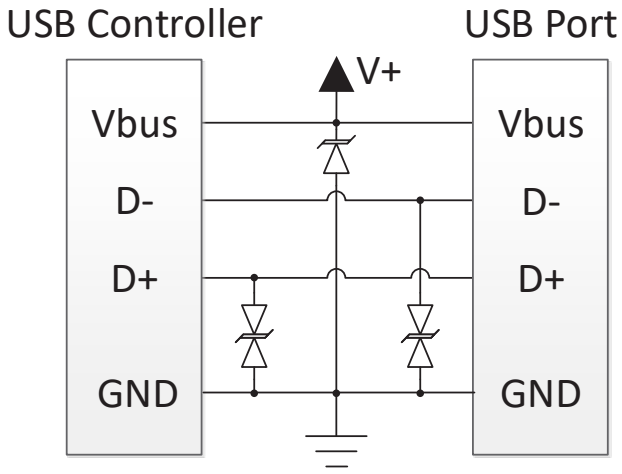


Figure 1 - USB 2.0 Diagram

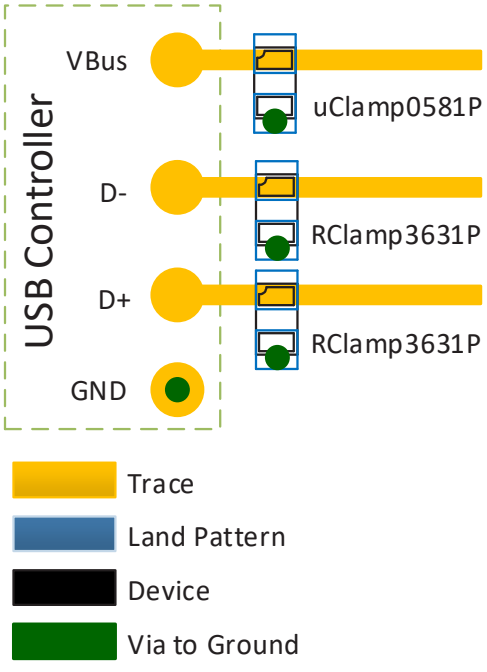


Figure 2 - USB 2.0 Layout

Application Information

Ethernet Protection

Ethernet ports are exposed to external transient events in the form of ESD, EFT, lightning, and cable discharge events (CDE). Test standards that model these events include IEC 61000-4-2 for ESD, IEC 61000-4-4 for EFT, and IEC 61000-4-5 and GR-1089 for lightning. Any of these events can cause catastrophic damage to the PHY IC.

When designing Ethernet protection, the entire system must be considered. Over-voltage events can be common mode (with respect to ground) or differential (line-to-line). An Ethernet port includes interface magnetics consisting of transformers integrated with common mode chokes. The transformer center taps are connected to ground via an RC network or "Bob Smith" termination. The purpose of this termination is to reduce common mode emissions. Note that components in the RC network should be chosen with a large enough current and voltage ratings to withstand ESD and EOS events.

The transformer provides common mode isolation to transient events, but no protection for differential surges. During a differential transient event current will flow through the transformer charging the windings on the line side. Energy is transferred to the secondary until the surge subsides or the transformer saturates.

A typical protection scheme which utilizes RClamp3631P is shown in Figure 1. Four RClamp3631P devices are located on the PHY side of the transformer. Each device will protect one line pair. Placing the protection on the PHY side of the magnetics is advantageous in that the magnitude and duration of the surge is attenuated by the transformer windings. The amount of attenuation will vary by vendor and configuration of the magnetics. The Ethernet transformer must be able to support the impulse tests without failure. A typical Ethernet transformer can withstand a few hundred amperes (tp=8/20us) before failure occurs, but this needs to be verified by testing.

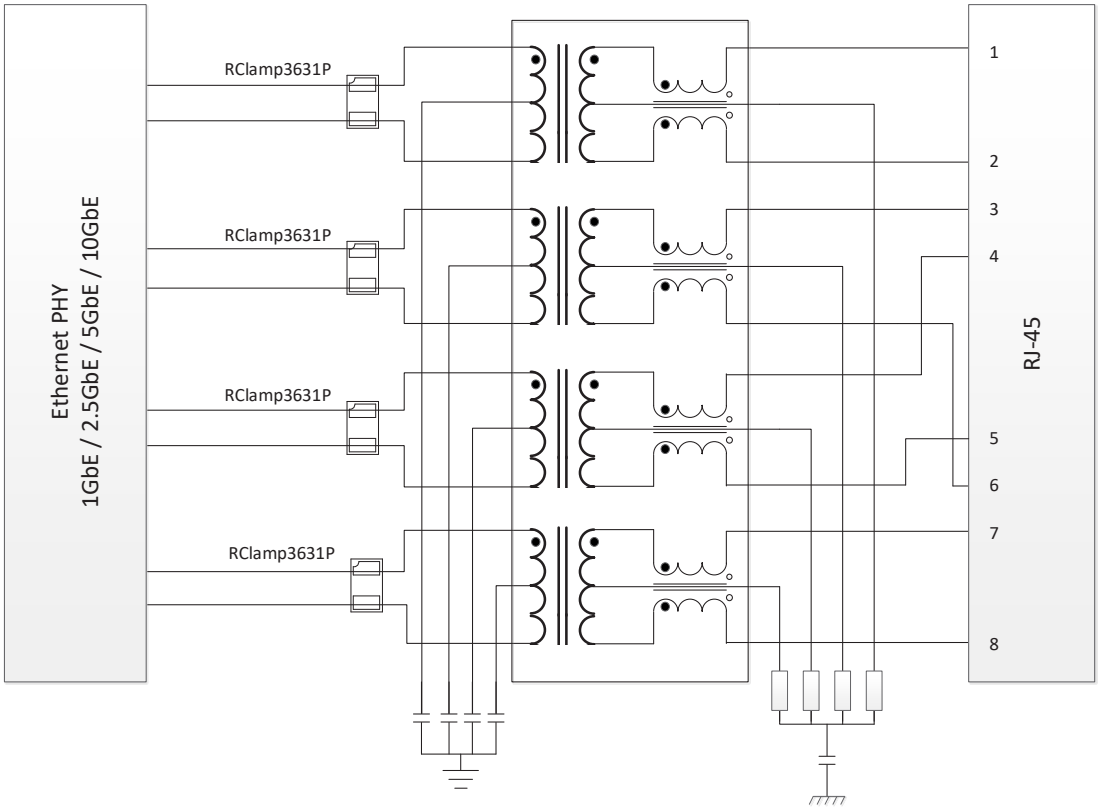


Figure 3 - Ethernet Protection Circuit

Application Information

Device Placement and Layout for Ethernet

Placement of the protection component is a critical element for effective transient voltage suppression. Parasitic inductance in the protection path should be minimized by locating RClamp3631P as physically close to the magnetics as possible, and preferably on the same side of the PCB. Traces can be routed straight through the device from the PHY to the magnetics, as shown in Figure 4.

Reducing parasitic inductance is especially important for suppressing fast rise time transients such as ESD and EFT. Inductance in the path of the protection device increases the peak clamping voltage seen by the protected device (V = L di/dt). For example, 1nH of inductance can increase the peak clamping voltage by 30V for a 30A (8kV) ESD pulse with a 1ns rise time.

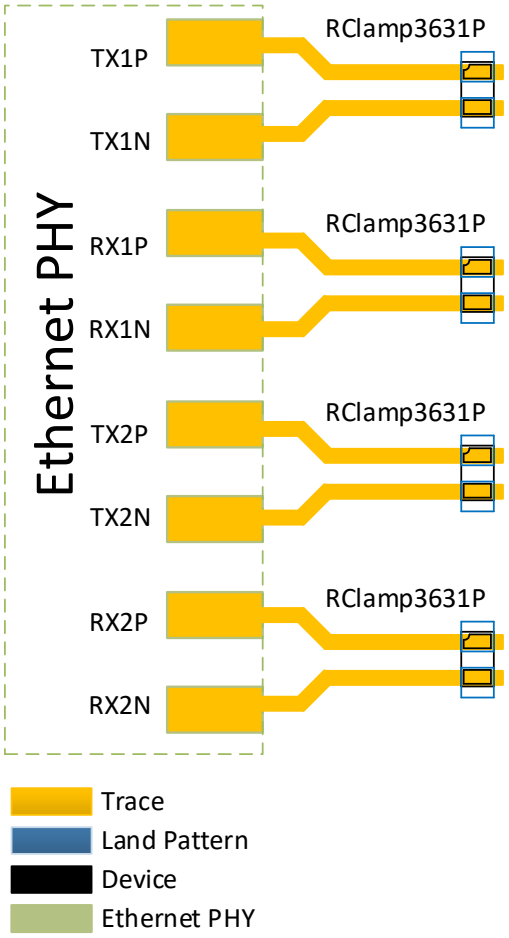
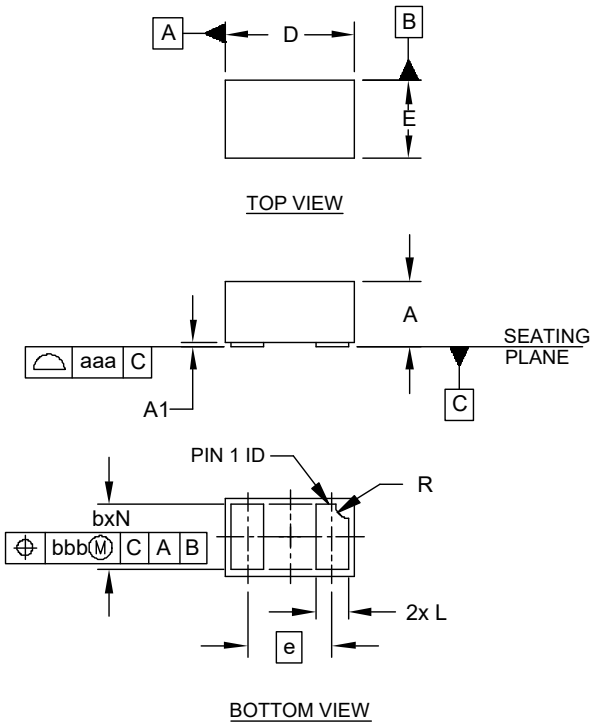


Figure 4 - Ethernet Layout Example

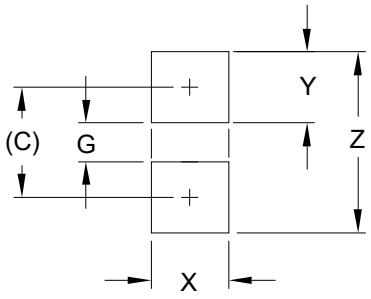
Outline Drawing - SLP1006P2



DIM	DIMENSIONS		
	MILLIMETERS		
	MIN	NOM	MAX
A	0.47	0.50	0.53
A1	0.00	0.03	0.05
b	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.20	0.25	0.30
R	0.05	0.10	0.15
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

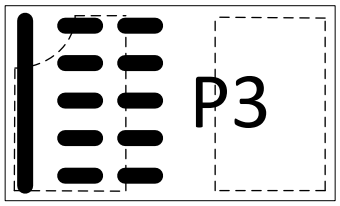
Land Pattern - SLP1006P2



DIM	DIMENSIONS
	MILLIMETERS
C	(0.85)
G	0.30
X	0.60
Y	0.55
Z	1.40

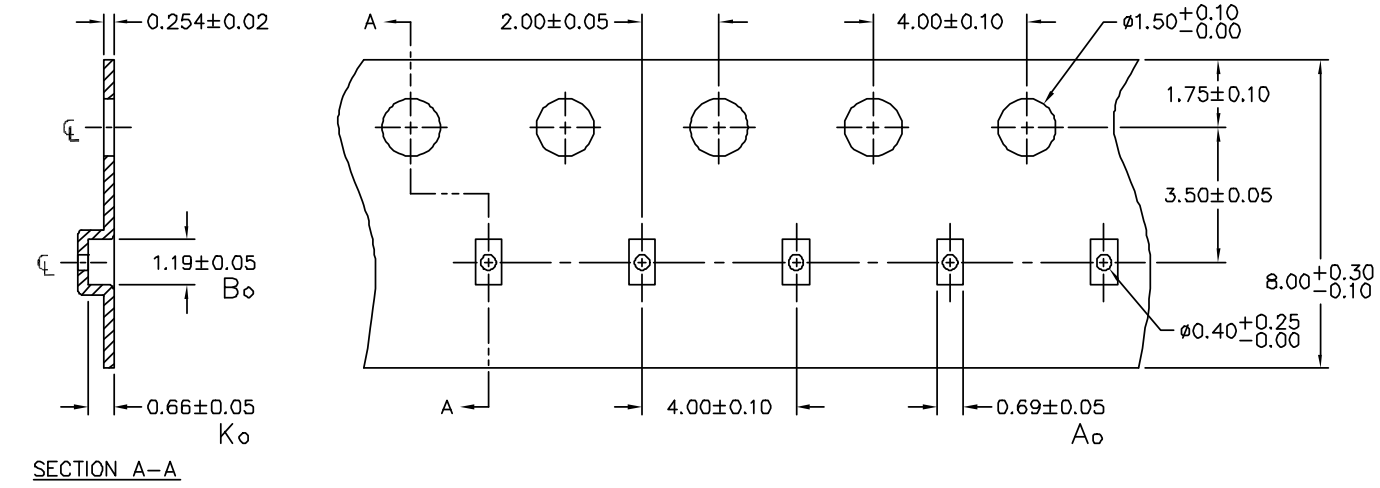
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking

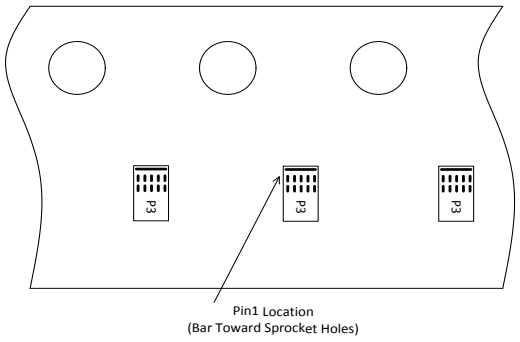


Notes:
1. Device is electrically symmetrical.
2. Marking will also include line matrix date code.
3. Bar indicates Pin 1 location

Tape and Reel Specification



NOTES: 1.) ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp3631P.TCT	3,000	7″
RClamp is trademark of Semtech Corporation		

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