RClamp7534P

Ultra Low Capacitance RailClamp® 4-Line ESD Protection

PROTECTION PRODUCTS

Description

RClamp®7534P is a high performance TVS array aimed at simultaneously protecting 4 signal lines from overvoltage events caused by ESD, CDE (Cable Discharge Events) and EFT (electrical fast transients). RClamp7534P features an extremely low typical capacitance of 0.19pF and is designed to protect high speed interfaces such as HDMI 2.0, Ethernet, and USB 3.0.

RCamp7534P is a bi-directional device designed to provide extremely low clamping voltage for both positive and negative ESD pulses. With a typical dynamic resistance of 1.0 Ohm, the RClamp7534P turns on quickly during overvoltage events to protect sensitive systems.

RClamp7534P is in a 5-pin SGP2010N5 package measuring 2.0 x 1.0mm with a nominal height of 0.50mm. The leads have a nominal pin-to-pin pitch of 0.40mm. Flow- through package design simplifies PCB layout and maintains signal integrity on high-speed lines. The combination of low peak ESD clamping, low dynamic resistance, and innovative package design enables this device to provide the highest level of ESD protection.

Features

- ESD protection for high-speed data lines to
- IEC 61000-4-2 (ESD) ±25kV (air), ±20kV (contact)
- IEC 61000-4-5 (Lightning) 4A (8/20µs)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- Package design optimized for high speed lines
- Protects four high-speed lines
- Low capacitance: 0.19pF Typical (I/O to Ground)
- Low ESD clamping voltage
- Low dynamic resistance: 1.0 Ohm (Typ)
- Low leakage current
- Solid-state silicon-avalanche technology

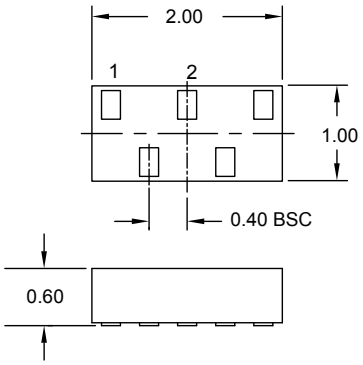
Mechanical Characteristics

- SGP2010N5 Package (2.0 x 1.0 x 0.50mm)
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: NiPdAu
- Marking : Marking Code
- Packaging : Tape and Reel

Applications

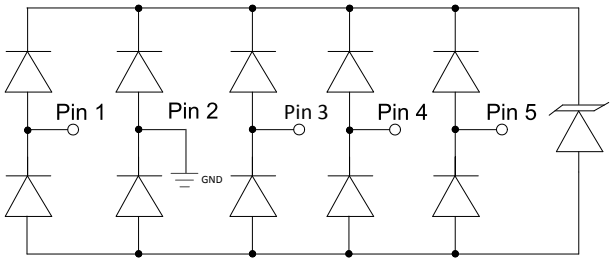
- HDMI 2.0
- USB 3.1
- Display Port 1.2
- Thunderbolt
- 1G / 2.5G / 5G /10G Ethernet
- V-By-One
- MHL

Nominal Dimensions



Nominal Dimensions in mm

Schematic



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20µs)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(1)	V_{ESD}	±20 ±25	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

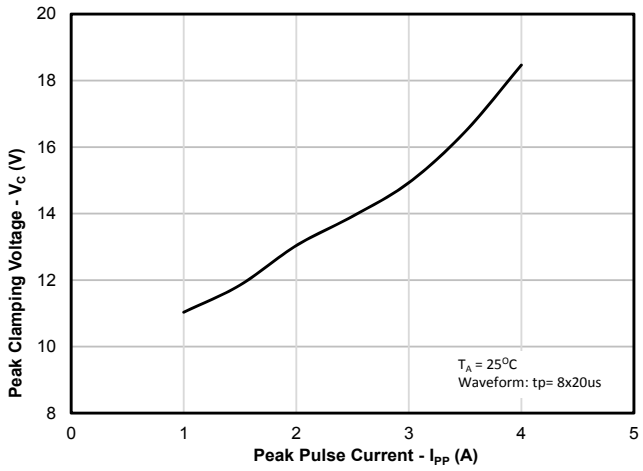
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O to GND			5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 1mA, Any I/O to GND	6.5	9.7	11.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5V, Any I/O to GND		5	100	nA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs			15	V
		I_{PP} = 4A, tp = 8/20µs			25	
ESD Clamping Voltage[2]	V_C	I = 4A, tp = 0.2/100ns (TLP)		14		V
ESD Clamping Voltage[2]	V_C	I = 16A, tp = 0.2/100ns (TLP)		24		V
Dynamic Resistance[2, 3]	R_{DYN}	tp = 0.2/100ns (TLP)		1.0		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz		0.19	0.22	pF

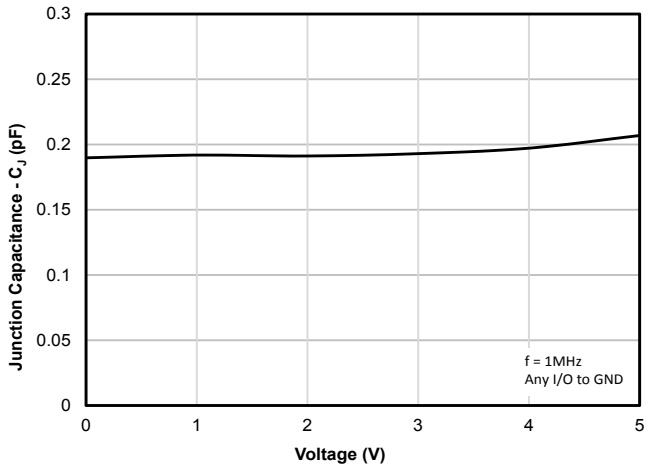
Notes:
(1) ESD gun return path connected to Ground Reference Plane (GRP)
(2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

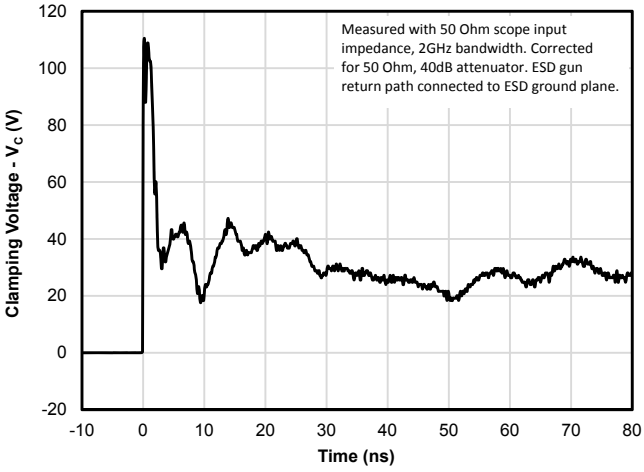
Clamping Voltage vs. Peak Pulse Current



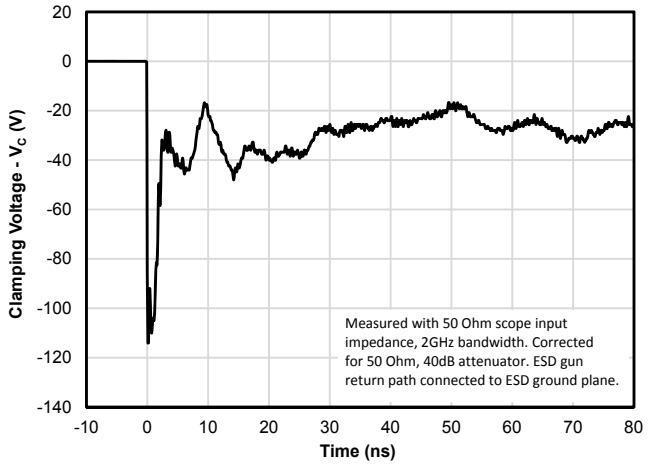
Junction Capacitance vs. Reverse Voltage



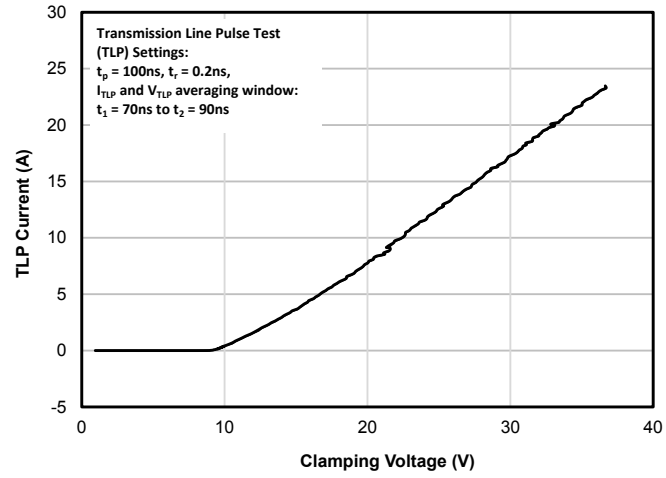
ESD Clamping Voltage (8kV Contact per IEC61000-4-2)



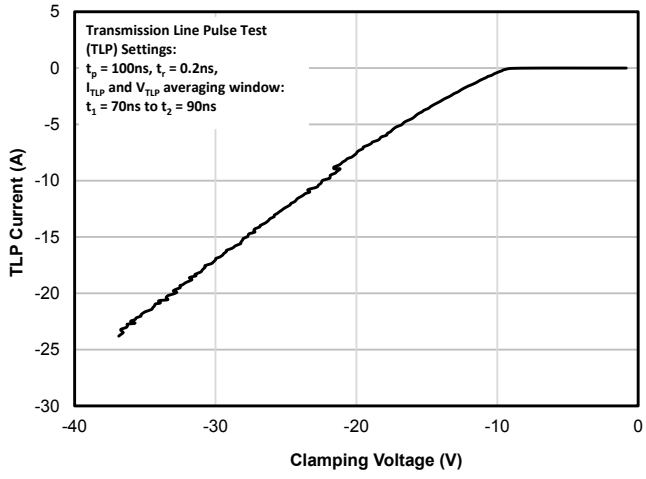
ESD Clamping Voltage (-8kV Contact per IEC61000-4-2)



TLP Characteristic (Positive Pulse)

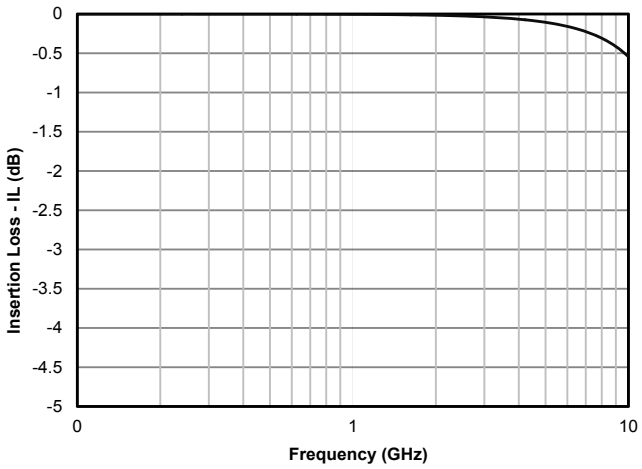


TLP Characteristic (Negative Pulse)

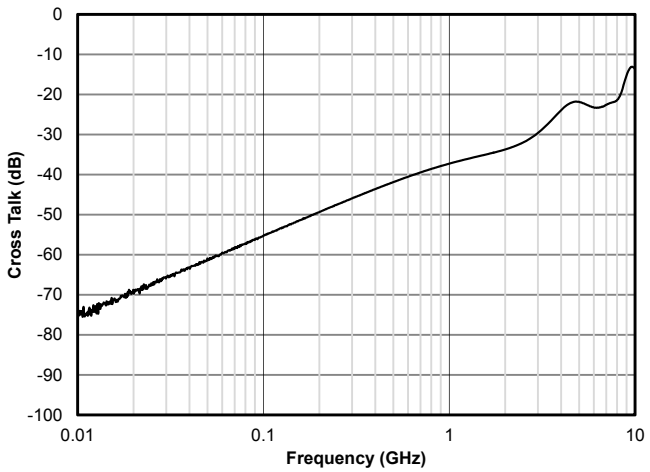


Typical Characteristics

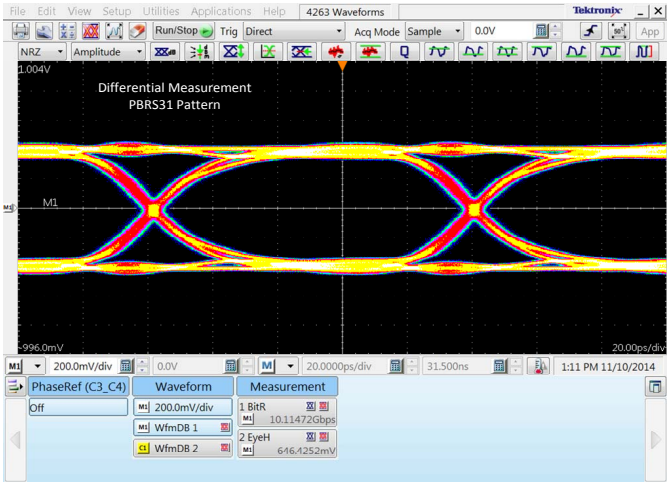
Insertion Loss (S21)



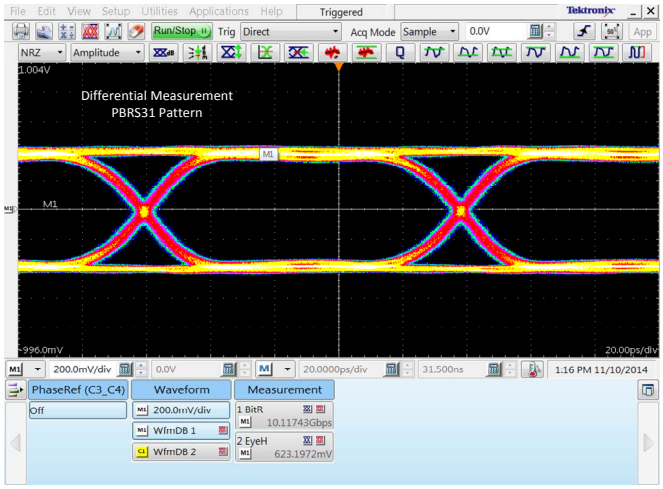
Analog Crosstalk



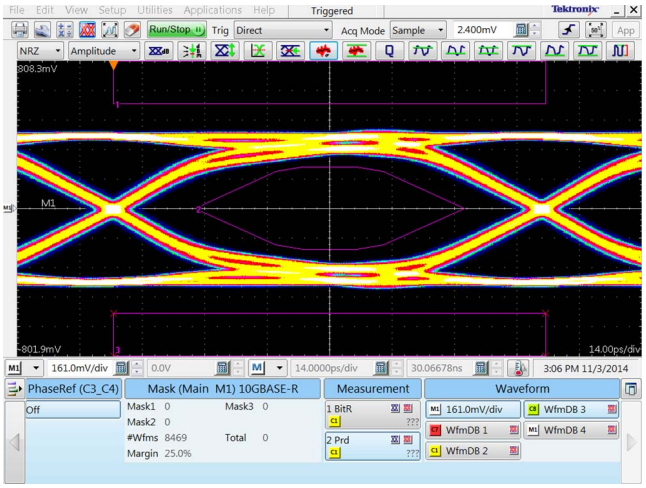
10Gb/s (USB 3.1) Eye Diagram with RClamp7534P



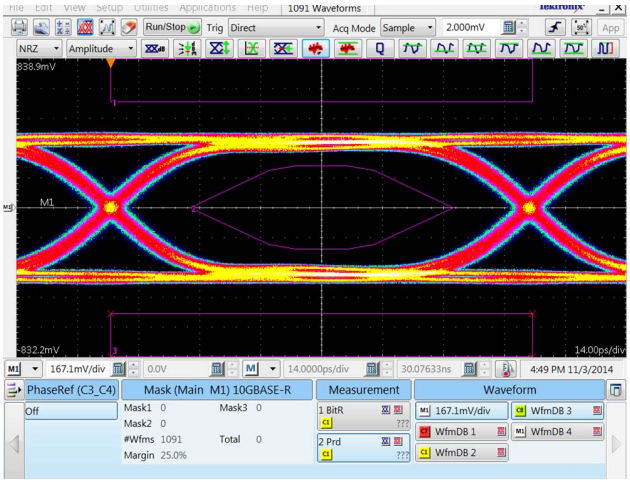
10Gb/s (USB 3.1) Eye Diagram without RClamp7534P



10GbE Eye Diagram with RClamp7534P



10GbE Eye Diagram without RClamp7534P



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern

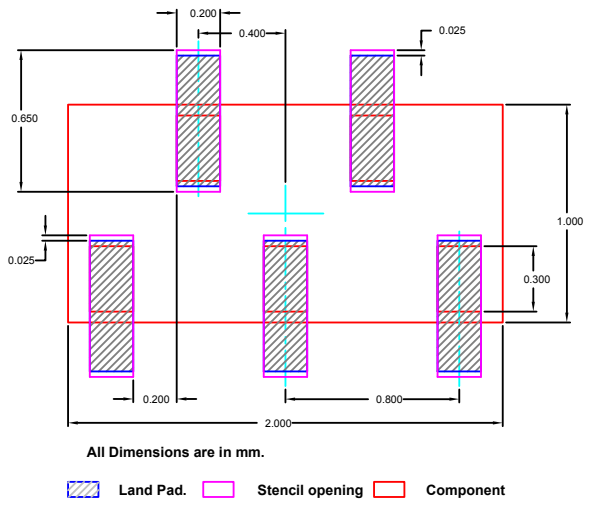
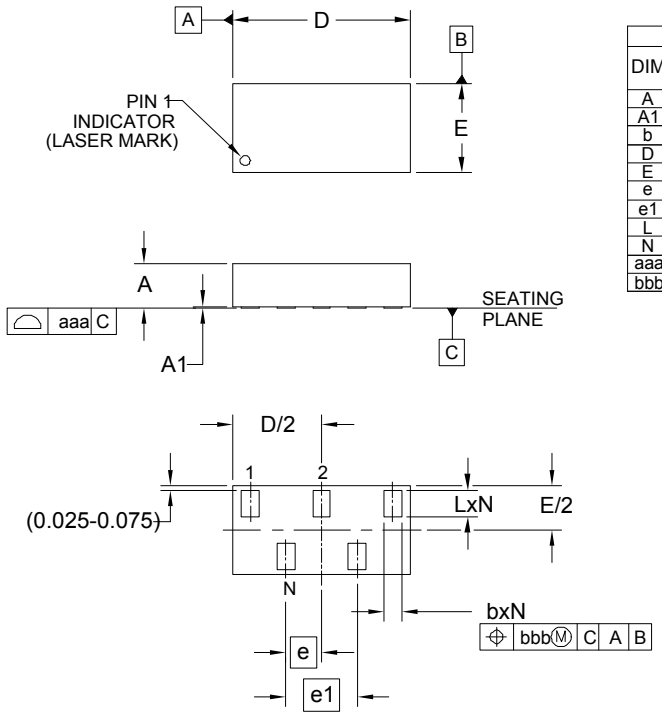


Table 1 - Recommended Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - SGP2010N5



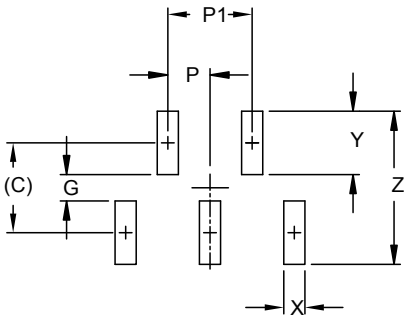
DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	1.95	2.00	2.08
E	0.95	1.00	1.08
e	0.40 BSC		
e1	0.80 BSC		
L	0.25	0.30	0.35
N	5		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Package Number-4-R0

Land Pattern - SGP2010N5

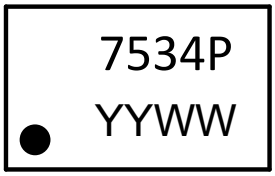


DIMENSIONS	
DIM	MILLIMETERS
C	(0.85)
G	0.25
P	0.40
P1	0.80
X	0.20
Y	0.60
Z	1.45

NOTES:

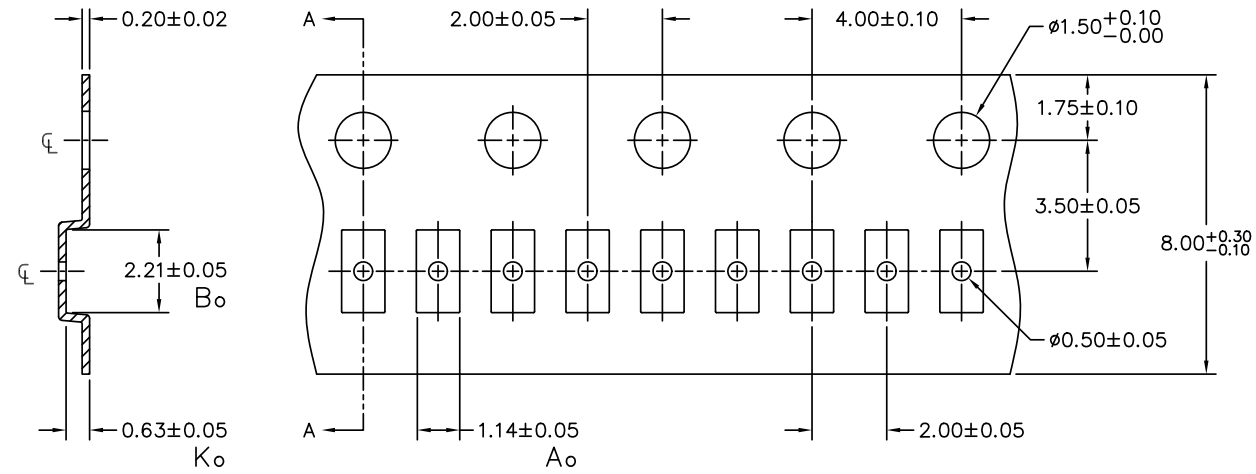
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

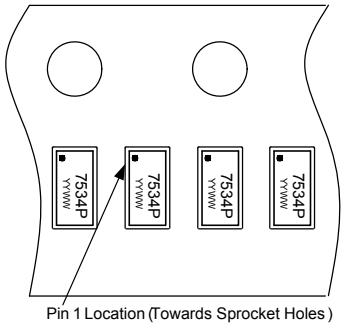


Notes: YYWW = Alphanumeric Date Code

Tape and Reel Specification



NOTE: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp7534P.TNT	10000	7 Inch

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