RD74LVC00B

Quad. 2-input NAND Gates

REJ03D0222–0100Z
Rev.1.00
May 11, 2004

Description

The RD74LVC00B has four 2-input NAND gates in a 14 pin package. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- V_{CC} = 1.65 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±4 mA (@V_{CC} = 1.65 V)
  ±8 mA (@V_{CC} = 2.3 V)
  ±12 mA (@V_{CC} = 2.7 V)
  ±24 mA (@V_{CC} = 3.0 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RD74LVC00BFPEL	SOP–14 pin (JEITA)	FP–14DAV	FP	EL (2,000 pcs/reel)
RD74LVC00BTELL	TSSOP–14 pin	TTP–14DV	T	ELL (2,000 pcs/reel)

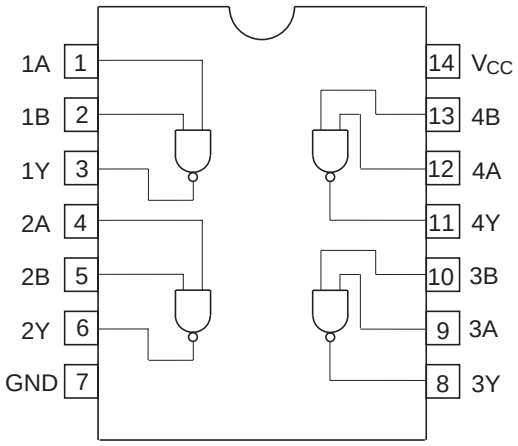
Function Table

Inputs		Output Y
A	B	
L	L	H
L	H	H
H	L	H
H	H	L

H : High level

L : Low level

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 7.0	V	
Input diode current	I_{IK}	–50	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 7.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50	mA	V_O = V_{CC}+0.5 V
Output voltage	V_O	–0.5 to V_{CC}+0.5	V	
Output current	I_O	±50	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	Tstg	–65 to +150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data hold
		1.65 to 5.5		At operation
Input / Output voltage	V_I	0 to 5.5	V	A, B
	V_O	0 to V_{CC}		Y
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–4	mA	V_{CC} = 1.65 V
		–8		V_{CC} = 2.3 V
		–12		V_{CC} = 2.7 V
		–24		V_{CC} = 3.0 V to 5.5 V
	I_{OL}	4		V_{CC} = 1.65 V
		8		V_{CC} = 2.3 V
		12		V_{CC} = 2.7 V
		24		V_{CC} = 3.0 V to 5.5 V
Input rise / fall time[*1]	t_r, t_f	20	ns/V	V_{CC} = 1.65 V to 2.7 V
		10		V_{CC} = 3.0 V to 5.5 V

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V_{IH}	1.65 to 1.95	V_{CC}×0.65	—	V	
		2.3 to 2.7	1.7	—		
		2.7 to 3.6	2.0	—		
		4.5 to 5.5	V_{CC}×0.7	—		
	V_{IL}	1.65 to 1.95	—	V_{CC}×0.35		
		2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
		4.5 to 5.5	—	V_{CC}×0.3		
Output voltage	V_{OH}	1.65 to 5.5	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		1.65	1.2	—		I_{OH} = –4 mA
		2.3	1.7	—		I_{OH} = –8 mA
		2.7	2.2	—		I_{OH} = –12 mA
		3.0	2.4	—		
		3.0	2.2	—		I_{OH} = –24 mA
		4.5	3.8	—		
	V_{OL}	1.65 to 5.5	—	0.2		I_{OL} = 100 µA
		1.65	—	0.45		I_{OL} = 4 mA
		2.3	—	0.7		I_{OL} = 8 mA
		2.7	—	0.4		I_{OL} = 12 mA
		3.0	—	0.55		I_{OL} = 24 mA
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	±5.0	µA	V_{IN} = 5.5 V or GND
Quiescent supply current	I_{CC}	2.7 to 3.6	—	±5.0	µA	V_{IN} = 3.6 V to 5.5 V
		2.7 to 5.5	—	5.0		V_{IN} = V_{CC} or GND
	ΔI_{CC}	2.7 to 3.6	—	500		V_{IN} = one input at (V_{CC}–0.6)V, other inputs at V_{CC} or GND

Switching Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t_{PLH}	1.8±0.15	1.0	—	12.5	ns	A or B	Y
	t_{PHL}	2.5±0.2	1.0	—	6.4			
		2.7	1.0	—	5.1			
		3.3±0.3	1.0	—	4.3			
		5.0±0.5	1.0	—	3.6			
Between output pins skew*[1]	t_{OSLH}	1.8±0.15	—	—	—	ns		
	t_{OSHL}	2.5±0.2	—	—	—			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C_{IN}	3.3	—	5.0	—	pF		

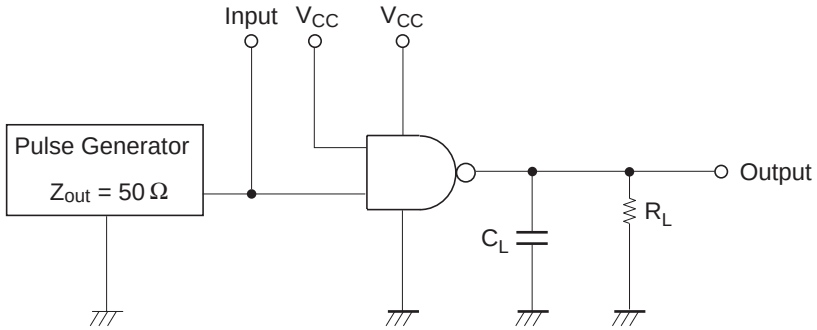
Note: 1. This parameter is characterized but not tested.

$t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Operating Characteristics

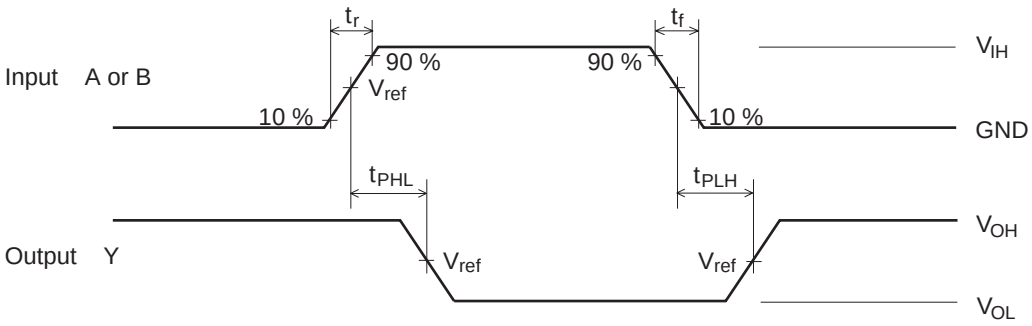
Item	Symbol	V_{CC} (V)	Ta = 25°C			Unit	Test conditions
			Min	Typ	Max		
Power dissipation Capacitance	C_{PD}	1.8	—	10	—	pF	f = 10 MHz
		2.5	—	12	—		
		3.3	—	12	—		
		5.0	—	15	—		

Test Circuit



Note: 1. C_L includes probe and jig capacitance.

Waveforms

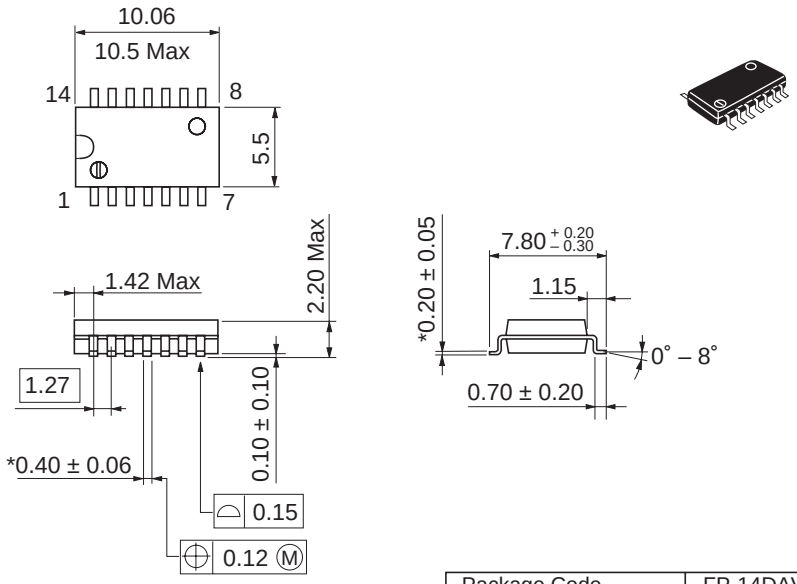


	INPUTS				
V_{CC} (V)	V_{IH}	t_r/t_f	V_{ref}	C_L	R_L
V_{CC} = 1.8±0.15 V	V_{CC}	≤ 2 ns	1/2 V_{CC}	30 pF	1.0 kΩ
V_{CC} = 2.5±0.2 V	V_{CC}	≤ 2 ns	1/2 V_{CC}	30 pF	500 Ω
V_{CC} = 2.7 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
V_{CC} = 3.3±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
V_{CC} = 5.0±0.5 V	V_{CC}	≤ 2.5 ns	1/2 V_{CC}	50 pF	500 Ω

Note: 1. Input waveform : PRR = 10 MHz, duty cycle 50%.

Package Dimensions

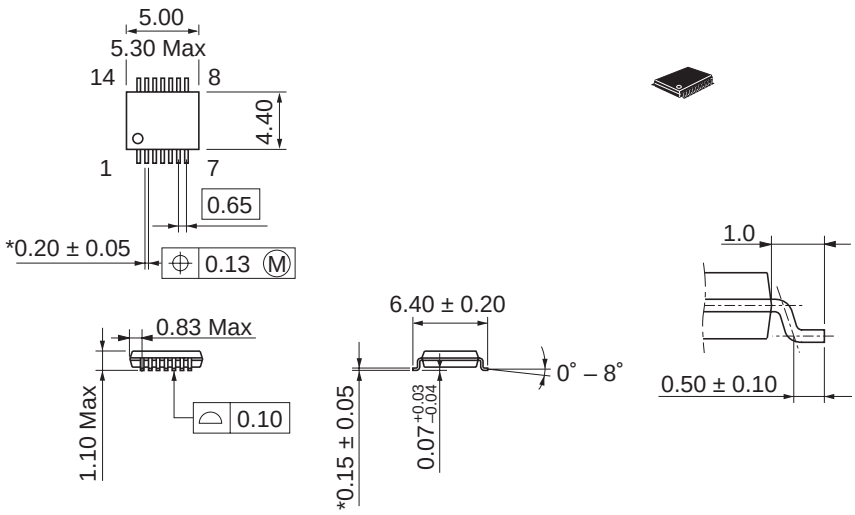
As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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