Data Sheet | August 1999 | File Number 3986.5

3.5A, 30V, 0.06 Ohm, Dual N-Channel LittleFET™ Power MOSFET

This Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching convertors, motor drivers, relay drivers, and low voltage bus switches. This device can be operated directly from integrated circuits.

Formerly developmental type TA49086.

Ordering Information

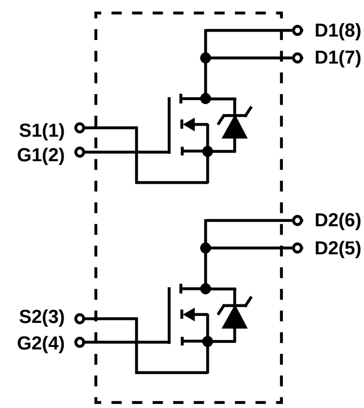
PART NUMBER	PACKAGE	BRAND
RF1K49086	MS-012AA	RF1K49086

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4908696.

Features

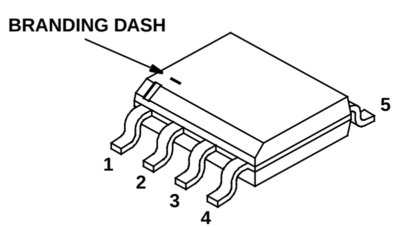
- 3.5A, 30V
- $r_{DS(ON)} = 0.060\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC MS-012AA



Absolute Maximum Ratings $T_A = 25^oC$ Unless Otherwise Specified

		RF1K49086	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ, Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Pulse Width = 5s)	I_D	3.5	A
Pulsed (Figure 5)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating (Figure 6)	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = 25^oC$	P_D	2	W
Derate Above 25^oC		0.016	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V, (Figure 12)		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA, (Figure 11)		1	-	3	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	$T_A = 25^oC$	-	-	1	µA
			$T_A = 150^oC$	-	-	50	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 3.5A (Figures 9, 10)	V_{GS} = 10V	-	-	0.060	Ω
			V_{GS} = 4.5V	-	-	0.132	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D ≈ 3.5A, R_L = 4.29Ω, V_{GS} = 10V, R_{GS} = 25Ω		-	-	50	ns
Turn-On Delay Time	$t_{d(ON)}$			-	10	-	ns
Rise Time	t_r			-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	60	-	ns
Fall Time	t_f			-	45	-	ns
Turn-Off Time	t_{OFF}			-	-	130	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 24V, I_D = 3.5A, R_L = 6.86Ω (Figure 14)	-	35	45	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	13	17	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	2.3	2.9	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 13)		-	575	-	pF
Output Capacitance	C_{OSS}			-	275	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse Width = 1s Device mounted on FR-4 material		-	-	62.5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 3.5A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 3.5A, dI_{SD}/dt = 100A/µs	-	-	45	ns

Typical Performance Curves

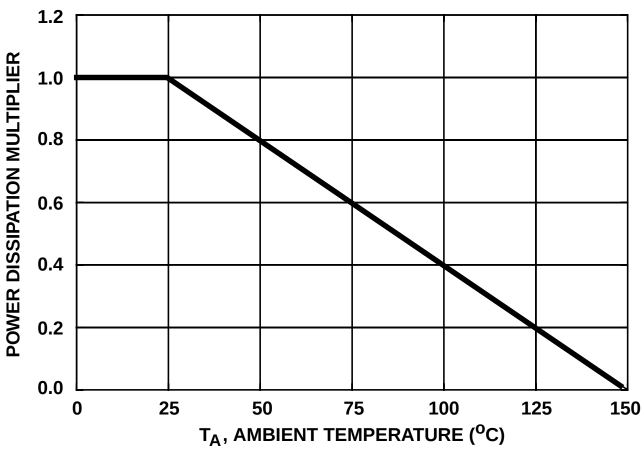


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

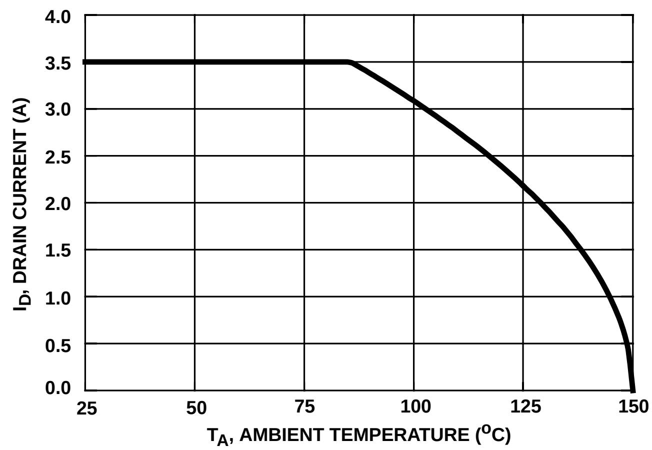


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

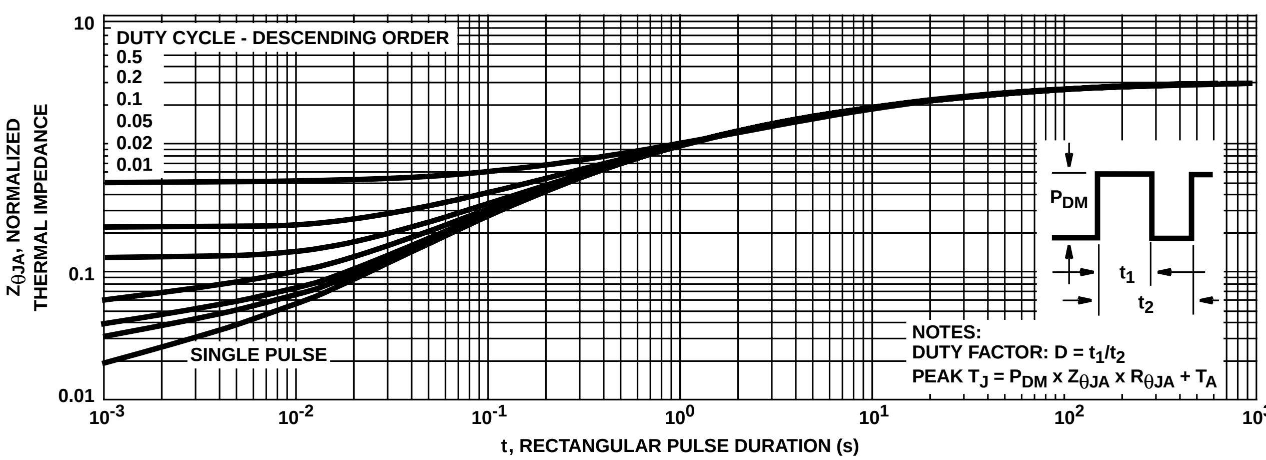


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

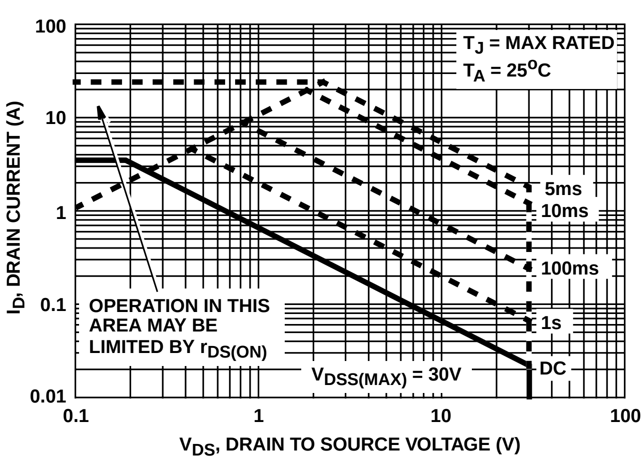


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

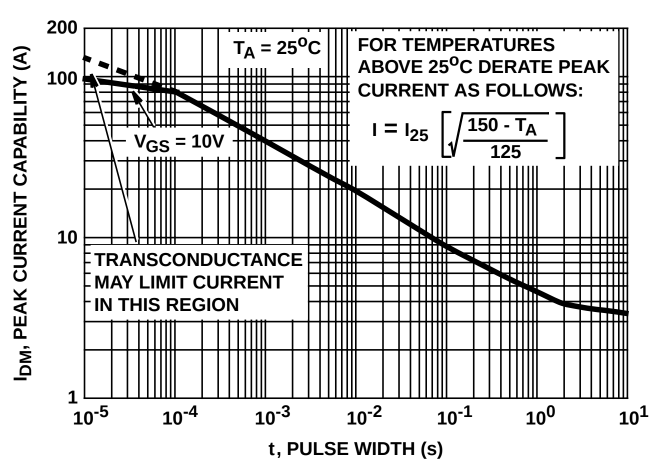
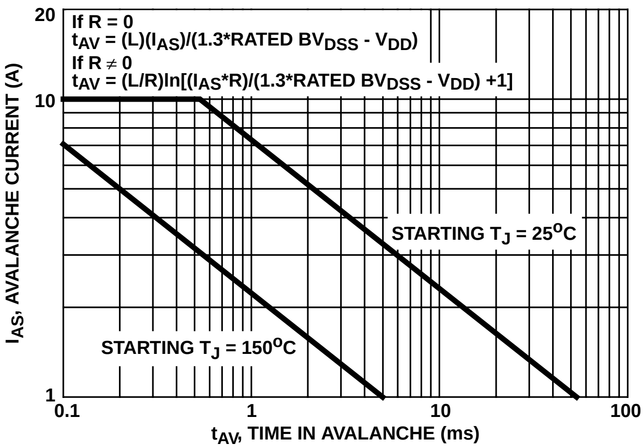


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

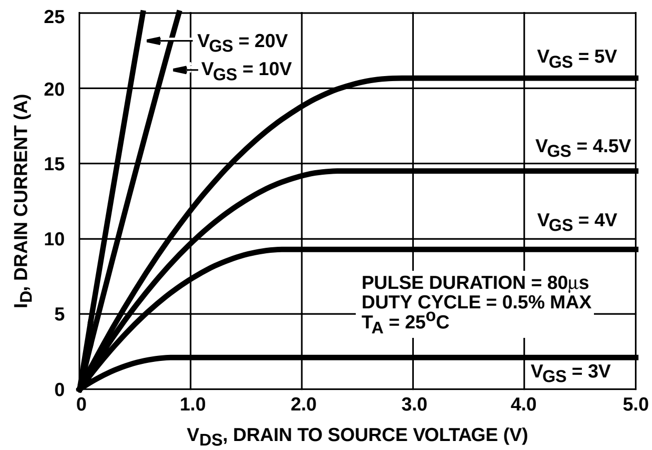


FIGURE 7. SATURATION CHARACTERISTICS

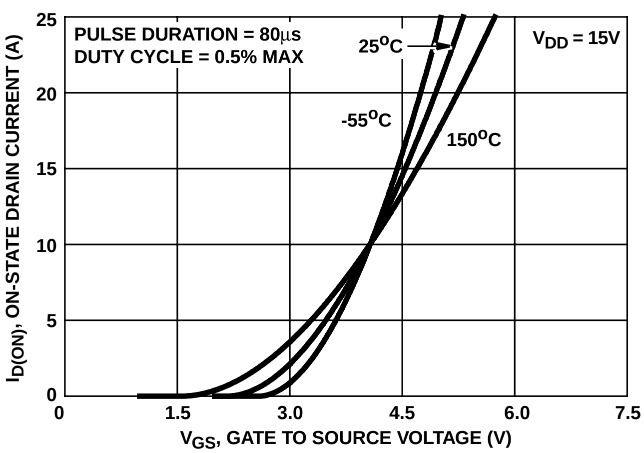


FIGURE 8. TRANSFER CHARACTERISTICS

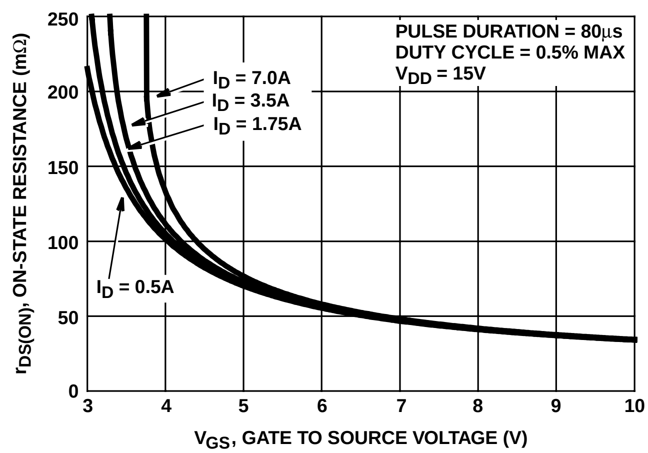


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

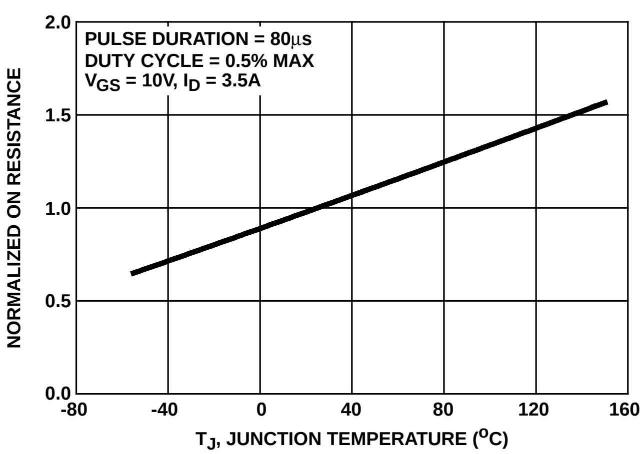


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

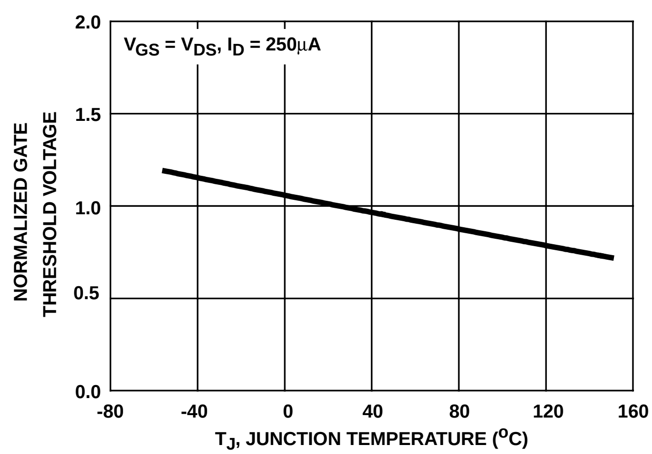


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

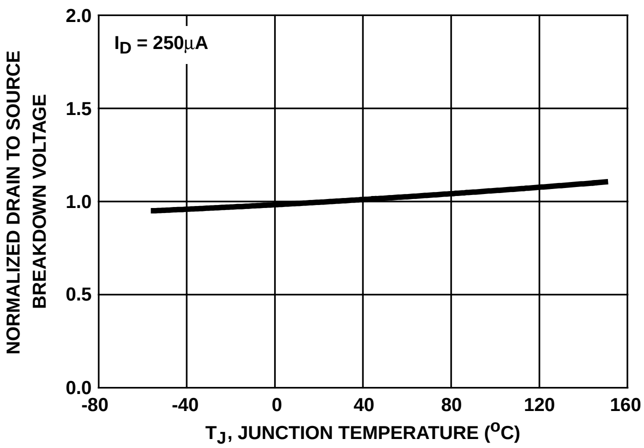


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

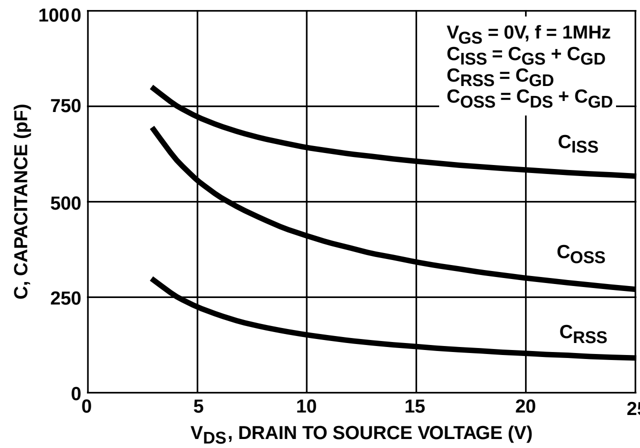
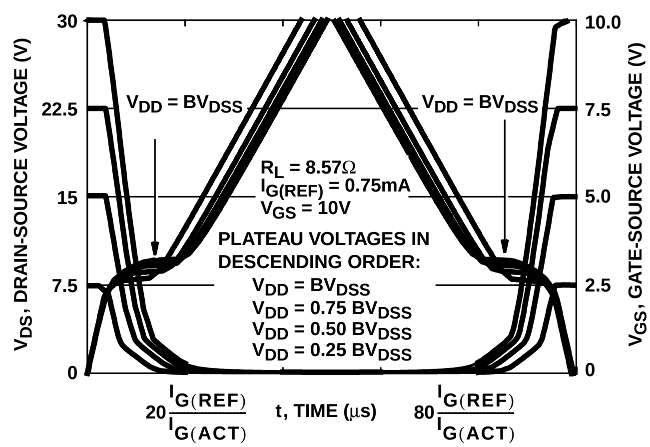


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

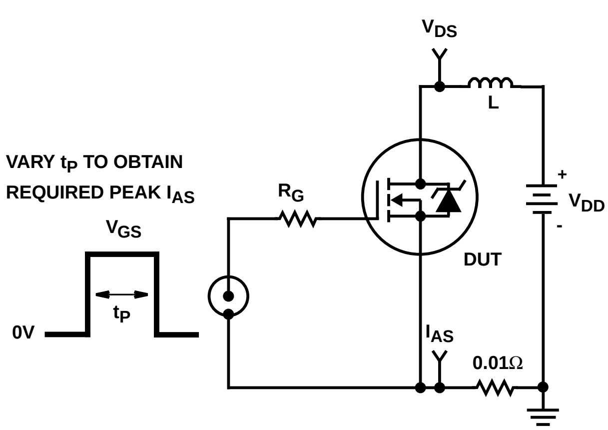


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

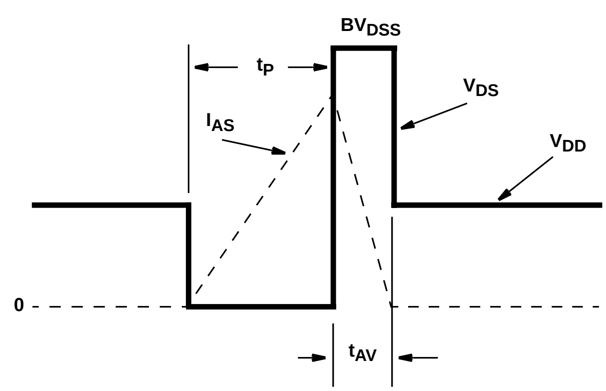


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

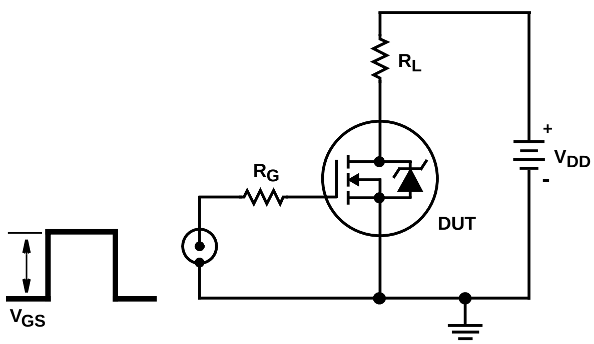


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

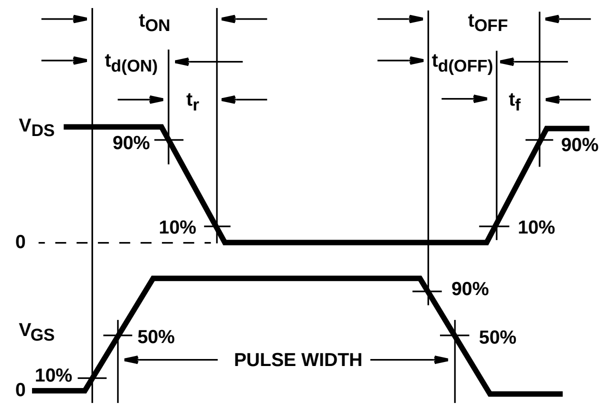


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

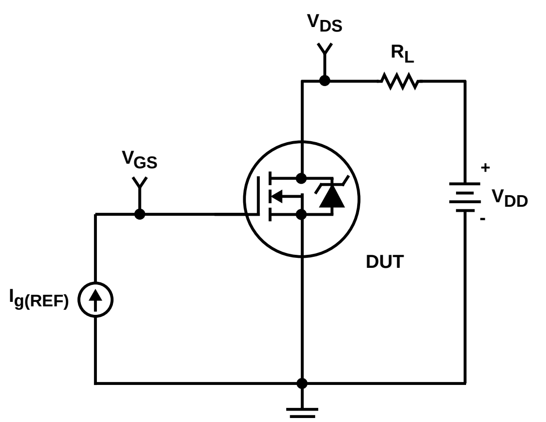


FIGURE 19. GATE CHARGE TEST CIRCUIT

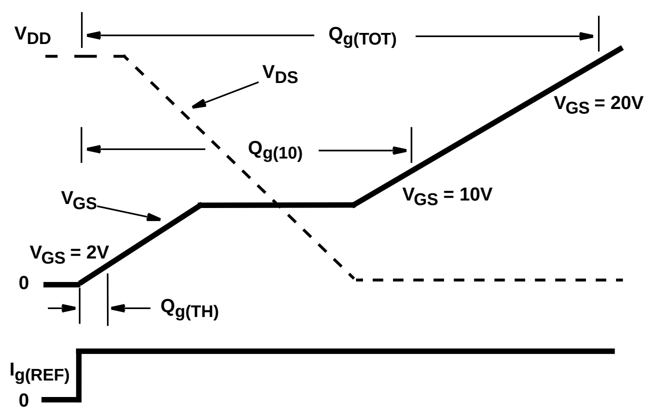


FIGURE 20. GATE CHARGE WAVEFORM

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100^oC. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5^oC per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30^oC higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260^oC for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

PSPICE Electrical Model

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SUBCKT  RF1K49086  2 1 3 ;       rev 12/15/94

CA  12  8  1.75e-9
CB  15  14  1.80e-9
CIN  6  8  1.20e-9

DBODY  7  5  DBDMOD
DBREAK  5 11  DBKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  33.29
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTO  20  6  18  8  1

IT  8  17  1

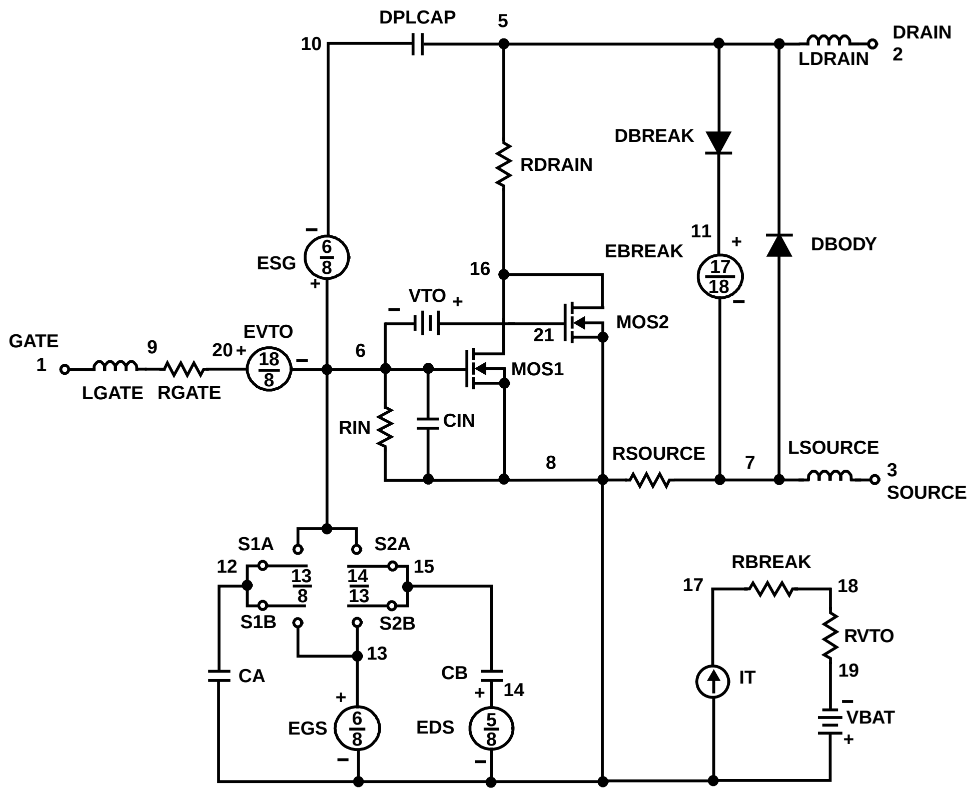
LDRAIN  2  5  1e-9
LGATE 1  9  1.233e-9
LSOURCE  3  7  0.452e-9

MOS1  16  6  8  8  MOSMOD  M = 0.99
MOS2  16  21  8  8  MOSMOD  M = 0.01

RBREAK  17  18  RBKMOD  1
RDRAIN  5  16  RDSMOD  1e-4
RGATE  9  20  1.83
RIN  6  8  1e9
RSOURCE  8  7  RDSMOD  13.5e-3
RVTO  18  19  RVTOMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  8  19  DC  1
VTO  21  6   0.1
```

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.MODEL DBDMOD D (IS = 2.50e-13  RS = 1.35e-2  TRS1 = 4.31e-5  TRS2 = 2.15e-5  CJO = 9.33e-10  TT = 2.08e-8)
.MODEL DBKMOD D (RS = 1.14  TRS1 = 2.23e-3  TRS2 = -8.91e-6)
.MODEL DPLCAPMOD D (CJO = 7.99e-10  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 2.15  KP = 6.25  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 7.74e-4  TC2 = 1.13e-6)
.MODEL RDSMOD RES (TC1 = 4.5e-3  TC2 = -7.45e-7)
.MODEL RVTOMOD RES (TC1 = -4.16e-3  TC2 = 2.16e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -7.15  VOFF= -5.15)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -5.15  VOFF= -7.15)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.6  VOFF= 2.4)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 2.4  VOFF= -2.6)

.ENDS
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NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.