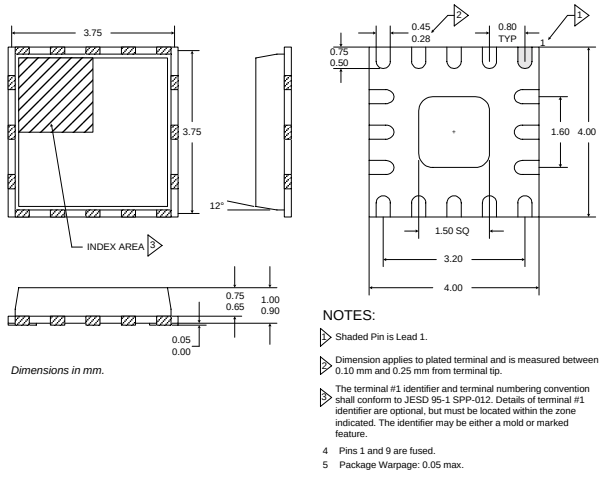
Typical Applications

- 3V 1850-1910MHz CDMA PCS Handsets
- 3V 1750-1780MHz CDMA PCS Handsets
- 3V TDMA PCS Handsets
- Spread-Spectrum Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

The RF2157 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA and TDMA handheld digital equipment, spread-spectrum systems, and other applications in the 1710MHz to 1910MHz band. The device is packaged in a compact 4mmx4mm LCC, as well as a 4mmx4mm MLF (micro leaded package). The frequency response can be optimized for linear performance over 1710MHz to 1910MHz. The device features a digital mode switch which can be used to minimize operating current under low output power conditions.



Dimensions in mm.

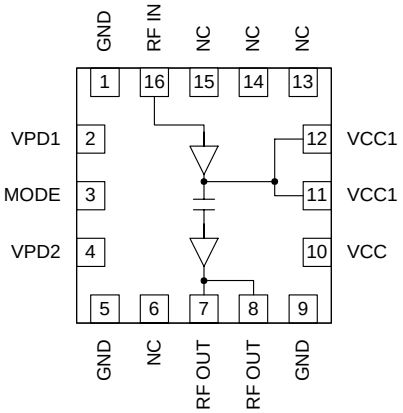
NOTES:

1. Shaded Pin is Lead 1.
2. Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.
3. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.
4. Pins 1 and 9 are fused.
5. Package Warpage: 0.05 max.

Package Style: LCC, 16-Pin, 4x4

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 24dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode
- 1750MHz to 1910MHz Operation

Ordering Information

RF2157	PCS CDMA Power Amplifier
RF2157 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

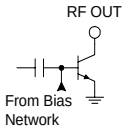
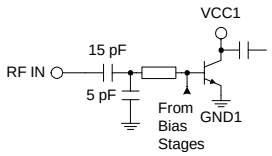
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+4.5	V_{DC}
Mode Voltage (V_{MODE})	+3.5	V_{DC}
Control Voltage (V_{PD})	+3.5	V_{DC}
Input RF Power	+12	dBm
Operating Case Temperature	-30 to +110	℃
Storage Temperature	-65 to +150	℃

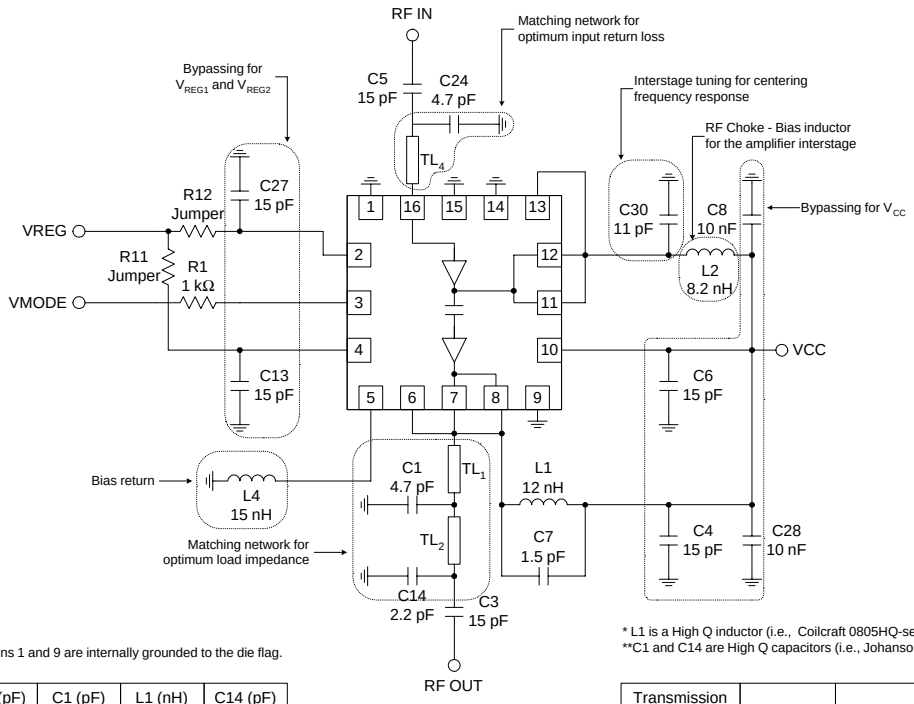
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, V_{PD}=2.8V, P_{OUT}=29dBm, unless otherwise specified
Usable Frequency Range	1750		1910	MHz	
Typical Frequency Range		1750-1780		MHz	Tuned Matching Network
		1850-1910		MHz	Tuned Matching Network
Linear Gain	23	25	28	dB	P_{OUT}=29dBm, V_{MODE}≤0.5V
	22	24	26	dB	P_{OUT}=29dBm, V_{MODE}≥2.5V
Small Signal Gain	22	27	29	dB	P_{IN}≤-20dBm
Second Harmonic (Including second harmonic trap)		-35		dBc	
Third Harmonic		-40		dBc	
Fourth Harmonic		-45		dBc	
CDMA					V_{MODE}≥2.5V
Linear Output Power	29			dBm	
	28			dBm	V_{CC}=3.0V
Linear Efficiency	33	37		%	
		6			P_{OUT}=16dBm
CDMA ACPR @ 1.25MHz		-46	-44	dBc	
Noise Power @ 80MHz Offset		-139		dBm/Hz	
CDMA					V_{MODE}≤0.5V
Linear Output Power	29			dBm	
Linear Efficiency	30	35		%	
CDMA ACPR @ 1.25MHz		-46	-44	dBc	
Noise Power @ 80MHz Offset		-139		dBm/Hz	
TDMA					
Linear Efficiency	30	37		%	
TDMA ACPR @ 30kHz Offset		-31	-28	dBc	
TDMA ACPR @ 60kHz Offset		-52	-48	dBc	
Input VSWR		< 2:1			
Output Load VSWR			10:1		No damage.
Stability	5:1				
Junction to Case Thermal Resistance		25		°C/W	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Power Supply Voltage		3.4	4.5	V	
Idle Current		325		mA	$V_{MODE} \leq 0.5V$
	110	140	175	mA	$V_{MODE}=2.8V$
V_{PD} Current	7		9	mA	$V_{CC}=3.4V$, $V_{PD}=2.8V$, $V_{MODE}=2.8V$ No RF input power applied.
Turn On/Off Time			100	ns	
Total Current (Power Down)			10	µA	$V_{PD} \leq 0.2V$
V_{PD} Low Voltage		0	0.2	V	
V_{PD} High Voltage	2.7	2.8	2.9	V	
MODE High Voltage	2.5	2.8			$R_1=1k\Omega$
MODE Low Voltage		0	0.5		

Pin	Function	Description	Interface Schematic
1	GND	This pin is internally grounded to the die flag.	
2	VPD1	Power down control for first stage. When this pin is “low”, first stage circuits are shut off. When this pin is 2.8V, all first stage circuits are operating normally. V_{PD1} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V.	
3	MODE	For full power operation, VMODE is set low. VMODE will reduce the bias current by approximately 50% when set HIGH. Large Signal Gain is reduced approximately 1.5dB at 29dBm P_{OUT}. Small Signal Gain is reduced by approximately 6dB at lower temperatures. An external series resistor is optional to limit the amount of current required.	
4	VPD2	Power down control for the second stage. When this pin is “low”, the second stage circuit is shut off. When this pin is 2.8V, the second stage circuit is operating normally. V_{PD} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 15pF high frequency bypass capacitor is recommended.	
5	GND	Connect to ground plane via 15nH inductor. DC return for the second stage bias circuit.	
6	NC	This pin is internally a no connection. It is recommended that this pin be connected to either the RF output matching network or to the ground plane.	
7	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1710MHz to 1910MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
8	RF OUT	Same as pin 7.	See pin 7.
9	GND	This pin is internally grounded to the die flag.	
10	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
11	VCC1	Power supply for first stage and interstage match. Pins 11 and 12 should be connected by a common trace where the pins contact the printed circuit board.	
12	VCC1	Same as pin 11.	
13	NC	This pin is internally a no connection. It is recommended that this pin be connected to either VCC1 or to the ground plane.	
14	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
15	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
16	RF IN	RF input. An external 15pF series capacitor is required as a DC block. In addition, a series transmission line and shunt capacitor, 5pF, are required to provide 2:1 VSWR.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic
Korea - CDMA



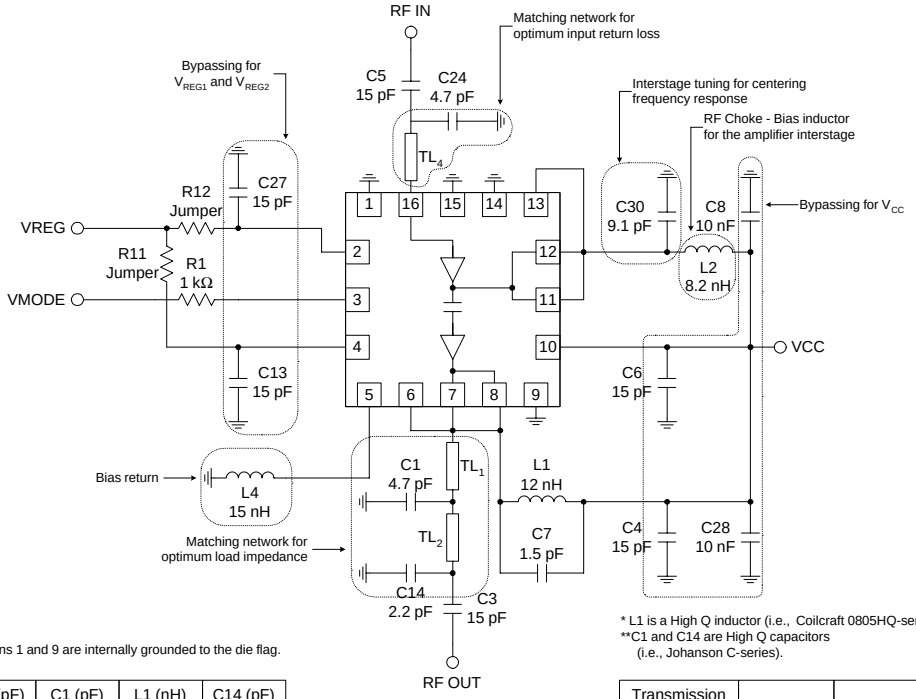
Pins 1 and 9 are internally grounded to the die flag.

* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors (i.e., Johanson C-series).

Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (Korea)	10	4.7	12	2.2

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (Korea)	30-40 mils	150 mils	20-30 mils	200 mils

Application Schematic
US - CDMA



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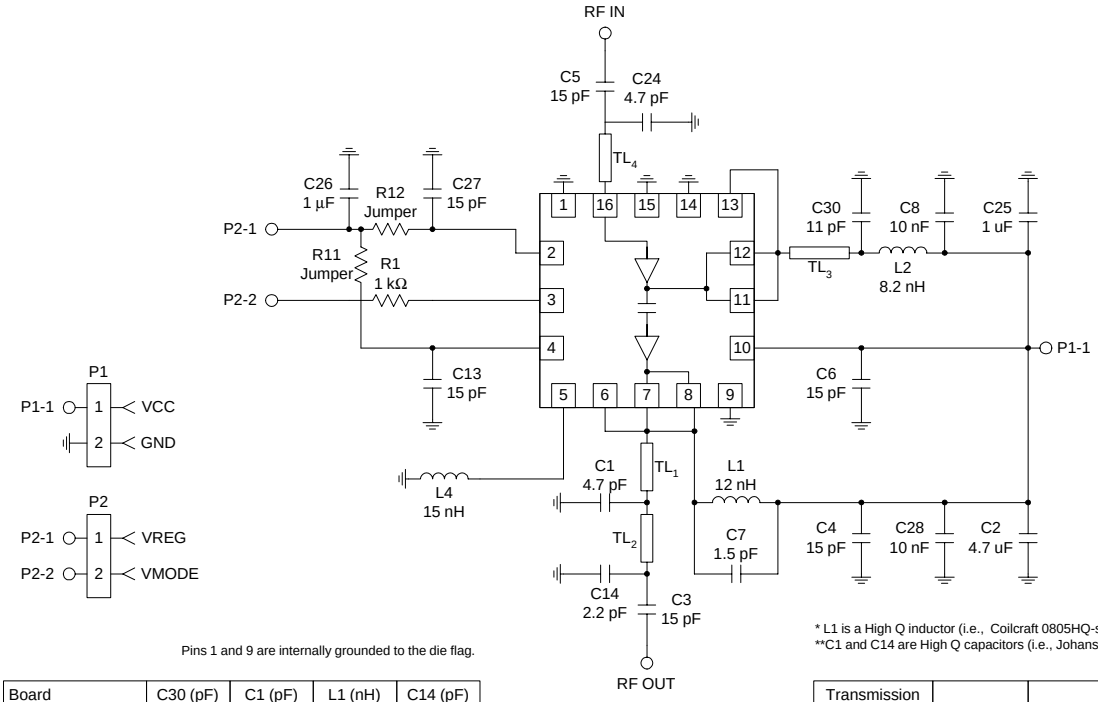
Evaluation Board Schematic
Korea - CDMA
(Download Bill of Materials from www.rfmd.com.)



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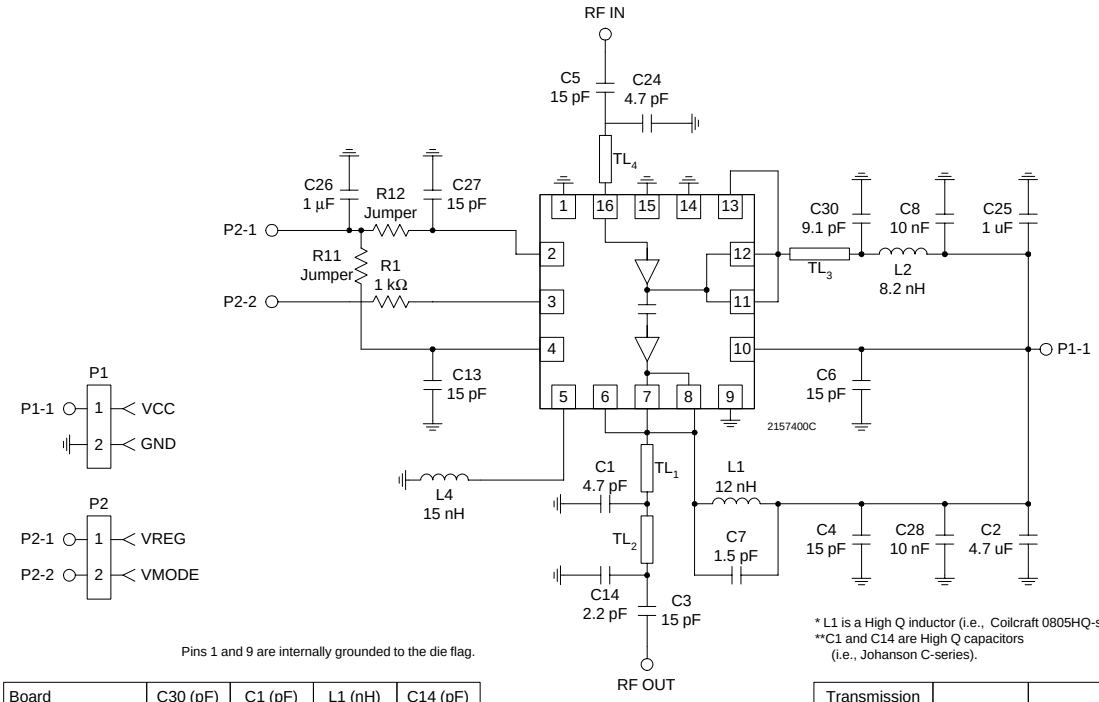
Evaluation Board Schematic
US - CDMA



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(i.e., Johanson C-series).

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (US)	30-40 mils	150 mils	20-30 mils	200 mils

Evaluation Board Layout
Board Size 2" x 2"
Board Thickness 0.031", Board Material FR-4, Multi-Layer