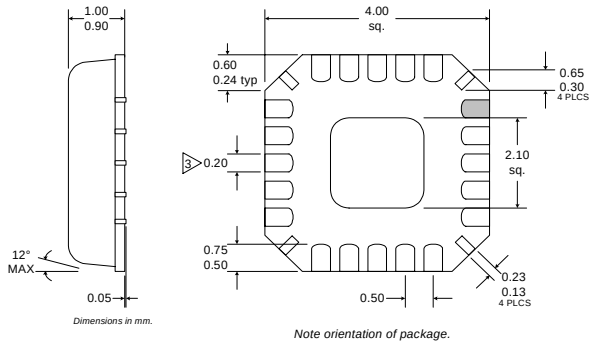
CDMA/FM LOW NOISE AMPLIFIER/MIXER 900MHZ DOWNCONVERTER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/JCDMA
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

The RF2461 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and downconvert RF signals, while providing 30dB of stepped gain control range. Features include digital control of LNA gain, mixer gain, and power down mode. Another feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. Noise figure, IP3, and other specs are designed to be compatible with the IS-98B interim standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Germanium HBT process and is in a 4mmx4mm, 20-pin, leadless chip carrier.



Dimensions in mm.

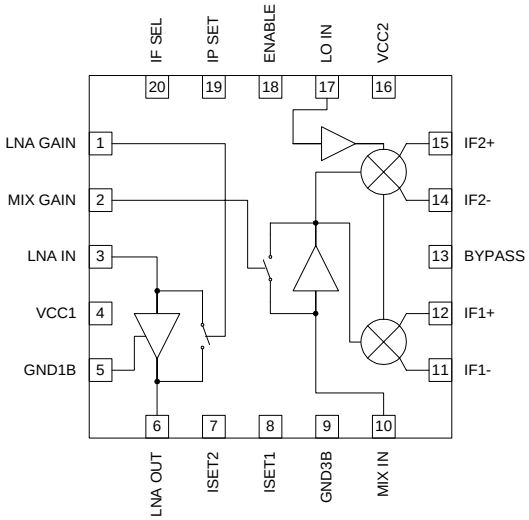
Note orientation of package.

NOTES:
1. Shaded lead is Pin 1.
2. Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
3. Dimension applies to plated terminal: to be measured between 0.02 mm and 0.25 mm from terminal end.
4. Package Warpage: 0.05 mm max.
5. Die Thickness Allowable: 0.305 mm max.

Package Style: LCC, 20-Pin, 4x4

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☑ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Complete Receiver Front-End
- Stepped LNA/Mixer Gain Control
- Adjustable LNA/Mixer Bias Current
- Adjustable LNA/Mixer IIP3
- Meets IMD Tests with Three Gain States/ Two Logic Control Lines

Ordering Information

RF2461	CDMA/FM Low Noise Amplifier/Mixer 900MHz Downconverter
RF2461 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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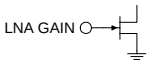
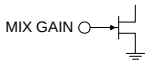
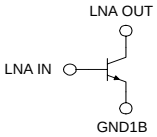
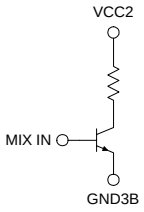
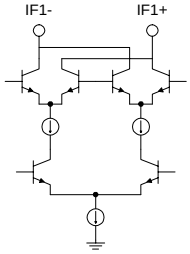
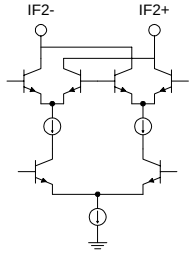
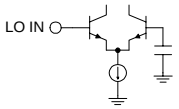
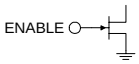
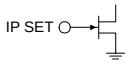
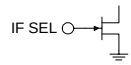
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V CDMA: RF=880MHz, IF=85MHz, LO=965MHz@-10dBm JCDMA: RF=851MHz, IF=110MHz, LO=741MHz@-4dBm
RF Frequency Range	800	869 to 894 832 to 870	1000	MHz	
LO Frequency Range	700	954 to 979 722 to 760	1000	MHz	
IF Frequency Range	0.1		250	MHz	
LNA - CDMA					
Gain	13.5	14.5	15	dB	
Noise Figure		1.8	2	dB	
Input IP3	+7.0	+9.0		dBm	IIP3 is adjustable. V_{IPSET}=0V
Current		5		mA	
LNA Bypass - CDMA					
Gain	-8	-6		dB	
Input IP3	+16.0	+18.0		dBm	
Current		0		mA	
LNA - JCDMA					
Gain	14	15	16	dB	
Noise Figure		1.8	2	dB	
Input IP3	+9.0	+11.0		dBm	IIP3 is adjustable. V_{IPSET}=3V
Current		6.5		mA	
LNA Bypass - JCDMA					
Gain	-9	-7		dB	
Input IP3	+20.0	+24.0		dBm	
Current		0		mA	
Mixer - High Gain Mode - CDMA					3kΩ balanced load.
Gain	13	14.5		dB	
Noise Figure		5.5	7	dB	
Input IP3	+3.0	+4.0		dBm	IIP3 is adjustable. Decreasing R4/R5 will increase IIP3.
RF to IF Isolation				dB	
Current (including LO Buffer/Bias)		21		mA	
Mixer - Low Gain Mode - CDMA					
Gain	4	5.8		dB	
Noise Figure		13	14	dB	
IIP3	+13.0	+14.0		dBm	
RF to IF Isolation				dB	
Current (including LO Buffer/Bias)		18		mA	

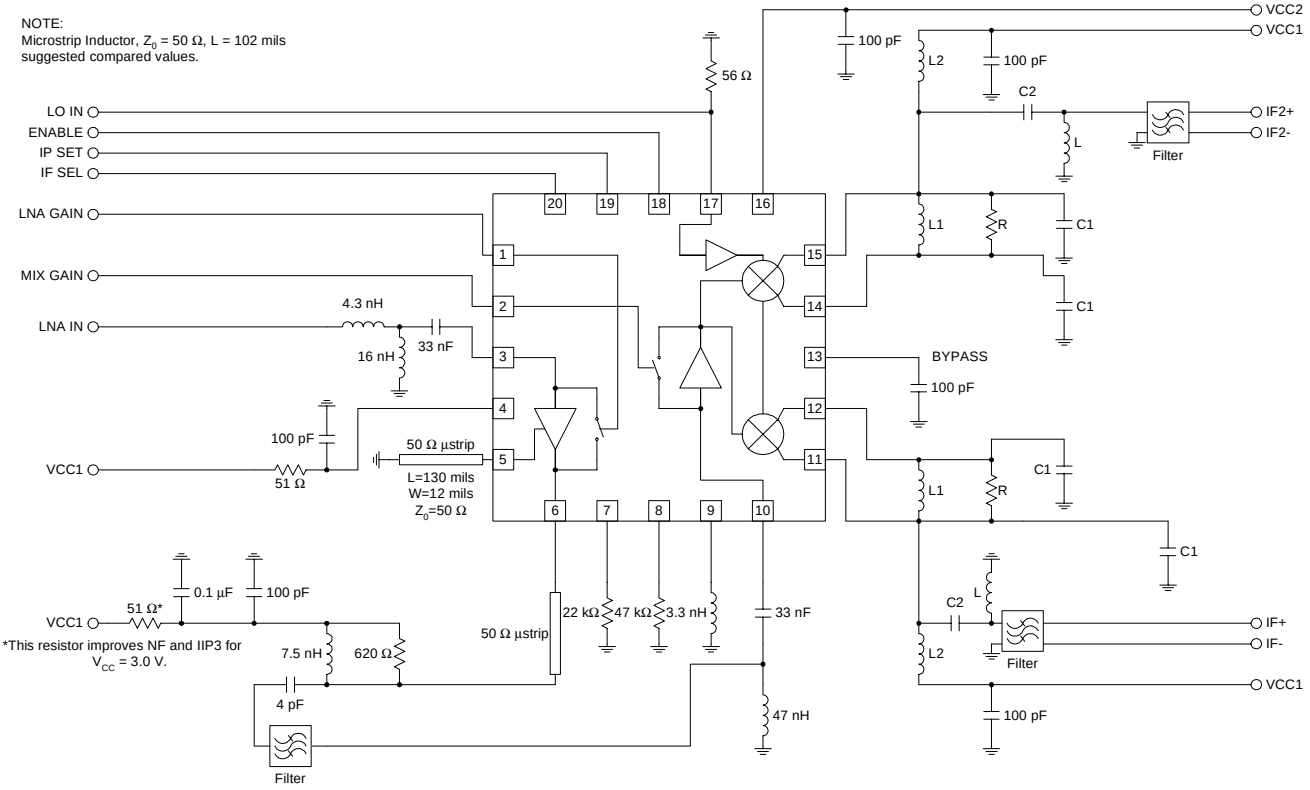
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Mixer - High Gain Mode - JCDMA					3kΩ balanced load.
Gain	12	13		dB	
Noise Figure		5.5	7	dB	
Input IP3	+2.0	+3.0		dBm	IIP3 is adjustable. Decreasing R4/R5 will increase IIP3.
Current (including LO Buffer/Bias)		24		mA	
Mixer - Low Gain Mode - JCDMA					
Gain	2.5	4.0		dB	
Noise Figure		13	14	dB	
IIP3	+10.0	+12.0		dBm	
Current (including LO Buffer/Bias)		21		mA	
Local Oscillator Input					
Input Level		-10		dBm	
LO to IF Isolation		-70		dB	
LO to LNA Isolation		-60		dB	Any gain state.
Cascade - LNA High/Mixer High					LNA High Gain/Mixer High Gain. Assumes 3dB Image filter insertion loss.
Gain	23.5	26	28	dB	
Noise Figure		2.4		dB	
Input IP3	-11	-9	0	dBm	
Current		26		mA	
Cascade - LNA High/Mixer Low					LNA High Gain/Mixer Low Gain. Assumes 3dB Image filter insertion loss.
Gain		16.5		dB	
Noise Figure		4.9		dB	
Input IP3		0		dBm	
Current		23		mA	
Cascade - LNA Low/Mixer High					LNA Low Gain/Mixer High Gain. Assumes 3dB Image filter insertion loss.
Gain		4		dB	
Noise Figure		15.5		dB	
Input IP3		11.8		dBm	
Current		22		mA	
Cascade - LNA Low/Mixer Low					LNA Low Gain/Mixer Low Gain. Assumes 3dB Image filter insertion loss.
Gain	-7	-4.5	-3	dB	
Noise Figure		22.5		dB	
Input IP3	+14	+20	40	dBm	
Current		18		mA	
Power Supply					
Voltage	2.65	3.0	3.15	V	

Pin	Function	Description	Interface Schematic
1	LNA GAIN	Controls the bypass feature of the LNA. A logic low (<1.0V) selects the bypass mode. A logic high (>2.0V) turns on the LNA.	
2	MIX GAIN	Controls the bypass feature of the mixer pre-amp. A logic low (<1.0V) selects the bypass mode. A logic high (>2.0V) turns on the pre-amp.	
3	LNA IN	LNA input pin.	
4	VCC1	VCC pin for all circuits except the LO. Buffer/bias circuitry.	
5	GND1B	LNA emitter. This pin provides the DC path to ground for the LNA. A lumped element or a transmission line inductor can be placed between this pin and ground to degenerate the LNA. This will decrease the gain, increase the IP3, and increase the NF of the LNA. As the value of inductance is increased, these effects will become more pronounced.	
6	LNA OUT	LNA output pin.	See pin 3.
7	ISET2	An external resistor R2 connected to this pin sets the current of the pre-amp and the mixer.	
8	ISET1	An external resistor R3 connected to this pin sets the current of the LNA when IP SET is high (see pin 19).	
9	GND3B	Ground pin for pre-amp circuit. A 3.3nH inductor is used between pin 9 and ground to degenerate the mixer pre-amp. Degenerating the pre-amp will reduce the gain, increase the IP3 and affect the pre-amp input impedance.	
10	MIX IN	Mixer pre-amp input pin.	See pin 9.
11	IF1-	Second differential output pin for the first mixer.	See pin 12.
12	IF1+	First differential output pin for the first mixer. Open collector. A current combiner external network performs a differential to single-ended conversion and sets the output impedance. A DC blocking cap must be present if the IF filter input has a DC path to ground. Mixer (IF2+ and IF-) needs to “see” a differential impedance between 2kΩ to 4kΩ.	
13	BYPASS	Bypass pin for the LO bias reference.	
14	IF2-	Second differential output pin for the second mixer.	See pin 15.

Pin	Function	Description	Interface Schematic
15	IF2+	First differential output pin for the second mixer. Open collector. A current combiner external network performs a differential to single-ended conversion and sets the output impedance. A DC blocking cap must be present if the IF filter input has a DC path to ground. Mixer (IF2+ and IF2-) needs to “see” a differential impedance between 2kΩ to 4kΩ.	
16	VCC2	VCC pin for the LO buffer/bias circuitry.*	
17	LO IN	LO limiter input pin.	
18	ENABLE	This pin is used to enable or disable the RF2461. A logic high (>2.0V) enables the circuitry. A logic low (<1.0V) disables the circuitry.	
19	IP SET	Controls the setting of the LNA current. A logic low (<1.0V) selects the internal resistance (49.5kΩ), resulting in an LNA current of 5mA. A logic high (>2.0V) selects the external resistance at pin 8.	
20	IF SEL	Determines which IF port is active. A logic low (<1.0V) activates IF1 and deactivates IF2. A logic high (>2.0V) activates IF2 and deactivates IF1.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

*The bias circuitry current drop when LO signal is not present. Total LO buffer/bias circuitry current is 7mA when LO signal is present.

Application Schematic



Output Interface Network

L1, C1, and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C1 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 11 and 12. An average value to use for C_{EQ} is 2.5pF to 3pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

where R_{OUT} is the desired output impedance and R_P is the parasitic equivalent parallel resistance of L1.

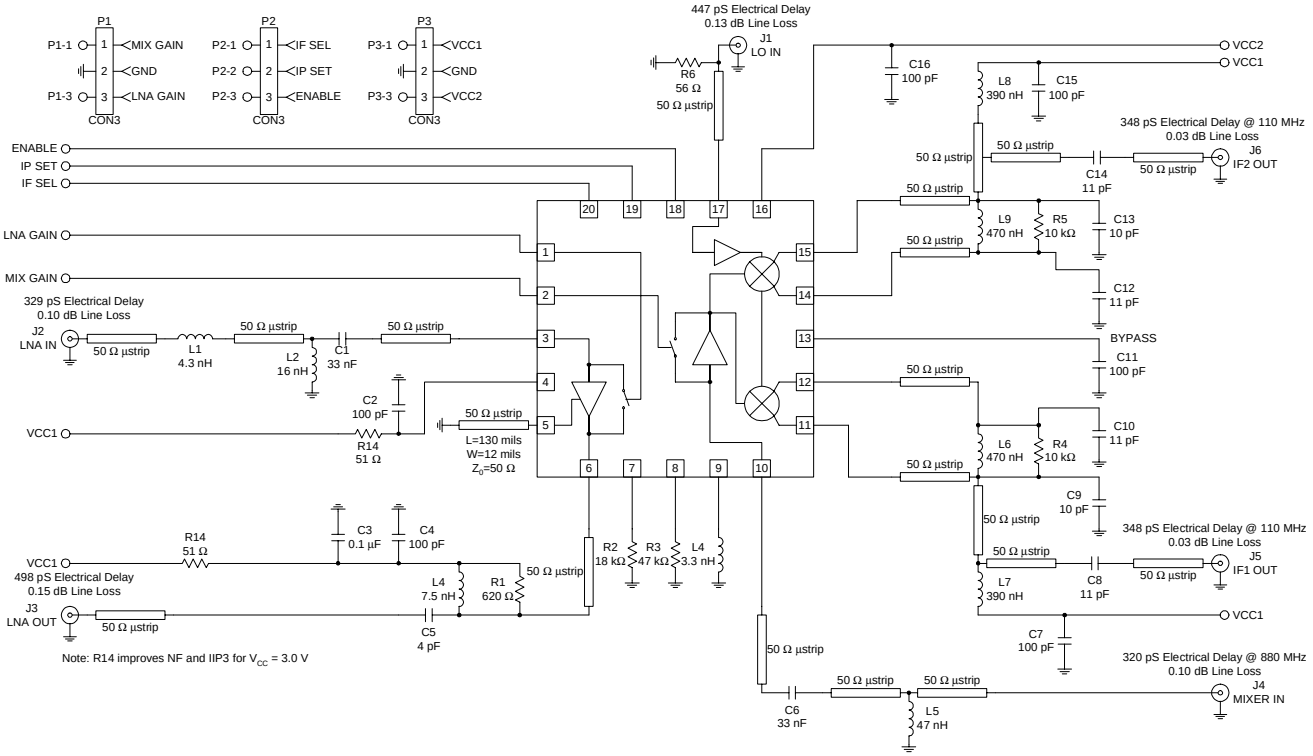
C1 should be chosen as high as possible (not greater than 15pF), while maintaining an R_P of L1 that allows for the desired R_{OUT}.

L2 and C2 serve dual purposes. L2 serves as an output bias choke, and C2 serves as a series DC block.

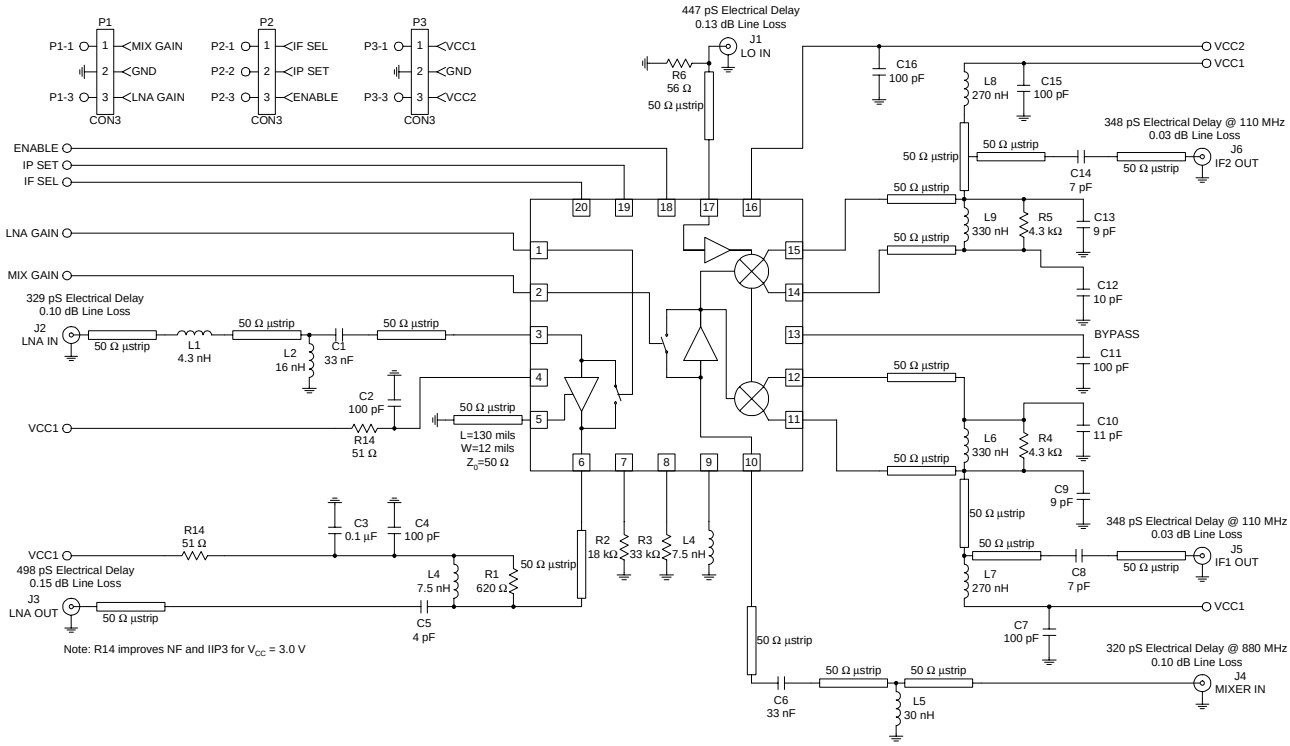
In addition, L2 and C2 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to ROUT. Otherwise, L2 is chosen to be large, and C2 is chosen to be large if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.

Evaluation Board Schematic - CDMA
LO@965MHz, RF@880MHz, IF@85MHz

(Download Bill of Materials from www.rfmd.com.)



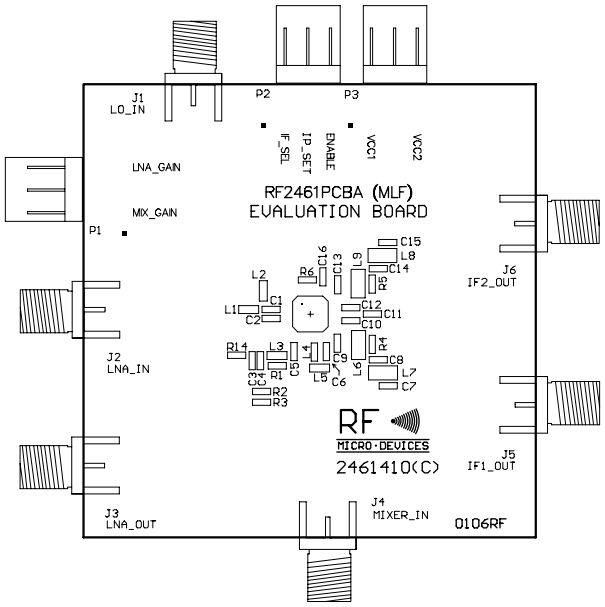
Evaluation Board Schematic - JCDMA
LO@741MHz, RF@851MHz, IF@110MHz



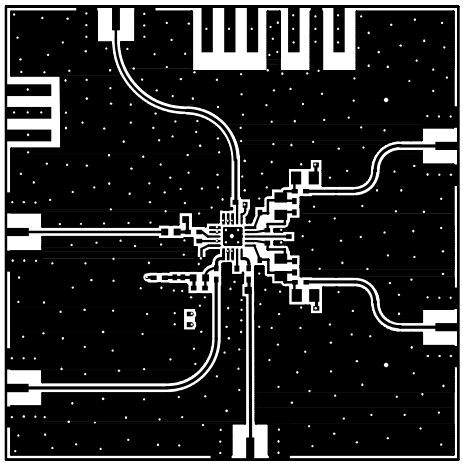
Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.031", Board Material FR-4, Multi-Layer

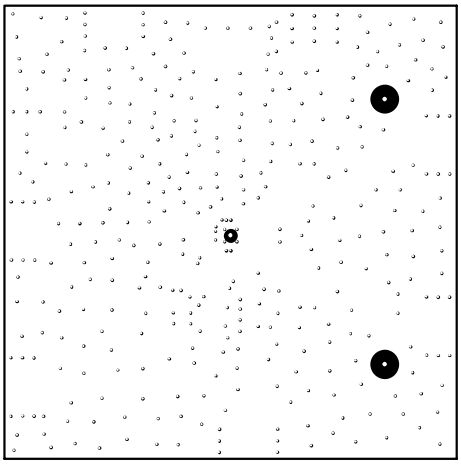
Assembly



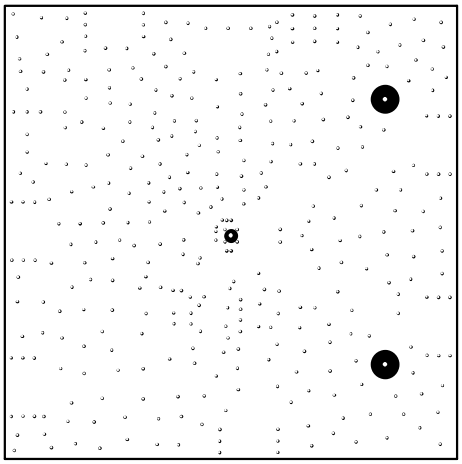
Top



Power Plane 1



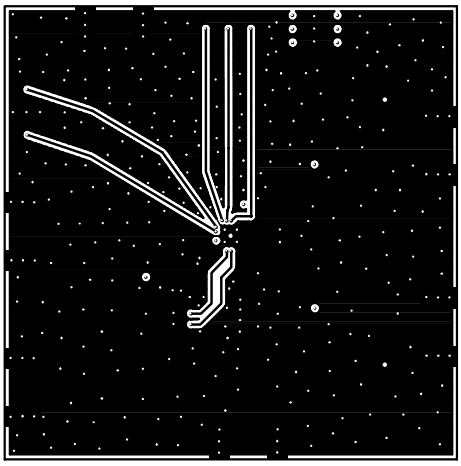
Power Plane 2

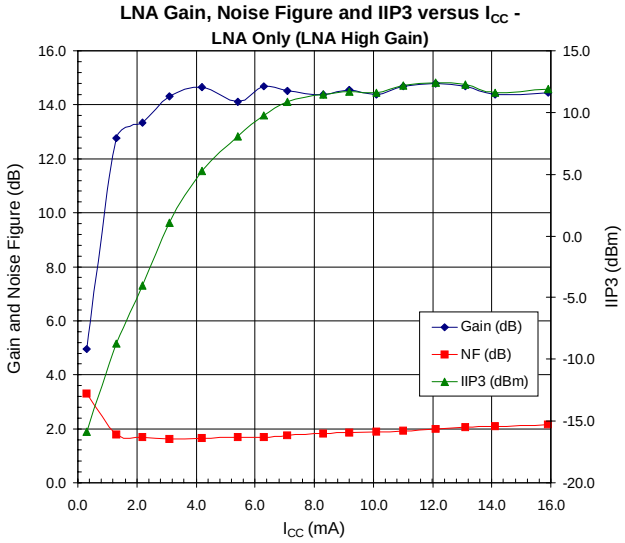


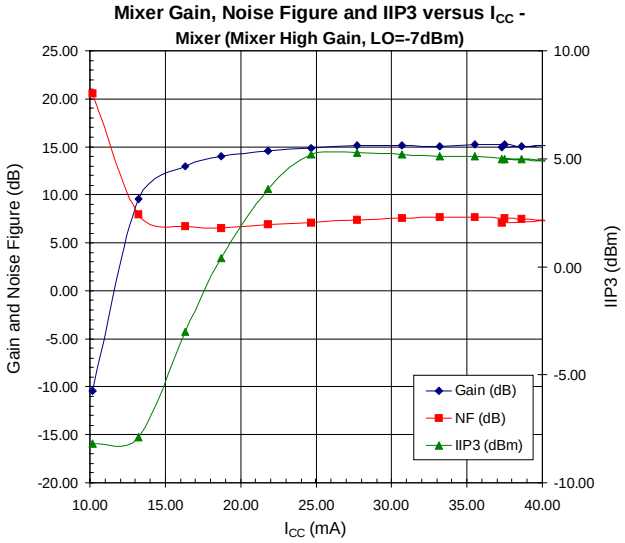
8

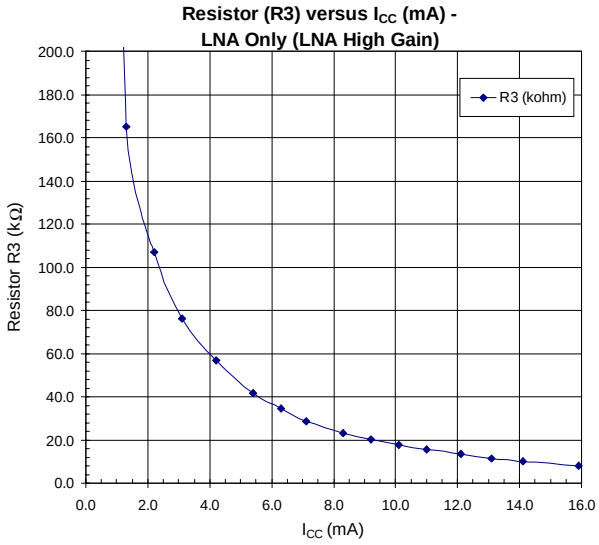
FRONT-ENDS

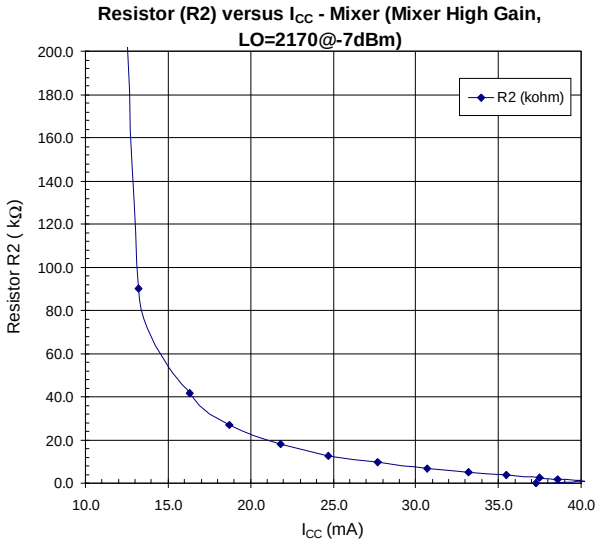
Back









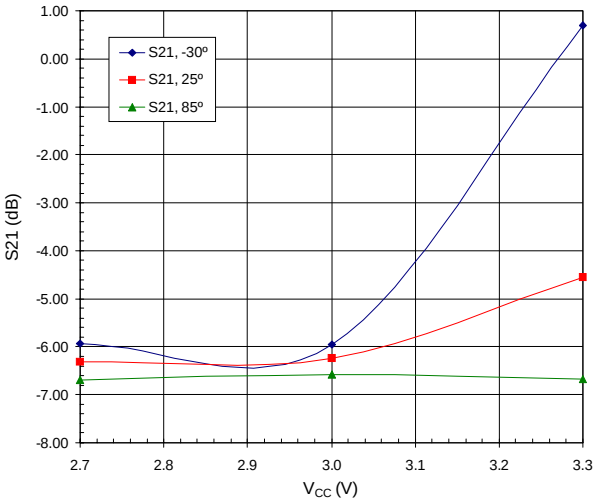


Condition T=25°C, VCC=2.75V, RF=880 and 881MHz, LO=965MHz @-10dBm

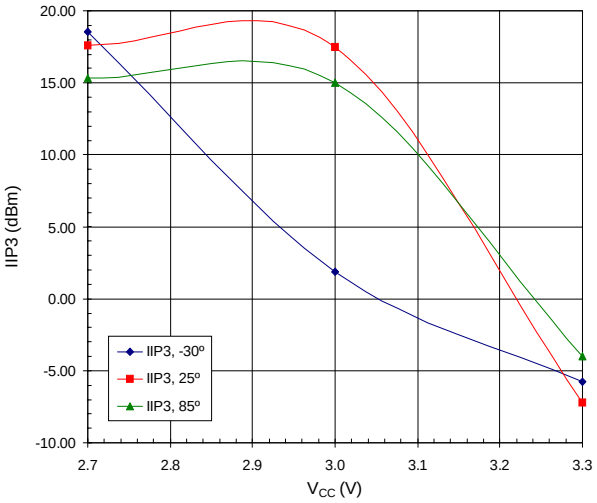
	IP_SET	IF_SEL	LNA GAIN	MIX GAIN	ENABLE
MIXER_GAIN	0	0	0	1	1
LNA_GAIN1	1	0	0	0	1
LNA_GAIN2	1	0	1	0	1

LNA Current=LNA Gain2-LNA-Gain1

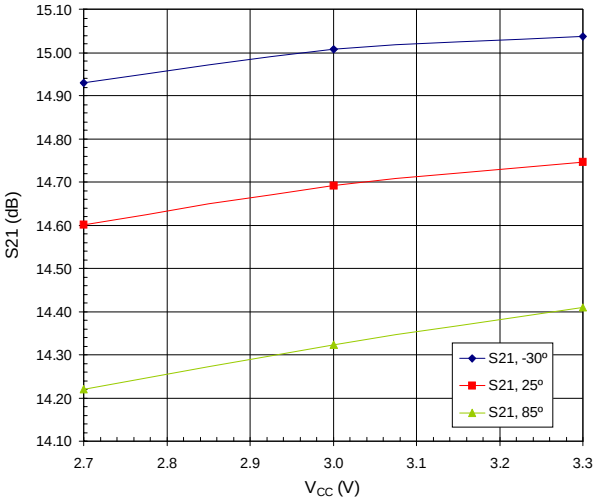
LNA (Low Gain Mode)



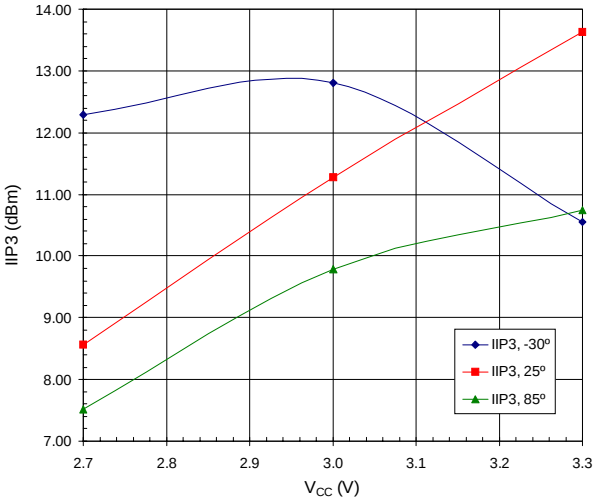
LNA (Low Gain Mode)



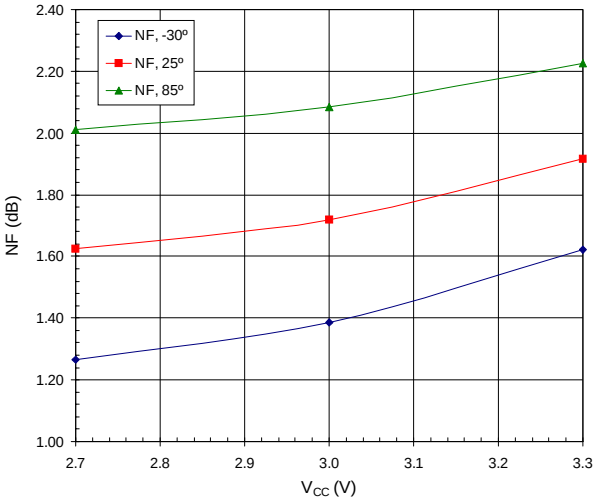
LNA (High Gain/Low IP Mode)



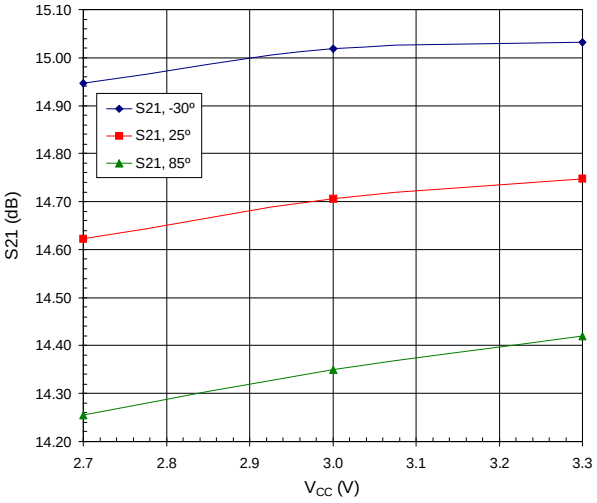
LNA (High Gain/Low IP Mode)



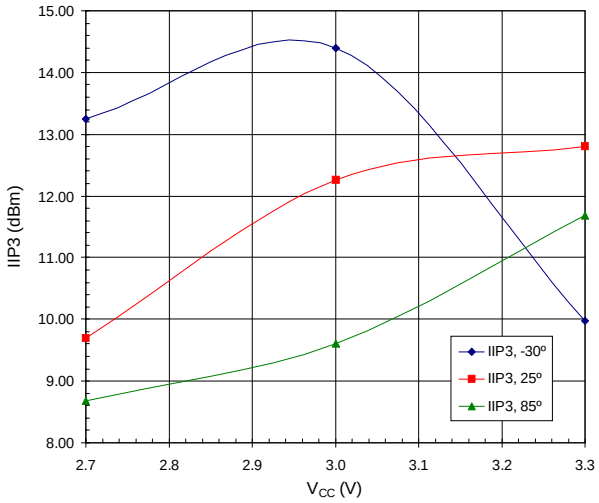
LNA (High Gain/Low IP Mode)



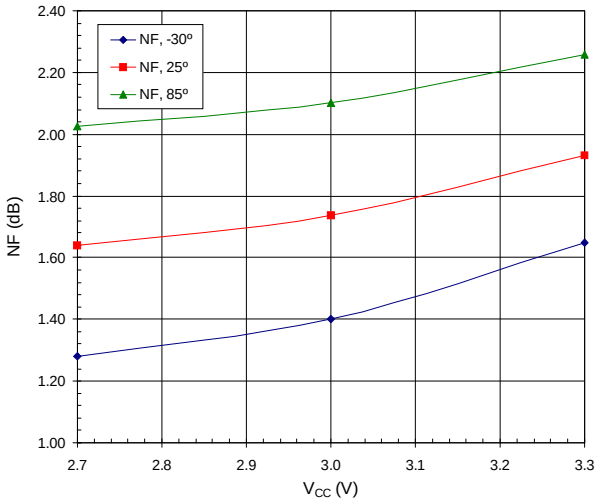
LNA (High Gain/High IP Mode)



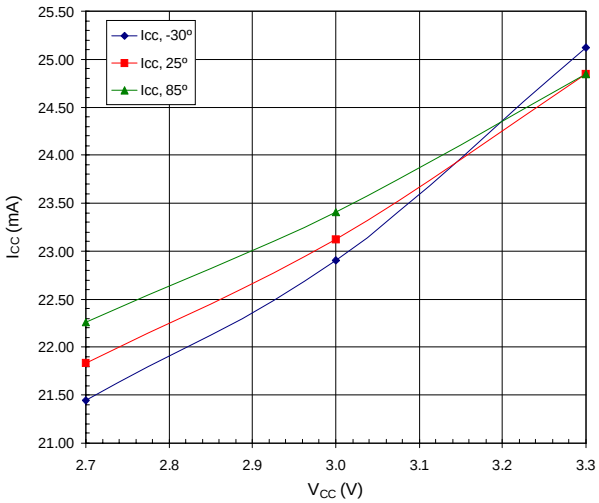
LNA (High Gain/High IP mode)



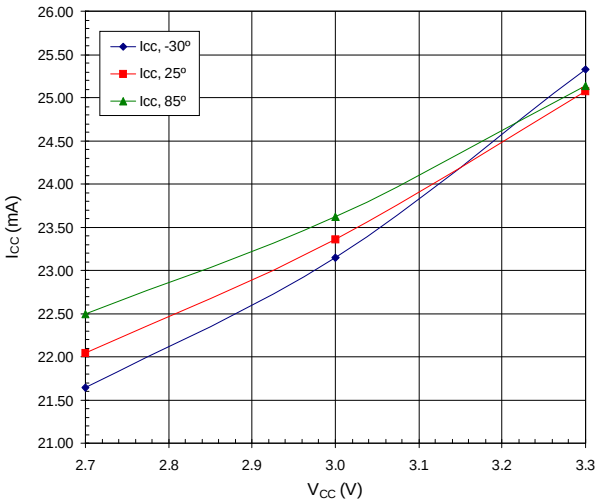
LNA (High Gain/High IP Mode)



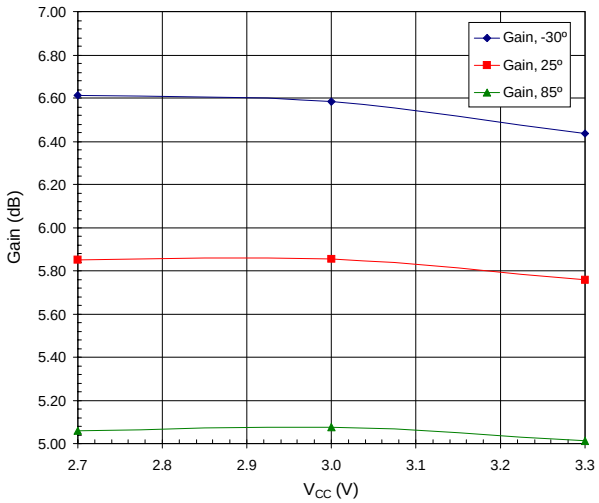
VCC versus I_{CC}, LNA High Mode, Low IP



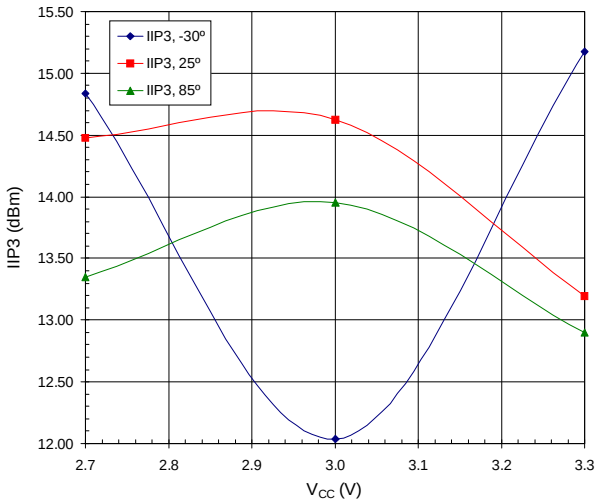
V_{CC} versus I_{CC}, LNA High Mode, High IP



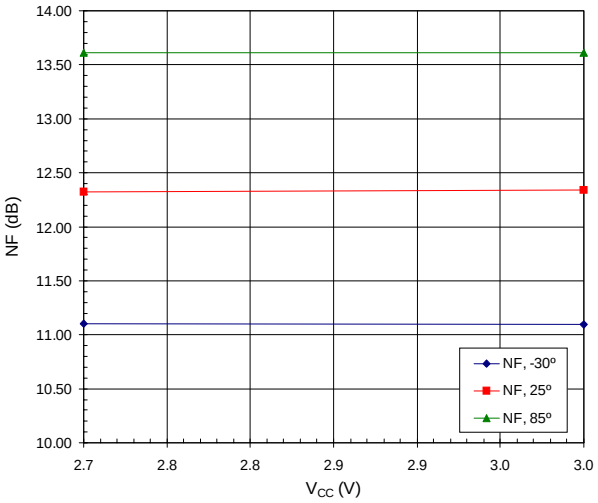
Mixer (IF1), Low Gain Mode, LO@-10dBm



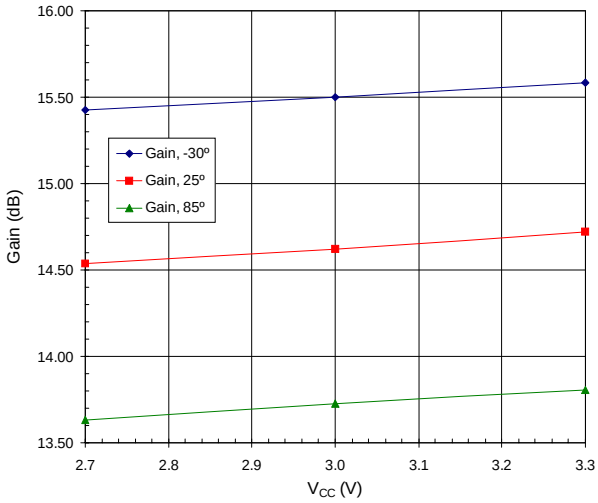
Mixer IF1, Low Gain Mode, LO@-10dBm



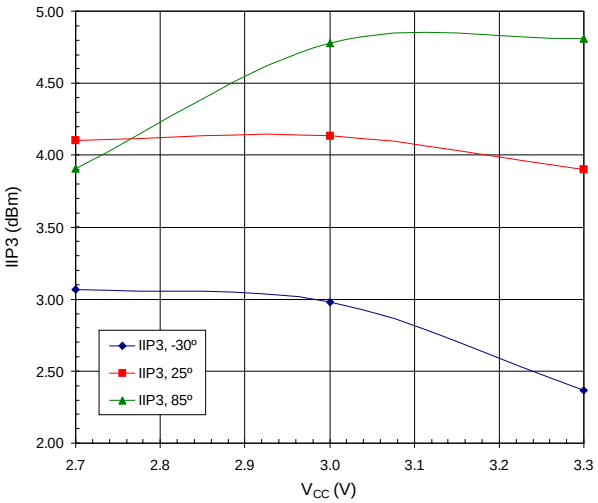
Mixer IF1, Low Gain Mode, LO@-10dBm



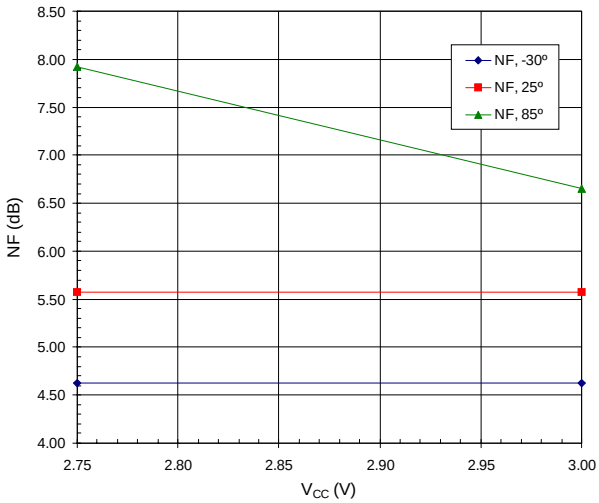
Mixer IF1, High Gain Mode, LO@-10dBm



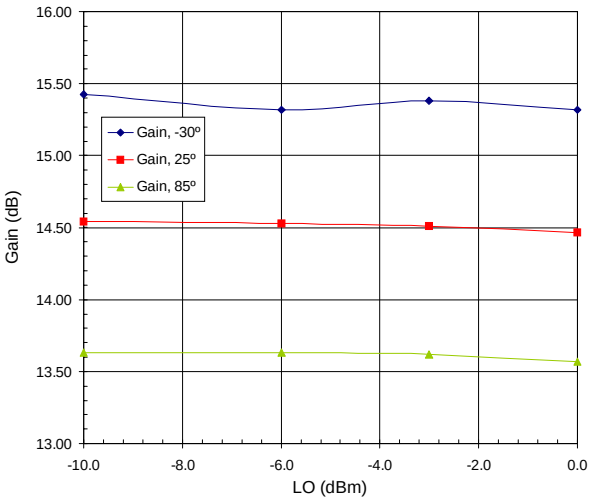
Mixer IF1, High Gain Mode, LO@-10dBm



Mixer IF1, High Gain Mode, LO@-10dBm



Mixer IF1, High Gain Mode, V_{CC}@2.75V



Mixer IF1, High Gain Mode, V_{CC}@2.75V